14Bit,200Ksps,Low-power AFE with I²C Interface

Features

- Selectable Gains of 1,8,16, 32, 64, 128, 256
- 150K/200K SPS 14-bit SAR ADC
- 12-bit offset calibration DAC
- Ultra-low PGA noise
- Support 400KHz/1MHz I²C
- Support 1.2V/1.8V/3.3V I²C
- 1 smart watch dog timer(SWDT)
- Support Temperature Sense
- Up to 2 INTN OD output pins
- Up to 2 PWM output pins
- Power-on reset
- Low power-consumption mode
- Built-in digital filter
- Built-in baseline-tracking algorithm for force touch
- Optional application mode (upload AFE data / report press pulse)

Applications

- TWS
- Mobile phones
- Smart Home
- Weigh Scales
- Toothbrush
- Electronic pen
- PC
- Pressure Sensors
- Temperature sensor

General Description

AW8687x is an AFE chip that can be used to collect, amplify, and process voltage signals. It integrated 1 I²C module, 1 system control module, 1 power management module and 1 AFE module (Include level 2 PGA, 12-bit offset calibration DAC, 14-bit SAR ADC).

From the number of pins, there are two types of AW8687x. **AW86872** can measures **two** pairs of differential analog inputs (AINP, AINN) in direct connection or buffered through the PGA. **AW86874** can measures **four** pairs of differential analog inputs (AINP, AINN) in direct connection or buffered through the PGA.

AW8687x can enter low power consumption mode automatically without the master participation and trigger AFE work through SWDT wake-up to sample and process the signal.

AW8687x can be used for force touch. We provide users with baseline tracking and pressure recognition modules to facilitate the identification of pressing force and signals. Interrupt signals such as sampling completion, threshold comparison and press event trigger can be configured to output through interrupt pin.

Product List

Table 1 shows the number of channels and package type of AW8687x series chips.

Table 1 Product List

Chip	Chip ID	Channel	Package
AW86874CSR	0x74	4	WLCSP 1.41mmX1.41mmX0.34mm-16B
AW86872CSR	0x72	2	WLCSP 1.41mmX1.41mmX0.34mm-16B
AW86872QNR	0x72	2	WBQFN 3mmX3mmX0.75mm-16L

Typical Application Circuit

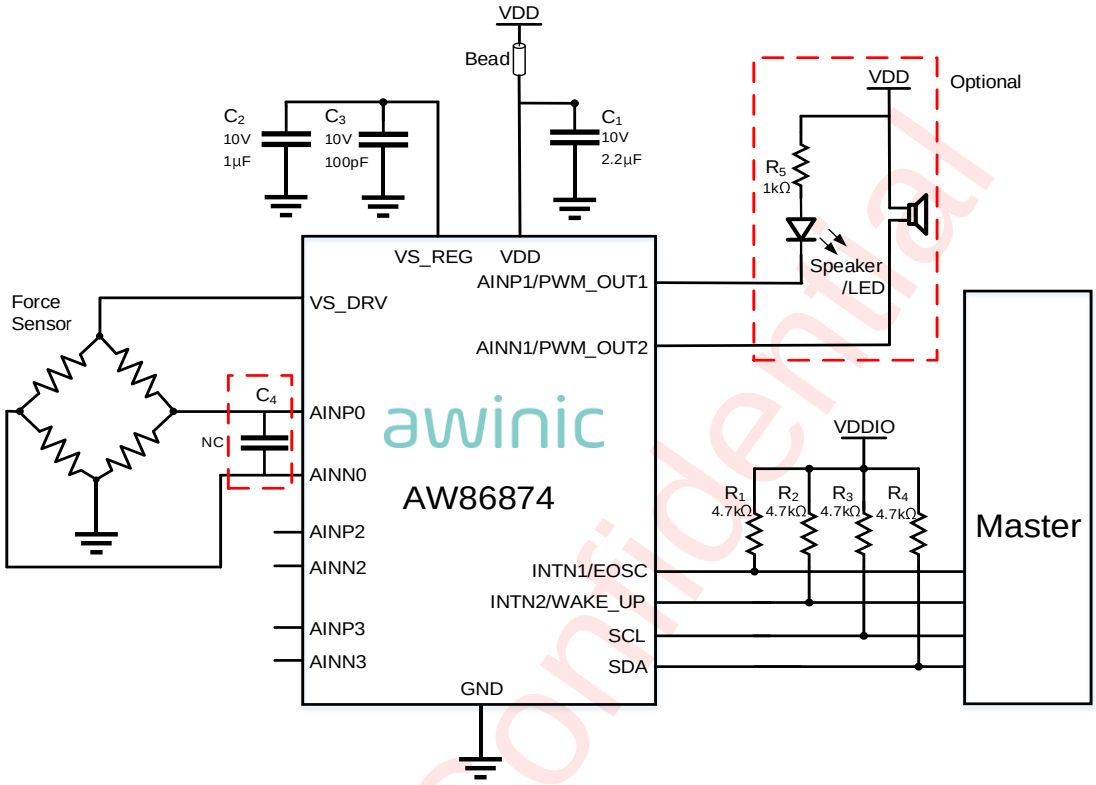


Figure 1 AW86874 Typical Application Circuit

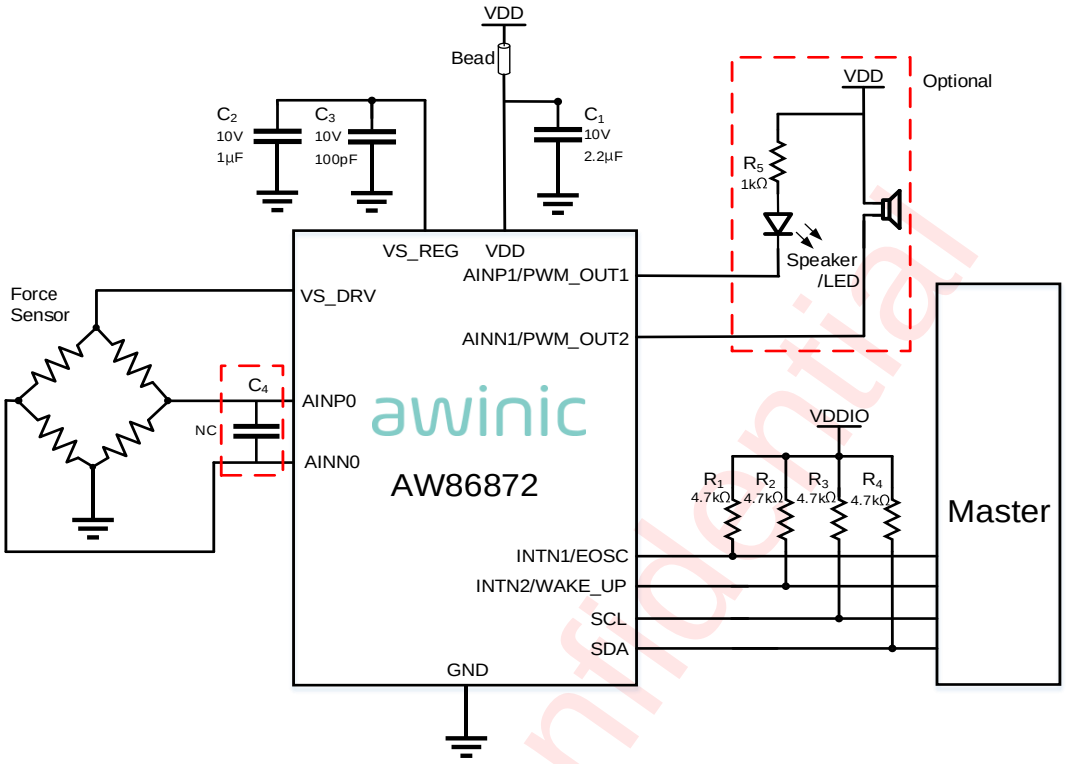


Figure 2 AW86872 Typical Application Circuit

Pin Configuration And Top Mark

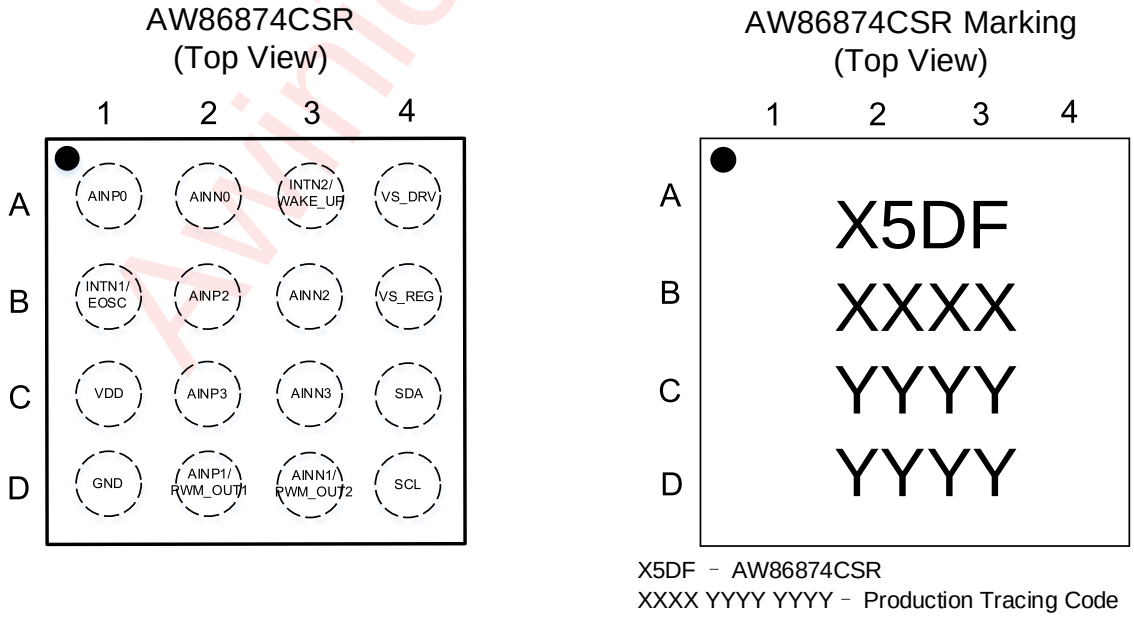


Figure 3 AW86874CSR Pin Configuration And Top Mark

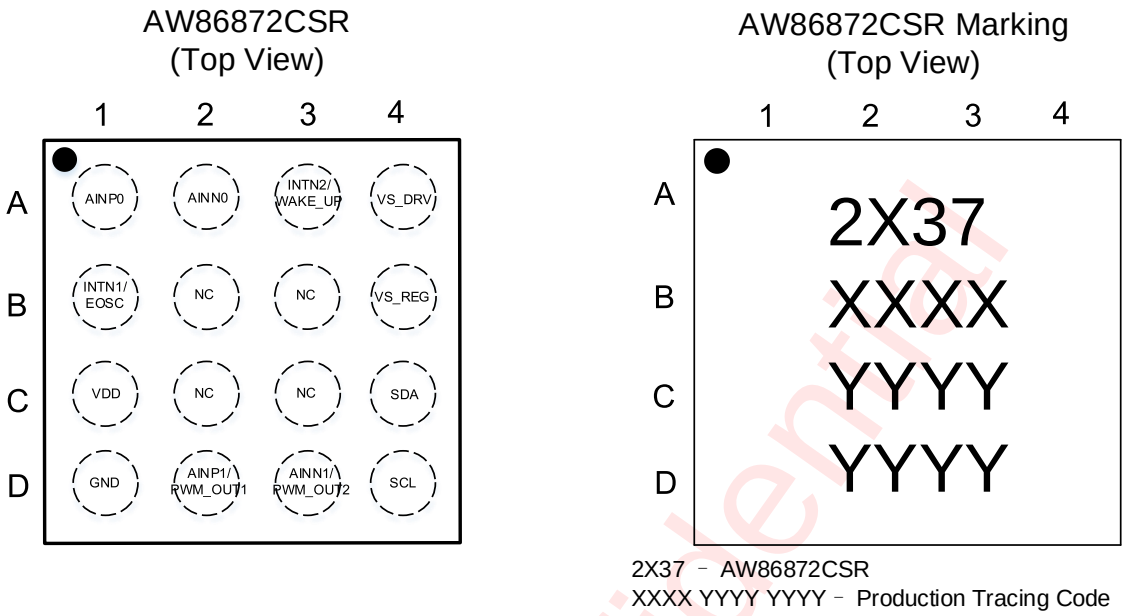


Figure 4 AW86872CSR Pin Configuration And Top Mark

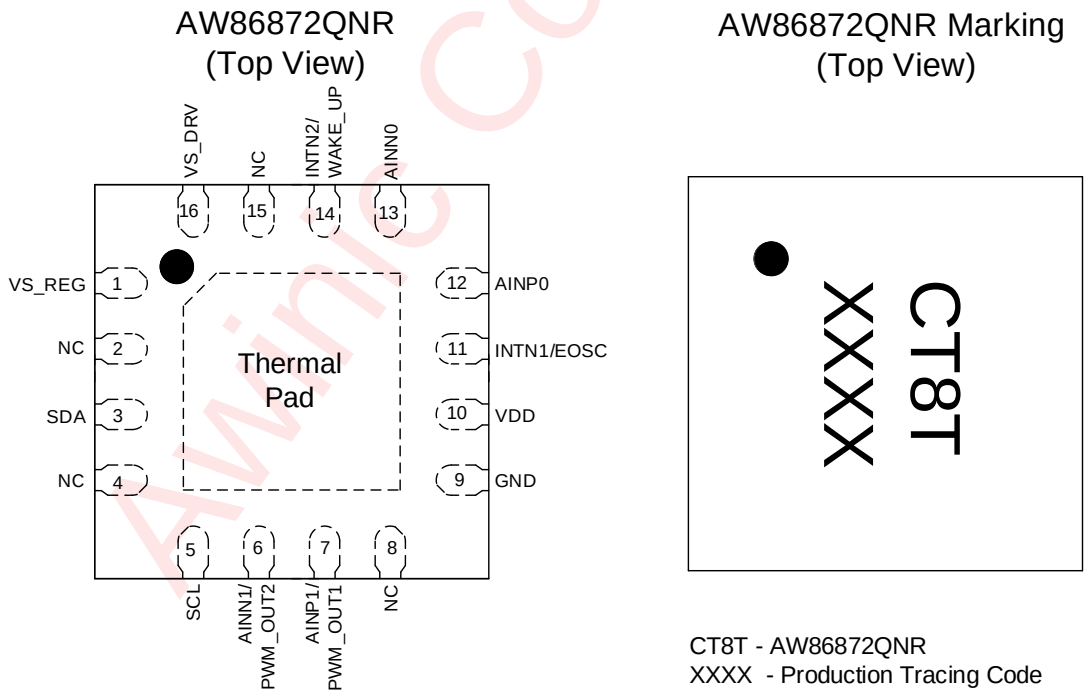


Figure 5 AW86872QNR Pin Configuration And Top Mark

Pin Definition

AW86874CSR Pin Definition

NO.	NAME	DESCRIPTION
A1	AINP0	Sensor Channel 0 Positive Input
A2	AINN0	Sensor Channel 0 Negative Input
A3	INTN2/WAKE_UP	Interrupt2, Open Drain; Wake up pin when GPIO wake up mode is enabled
A4	VS_DRV	VS Regulated output, Driving sensor
B1	INTN1/EOSC	Interrupt1, Open Drain; External clock input port
B2	AINP2	Sensor Channel 2 Positive Input
B3	AINN2	Sensor Channel 2 Negative Input
B4	VS_REG	VS output, need to be connected to 1μF capacitor
C1	VDD	Power
C2	AINP3	Sensor Channel 3 Positive Input
C3	AINN3	Sensor Channel 3 Negative Input
C4	SDA	I²C DATA , Open Drain
D1	GND	Ground
D2	AINP1/PWM_OUT1	Sensor Channel 1 Positive Input; PWM output1, driving LED or Speaker, Push-Pull/Open Drain
D3	AINN1/PWM_OUT2	Sensor Channel 1 Negative Input; PWM output2, driving LED or Speaker, Push-Pull/Open Drain
D4	SCL	I²C CLOCK, Open Drain

AW86872CSR Pin Definition

NO.	NAME	DESCRIPTION
A1	AINP0	Sensor Channel 0 Positive Input
A2	AINN0	Sensor Channel 0 Negative Input
A3	INTN2/WAKE_UP	Interrupt2, Open Drain; Wake up pin when GPIO wake up mode is enabled
A4	VS_DRV	VS Regulated output, Driving sensor
B1	INTN1/EOSC	Interrupt1, Open Drain; External clock input port
B2	NC	Not Connect, recommended to connect the pin to the ground.
B3	NC	Not Connect, recommended to connect the pin to the ground.
B4	VS_REG	VS output, need to be connected to 1μF capacitor
C1	VDD	Power
C2	NC	Not Connect, recommended to connect the pin to the ground.
C3	NC	Not Connect, recommended to connect the pin to the ground.
C4	SDA	I²C DATA , Open Drain

D1	GND	Ground
D2	AINP1/PWM_OUT1	Sensor Channel 1 Positive Input; PWM output1, driving LED or Speaker, Push-Pull/Open Drain
D3	AINN1/PWM_OUT2	Sensor Channel 1 Negative Input; PWM output2, driving LED or Speaker, Push-Pull/Open Drain
D4	SCL	I²C CLOCK, Open Drain

AW86872QNR Pin Definition

NO.	NAME	DESCRIPTION
1	VS_REG	VS output, need to be connected to 1μF capacitor
2	NC	Not Connect, recommended to connect the pin to the ground.
3	SDA	I²C DATA , Open Drain
4	NC	Not Connect, recommended to connect the pin to the ground.
5	SCL	I²C CLOCK, Open Drain
6	AINN1/PWM_OUT2	Sensor Channel 1 Negative Input; PWM output2, driving LED or Speaker, Push-Pull/Open Drain
7	AINP1/PWM_OUT1	Sensor Channel 1 Positive Input; PWM output1, driving LED or Speaker, Push-Pull/Open Drain
8	NC	Not Connect, recommended to connect the pin to the ground.
9	GND	Ground
10	VDD	Power
11	INTN1/EOSC	Interrupt1, Open Drain; External clock input port
12	AINP0	Sensor Channel 0 Positive Input
13	AINN0	Sensor Channel 0 Negative Input
14	INTN2/WAKE_UP	Interrupt2, Open Drain; Wake up pin when GPIO wake up mode is enabled
15	NC	Not Connect, recommended to connect the pin to the ground.
16	VS_DRV	VS Regulated output, Driving sensor

Functional Block Diagram

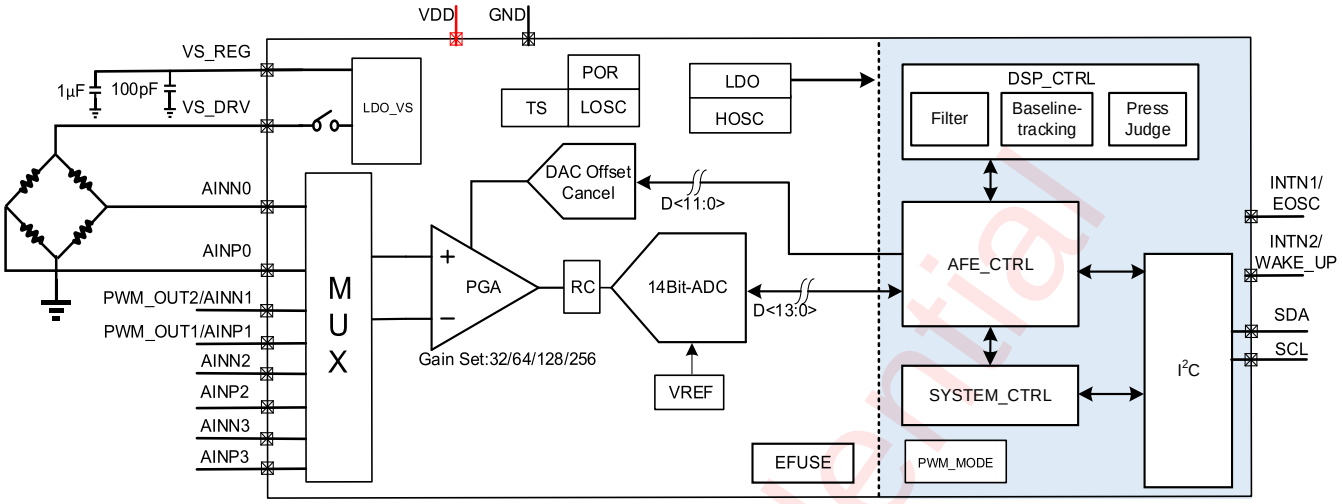


Figure 6 AW86874 Function Block Diagram

Typical Application Circuits

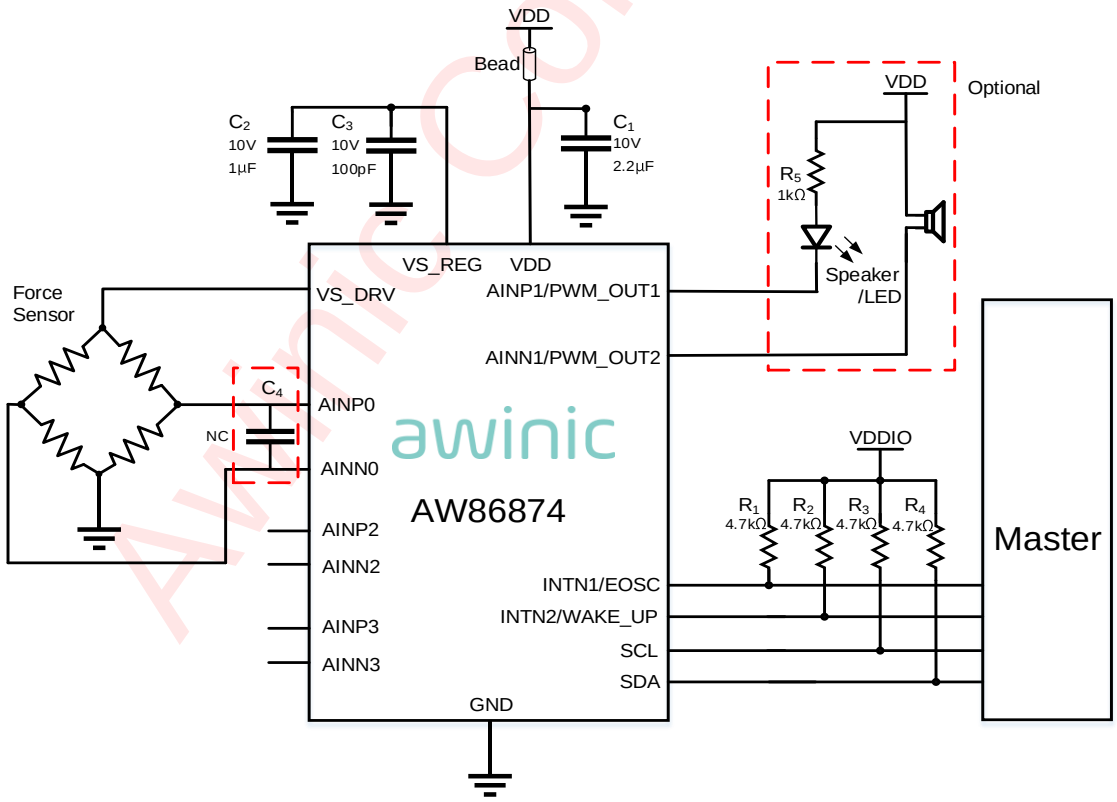


Figure 7 AW86874 Typical Application Circuit

1：Please place C_1, C_2, C_3, C_4 as close to the chip as possible.
2：Please place C_4 which is NC, if the noise of force sensor is too high.

3：For the sake of driving capability, the power lines (especially the one to VDD), output lines (especially the one to VS_DRV), and the differential signal lines should be short and wide as possible.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW86874CSR	-40°C ~105°C	WLCSP 1.41mm×1.41mm×0.34mm -16B	X5DF	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW86872CSR	-40°C ~105°C	WLCSP 1.41mm×1.41mm×0.34mm -16B	2X37	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW86872QNR	-40°C ~105°C	WBQFN 3mmX3mmX0.75mm-16L	CT8T	MSL1	ROHS+HF	6000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS	RANGE
Supply voltage range V_{DD}	-0.3V to 6V
AINP0, AINN0	-0.3V to 3.6V
INTN1/EOSC,INTN2/WAKE_UP	-0.3V to 3.6V
AINP1/PWM_OUT1, AINN1/PWM_OUT2(<VDD+0.3V)	-0.3V to 6V
Ambient Temperature Range	-40°C to 105°C
Maximum operating junction temperature T_{JMAX}	150°C
Storage Temperature Range T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD Rating (NOTE 2 3)	
HBM（Human Body Model）	±2kV
CDM(Charge Device Model)	±1.5kV
Latch-up	
Test Condition: JESD78E	+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE 3：Charge Device Model test method: ESDA/JEDEC JS-002-2018.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Analog supply voltage	2.6	3.3	5.5	V
C_{VDD}	VDD decoupling capacitance		2.2		μF
C_{VS_REG}	VS_REG decoupling capacitor		1		μF
T_A	Operating free-air temperature range	-40	25	105	°C

Electrical Characteristics

VDD=3.3V, T_A=25°C for typical values (unless otherwise noted)

Parameter		Test Conditions	Min	Typical	Max	Unit
VDD	Analog supply voltage		2.6		5.5	V
VIH	Logic input high level	SDA,SCL,INTN1/EOSC,INTN2/WAKE UP	0.9			V
VIL	Logic input low level	SDA,SCL,INTN1/EOSC,INTN2/WAKE UP			0.3	V
VOL	Logic output low level	SDA,SCL,INTN1/EOSC,INTN2/WAKE UP(Iout=16mA)			0.4	V
		AINP1/PWM_OUT1,AINN1/PWM_OUT2(Iout=25mA)				
VOH	Logic output high level	AINP1/PWM_OUT1,AINN1/PWM_OUT2(Iout=6mA)	VDD-0.4			V
ILP	Standby current			4		μA
IACT	Active current	Without load		1.4		mA
6MHz HOSC						
FHOSC	HOSC working frequency			6		MHz
RHOSC	HOSC Accuracy		-2		2	%
8MHz HOSC						
FHOSC	HOSC working frequency			8		MHz
RHOSC	HOSC Accuracy		-3		3	%
32kHz LOSC						
FLOSC	LOSC working frequency			32		kHz
RLOSC	LOSC Accuracy		-10		10	%
14bit SAR ADC						
VADIN	Input voltage		0		VREF	V

Parameter		Test Conditions	Min	Typical	Max	Unit
VREF	ADC Reference voltage			2.4		V
FADC	Conversion rate			150	200	ksps
PGA(Signal input path)						
VCMI	Common mode input voltage		0.1		VDD-1	V
VDMI	Differential input voltage				VDD/ GPGA	V
GPGA_min	PGA gain min			1		
GPGA_max	PGA gain max			256		
GE	Gain error			6		%
RIN	Differential input impedance			550		KΩ
ISOch-ch	Channel isolation			80		dB
CMRR	Common mode rejection ratio	1.5 mVPP on SIN,200Hz		105		dB
PSRR	Power supply rejection ratio	200Hz		50		dB
VOS	Input offset voltage			±0.04		mV
DAC						
RDAC	Resolution			12		bit
MDAC	Monotonic			11		bit
VEOSI	Equivalent offset calibration range		- 0.1× K(1)		+0.1× K(1)	mV
VS						
VS_REG	VS_REG minimum output voltage	VS_ADJL=1, VS_SELVDD=0, VS_HL=0, VS_ADJ=0		0.9		V
	VS_REG maximum output voltage	VS_SELVDD=1		VDD		V
C_{VS_REG}	VS_REG Decoupling capacitor			1		μF
PWM						
R_{PMOS}	Internal top p-channel MOSFET on-resistance			45		Ω
R_{NMOS}	Internal bottom n-channel MOSFET on-resistance			9		Ω
f_{OSC}	Oscillator frequency			1		MHz
	Frequency accuracy			±2		%
D_{MIN}	Minimum duty cycle	PWM_PRD set 5，PWM_DUTY set 0		17		%

Parameter		Test Conditions	Min	Typical	Max	Unit
D_{MAX}	Maximum duty cycle	PWM_PRD set 5，PWM_DUTY set 5		100		%
POR						
VPOR	Power-on reset voltage			1.5		V

*(1) K= VS×(VDAC_RANGE*0.5+1)，VDAC_RANGE is the actual data read from the register VDAC_RANGE.*

Note : Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

Detailed Functional Description

Power On Sequence

The power on sequence of this device is illustrated in the following figure:

Parameter		Value			Unit
Symbol	**Name**	Min	Typical	Max	
t_{WAIT}	Waiting time for communication with I^2C after power on	3			ms
PUR	Instant Power-up rate	1.6			mV/μs
t_{VIO}	The delay time between VDD power on and INTNx pin being pulled up to 80% external voltage	500			μs

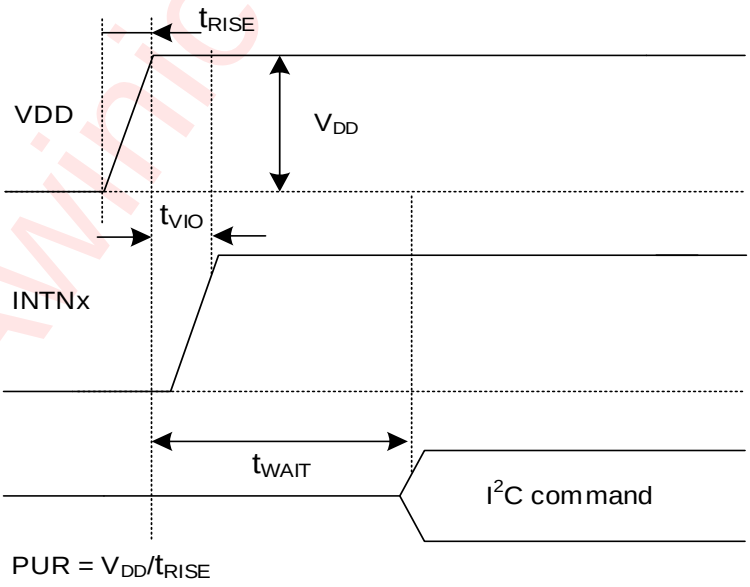


Figure 8 Power On Sequence

Reset

AW8687x has two kinds of reset signal: power on reset (POR) and software reset (Soft Reset). The POR is effective after the chip is powered on, and the reset signal of the system is generated by the control circuit of the power on sequence. Soft Reset resets the chip internal circuit and all configuration registers by writing 0xAA to 0x00 register. It is necessary to ensure that the chip has a general HOSC When operating Soft Reset, so it cannot be in standby mode.

General I²C Operation

This device supports the I²C serial bus and data transmission protocol in fast mode at 400kHz and super-fast mode at 1000kHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. This device can support different high level (1.2V~3.3V) of this I²C interface.

- Only slave mode is supported
- Data bidirectional transmission between master and slaver
- The chip device address is 0x6A by default, and the bit is 7bit
- The register address is 8 bit, the data bit width is 8 bit
- Support general call, the enable can be configured
- Whether the function of general call responds to ACK can be configured
- Support fast mode and standard mode
- Up to 1MHz communication speed

Parameter			Fast mode			Super-fast mode			Unit
No.	Symbol	Name	Min	Typical	Max	Min	Typical	Max	
1	f_{SCL}	SCL Clock frequency			400			1000	kHz
2	t_{LOW}	SCL Low level Duration	1.3			0.5			μs
3	t_{HIGH}	SCL High level Duration	0.6			0.26			μs
4	t_{RISE}	SCL, SDA rise time			0.3			0.12	μs
5	t_{FALL}	SCL, SDA fall time			0.3			0.12	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			0.3			μs
7	$t_{HD:STA}$	(repeat-start) start condition hold time	0.6			0.3			μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			0.26			μs
9	t_{BUF}	Time between start and stop condition	1.3			0.5			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			0.1			μs
11	$t_{HD:DAT}$	SDA hold time	0			0			ns

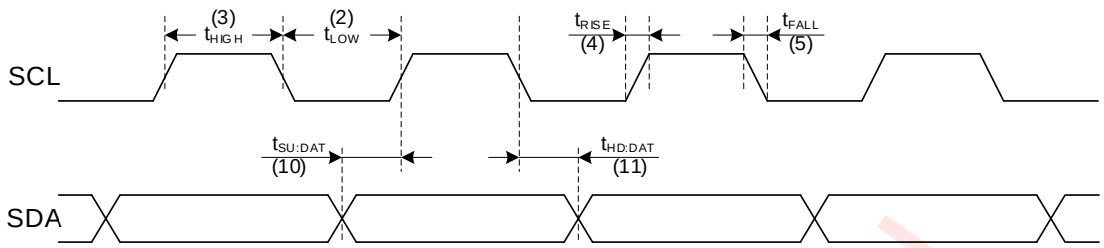


Figure 9 SCL and SDA timing relationships in the data transmission process

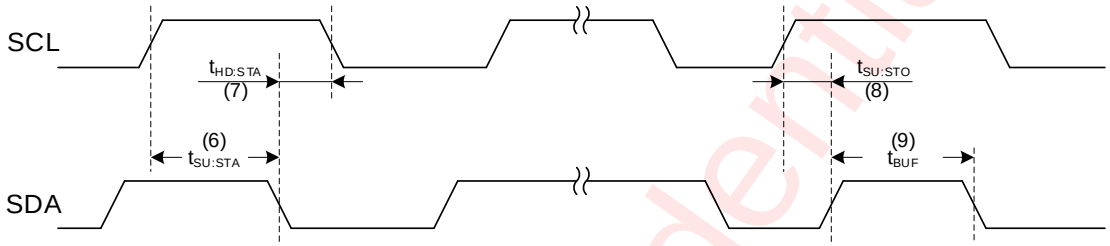


Figure 10 The timing relationship between START and STOP state

Data Validation

When SCL is high level, SDA level must be stable. SDA can be changed only when SCL is low level.

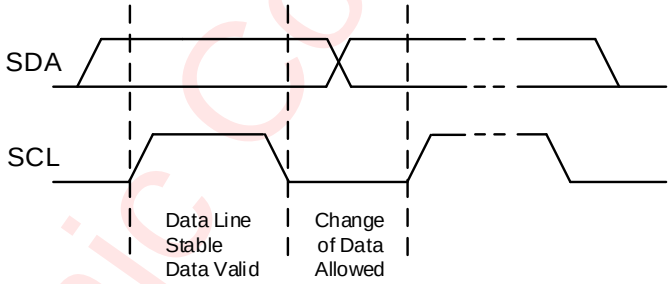


Figure 11 Data Validation Diagram

I²C Start/Stop

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

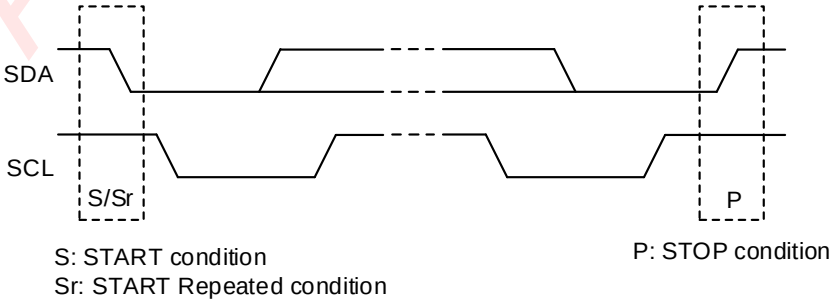


Figure 12 I²C Start/Stop Condition Timing

Acknowledge(ACK)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

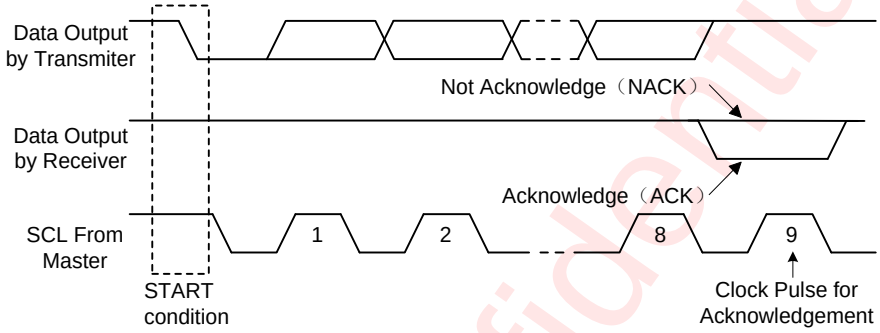


Figure 13 I²C ACK Timing

WRITE PROCESS

Writing process refers to the master device write data into the slave device. In this process, the transfer direction of the data is always unchanged from the master device to the slave device. All acknowledge bits are transferred by the slave device, in particular, the device as the slave device, the transmission process in accordance with the following steps, as shown in Figure 14.

a) Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.

b) Master device transmits the 7-bits device address of the slave device, followed by the "read / write" flag (flag $R/\overline{W}$ = 0);

c) The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

d) The master device transmits the 8-bit register address to which the first data byte will be written;

e) The slave device asserts an acknowledgment (ACK) bit to confirm the register address is correct;

f) Master sends 8 bits of data to register which needs to be written;

g) The slave device asserts an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

h) If the master device needs to continue transmitting data by sending another pair of data bytes, just need to repeat the sequence from step f). In the latter case, the targeted register address will have been auto-incremented by the device.

i) The master device generates the STOP state to end the data transmission.

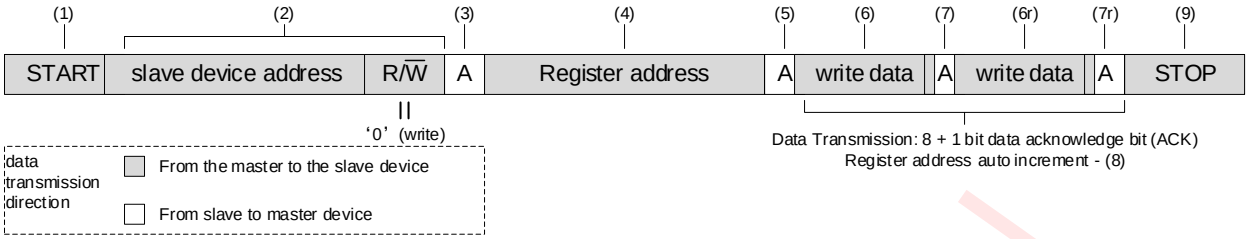


Figure 14 Writing process

READ PROCESS

Reading process refers to the slave device reading data back to the master device. In this process, the direction of data transmission will change. Before and after the change, the master device sends START state and slave address twice, and sends the opposite "read/write" flag. In particular, AW8687x as the slave device, the transmission process carried out by following steps listed in Figure 15.

a) Master device asserts a start condition;

b) Master device transmits the 7 bits address of the device, and followed by a "read / write" flag ($R/\overline{W}$ = 0);

c) The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

d) The master device transmits the register address to make sure where the first data byte will read;

e) The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;

f) The master device restarts the data transfer process by continuously generating STOP state and START state or a separate Repeated START;

g) Master sends 7-bits address of the slave device and followed by a read / write flag (flag $R/\overline{W}$ = 1) again;

h) The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;

i) Master transmits 8 bits of data to register which needs to be read;

j) The slave device sends an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

k) The device automatically increment register address once after sent each acknowledge bit (ACK);

l) The master device generates the STOP state to end the data transmission.

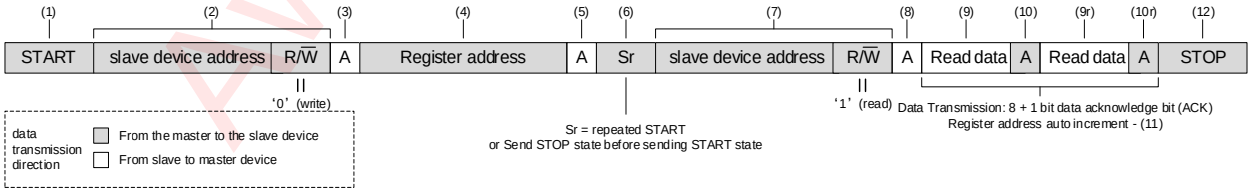


Figure 15 Reading process

Clock

Source of system clock: internal high-speed clock (HOSC) and external pin clock (EOSC, multiplexing INTN1/EOSC pin). AW8687x incorporates two highly stable internal oscillator, which are provided HOSC and LOSC respectively. HOSC can be configured as 6M or 8M through registers. LOSC is the clock of low power

consumption module, which is used for SWDT timing wake-up.

As shown in Figure 16, the osc_clk_sel signal is used to select HOSC or EOSC. The system clock is obtained by frequency division of the selected clock.

Before configuring the clock selection signal, the clock enable should be configured first. The system will give priority to the enabled clock. ADC clock uses the system clock.

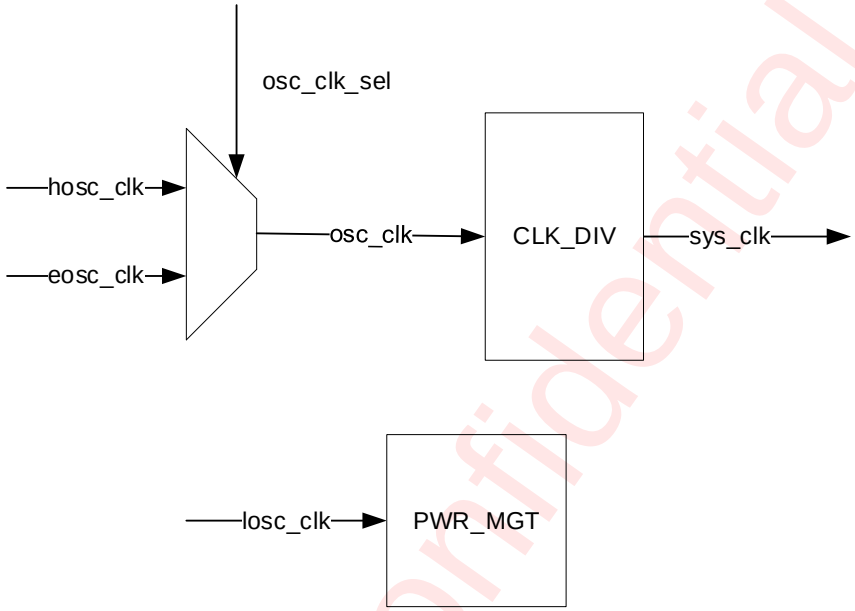


Figure 16 Clock Tree

System Control and PINS

Master can configure the way of chip entering low power consumption mode and clearing wake-up request through I²C. After chip is awakened, the wake-up request signal needs to be cleared if the system wants to enter low power consumption mode again. System control module can configure the delay time of automatic trigger AFE in the operation state, and the AFE will be triggered immediately after entering operation state.

The interrupts produced in the operation state, including AFE interrupt, SWDT interrupt, WAKEUP interrupt, force event interrupt and so on, can be output through interrupt pin INTN1/EOSC and INTN2/WAKE_UP. The output enable of each interrupt can be configured and the effective level of interrupt output can be configured. INTN2/WAKE_UP is used as wake-up pin in low power consumption mode and its wake-up effective level can be configured. It should be noted that since the wake-up function multiplexes INTN2/WAKE_UP, the effective level of the interrupt output should be consistent with the wake-up active level, and the recommended configuration is low level active (default configuration).

SCL, SDA, INTN1/EOSC, INTN2/WAKE_UP, AINP1/PWM_OUT1 and AINN1/PWM_OUT2 are multiplexed as IO pins, and its analog characteristics can be configured through registers.

- SCL is open drain output. There is no pull-up resister or pull-down resister in the chip. The input can be configured with the enable of Schmidt trigger and fast mode. It is the SCL pin of I²C interface.
- SDA is open drain output. There is no pull-up resister or pull-down resister in the chip. The input can be configured with the enable of Schmidt trigger and fast mode. It is the SDA pin of I²C interface.
- INTN1/EOSC is open drain output. There is no pull-up resister or pull-down resister in the chip. The input can be configured with the enable of Schmidt trigger and fast mode. It is the interrupt output pin, which can be multiplexed as input pin of external clock.

- INTN2/WAKE_UP is open drain output. There is no pull-up resister or pull-down resister in the chip. The input can be configured with the enable of Schmidt trigger and fast mode. It is the interrupt output pin and wake-up pin.
- AINP1/PWM_OUT1 can be configured as differential signal positive input port. When the PWM output mode is enabled, It also can be an output port in push-pull or open-drain.
- AINN1/PWM_OUT2 can be configured as differential signal negative input port. When the PWM output mode is enabled, It also can be an output port in push-pull or open-drain.

Low Power Consumption and SWDT

When the chip enters low power consumption mode, it can be awakened by SWDT in the 1.5V domain, or can be configured to wake up through I²C and INTN2/WAKE_UP. HOSC and VS are automatically turned off, LOSC can choose to turn off. If you turn off LOSC and disable the wake-up method through I²C or INTN2/WAKE_UP, the system will automatically turn on LOSC forcibly.

Low power consumption mode	**Power Up**	**Work**	**Deep Sleep1 LDO open LOSC open**	**Deep Sleep2 LDO open LOSC close**
HOSC+BIAS	open	open	close	close
LOSC	open	open	open	close
SWDT	close	can configure	open	open
LDO	open	open	open	open
AFE module（ PGA+ ADC + DAC + VS）	close	Switch is configurable	close	close
AFE+SYS configuration + ALGO configuration	/	Retain configuration	Retain configuration	Retain configuration
Awakening conditions	/	/	I²C(configurable) INTN2/WAKE_UP (configurable) SWDT	I²C(configurable) INTN2/WAKE_UP (configurable) In Deep Sleep2, if both I²C wake-up and INTN2/WAKE_UP wake-up are turned off, LOSC and SWDT wake-up will be forced to open.

- Four low-power mode
- Send I²C command to enter low-power mode immediately
- Two ways to enter low-power mode after the delay T1
  - Filter interrupt trigger
  - Trigger after reading AFE data register
- SWDT
  - Working under 1.5V domain power
  - The clock source is LOSC, 32kHz

- 16 bit counter, wake up time T2 configurable

* T1 = GO_STDBY_DLY [23:0]/F_{sys} , T2 = LD_SWDT_CNT[15:0]/F_{lclk} = LD_SWDT_CNT[15:0]*32 ms.
F_{sys} indicates the frequency of system clock(can be configured by HOSC_SEL and CLK_DIV register).
F_{lclk} indicates the frequency of LOSC(32kHz).

AFE

The AFE module include two PGAs(Programmable Gain Amplifier), one 12-bit DAC and one 14-bit ADC.

- AW86874 including 4 external sensor inputs and 1 internal input (2 channels for external sensor inputs can be configured with external impedance self-checking, and the single-ended internal channel are used to measure temperature). AW86872 including 2 external sensor inputs and 1 internal input.
- Provide 2 working modes.
  - Single cycle scan mode : Complete a conversion on all designated channels.
  - Finite cycle scan mode : Each channel switches to the next channel after a specified number of conversions.
- Conditions for starting A/D conversion
  - Software writes 1 to ADST bit.
  - Timer trigger (can be configured to enable).
- The conversion result can be compared with the specified value, the user can set whether to generate an interruption when matching.
- Built-in two press detection modules, which can detect the press events of two channels at the same time and generate interruptions.
- Built-in Level 2 PGA, The first stage PGA gain coefficient can be configured as 1/16/32, The second stage PGA gain coefficient can be configured as 1/2/3/4/5/6/7/8.
- Built-in 12-bit DAC for offset voltage calibration.
- Built-in 14-bit SAR ADC, up to 200kHz SPS, and the sampling can be switched by modifying OSC_FREQ_SEL register.
- ADC reference voltage VREF is configurable: 2.4V/2.8V/3.0V/3.1V/VDD.
- In general, AW8687x need to be connected to differential inputs. If a single ended application is used, it can be considered to do so by mapping one of the pins to a fixed voltage through MUX, such as VDD/2, VS/2, GND, etc. The MUX of the other pin remains mapped to the sensor. Then calculate the final measured single ended voltage and add the fixed voltage back.
- When PGA1 is set to 1 or disabled, the function of DAC will be automatically turned off.

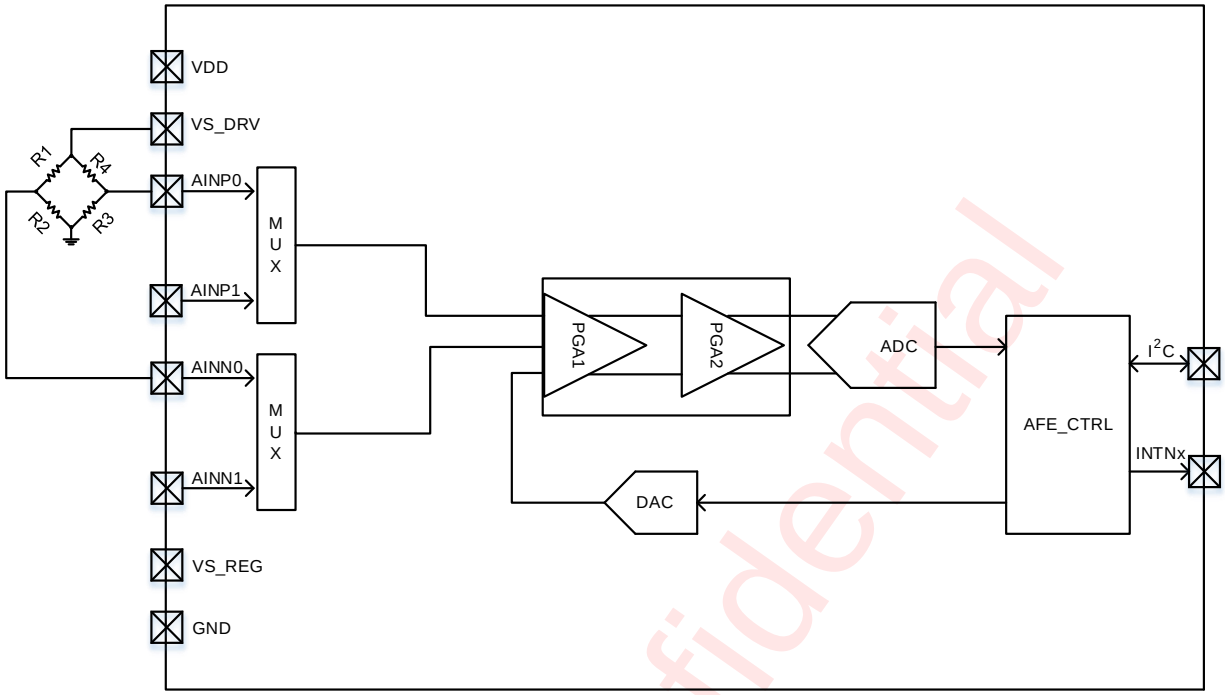


Figure 17 AFE Function Block Diagram

Algorithm

To better support Force Touch, the ASIC CHIP integrates an Algorithm module for press recognition. The Algorithm can support up to three channels for press recognition, with two channels sharing a set of algorithm parameters. And it can also support adding a reference channel for auxiliary detection. These can be achieved by configuring the registers of the DSP module in the register table.

The Algorithm needs to be used in conjunction with the low-power mode of the chip. When we enable the AFE module and algorithm module, the data converted by AFE will be automatically transmitted to the algorithm. And algorithm can output diff_code, base_code and press flag.

The main controller can identify the pressing status by monitoring of INTNx pin level or querying the chip register through I²C.

Register Configuration

Register List

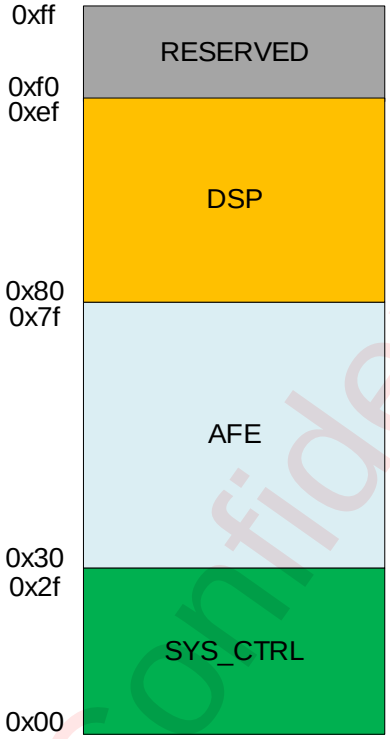


Figure 18 AW8687x Register Address Distribution

SYS

ADDR	NAME	R/W	Description	Default
0x00	**CHIP_ID**	**RO**	chip identification register,soft reset register	0x7x
0x01	**WR_UNLOCK**	**R/W**	system register write unlock register	0x00
0x02	**GNR_CFG**	**R/W**	I^2C general address configuration register	0x00
0x03	**SYS_CFG**	**R/W**	system configuration register	0x13
0x04	**OSC_CLK_DIV**	**R/W**	OSC clk division register	0x01
0x05	**EF_CLK_DIV**	**R/W**	efuse clk division register	0x06
0x06	**ADC_CLK_DIV**	**R/W**	ADC clk division register	0x01
0x07	**CHOP_DIV_SEL**	**R/W**	chop clk division register	0x00
0x08	**SYS_ST**	**RO**	system state register	0x2D
0x0A	**SWDT_CNT1**	**RO**	swdt counter current number register [15:8]	0x0B
0x0B	**SWDT_CNT0**	**RO**	swdt counter current number register [7:0]	0xB7
0x0C	**LD_SWDT_CNT1**	**R/W**	swdt delay counter load data register [15:8]	0x0B
0x0D	**LD_SWDT_CNT0**	**R/W**	swdt delay counter load data register [7:0]	0xB7
0x0E	**SWDT_CFG**	**R/W**	swdt configuration register	0x04
0x0F	**WKUP_REQ**	**RO**	wakeup request register	0x00

ADDR	NAME	R/W	Description	Default
0x10	GO_STDBY_DLY	R/W	go standby delay time register	0x00
0x11	GO_STDBY_CFG	R/W	go standby configuration register	0x08
0x12	INTR_MASK0	R/W	interrupt mask register 0	0x50
0x13	INTR_MASK1	R/W	interrupt mask register 1	0x60
0x14	INTR_STAT	RO	interrupt state register	0x00
0x18	ANA_ST	RO	analog state register	0x02
0x19	VS_CFG	R/W	vs voltage configuration register	0x0A
0x1A	PAD_ADJ0	R/W	pad adjustment configuration register 0	0xC0
0x1E	PWM_CTRL0	R/W	PWM control register 0	0x50
0x1F	PWM_CTRL1	R/W	PWM control register 1	0x22
AFE				
ADDR	**NAME**	**R/W**	**Description**	**Default**
0x3D	USCHEN	R/W	Unused sensor channel selection register	0x00
0x3E	ADCHEN	R/W	ADC channel enable register	0x01
0x3F	CHMUX	R/W	channel configuration selection register	0x00
0x40	ADCHCR0_0	R/W	ADC channel configuration register0_0	0x00
0x41	ADCHCR0_1	R/W	ADC channel configuration register0_1	0x43
0x42	ADCHCR0_2	R/W	ADC channel configuration register0_2	0x10
0x43	ADCHCR0_3	R/W	ADC channel configuration register0_3	0x10
0x44	ADCHCR1_0	R/W	ADC channel configuration register1_0	0x1C
0x45	ADCHCR1_1	R/W	ADC channel configuration register1_1	0x23
0x46	ADCHCR1_2	R/W	ADC channel configuration register1_2	0x00
0x47	ADCHCR1_3	R/W	ADC channel configuration register1_3	0x41
0x48	DACHCR_0	R/W	DAC channel configuration register0	0x95
0x4A	DACHCR_2	R/W	DAC channel configuration register2	0x0B
0x4C	DACHDR_0	R/W	DAC channel data register0	0x00
0x4D	DACHDR_1	R/W	DAC channel data register1	0x00
0x4E	DACHDR_2	R/W	DAC channel data register2	0x00
0x4F	DACHDR_3	R/W	DAC channel data register3	0x20
0x50	ADMCR_0	R/W	ADC mode control register0	0xDB
0x51	ADMCR_1	R/W	ADC mode control register1	0x00
0x52	ADTDR0_0	R/W	ADC trigger delay control register0_0	0x80
0x53	ADTDR0_1	R/W	ADC trigger delay control register0_1	0x02
0x54	ADTDR1_0	R/W	ADC trigger delay control register1_0	0x40
0x55	ADTDR1_1	R/W	ADC trigger delay control register1_1	0x01
0x56	ADSR	RO	ADC status register	0x00
0x57	DASR	RO	DAC status register	0x00
0x5C	AUOSCR0	R/W	automatic calibration configuration register0	0x00
0x5D	AUOSCR1	R/W	automatic calibration configuration register1	0x00

ADDR	NAME	R/W	Description	Default
0x60	FILT_CFG	R/W	filter configuration register	0x10
0x61	AVG_ST	RO	average status register	0x0B
0x70	RAWDATA0	RO	ADC raw data register0	0x00
0x71	RAWDATA1	RO	ADC raw data register1	0x00
0x72	RAWDATA2	RO	ADC raw data register2	0x00
0x73	RAWDATA3	RO	ADC raw data register3	0x00
0x74	RAWDATA4	RO	ADC raw data register4	0x00
0x75	RAWDATA5	RO	ADC raw data register5	0x00
0x76	RAWDATA6	RO	ADC raw data register6	0x00
0x77	RAWDATA7	RO	ADC raw data register7	0x00
0x78	RAWDATA8	RO	ADC raw data register8	0x00
0x79	RAWDATA9	RO	ADC raw data register9	0x00
DSP				
ADDR	NAME	R/W	Description	Default
0x80	DSP_CH_EN	R/W	DSP channel enable register	0x01
0x81	DSP_OS0	R/W	DSP offset register0	0x0F
0x82	DSP_OS1	R/W	DSP offset register1	0xFF
0x83	DSP_INTR_SEL	R/W	DSP interrupt configuration register	0x04
0x90	DSP_CHA_LAMDA1	R/W	DSP channel A lamda1 register	0x73
0x91	DSP_CHA_LAMDA2	R/W	DSP channel A lamda2 register	0x08
0x92	DSP_CHA_DRIFT0	R/W	DSP channel A drift register0	0x00
0x93	DSP_CHA_DRIFT1	R/W	DSP channel A drift register1	0x1E
0x94	DSP_CHA_FORCE0	R/W	DSP channel A force register0	0x00
0x95	DSP_CHA_FORCE1	R/W	DSP channel A force register1	0xC8
0x96	DSP_CHA_FORCE2	R/W	DSP channel A force register2	0x00
0x97	DSP_CHA_FORCE3	R/W	DSP channel A force register3	0x00
0x98	DSP_CHA_DELAY	R/W	DSP channel A delay register	0x33
0x99	DSP_CHA_TIMEOUT0	R/W	DSP channel A timeout register0	0x01
0x9A	DSP_CHA_TIMEOUT1	R/W	DSP channel A timeout register1	0x2C
0x9B	DSP_CHA_RECOIL	R/W	DSP channel A recoil time register	0x14
0x9C	DSP_CHA_STABLE	R/W	DSP channel A stable time register	0x64
0x9D	DSP_CHA_RELEASE	R/W	DSP channel A release time register	0xFF
0x9E	DSP_CHA_CFG	R/W	DSP channel A configuration register	0x03
0x9F	DSP_CHA_INTR_MASK	R/W	DSP channel A interrupt mask register	0x10
0xA0	DSP_CHA_INTR_CLR	R/W	DSP channel A interrupt clear register	0x00
0xA1	DSP_CHA_INTR_FLAG	RO	DSP channel A interrupt flag register	0x00
0xA2	DSP_CHA_STAT	RO	DSP channel A status register	0x00
0xB0	DSP_CHB_LAMDA1	R/W	DSP channel B lamda1 register	0x73
0xB1	DSP_CHB_LAMDA2	R/W	DSP channel B lamda2 register	0x08

ADDR	NAME	R/W	Description	Default
0xB2	**DSP_CHB_DRIFT0**	**R/W**	DSP channel B drift register0	0x00
0xB3	**DSP_CHB_DRIFT1**	**R/W**	DSP channel B drift register1	0x1E
0xB4	**DSP_CHB_FORCE0**	**R/W**	DSP channel B force register0	0x00
0xB5	**DSP_CHB_FORCE1**	**R/W**	DSP channel B force register1	0xC8
0xB6	**DSP_CHB_FORCE2**	**R/W**	DSP channel B force register2	0x00
0xB7	**DSP_CHB_FORCE3**	**R/W**	DSP channel B force register3	0x00
0xB8	**DSP_CHB_DELAY**	**R/W**	DSP channel B delay register	0x33
0xB9	**DSP_CHB_TIMEOUT0**	**R/W**	DSP channel B timeout register0	0x01
0xBA	**DSP_CHB_TIMEOUT1**	**R/W**	DSP channel B timeout register1	0x2C
0xBB	**DSP_CHB_RECOIL**	**R/W**	DSP channel B recoil time register	0x14
0xBC	**DSP_CHB_STABLE**	**R/W**	DSP channel B stable time register	0x64
0xBD	**DSP_CHB_RELEASE**	**R/W**	DSP channel B release time register	0xFF
0xBE	**DSP_CHB_CFG**	**R/W**	DSP channel B configuration register	0x03
0xBF	**DSP_CHB_INTR_MASK**	**R/W**	DSP channel B interrupt mask register	0x10
0xC0	**DSP_CHB_INTR_CLR**	**R/W**	DSP channel B interrupt clear register	0x00
0xC1	**DSP_CHB_INTR_FLAG**	**RO**	DSP channel B interrupt flag register	0x00
0xC2	**DSP_CHB_STAT**	**RO**	DSP channel B status register	0x00
0xDE	**DSP_CHC_CFG**	**R/W**	DSP channel C configuration register	0x03
0xDF	**DSP_CHC_INTR_MASK**	**R/W**	DSP channel C interrupt mask register	0x10
0xE0	**DSP_CHC_INTR_CLR**	**R/W**	DSP channel C interrupt clear register	0x00
0xE1	**DSP_CHC_INTR_FLAG**	**RO**	DSP channel C interrupt flag register	0x00
0xE2	**DSP_CHC_STAT**	**RO**	DSP channel C status register	0x00
0xE4	**DSP_DATA0**	**RO**	DSP data register0	0x00
0xE5	**DSP_DATA1**	**RO**	DSP data register1	0x00
0xE6	**DSP_DATA2**	**RO**	DSP data register2	0x00
0xE7	**DSP_DATA3**	**RO**	DSP data register3	0x00
0xE8	**DSP_DATA4**	**RO**	DSP data register4	0x00
0xE9	**DSP_DATA5**	**RO**	DSP data register5	0x00
0xEA	**DSP_DATA6**	**RO**	DSP data register6	0x00
0xEB	**DSP_DATA7**	**RO**	DSP data register7	0x00
0xEC	**DSP_DATA8**	**RO**	DSP data register8	0x00
0xED	**DSP_DATA9**	**RO**	DSP data register9	0x00
0xEE	**DSP_DATA10**	**RO**	DSP data register10	0x00
0xEF	**DSP_DATA11**	**RO**	DSP data register11	0x00

Register Detailed Description

CHIP_ID: (Address 00h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	CHIPID	RO	CHIP_ID：0x72 for AW86872, and 0x74 for AW86874； Write 0xAA to this register to soft reset chip	0x7x

WR_UNLOCK: (Address 01h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	WR_UNLOCK_0	R/W	write 0xA5 to unlock system registers write operation，write 0x00 to lock system registers write operation，only bit 0 available when read 0：lock 1：unlock successfully	0

GNR_CFG: (Address 02h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	EN_GNR	R/W	Enable I²C slave general address access function	0
6	EN_GNR_ACK	R/W	Enable general address access ack when I²C slave general address access function enabled	0
5:0	GNR_ADDR	R/W	General address value when I²C slave general address access function enabled	0

SYS_CFG: (Address 03h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	OSC_FREQ_SEL	R/W	Internal HOSC frequence setting: 0: OSC frequence 6M; 1: OSC frequence 8M;	0
6	OSC_SEL	R/W	clock select configuration: 0: internal HOSC; 1: external clock from multi-purpose IO;	0
5	EN_EOSC	R/W	External clock enable configuration; 0: disable 1: enable	0
4	EN_HOSC	R/W	Internal high speed clock enable configuration;	1
3	Reserved	R/W	Not used	0
2	REG_DIV_EN	R/W	osc clock frequency division enable configuration: 0: clock division setting by work_mode; 1: clock division setting by OSC_CLK_DIV(0x04);	0

1:0	WORK_MODE	R/W	work mode configuration: 0x0: low frequency press detection mode; 0x1: conventional ADC data acquisition mode; 0x2: press detection mode0; 0x3: press detection mode1（forcibly enabled osc clock frequency division function,, no matter what reg_div_en is）;	3

OSC_CLK_DIV: (Address 04h)

Bit	Symbol	R/W	Description	Default
7:0	OSC_CLK_DIV_0	R/W	OSC clock division configuration for normal mode: 0x00-0x01: keep source frequence; others: 1/OSC_CLK_DIV * frequence;	1

EF_CLK_DIV: (Address 05h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
7:0	EF_CLK_DIV_0	R/W	efuse access clock configuration: 0x00-0x01: keep source frequence; others: 1/EF_CLK_DIV * frequence;	6

ADC_CLK_DIV: (Address 06h)

Bit	Symbol	R/W	Description	Default
7:0	ADC_CLK_DIV_0	R/W	ADC module clock configuration: 0x00-0x01: keep source frequence; others: 1/ADC_CLK_DIV * frequence;	1

CHOP_DIV_SEL: (Address 07h)

Bit	Symbol	R/W	Description	Default
7:2	Reserved	R/W	Not used	0
1:0	CHOP_DIV_SEL_0	R/W	Chop module clock configuration: 0x0: 1/6 * osc frequence; 0x1: 1/8 * osc frequence; 0x2: 1/10 * osc frequece; 0x3: 1/12 * osc frequece;	0

SYS_ST: (Address 08h)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0
6	OSC_CLK_SEL	RO	osc clock selection indication 0：HOSC selection 1：EOSC selection	0
5	OSC_CLK_OK	RO	osc clock OK indication 0：not ready 1：ready	1
4	EOSC_CLK_OK	RO	extenal clock OK indication 0：not ready 1：ready	0

3	HOSC_CLK_OK	RO	internal high freq clock OK indication 0：not ready 1：ready	1
2	LOSC_CLK_OK	RO	internal low freq clock OK indication 0：not ready 1：ready	1
1:0	SYS_CTR_STATE	RO	system work state 00：power up status 01：active status 11：standby status 10：reserved	1

SWDT_CNT1: (Address 0Ah)

Bit	Symbol	R/W	Description	Default
7:0	SWDT_CNTH	RO	SWDT counter high 8bits value	0x0B

SWDT_CNT0: (Address 0Bh)

Bit	Symbol	R/W	Description	Default
7:0	SWDT_CNTL	RO	SWDT counter low 8bits value	0xB7

LD_SWDT_CNT1: (Address 0Ch)

Bit	Symbol	R/W	Description	Default
7:0	LD_SWDT_CNTH	R/W	Load SWDT counter high 8bits value	0x0B

LD_SWDT_CNT0: (Address 0Dh)

Bit	Symbol	R/W	Description	Default
7:0	LD_SWDT_CNTL	R/W	Load SWDT counter low 8bits value	0xB7

SWDT_CFG: (Address 0Eh)

Bit	Symbol	R/W	Description	Default
7	WRCLR_WKUP_REQ	R/W	write bit to 1 to clear wakeup request after request	0
6	CLR_WKUP_MOD	R/W	clear wakeup mode: 0: write wrclr_wkup_req bit to clear wakeup request; 1: clear wakeup request after request automatically;	0
5	I2C_WKUP_MASK	R/W	I^2C wakeup mask: 0: mask I^2C wakeup, I^2C wakeup disable; 1: unmask I^2C wakeup, I^2C wakeup enable;	0
4	GPIO_WKUP_MASK	R/W	GPIO wakeup mask: 0: mask GPIO wakeup, GPIO wakeup disable; 1: unmask GPIO wakeup, GPIO wakeup enable;	0
3	GPIO_INTR_MOD	R/W	GPIO wakeup mode: 0: low level to trig wakeup; 1: high level to trig wakeup;	0
2	EN_LOAD	R/W	SWDT counter value load enable	1
1	EN_SWDT	R/W	SWDT function enable	0

			EN_LOAD=0 , EN_SWDT=0 , SWDT only counts in standby and does not automatically update the SWDT count configuration ; EN_LOAD=0 , EN_SWDT=1 , SWDT counts in standby and active, does not automatically update the SWDT count configuration ; EN_LOAD=0 , EN_SWDT=1 , SWDT only counts in standby and automatically updates the SWDT count configuration in active mode ; EN_LOAD=1 , EN_SWDT=1 , SWDT only counts in standby and automatically updates the SWDT count configuration in active mode ;	
0	EN_SWDT_INTR	R/W	enable SWDT interrupt when SWDT counter hit	0

WKUP_REQ: (Address 0Fh)

Bit	Symbol	R/W	Description	Default
7:3	Reserved	RO	Not used	0
2	I2C_WKUP_REQ	RO	I^2C wakeup request	0
1	GPIO_WKUP_REQ	RO	GPIO wakeup request	0
0	SWDT_WKUP_REQ	RO	SWDT wakeup request	0

GO_STDBY_DLY: (Address 10h)

Bit	Symbol	R/W	Description	Default
7:2	GO_STDBY_DLY_0	R/W	auto enter standby delay base time go_standby_dly_time = ({go_standby_dly,4'd0} << go_staby_dly_gain) * sys_clk	0
1:0	GO_STDBY_DLY_GAIN	R/W	1x/2x/4x/8x base time delay before auto enter standby	0

GO_STDBY_CFG: (Address 11h)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	R/W	Not used	0
4	CMD_STDBY_REQ	R/W	Command enter standby, write 1 to request enter standby	0
3	STDBY_EN_LOSC	R/W	enable LOSC when enter standby	1
2:0	AUTO_STDBY_MOD	R/W	0b001: enter standby after adc data average calculation; 0b010: enter standby after configurated channel data read out done; 0b111: enter standby after either adc data average calculation done or configurated channel data read out done; others: no auto standby mode	0

INTR_MASK0: (Address 12h)

Bit	Symbol	R/W	Description	Default
7	INTR_LEVEL0	R/W	interrupt available level: 0: low level 1: high level	0

6	INTN1_EN_OD	R/W	INTN1 enable OD	1
5	FORCE_INTR2_UNMASK0	R/W	Force event interrupt1 unmask for INTN1: 0: disable force intr[1] interrupt; 1: enable force intr[1] interrupt;	0
4	FORCE_INTR1_UNMASK0	R/W	Force event interrupt0 unmask for INTN1: 0: disable force intr[0] interrupt; 1: enable force intr[0] interrupt;	1
3	SWDT_INTR_UNMASK0	R/W	SWDT interrupt unmask: 0: disable SWDT interrupt; 1: enable SWDT interrupt;	0
2	WKUP_REQ_UNMASK0	R/W	WAKEUP Request unmask: 0: disable wakeup request; 1: enable wakeup request;	0
1	FLT_INTR_UNMASK0	R/W	Filter Request unmask: 0: disable wakeup request; 1: enable wakeup request;	0
0	AFE_INTR_UNMASK0	R/W	AFE Request unmask: 0: disable wakeup request; 1: enable wakeup request;	0

INTR_MASK1: (Address 13h)

Bit	Symbol	R/W	Description	Default
7	INTR_LEVEL1	R/W	interrupt available level: 0: low level 1: high level	0
6	INTN2_EN_OD	R/W	INTN2 enable OD	1
5	FORCE_INTR2_UNMASK1	R/W	Force event interrupt1 unmask for INTN2: 0: disable force intr[1] interrupt; 1: enable force intr[1] interrupt;	1
4	FORCE_INTR1_UNMASK1	R/W	Force event interrupt0 unmask for INTN2: 0: disable force intr[0] interrupt; 1: enable force intr[0] interrupt;	0
3	SWDT_INTR_UNMASK1	R/W	SWDT interrupt unmask: 0: disable SWDT interrupt; 1: enable SWDT interrupt;	0
2	WKUP_REQ_UNMASK1	R/W	WAKEUP Request unmask: 0: disable wakeup request; 1: enable wakeup request;	0
1	FLT_INTR_UNMASK1	R/W	Filter Request unmask: 0: disable wakeup request; 1: enable wakeup request;	0
0	AFE_INTR_UNMASK1	R/W	AFE Request unmask: 0: disable wakeup request; 1: enable wakeup request;	0

INTR_STAT: (Address 14h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	FORCE_INTR2	RO	Force event2 interrupt:	0
4	FORCE_INTR1	RO	Force event1 interrupt:	0
3	SWDT_INTR	RO	SWDT interrupt	0
2	WKUP_REQ_0	RO	Wakeup interrupt	0

1	FLT_INTR	RO	Filter interrupt	0
0	AFE_INTR	RO	AFE interrupt	0

ANA_ST: (Address 18h)

Bit	Symbol	R/W	Description	Default
7:2	Reserved	RO	Not used	0
1	VBG_OK	RO	VBG OK indication	1
0	LDO_OK	RO	LDO OK indication	0

VS_CFG: (Address 19h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	VS_ADJL	R/W	vs_ref voltage adjustment 0: 1.219V 1: 0.609V	0
4	VS_SELVDD	R/W	vs voltage specified as VDD 0: disable 1: enable	0
3	PJ_VS	R/W	vs mode selection 0: cvs discharge 1: cvs don't discharge	1
2	VS_HL	R/W	vs high voltage enable 1: vs voltage increase 2V	0
1:0	VS_ADJ	R/W	vs voltage adjustment VS_ADJL=0, VS_SELVDD=0, VS_HL=0 0b00: 1.8V 0b01: 2.4V 0b10: 2.8V 0b11: 3.1V VS_ADJL=1, VS_SELVDD=0, VS_HL=0 0b00: 0.9V 0b01: 1.2V 0b10: 1.4V 0b11: 1.505V VS_ADJL=x, VS_SELVDD=1, VS_HL=x vs= VDD VS_ADJL=0, VS_SELVDD=0, VS_HL=1 0b00: 3.8V 0b01: 4.4V 0b10: 4.8V 0b11: 5.1V VS_ADJL=1, VS_SELVDD=0, VS_HL=1 0b00: 1.9V 0b01: 2.2V 0b10: 2.4V 0b11: 2.505V	2

PAD_ADJ0: (Address 1Ah)

Bit	Symbol	R/W	Description	Default
7	SEL_TEMP	R/W	temp sense enable 0: disable 1: enable	1
6	EN_VLDOH	R/W	LDO high voltage enable 1:LDO voltage increase 60mV	1

5	CTRL_ACTI	R/W	LDO active state output current configuration 0: normal 1: decrease 43μA	0
4	Reserved	R/W	Not used	0
3:2	EN_OD_DRV	R/W	open drain output mode selection when EN_OD_DRV=1 0b00: AINP1 push pull output ,AINN1 push pull output 0b01: AINP1 open drain output ,AINN1 push pull output 0b10: AINP1 push pull output ,AINN1 open drain output 0b11: AINP1 open drain output ,AINN1 open drain output	0
1:0	EN_DRV_OUT	R/W	IO output mode selection 0bx1: enable AINP1 output mode 0b1x: enable AINN1 output mode	0

PWM_CTRL0: (Address 1Eh)

Bit	Symbol	R/W	Description	Default
7	Reserved	R/W	Not used	0
6:4	PWM_PRD	R/W	PWM period , PWM period= (PWM_PRD+1) * SYS_CLK	5
3:2	Reserved	R/W	Not used	0
1:0	PWM_EN	R/W	PWM output enable 0bx1: PWM0 enable 0b1x: PWM1 enable	0

PWM_CTRL1: (Address 1Fh)

Bit	Symbol	R/W	Description	Default
7	Reserved	R/W	Not used	0
6:4	PWM_DUTY1	R/W	PWM1 duty , duty = (PWM_DUTY+1)/(PWM_PRD+1)	2
3	Reserved	R/W	Not used	0
2:0	PWM_DUTY0	R/W	PWM0 duty , duty = (PWM_DUTY+1)/(PWM_PRD+1)	2

USCHEN: (Address 3Dh)

Bit	Symbol	R/W	Description	Default
7:5	RESERVED	RO	Not used	0x0
4:0	UNSENSOR_CH_EN	R/W	Unused sensor Channel selection. 0: not select 1: select	0x0

ADCHEN: (Address 3Eh)

Bit	Symbol	R/W	Description	Default
7:5	RESERVED	RO	Not used	0x0
4:0	ADCH_EN	R/W	Channel Enable 0: disable 1: enable	0x1

CHMUX: (Address 3Fh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:3	RESERVED	RO	Not used	0x0
2:0	CHMUX_0	R/W	Channel Configuration Selection(5 channels in total)	0x0

ADCHCR0_0: (Address 40h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	RESERVED	RO	Not used	0x0
6:4	PD_AINP	R/W	CHx sensor positive input selection 0b000: sensor0 positive 0b001: sensor1 positive 0b010: sensor2 positive 0b011: sensor3 positive X from 0 to 4	0x0
3	RESERVED	RO	Not used	0x0
2:0	PD_AINN	R/W	CHx sensor negative input selection 0b000: sensor0 negative 0b001: sensor1 negative 0b010: sensor2 positive 0b011: sensor3 positive X from 0 to 4	0x0

ADCHCR0_1: (Address 41h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	RESERVED	RO	Not used	0x0
6	VREF_GEN_SEL	R/W	ADC reference voltage selection 0: VDD 1: VRP	0x1
5:4	VREF_SEL	R/W	VRP voltage selection 0b00: 2.4v 0b01: 2.8v 0b10: 3.0v 0b11: 3.1v	0x0
3	SUB_OS_EN	R/W	offset Residual cancellation enable signal 0: no elimination of residuals 1: elimination of residuals enable	0x0
2	PD_DOUBLE_VIN	R/W	in ADC single-ended mode, turn off the double-ended input 0: double-ended input 1: single-ended input	0x0
1	EN_DIFF	R/W	ADC input working mode 0: single-ended mode 1: differential mode forcibly	0x1
0	PD_SW_IN	R/W	VS_DRV analog switch control 0: strobe vs 1: disable	0x1

ADCHCR0_2: (Address 42h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	RESERVED	RO	Not used	0x0

6:0	SN_MUX	R/W	Negative terminal of DC voltage channel. 0b1000000: vdd/2->Negative terminal of PGA 0b0100000: sensor Negative input channel -> Positive terminal of PGA 0b0010000: sensor Negative input channel -> Negative terminal of PGA 0b0001000: vtemp -> Negative terminal of PGA 0b0000100: vs -> Negative terminal of PGA 0b0000010: gnd -> Negative terminal of PGA 0b0000001: vs/2 -> Negative terminal of PGA	0x10

ADCHCR0_3: (Address 43h)

Bit	Symbol	R/W	Description	Default
7	RESERVED	RO	Not used	0x0
6:0	SP_MUX	R/W	Positive terminal of DC voltage channel. 0b1000000: vdd/2 -> Positive terminal of PGA 0b0100000: sensor Positive input channel -> Negative terminal of PGA 0b0010000: sensor Positive input channel -> Positive terminal of PGA 0b0001000: vtemp -> Positive terminal of PGA 0b0000100: vs -> Positive terminal of PGA 0b0000010: gnd -> Positive terminal of PGA 0b0000001: vs/2 -> Positive terminal of PGA	0x10

ADCHCR1_0: (Address 44h)

Bit	Symbol	R/W	Description	Default
7:6	RESERVED	RO	Not used	0x0

5:0	ADC_IBIAS	R/W	ADC BIAS[2:0] main current control 0b000: 1μA 0b001: 1.25μA 0b010: 1.5μA 0b011: 1.75μA 0b100: 2μA 0b101: 2.25μA 0b110: 2.5μA 0b111: 2.75μA ADC BIAS[3] second level amplifier current control 0b0:IREF*1 0b1:IREF*2 ADC BIAS[5:4] IREFN control for REF_GEN module 0b00:2μA 0b01:3μA 0b10:4μA 0b11:5μA	0x1C

ADCHCR1_1: (Address 45h)

Bit	Symbol	R/W	Description	Default
7	RESERVED	RO	Not used	0x0
6:4	GAIN_PGA1	R/W	First level of PGA gain selection 0b000: 1 0b001: 16 0b010: 32	0x2
3	RESERVED	RO	Not used	0x0
2:0	GAIN_PGA2	R/W	second level of PGA gain selection 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

ADCHCR1_2: (Address 46h)

Bit	Symbol	R/W	Description	Default
7	RESERVED	RO	Not used	0x0
6	PD_PGA1	R/W	First level of PGA enable switch 1: disable 0: enable	0x0
5	PD_PGA2	R/W	second level of PGA enable switch 1: disable 0: enable	0x0

4	VCM_ADJ	R/W	PGA output common mode voltage selection 0: VDD/2 1: VDD/3	0x0
3	RESERVED	RO	Not used	0x0
2	SEL_FILTER_PA	R/W	multiplexing AINP2/AINN2 to external PGA1 filter cap 1: enable 0: disable	0x0
1	PD_FILTER	R/W	turn off the PGA filter 1: turn off 0: turn on	0x0
0	BW_FILTER	R/W	PGA RC filter output frequency selection 0b0:250kHz 0b1:150kHz	0x0

ADCHCR1_3: (Address 47h)

Bit	Symbol	R/W	Description	Default
7	RESERVED	RO	Not used	0x0
6:4	PGA_IBIASE	R/W	PGA module overall current selection 0b000: 1μA 0b001: 1.25μA 0b010: 1.5μA 0b011: 1.75μA 0b100: 2μA 0b101: 2.25μA 0b110: 2.5μA 0b111: 2.75μA	0x4
3:2	RESERVED	RO	Not used	0x0
1	EN_PASSBY	R/W	PGA bypass enable 0: disable 1: enable	0x0
0	EN_PGA	R/W	PGA enable switch 0: disable 1: enable	0x1

DACHCR_0: (Address 48h)

Bit	Symbol	R/W	Description	Default
7	EN_DAC_VIN	R/W	turn on DAC negative current input 0: turn off 1: turn on	0x1
6	DIR_DAC	R/W	DAC direction select 0: disable current direction 1: enable current direction	0x0
5	DIR_MODE0	R/W	DAC direction select 0: disable affect offset 1: enable affect offset	0x0
4	DIR_MODE1	R/W	DAC direction select 0: disable affect offset 1: enable affect offset	0x1

3:2	VDAC_RANGE	R/W	DAC calibration offset range PGA1 Gain≤64: 0b00: 0.1*VS 0b01:(0.1*VS)*1.5 0b10:(0.1*VS)*2 0b11:(0.1*VS)*2.5	0x1
1	MAN_EN_CAL	R/W	Enable digital DAC manual calibration loop operation 0: disable 1: enable	0x0
0	EN_DAC	R/W	enable calibration offset DAC 0: disable 1: enable	0x1

DACHCR_2: (Address 4Ah)

Bit	Symbol	R/W	Description	Default
7:5	UNVLD_TIMES	R/W	Invalid conversions 0b000: 0 0b001: 1 0b010: 2 0b011: 3 0b100: 4 0b101: 5 0b110: 6 0b111: 7	0x0
4	RM_SUBEXT_EN	R/W	Enable subextrme value auto removal for channel . If this bit enabled, sample time will add by 2, and the maximum and minimum value will be removed when average calculated. 0：disable 1：enable	0x0
3	RM_EXT_EN	R/W	Enable extreme value auto removal for channel . If this bit enabled, sample time will add by 2, and the maximum and minimum value will be removed when average calculated. 0：disable 1：enable	0x1
2:0	VALID_TIMES	R/W	Effective conversions 0b000：1 0b001：2 0b010：4 0b011：8 0b100：16 0b101：32 0b110：64 0b111：64	0x3

DACHDR_0: (Address 4Ch)				
Bits	**Symbol**	**R/W**	**Description**	**Default**
7:0	DA_CODE_L	R/W	D/A data register[7:0] ,which is used for DAC offset {DA_CODE_H[3:0],DA_CODE_L[7:0]}	0x0

DACHDR_1: (Address 4Dh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	RESERVED	RO	Not used	0x0
3:0	DA_CODE_H	R/W	D/A data register[11:8],which is used for DAC offset {DA_CODE_H[3:0],DA_CODE_L[7:0]}	0x0

DACHDR_2: (Address 4Eh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	AD_OS_L	R/W	ADC OFFSET residual. directly save the adc result[7:0] {AD_OS_H[5:0],AD_OS_L[7:0]}	0x0

DACHDR_3: (Address 4Fh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	RESERVED	RO	Not used	0x0
5:0	AD_OS_H	R/W	ADC OFFSET residual. directly save the adc result[13:8] {AD_OS_H[5:0],AD_OS_L[7:0]}	0x20

ADMCR_0: (Address 50h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	OVER_TIME_EN	R/W	Enable the sampling timeout function. 0:disable 1:Enable	0x1
6	CONT_EN	R/W	Enable continuous converting mode. In this mode, ADC will start new conversion after previous conversion end. 0：disable 1：enable	0x1
5	RESERVED	RO	Not used	0x0
4	CHAN_TEST_MODE	R/W	Sensor impedance detection mode selection 0：detect sensor impedance ratio mode 1：detect sensor impedance value mode	0x1
3	ADIE	R/W	A/D interrupt enable control. 0: disable 1: enable	0x1
2	TRGS_MODE	R/W	A/D conversion trigger source selection. 0: AD conversion is initiated by software ADST 1: AD conversion is initiated by work mode or software ADST	0x0
1	EN_AD_RST	R/W	Reset ADC after changing channel 0: disable 1: enable	0x1

0	EN_ADC	R/W	A/D enable control. 0: disable 1: enable	0x1

ADMCR_1: (Address 51h)

Bit	Symbol	R/W	Description	Default
7:1	RESERVED	RO	Not used	0x0
0	ADST	R/W	A/D conversion begins. ADST will be automatically cleared by hardware after conversion in Single conversion mode and single-cycle scan mode. A/D conversion will continue until the software writes 0 or the system resets in the wireless periodic scan mode. 0: end 1: start	0x0

ADTDR0_0: (Address 52h)

Bit	Symbol	R/W	Description	Default
7:0	ADC_WAIT0_L	R/W	ADC startup wait time firstly, included PGA startup wait time(unit is clock period, preferably greater T= (ADC_WAIT+1) * SYS_CLK	0x80

ADTDR0_1: (Address 53h)

Bit	Symbol	R/W	Description	Default
7:4	RESERVED	RO	Not used	0x0
3:0	ADC_WAIT0_H	R/W	ADC startup wait time firstly, included PGA startup wait time(unit is clock period, preferably greater T= (ADC_WAIT+1) * SYS_CLK	0x2

ADTDR1_0: (Address 54h)

Bit	Symbol	R/W	Description	Default
7:0	ADC_WAIT1_L	R/W	ADC startup wait time(unit is clock period, preferably greater T= (ADC_WAIT+1) * SYS_CLK	0x40

ADTDR1_1: (Address 55h)

Bit	Symbol	R/W	Description	Default
7:4	RESERVED	RO	Not used	0x0
3:0	ADC_WAIT1_H	R/W	ADC startup wait time(unit is clock period, preferably greater T= (ADC_WAIT+1) * SYS_CLK	0x1

ADSR: (Address 56h)

Bit	Symbol	R/W	Description	Default
7	BUSY	RO	ADC busy/free 0: free 1: busy	0x0
6:4	BUSY_CH	RO	current channel	0x0

3	RESERVED	RO	Not used	0x0
2	HIS_ADC_ERR	RO	ADC history conversion timeout. This bit will be clear by writing 1	0x0
1	CUR_ADC_ERR	RO	ADC current conversion timeout. This bit will be clear by writing 1 or ADC work	0x0
0	ADF	RO	The status of ADC transfer done	0x0

DASR: (Address 57h)

Bit	Symbol	R/W	Description	Default
7:5	AUTO_OS_STATUS	RO	Automatic calibration status	0x0
4	INN_AUTO_EN_CAL	RO	DSP automatic calibration status	0x0
3	HIS_OS_ERR	RO	History automatic calibration timeout. This bit will be clear by writing 1	0x0
2	CUR_OS_ERR	RO	Current automatic calibration timeout. This bit will be clear by writing 1 or automatic calibration work	0x0
1	AUTO_CAL_OK	RO	Automatic calibration successful flag	0x0
0	AUTO_CAL_DONE	RO	Automatic calibration end flag	0x0

AUOSCR0: (Address 5Ch)

Bit	Symbol	R/W	Description	Default
7	DAOSUP	R/W	DAC offset calibration update channel DACHDR register enable 0: disable 1: enable	0x0
6:4	WAIT_TIME_SEL	R/W	Automatic wait time selection T= (WAIT_TIME+1) * SYS_CLK 0b000：0 0b001：40 0b010：100 0b011：200 0b100：300 0b101：400 0b110：500 0b111：600	0x0
3	DISC_BYPASS	R/W	Bypass discharge 0: disable 1: enable	0x0
2:0	DISC_TIME_SEL	R/W	Discharge time selection T= (DISC_TIME+1) * SYS_CLK 0b000：0 0b001：10 0b010：20 0b011：40 0b100：100 0b101：160 0b110：200 0b111：300	0x0

AUOSCR1: (Address 5Dh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:1	RESERVED	RO	Not used	0x0
0	AUTO_EN_CAL	R/W	Enable digital DAC automatic calibration loop operation 0: disable 1: enable	0x0

FILT_CFG: (Address 60h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	FLT_WD_DONE	RO	Filter work done flag. This bit will be clear by writing 1 or enter into standby mode	0x0
6	SINGLE_PORT	RO	ADC single-ended mode for current filter channel 0: differential mode 1: single-ended mode	0x0
5	VLD_WD_SEL	R/W	Valid data width selection, which influence the register whose address is from 8'h70 to 8'h79 0:14bit 1:15bit	0x0
4	FLT_WD_EN	R/W	Filter work done interrupt enable control 0: disable 1: enable	0x1
3:1	REF_CH_CFG	R/W	Only for debug , must write 0.	0x0
0	REF_OFFSET_EN	R/W	Reference channel enable control 0: disable 1: enable	0x0

AVG_ST: (Address 61h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:5	CUR_CH	RO	Current channel for filter	0x0
4	SUB_CAL_S	RO	Enable subextreme value auto removal for current filter channel . If this bit enabled, sample time will add by 2, and the maximum and minimum value will be removed when average calculated. 0: disable 1: enable	0x0
3	CAL_S	RO	Enable extreme value auto removal for current filter channel . If this bit enabled, sample time will add by 2, and the maximum and minimum value will be removed when average calculated. 0: disable 1: enable	0x1

2:0	VALID_NS	RO	Invalid conversions for current filter channel valid_times = 2^valid_ns 0b000: 0 0b001: 1 0b010: 2 0b011: 3 0b100: 4 0b101: 5 0b110: 6 0b111: 7	0x3

RAWDATA0: (Address 70h)

Bit	Symbol	R/W	Description	Default
7	RESERVED	RO	Not used	0x0
6:0	RAWDATA_CH0H	RO	channel 0 value[14:8], valid data width is controlled by VLD_WD_SEL	0x0

RAWDATA1: (Address 71h)

Bit	Symbol	R/W	Description	Default
7:0	RAWDATA_CH0L	RO	channel 0 value[7:0], valid data width is controlled by VLD_WD_SEL	0x0

RAWDATA2: (Address 72h)

Bit	Symbol	R/W	Description	Default
7	RESERVED	RO	Not used	0x0
6:0	RAWDATA_CH1H	RO	channel 1 value[14:8], valid data width is controlled by VLD_WD_SEL	0x0

RAWDATA3: (Address 73h)

Bit	Symbol	R/W	Description	Default
7:0	RAWDATA_CH1L	RO	channel 1 value[7:0], valid data width is controlled by VLD_WD_SEL	0x0

RAWDATA4: (Address 74h)

Bit	Symbol	R/W	Description	Default
7	RESERVED	RO	Not used	0x0
6:0	RAWDATA_CH2H	RO	channel 2 value[14:8], valid data width is controlled by VLD_WD_SEL	0x0

RAWDATA5: (Address 75h)

Bit	Symbol	R/W	Description	Default
7:0	RAWDATA_CH2L	RO	channel 2 value[7:0], valid data width is controlled by VLD_WD_SEL	0x0

RAWDATA6: (Address 76h)

Bit	Symbol	R/W	Description	Default
7	RESERVED	RO	Not used	0x0
6:0	RAWDATA_CH3H	RO	channel 3 value[14:8], valid data width is controlled by VLD_WD_SEL	0x0

RAWDATA7: (Address 77h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	RAWDATA_CH3L	RO	channel 3 value[7:0], valid data width is controlled by VLD_WD_SEL	0x0

RAWDATA8: (Address 78h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	RESERVED	RO	Not used	0x0
6:0	RAWDATA_CH4H	RO	channel 4 value[14:8], valid data width is controlled by VLD_WD_SEL	0x0

RAWDATA9: (Address 79h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	RAWDATA_CH4L	RO	channel 4 value[7:0], valid data width is controlled by VLD_WD_SEL	0x0

DSP_CH_EN: (Address 80h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:5	Reserved	RO	Not used	0x0
4	ADC_OS_EN	R/W	Enable DSP trig DAC offset calibration 0b0 : Disable 0b1 : Enable	0x0
3	Reserved	R/W	Not used	0x0
2:0	ALG_CH_EN	R/W	algorithm channel enable 0b000 : disable 0bxx1 : algorithm channel a enable 0bx1x : algorithm channel b enable 0b1xx : algorithm channel c enable	0x1

DSP_OS0: (Address 81h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RO	Not used	0x0
6:0	ADC_OFFSET_MAXH	R/W	ADC_OFFSET_MAX[14:0] . When the base value greater than ADC_OFFSET_MAX , DAC offset calibration will be triggered	0xf

DSP_OS1: (Address 82h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	ADC_OFFSET_MAXL	R/W	ADC_OFFSET_MAX[7:0] . When the base value greater than ADC_OFFSET_MAX , DAC offset calibration will be triggered	0xff

DSP_INTR_SEL: (Address 83h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	Reserved	RO	Not used	0x0

3:2	FORCE2_INTR_SEL	R/W	FORCE2 interrupt source selection 0b00 : algorithm channel a 0b01 : algorithm channel b 0b10 : algorithm channel c 0b11 : all	0x1
1:0	FORCE1_INTR_SEL	R/W	FORCE1 interrupt source selection 0b00 : algorithm channel a 0b01 : algorithm channel b 0b10 : algorithm channel c 0b11 : all	0x0

DSP_CHA_LAMDA1: (Address 90h)

Bit	Symbol	R/W	Description	Default
7:0	CHA_LAMDA1	R/W	Base data filtering parameter	0x73

DSP_CHA_LAMDA2: (Address 91h)

Bit	Symbol	R/W	Description	Default
7:0	CHA_LAMDA2	R/W	Base data filtering parameter	0x8

DSP_CHA_DRIFT0: (Address 92h)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0x0
6:0	CHA_DRIFT_MAXH	R/W	Data drift maximum value [14:8]	0x0

DSP_CHA_DRIFT1: (Address 93h)

Bit	Symbol	R/W	Description	Default
7:0	CHA_DRIFT_MAXL	R/W	Data drift maximum value [7:0]	0x1E

DSP_CHA_FORCE0: (Address 94h)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0x0
6:0	CHA_FORCE_MIN_P_H	R/W	Positive force threshold [14:8]	0x00

DSP_CHA_FORCE1: (Address 95h)

Bit	Symbol	R/W	Description	Default
7:0	CHA_FORCE_MIN_P_L	R/W	Positive force threshold [7:0]	0xC8

DSP_CHA_FORCE2: (Address 96h)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0x0
6:0	CHA_FORCE_MIN_N_H	R/W	Negative force threshold [14:8]	0x0

DSP_CHA_FORCE3: (Address 97h)

Bit	Symbol	R/W	Description	Default
7:0	CHA_FORCE_MIN_N_L	R/W	Negative force threshold [7:0]	0x0

DSP_CHA_DELAY: (Address 98h)

Bit	Symbol	R/W	Description	Default
7:4	CHA_DELAY_UP_CNT	R/W	Pressing the rising edge delay T= DELAY_UP_CNT * AFE sampling period	0x3

3:0	CHA_DELAY_DOWN_CNT	R/W	Pressing the falling edge delay T= DELAY_DOWN_CNT * AFE sampling period	0x3

DSP_CHA_TIMEOUT0: (Address 99h)

Bit	Symbol	R/W	Description	Default
7:0	CHA_TIMEOUT_CNT_H	R/W	Force timeout value [15:8] T= TIMEOUT_CNT * AFE sampling period	0x1

DSP_CHA_TIMEOUT1: (Address 9Ah)

Bit	Symbol	R/W	Description	Default
7:0	CHA_TIMEOUT_CNT_L	R/W	Force timeout value [7:0] T= TIMEOUT_CNT * AFE sampling period	0x2C

DSP_CHA_RECOIL: (Address 9Bh)

Bit	Symbol	R/W	Description	Default
7:0	CHA_RECOIL_CNT	R/W	Recoil counter value T= RECOIL_CNT * AFE sampling period	0x14

DSP_CHA_STABLE: (Address 9Ch)

Bit	Symbol	R/W	Description	Default
7:0	CHA_STABLE_CNT	R/W	Stable time after timeout T= STABLE_CNT * AFE sampling period	0x64

DSP_CHA_RELEASE: (Address 9Dh)

Bit	Symbol	R/W	Description	Default
7:0	CHA_RELEASE_CNT	R/W	Release time after timeout T= RELEASE_CNT * AFE sampling period	0xFF

DSP_CHA_CFG: (Address 9Eh)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0x0
6:4	CHA_ALG_SEL	R/W	algorithm channel data source selection 0b000 : afe channel 0 0b001 : afe channel 1 0b010 : afe channel 2 0b011 : afe channel 3 0b100 : afe channel 4 others : disable	0x0
3	Reserved	RO	Not used	0x0
2	CHA_DE_RECOIL_EN	R/W	Recoil elimination enable 0b0 : Disable 0b1 : Enable	0x0
1	CHA_TIMEOUT_EN	R/W	Timeout reset enable 0b0 : Disable 0b1 : Enable	0x1
0	CHA_SINGLE_EN	R/W	single algorithm enable 0b0 : double 0b1 : single	0x1

DSP_CHA_INTR_MASK: (Address 9Fh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RO	Not used	0x0
5:4	CHA_INTR_MODE	R/W	interrupt output mode 0b00 : level 0b01 : latch 0b10 : pulse 0b11 : disable	0x1
3	CHA_RLS_N_MASK	R/W	Negative force release interrupt mask 0b0 : Enable 0b1 : Disable	0x0
2	CHA_PRS_N_MASK	R/W	Negative force press interrupt mask 0b0 : Enable 0b1 : Disable	0x0
1	CHA_RLS_P_MASK	R/W	Positive force release interrupt mask 0b0 : Enable 0b1 : Disable	0x0
0	CHA_PRS_P_MASK	R/W	Positive force press interrupt mask 0b0 : Enable 0b1 : Disable	0x0

DSP_CHA_INTR_CLR: (Address A0h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	Reserved	RO	Not used	0x0
3	CHA_RLS_N_CLR	WO	Negative force release interrupt clear register . write 1 to clear RLS_N_FLAG	0x0
2	CHA_PRS_N_CLR	WO	Negative force press interrupt clear register . write 1 to clear PRS_N_FLAG	0x0
1	CHA_RLS_P_CLR	WO	Positive force release interrupt clear register . write 1 to clear RLS_P_FLAG	0x0
0	CHA_PRS_P_CLR	WO	Positive force press interrupt clear register . write 1 to clear PRS_P_FLAG	0x0

DSP_CHA_INTR_FLAG: (Address A1h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	Reserved	RO	Not used	0x0
3	CHA_RLS_N_FLAG	RO	Negative force release interrupt flag	0x0
2	CHA_PRS_N_FLAG	RO	Negative force press interrupt flag	0x0
1	CHA_RLS_P_FLAG	RO	Positive force release interrupt flag	0x0
0	CHA_PRS_P_FLAG	RO	Positive force press interrupt flag	0x0

DSP_CHA_STAT: (Address A2h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RO	Not used	0x0
5	CHA_TOUCH_N	RO	Negative force status	0x0
4	CHA_TOUCH_P	RO	Positive force status	0x0
3:2	CHA_RLS_ST	RO	Release FSM state	0x0
1:0	CHA_PRS_ST	RO	Press FSM state	0x0

DSP_CHB_LAMDA1: (Address B0h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**

7:0	CHB_LAMDA1	R/W	Base data filtering parameter	0x73

DSP_CHB_LAMDA2: (Address B1h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	CHB_LAMDA2	R/W	Base data filtering parameter	0x8

DSP_CHB_DRIFT0: (Address B2h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RO	Not used	0x0
6:0	CHB_DRIFT_MAXH	R/W	Data drift maximum value [14:8]	0x0

DSP_CHB_DRIFT1: (Address B3h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	CHB_DRIFT_MAXL	R/W	Data drift maximum value [7:0]	0x1E

DSP_CHB_FORCE0: (Address B4h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RO	Not used	0x0
6:0	CHB_FORCE_MIN_P_H	R/W	Positive force threshold [14:8]	0x00

DSP_CHB_FORCE1: (Address B5h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	CHB_FORCE_MIN_P_L	R/W	Positive force threshold [7:0]	0xC8

DSP_CHB_FORCE2: (Address B6h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RO	Not used	0x0
6:0	CHB_FORCE_MIN_N_H	R/W	Negative force threshold [14:8]	0x0

DSP_CHB_FORCE3: (Address B7h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	CHB_FORCE_MIN_N_L	R/W	Negative force threshold [7:0]	0x0

DSP_CHB_DELAY: (Address B8h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	CHB_DELAY_UP_CNT	R/W	Pressing the rising edge delay T= DELAY_UP_CNT * AFE sampling period	0x3
3:0	CHB_DELAY_DOWN_CNT	R/W	Pressing the falling edge delay T= DELAY_DOWN_CNT * AFE sampling period	0x3

DSP_CHB_TIMEOUT0: (Address B9h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	CHB_TIMEOUT_CNT_H	R/W	Force timeout value [15:8] T= TIMEOUT_CNT * AFE sampling period	0x1

DSP_CHB_TIMEOUT1: (Address BAh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**

7:0	CHB_TIMEOUT_CNT_L	R/W	Force timeout value [7:0] T= TIMEOUT_CNT * AFE sampling period	0x2C

DSP_CHB_RECOIL: (Address BBh)

Bit	Symbol	R/W	Description	Default
7:0	CHB_RECOIL_CNT	R/W	Recoil counter value T= RECOIL_CNT * AFE sampling period	0x14

DSP_CHB_STABLE: (Address BCh)

Bit	Symbol	R/W	Description	Default
7:0	CHB_STABLE_CNT	R/W	Stable time after timeout T= STABLE_CNT * AFE sampling period	0x64

DSP_CHB_RELEASE: (Address BDh)

Bit	Symbol	R/W	Description	Default
7:0	CHB_RELEASE_CNT	R/W	Release time after timeout T= RELEASE_CNT * AFE sampling period	0xFF

DSP_CHB_CFG: (Address BEh)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0x0
6:4	CHB_ALG_SEL	R/W	algorithm channel data source selection 0b000 : afe channel 0 0b001 : afe channel 1 0b010 : afe channel 2 0b011 : afe channel 3 0b100 : afe channel 4 others : disable	0x0
3	Reserved	RO	Not used	0x0
2	CHB_DE_RECOIL_EN	R/W	Recoil elimination enable 0b0 : Disable 0b1 : Enable	0x0
1	CHB_TIMEOUT_EN	R/W	Timeout reset enable 0b0 : Disable 0b1 : Enable	0x1
0	CHB_SINGLE_EN	R/W	single algorithm enable 0b0 : double 0b1 : single	0x1

DSP_CHB_INTR_MASK: (Address BFh)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0x0
5:4	CHB_INTR_MODE	R/W	interrupt output mode 0b00 : level 0b01 : latch 0b10 : pulse 0b11 : disable	0x1
3	CHB_RLS_N_MASK	R/W	Negative force release interrupt mask 0b0 : Enable 0b1 : Disable	0x0

2	CHB_PRS_N_MASK	R/W	Negative force press interrupt mask 0b0 : Enable 0b1 : Disable	0x0
1	CHB_RLS_P_MASK	R/W	Positive force release interrupt mask 0b0 : Enable 0b1 : Disable	0x0
0	CHB_PRS_P_MASK	R/W	Positive force press interrupt mask 0b0 : Enable 0b1 : Disable	0x0

DSP_CHB_INTR_CLR: (Address C0h)

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RO	Not used	0x0
3	CHB_RLS_N_CLR	WO	Negative force release interrupt clear register . write 1 to clear RLS_N_FLAG	0x0
2	CHB_PRS_N_CLR	WO	Negative force press interrupt clear register . write 1 to clear PRS_N_FLAG	0x0
1	CHB_RLS_P_CLR	WO	Positive force release interrupt clear register . write 1 to clear RLS_P_FLAG	0x0
0	CHB_PRS_P_CLR	WO	Positive force press interrupt clear register . write 1 to clear PRS_P_FLAG	0x0

DSP_CHB_INTR_FLAG: (Address C1h)

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RO	Not used	0x0
3	CHB_RLS_N_FLAG	RO	Negative force release interrupt flag	0x0
2	CHB_PRS_N_FLAG	RO	Negative force press interrupt flag	0x0
1	CHB_RLS_P_FLAG	RO	Positive force release interrupt flag	0x0
0	CHB_PRS_P_FLAG	RO	Positive force press interrupt flag	0x0

DSP_CHB_STAT: (Address C2h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0x0
5	CHB_TOUCH_N	RO	Negative force status	0x0
4	CHB_TOUCH_P	RO	Positive force status	0x0
3:2	CHB_RLS_ST	RO	Release FSM state	0x0
1:0	CHB_PRS_ST	RO	Press FSM state	0x0

DSP_CHC_CFG: (Address DEh)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0x0
6:4	CHC_ALG_SEL	R/W	algorithm channel data source selection 0b000 : afe channel 0 0b001 : afe channel 1 0b010 : afe channel 2 0b011 : afe channel 3 0b100 : afe channel 4 others : disable	0x0
3	Reserved	RO	Not used	0x0

2	CHC_DE_RECOIL_EN	R/W	Recoil elimination enable 0b0 : Disable 0b1 : Enable	0x0
1	CHC_TIMEOUT_EN	R/W	Timeout reset enable 0b0 : Disable 0b1 : Enable	0x1
0	CHC_SINGLE_EN	R/W	single algorithm enable 0b0 : double 0b1 : single	0x1

DSP_CHC_INTR_MASK: (Address DFh)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0x0
5:4	CHC_INTR_MODE	R/W	interrupt output mode 0b00 : level 0b01 : latch 0b10 : pulse 0b11 : disable	0x1
3	CHC_RLS_N_MASK	R/W	Negative force release interrupt mask 0b0 : Enable 0b1 : Disable	0x0
2	CHC_PRS_N_MASK	R/W	Negative force press interrupt mask 0b0 : Enable 0b1 : Disable	0x0
1	CHC_RLS_P_MASK	R/W	Positive force release interrupt mask 0b0 : Enable 0b1 : Disable	0x0
0	CHC_PRS_P_MASK	R/W	Positive force press interrupt mask 0b0 : Enable 0b1 : Disable	0x0

DSP_CHC_INTR_CLR: (Address E0h)

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RO	Not used	0x0
3	CHC_RLS_N_CLR	WO	Negative force release interrupt clear register . write 1 to clear RLS_N_FLAG	0x0
2	CHC_PRS_N_CLR	WO	Negative force press interrupt clear register . write 1 to clear PRS_N_FLAG	0x0
1	CHC_RLS_P_CLR	WO	Positive force release interrupt clear register . write 1 to clear RLS_P_FLAG	0x0
0	CHC_PRS_P_CLR	WO	Positive force press interrupt clear register . write 1 to clear PRS_P_FLAG	0x0

DSP_CHC_INTR_FLAG: (Address E1h)

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RO	Not used	0x0
3	CHC_RLS_N_FLAG	RO	Negative force release interrupt flag	0x0
2	CHC_PRS_N_FLAG	RO	Negative force press interrupt flag	0x0
1	CHC_RLS_P_FLAG	RO	Positive force release interrupt flag	0x0
0	CHC_PRS_P_FLAG	RO	Positive force press interrupt flag	0x0

DSP_CHC_STAT: (Address E2h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RO	Not used	0x0
5	CHC_TOUCH_N	RO	Negative force status	0x0
4	CHC_TOUCH_P	RO	Positive force status	0x0
3:2	CHC_RLS_ST	RO	Release FSM state	0x0
1:0	CHC_PRS_ST	RO	Press FSM state	0x0

DSP_DATA0: (Address E4h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RO	Not used	0x0
6:0	CHA_BASE_H	RO	Algorithm channel a base value [14:8]	0x0

DSP_DATA1: (Address E5h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	CHA_BASE_L	RO	Algorithm channel a base value [7:0]	0x0

DSP_DATA2: (Address E6h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RO	Not used	0x0
6:0	CHA_DIFF_H	RO	Algorithm channel a diff value [14:8]	0x0

DSP_DATA3: (Address E7h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	CHA_DIFF_L	RO	Algorithm channel a diff value [7:0]	0x0

DSP_DATA4: (Address E8h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RO	Not used	0x0
6:0	CHB_BASE_H	RO	Algorithm channel b base value [14:8]	0x0

DSP_DATA5: (Address E9h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	CHB_BASE_L	RO	Algorithm channel b base value [7:0]	0x0

DSP_DATA6: (Address EAh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RO	Not used	0x0
6:0	CHB_DIFF_H	RO	Algorithm channel b diff value [14:8]	0x0

DSP_DATA7: (Address EBh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	CHB_DIFF_L	RO	Algorithm channel b diff value [7:0]	0x0

DSP_DATA8: (Address ECh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RO	Not used	0x0
6:0	CHC_BASE_H	RO	Algorithm channel c base value [14:8]	0x0

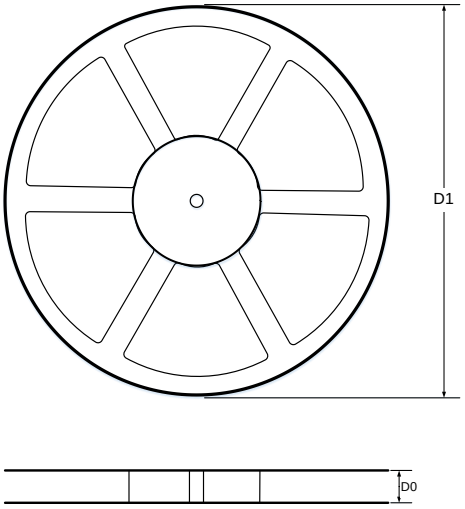
DSP_DATA9: (Address EDh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	CHC_BASE_L	RO	Algorithm channel c base value [7:0]	0x0

DSP_DATA10: (Address EEh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RO	Not used	0x0
6:0	CHC_DIFF_H	RO	Algorithm channel c diff value [14:8]	0x0

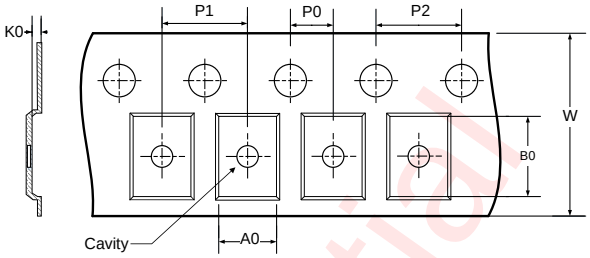
DSP_DATA11: (Address EFh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	CHC_DIFF_L	RO	Algorithm channel c diff value [7:0]	0x0

Tape And Reel Information

REEL DIMENSIONS

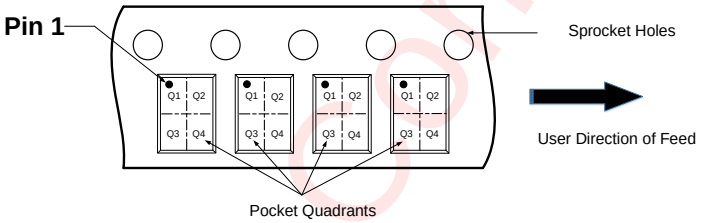


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



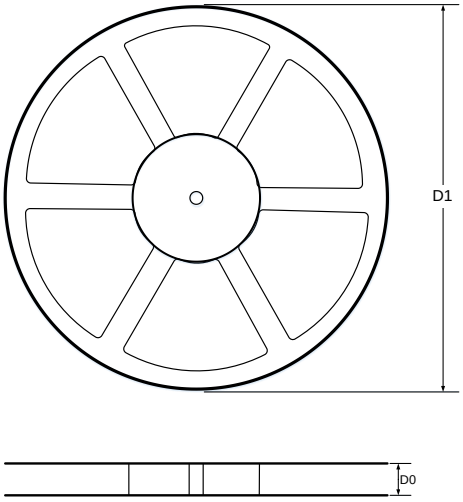
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	1.58	1.58	0.45	2.00	4.00	4.00	8.00	Q1

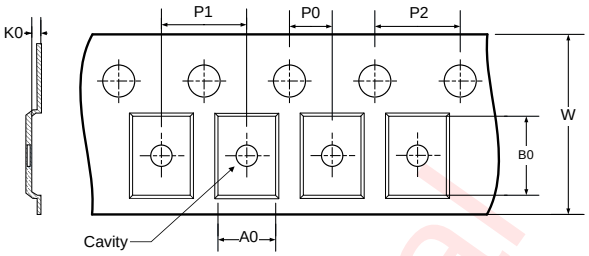
All dimensions are nominal

AW86874CSR/AW86872CSR Tape And Reel Information

REEL DIMENSIONS

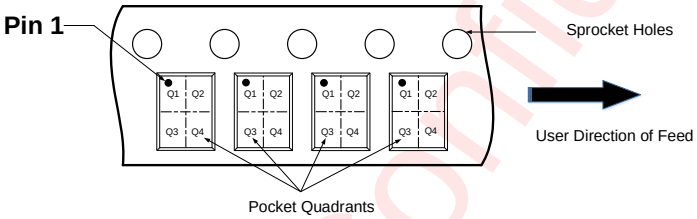


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

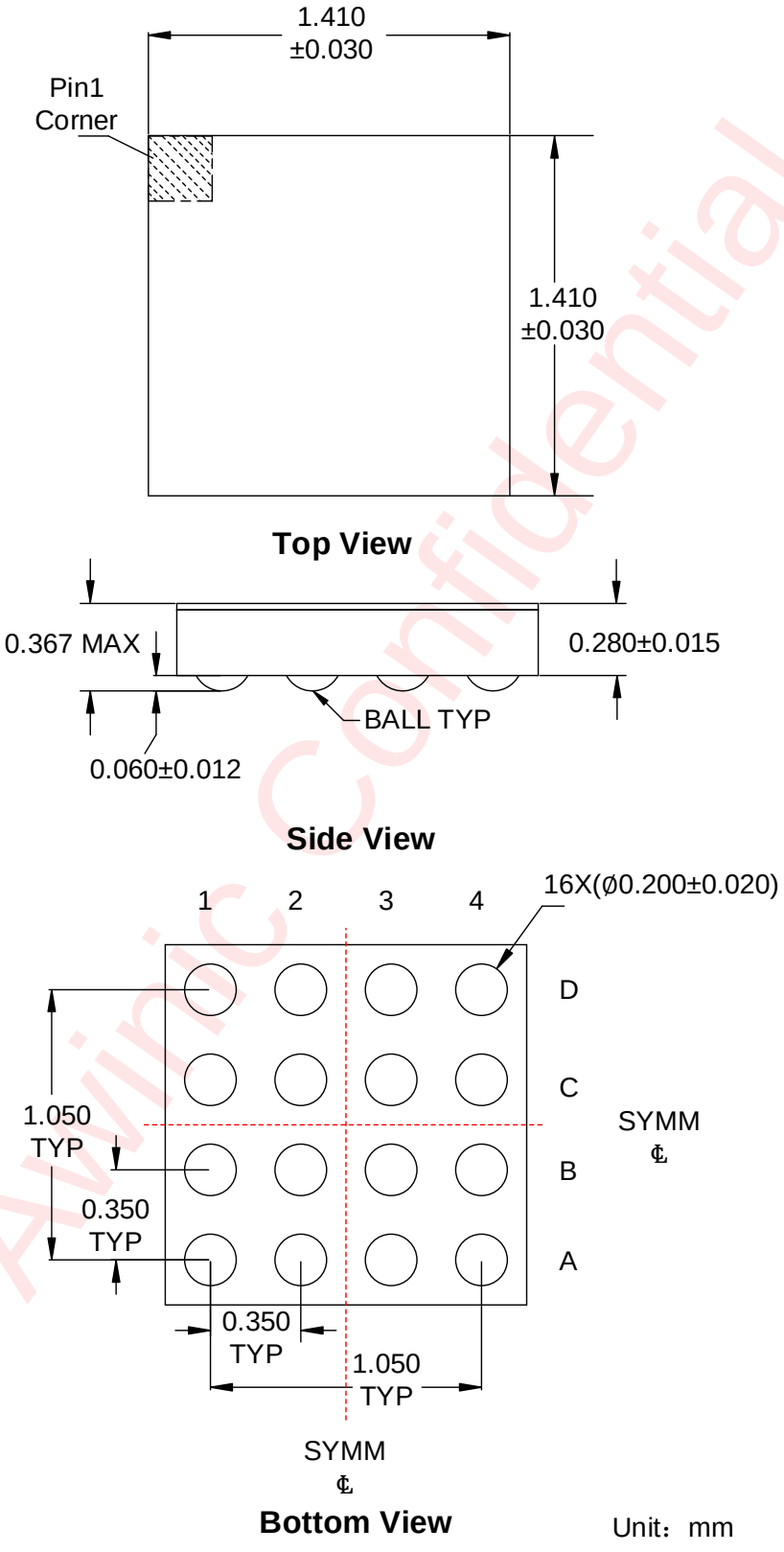
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	3.3	3.3	1.1	2	8	4	12	Q1

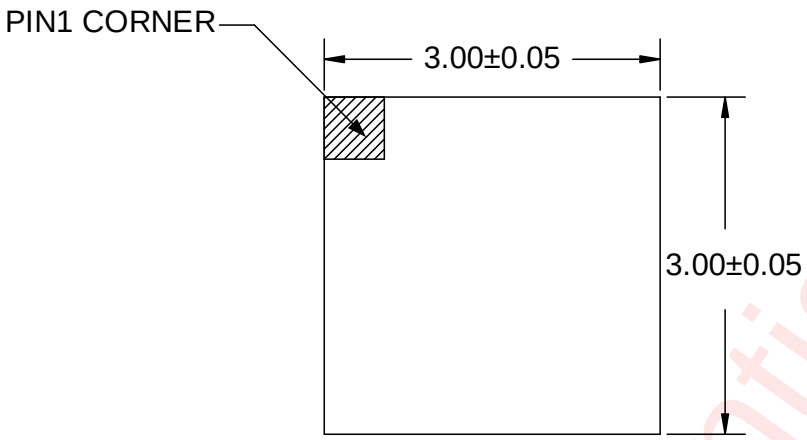
All dimensions are nominal

AW86872QNR Tape And Reel Information

Package Description

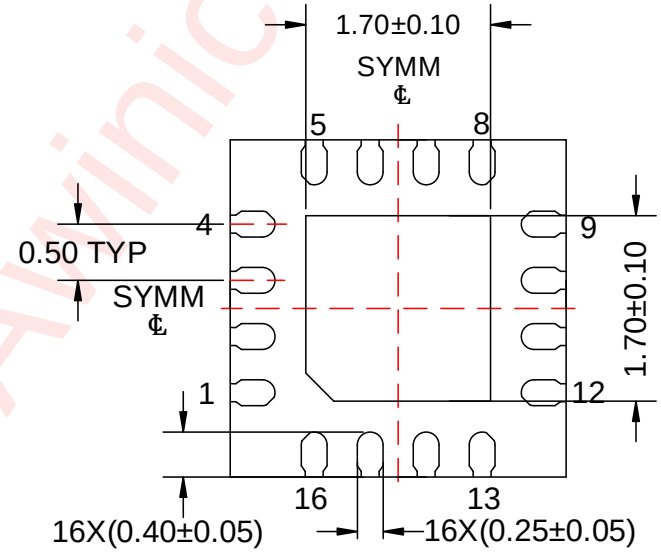


AW86874CSR/AW86872CSR Package Description



Top View

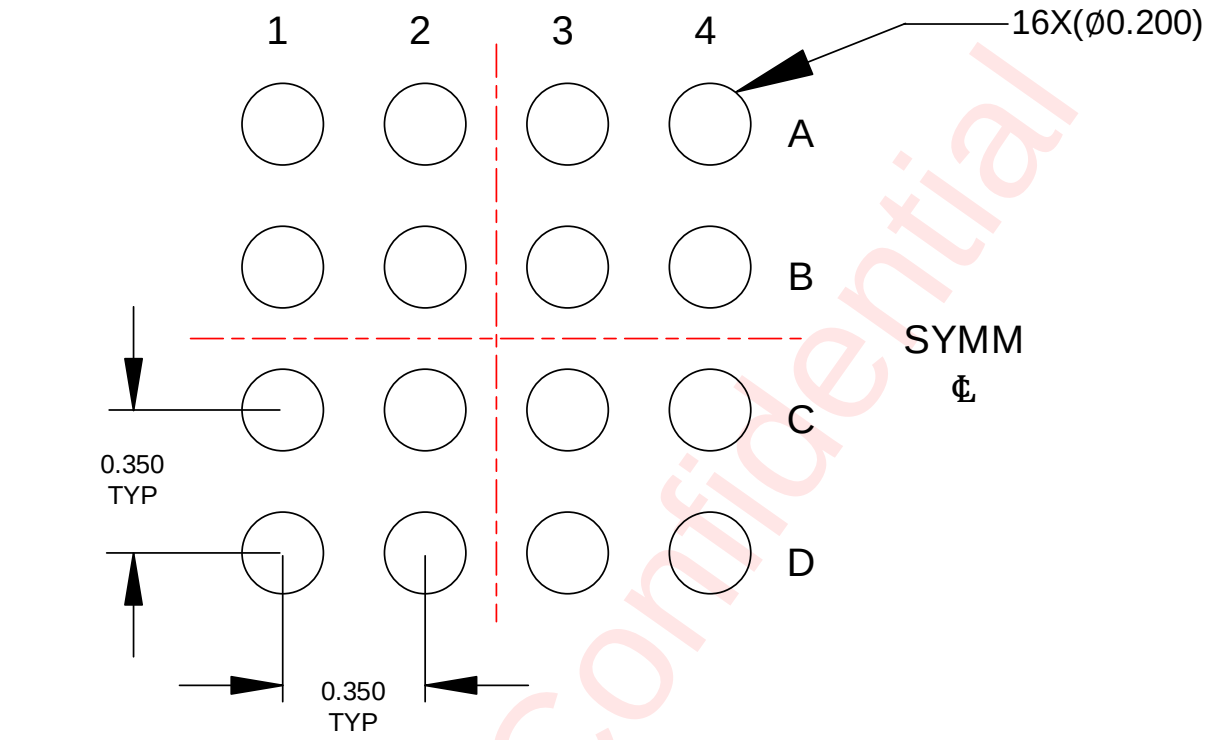
Side View

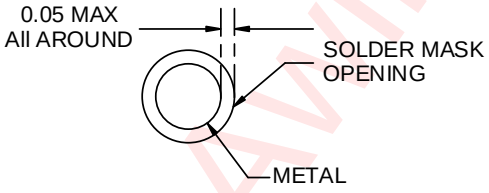


Bottom View Unit: mm

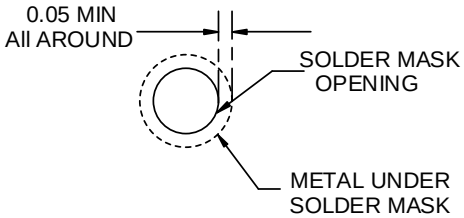
AW86872QNR Package Description

Land Pattern Data





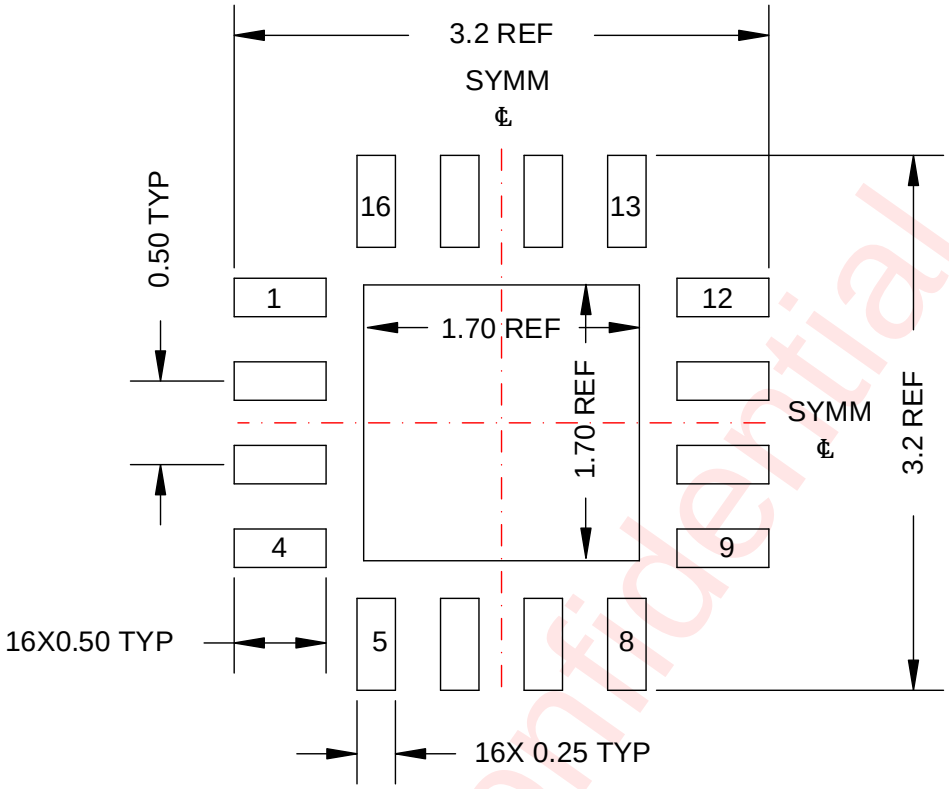
NON-SOLDER MASK DEFINED

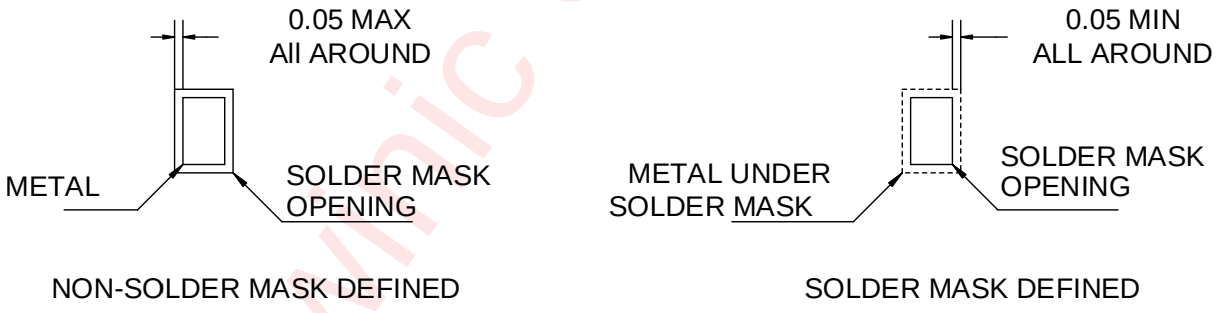


SOLDER MASK DEFINED

Unit: mm

AW86874CSR/AW86872CSR Land Pattern Data





Unit: mm

AW86872QNR Land Pattern Data

Revision History

Version	Date	Change Record
V1.0	Apr. 2024	Officially Released.
V1.1	Nov. 2024	Based on AW86874CSR, add relevant descriptions of AW86872CSR and AW86872QNR, and modify the titles.
V1.2	Mar. 2025	Modify the description of registers with addresses 0x42 and 0x43.(P31 and P32)

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