# Dual-bit, Dual-supply Voltage Level Translator

## Features

- Wide supply voltage range: 0.8V to 3.6V
- VCC Isolation Feature
- IOFF Supports Partial-Power-Down Mode Operation
- Maximum data rates:
  - 500 Mbit/s (1.8V to 3.3V translation)
  - 320 Mbit/s (<1.8V to 3.3V translation)
  - 320 Mbit/s (translate to 2.5V or 1.8V)
  - 280 Mbit/s (translate to 1.5V)
  - 140 Mbit/s (translate to 1.2V)
- TSSOP 3.0mm X3.0mm X1.1mm-8L package

## Applications

- Smartphones
- Servers
- Desktop PCs and Notebooks
- Other Portable Devices

## General Description

AWS74AVC2T45TSR is a dual-bit, dual-supply high-performance voltage-level translator with direction control pin that enables bidirectional level translation. Both A pins and DIR pin are referenced to $V_{CCA}$ and accepts any supply voltage from 0.8 V to 3.6 V. B pins are referenced to $V_{CCB}$ and accepts any supply voltage from 0.8 V to 3.6 V. This allows for universal low-voltage bidirectional translation and level-shifting between any of the 0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V voltage nodes. The device transmits data from the A port to the B port when the DIR pin is HIGH. The device transmits data from the B port to the A port when the DIR pin is LOW. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess internal leakage of the CMOS.

The AWS74AVC2T45TSR is fully specified for partial power-down applications using off output current ($I_{OFF}$).The outputs for this device enter a high-impedance state when the device is powered down, preventing any damaging backflow current through the device. The $V_{CC}$ isolation feature ensures that if either $V_{CCA}$ or $V_{CCB}$ are at GND, both A and B ports are put in a high-impedance state.

## Typical Application Circuit

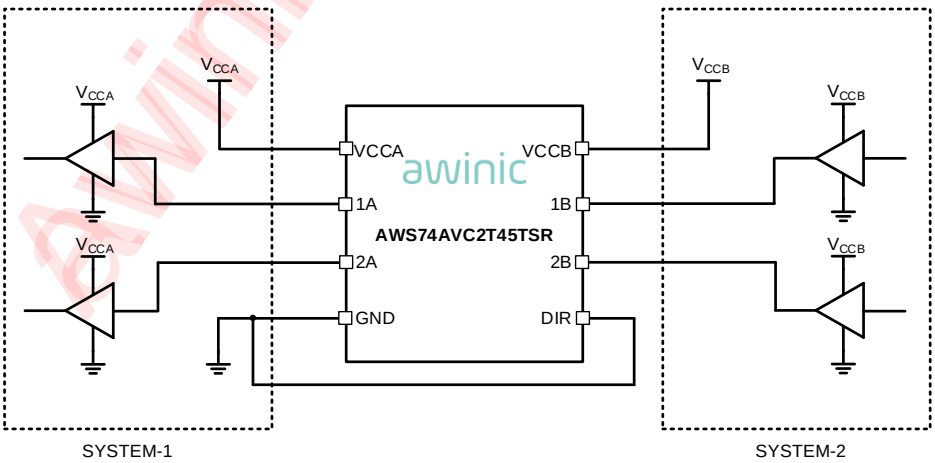



**Figure 1 Unidirectional Logic Level-Shifting Application**

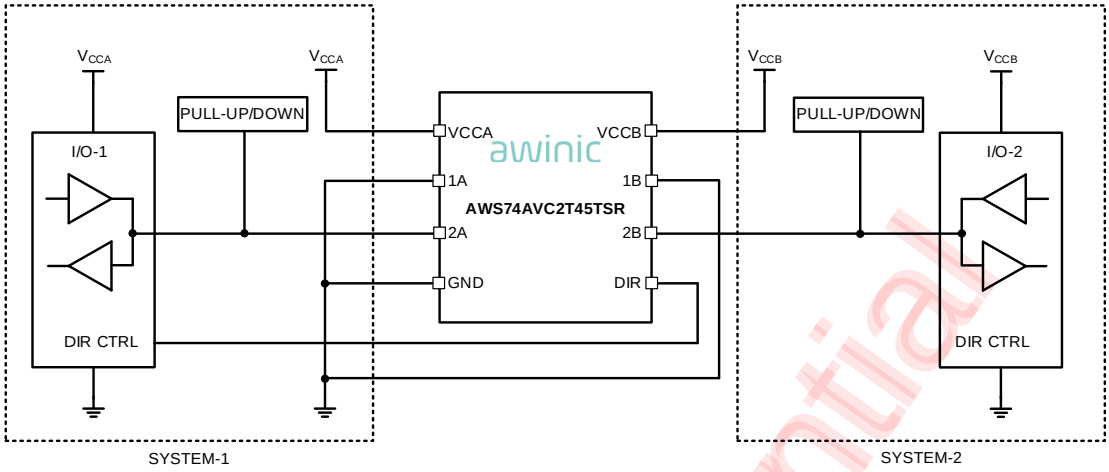



**Figure 2 Bidirectional Logic Level-Shifting Application**

## Pin Configuration And Top Mark

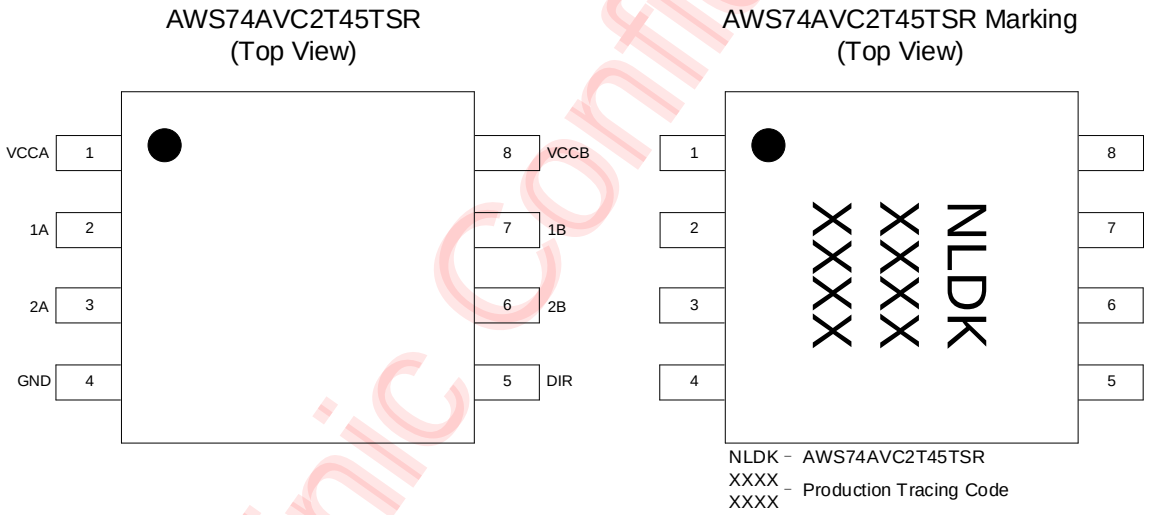



**Figure 3 Pin Configuration and Top Mark**

## Pin Definition

| No. | NAME | DESCRIPTION |
|---|---|---|
| 1 | VCCA | Supply voltage A (referenced to pins 1A, 2A and DIR) |
| 2 | 1A | Data input or output |
| 3 | 2A | Data input or output |
| 4 | GND | Ground |
| 5 | DIR | Direction control |
| 6 | 2B | Data input or output |
| 7 | 1B | Data input or output |
| 8 | VCCB | Supply voltage B (referenced to pins 1B and 2B) |

## Pin Functions

| VCCA, VCCB | DIR(NOTE1) | nA(NOTE2) | nB(NOTE2) |
|---|---|---|---|
| 0.8V to 3.6V | L | nA = nB | input |
| 0.8V to 3.6V | H | input | nB = nA |
| GND(NOTE3) | X | Hi-Z | Hi-Z |

*NOTE1: The DIR input circuit is referenced to VCCA.*

*NOTE2: The input circuit of the data I/O is always active.*

*NOTE3: If at least one of VCCA or VCCB is at GND, both A and B ports are put in a high-impedance state.*

## Functional Block Diagram

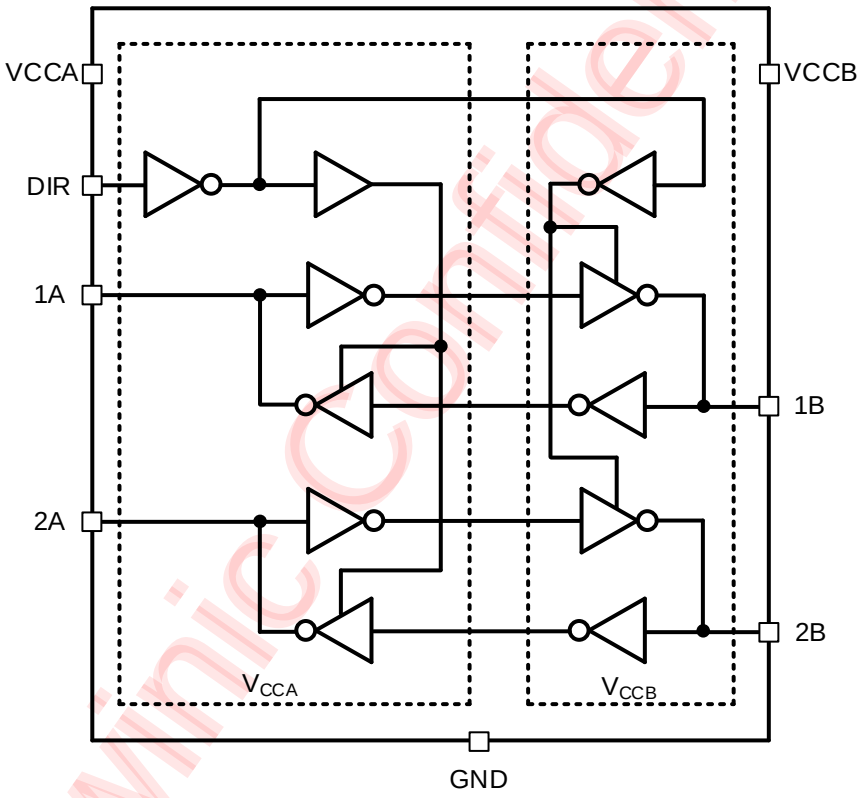



**Figure 4 Functional Block Diagram**

## Typical Application Circuits

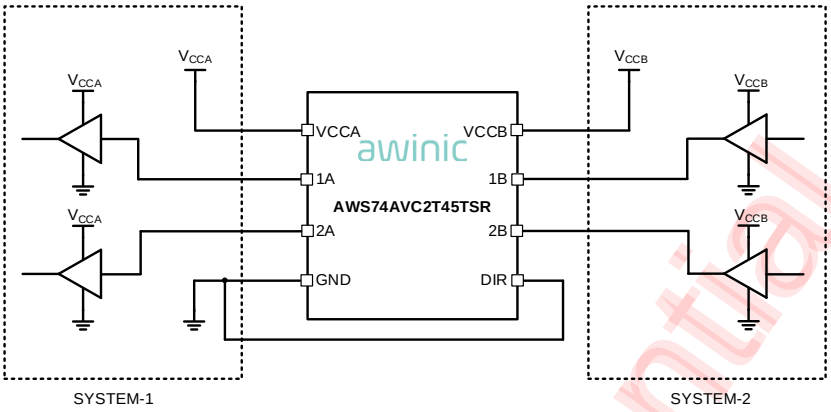



**Figure 5 Unidirectional Logic Level-Shifting Application**

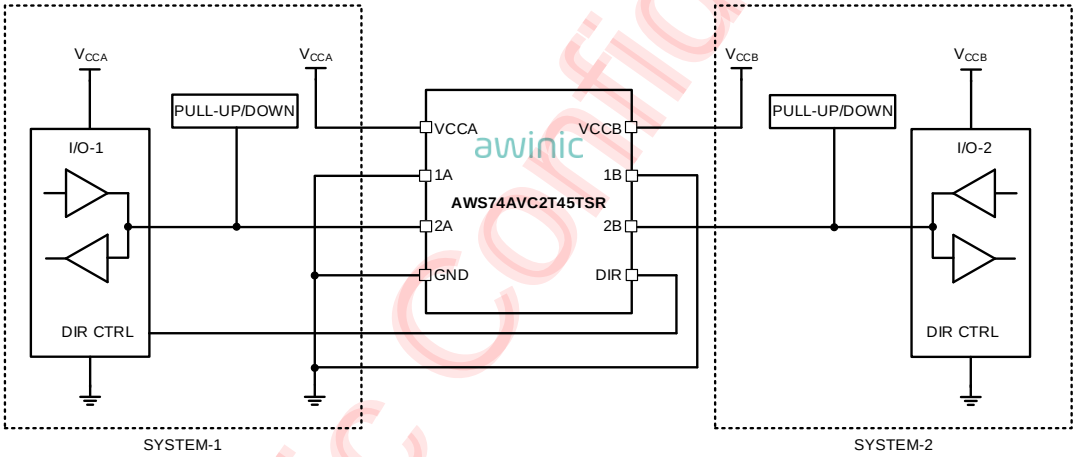



**Figure 6 Bidirectional Logic Level-Shifting Application**

- ***Notice for typical application circuits:***

1. Figure 5 shows the AWS74AVC2T45TSR being used in a unidirectional logic level-shifting application. The following table lists the pins and pin descriptions of the AWS74AVC2T45TSR connections with SYSTEM-1 and SYSTEM-2.

| No. | NAME | FUNCTION | DESCRIPTION |
|---|---|---|---|
| 1 | VCCA | VCC1 | Supply voltage of SYSTEM-1 (0.8V to 3.6V) |
| 2 | 1A | OUT1 | Output level depends on VCCA |
| 3 | 2A | OUT2 | Output level depends on VCCA |
| 4 | GND | GND | Device GND |
| 5 | DIR | DIR | The GND (low level) determines B port to A port direction |
| 6 | 2B | IN2 | Input threshold value depends on VCCB |
| 7 | 1B | IN1 | Input threshold value depends on VCCB |
| 8 | VCCB | VCC2 | Supply voltage of SYSTEM-2 (0.8V to 3.6V) |

2. This device uses drivers which are enabled depending on the state of the DIR pin. The designer must know the intended flow of data and take care not to violate any of the high or low logic levels. Unused data inputs must not be floating, as this can cause excessive internal leakage on the input CMOS structure. Make sure to tie any unused input and output ports directly to ground.
3. Figure 6 shows the AWS74AVC2T45TSR being used in a bidirectional logic level-shifting application. Since the device does not have an output enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.
4. The following table gives a sequence that will illustrate data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

| STATE | DIR CTRL | IO-1 | IO-2 | DESCRIPTION |
|---|---|---|---|---|
| 1 | H | Output | Input | SYSTEM-1 data to SYSTEM-2. |
| 2 | H | Hi-Z | Hi-Z | SYSTEM-2 is getting ready to send data to SYSTEM-1. IO-1 and IO-2 are disabled. The bus-line state depends on pull-up or pull-down. |
| 3 | L | Hi-Z | Hi-Z | DIR bit is set to LOW. IO-1 and IO-2 still are disabled. The bus-line state depends on pull-up or pull-down. |
| 4 | L | Input | Output | SYSTEM-2 data to SYSTEM-1. |

5. For bidirectional logic level-shifting application, SYSTEM-1 and SYSTEM-2 must use the same conditions, that is, both pullup or both pulldown.
6. In a bidirectional application calculate the enable times for the AWS74AVC2T45TSR using the following formulas:
   - $t_{en}$ (DIR to nA) = $t_{dis}$ (DIR to nB) + $t_{pd}$ (nB to nA)
   - $t_{en}$ (DIR to nB) = $t_{dis}$ (DIR to nA) + $t_{pd}$ (nA to nB)

   these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the AWS74AVC2T45TSR initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

## Ordering Information

| Part Number | Temperature | Package | Marking | Moisture Sensitivity Level | Environmental Information | Delivery Form |
|---|---|---|---|---|---|---|
| AWS74AVC2T45TSR | -40°C~125°C | WBTSSOP 3mmX3mmX 1.1mm-8L | NLDK | MSL1 | ROHS+HF | 3000 units/ Tape and Reel |

## Absolute Maximum Ratings(NOTE1)

| PARAMETERS | | RANGE |
|---|---|---|
| Supply voltage range, $V_{CCA}$ and $V_{CCB}$ | | -0.3V to 4.6V |
| Input voltage range | DIR, A port, B port | -0.3V to 4.6V |
| Output voltage range | A port, B port | -0.3V to 4.6V |
| Input clamp current, $I_{Ik}$ | $V_I$ <0 | ±50mA |
| Output clamp current, $I_{OK}$ | $V_O$ <0 | ±50mA |
| Output current, $I_O$ | $V_O$ =0V or $V_{CCO}$ | ±50mA |
| Maximum operating junction temperature $T_{JMAX}$ | | 150°C |
| Storage temperature $T_{STG}$ | | -65°C to 150°C |
| Lead temperature (soldering 10 seconds) | | 260°C |
| ESD | | |
| HBM (All pins, per JEDEC JS-001) (NOTE 2) | | ±2kV |
| CDM (All pins, per JEDEC JS-002) (NOTE 3) | | ±1.5kV |
| Latch-Up | | |
| Test condition: JESD78E | | +IT：200mA<br>-IT：-200mA |

*NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

*NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.*

*NOTE3: Test method: ESDA/JEDEC JS-002-2018.*

## Recommended Operating Conditions

| PARAMETERS | | CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage for A port | | 0.8 | 3.6 | V |
| $V_{CCB}$ | Supply voltage for B port | | 0.8 | 3.6 | V |
| $V_I$ | Input voltage(NOTE1) | | 0 | 3.6 | V |
| $V_O$ | Output voltage | Active state | 0 | $V_{CCO}$(NOTE2) | V |
| | | 3 state | 0 | 3.6 | V |
| Δt/ΔV | Input transition rise or fall rate | $V_{CCI}$ =0.8V to 3.6V(NOTE3) | | 5 | ns/V |
| $T_A$ | Operating junction temperature $T_A$ | | -40 | 125 | °C |

*NOTE1: All unused data inputs of the device must be held at $V_{CCI}$ or GND to ensure proper device operation.*
*NOTE2: $V_{CCO}$ is the supply voltage associated with the output port supply $V_{CCA}$ or $V_{CCB}$.*
*NOTE3: $V_{CCI}$ is the supply voltage associated with the input port supply $V_{CCA}$ or $V_{CCB}$.*

# Electrical Characteristics

## DC ELECTRICAL CHARACTERISTICS

$T_A$=25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITION | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CCA}$ | VCCA supply current | $V_I$=0V or $V_{CCI}$, $I_O$=0A | $V_{CCA}$=0.8V to 3.6V, $V_{CCB}$=0.8V to 3.6V | | | 1 | μA |
| | | | $V_{CCA}$=3.6V, $V_{CCB}$=0V | | 27 | | nA |
| | | | $V_{CCA}$=0V, $V_{CCB}$=3.6V | | -23 | | |
| $I_{CCB}$ | VCCB supply current | $V_I$=0V or $V_{CCI}$, $I_O$=0A | $V_{CCA}$=0.8V to 3.6V, $V_{CCB}$=0.8V to 3.6V | | | 1 | μA |
| | | | $V_{CCA}$=3.6V, $V_{CCB}$=0V | | -12 | | nA |
| | | | $V_{CCA}$=0V, $V_{CCB}$=3.6V | | 40 | | |
| $I_{CCA}$+ $I_{CCB}$ | Combined supply current | $V_I$=0V or $V_{CCI}$, $I_O$=0A | $V_{CCA}$=0.8V to 3.6V, $V_{CCB}$=0.8V to 3.6V | | | 2 | μA |
| $I_I$ | DIR input leakage current | $V_I$=3.6V, $V_{CCA}$=$V_{CCB}$=0.8V to 3.6V | | | 0.44 | | μA |
| $I_{OZ}$ | OFF-state output current | A port | $V_O$=0V or $V_{CCO}$, $V_{CCA}$=$V_{CCB}$=3.6V | | ±0.02 | | μA |
| | | B port | $V_O$=0V or $V_{CCO}$, $V_{CCA}$=$V_{CCB}$=3.6V | | ±0.02 | | |
| $I_{OFF}$ | Power off leakage current | A port | $V_I$ or $V_O$=0V to 3.6V, $V_{CCA}$=0V, $V_{CCB}$=0.8V to 3.6V | | ±0.02 | | μA |
| | | B port | $V_I$ or $V_O$=0V to 3.6V, $V_{CCB}$=0V, $V_{CCA}$=0.8V to 3.6V | | ±0.02 | | |
| $V_{IH}$ | High-level input voltage | Data inputs (A port, B port) | $V_{CCI}$=0.8V | 0.7$V_{CCI}$ | | | V |
| | | | $V_{CCI}$=1.1V to 1.95V | 0.65$V_{CCI}$ | | | |
| | | | $V_{CCI}$=2.3V to 2.7V | 1.6 | | | |
| | | | $V_{CCI}$=3.0V to 3.6V | 2 | | | |
| | | DIR | $V_{CCA}$=0.8V | 0.7$V_{CCA}$ | | | |
| | | | $V_{CCA}$=1.1V to 1.95V | 0.65$V_{CCA}$ | | | |
| | | | $V_{CCA}$=2.3V to 2.7V | 1.6 | | | |
| | | | $V_{CCA}$=3.0V to 3.6V | 2 | | | |

| PARAMETER | | TEST CONDITION | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Low-level input voltage | Data inputs (A or B port) | $V_{CCI}$=0.8V | | | 0.3$V_{CCI}$ | V |
| | | | $V_{CCI}$=1.1V to 1.95V | | | 0.35$V_{CCI}$ | |
| | | | $V_{CCI}$=2.3V to 2.7V | | | 0.7 | |
| | | | $V_{CCI}$=3.0V to 3.6V | | | 0.9 | |
| | | DIR | $V_{CCA}$=0.8V | | | 0.3$V_{CCA}$ | |
| | | | $V_{CCA}$=1.1V to 1.95V | | | 0.35$V_{CCA}$ | |
| | | | $V_{CCA}$=2.3V to 2.7V | | | 0.7 | |
| | | | $V_{CCA}$=3.0V to 3.6V | | | 0.9 | |
| $V_{OH}$ | High-level output voltage | $V_I$=$V_{IH}$ | $I_O$= -100μA; $V_{CCA}$=$V_{CCB}$=0.8V to 3.6V | $V_{CCO}$-0.1 | | | V |
| | | | $I_O$= -3mA; $V_{CCA}$=$V_{CCB}$=1.1V | 0.85 | | | |
| | | | $I_O$= -6mA; $V_{CCA}$=$V_{CCB}$=1.4V | 1.05 | | | |
| | | | $I_O$= -8mA; $V_{CCA}$=$V_{CCB}$=1.65V | 1.2 | | | |
| | | | $I_O$= -9mA; $V_{CCA}$=$V_{CCB}$=2.3V | 1.75 | | | |
| | | | $I_O$= -12mA; $V_{CCA}$=$V_{CCB}$=3.0V | 2.3 | | | |
| $V_{OL}$ | Low-level output voltage | $V_I$=$V_{IL}$ | $I_O$= 100μA; $V_{CCA}$=$V_{CCB}$=0.8V to 3.6V | | | 0.1 | V |
| | | | $I_O$= 3mA; $V_{CCA}$=$V_{CCB}$=1.1V | | | 0.25 | |
| | | | $I_O$= 6mA; $V_{CCA}$=$V_{CCB}$=1.4V | | | 0.35 | |
| | | | $I_O$= 8mA; $V_{CCA}$=$V_{CCB}$=1.65V | | | 0.45 | |
| | | | $I_O$= 9mA; $V_{CCA}$=$V_{CCB}$=2.3V | | | 0.55 | |
| | | | $I_O$= 12mA; $V_{CCA}$=$V_{CCB}$=3.0V | | | 0.7 | |
| $C_I$(1) | Input capacitance | DIR, $V_I$=0V or 3.3V, $V_{CCA}$=$V_{CCB}$=3.3V | | | 2.0 | | pF |
| $C_{I/O}$(1) | Input/ output capacitance | A or B port, $V_O$=$V_{CCO}$ or GND, $V_{CCA}$=$V_{CCB}$=3.3V | | | 4.0 | | pF |

（1）Typical value set by simulation only.

## SWITCHING CHARACTERISTICS

$T_A$=25°C for typical values (unless otherwise noted)

| PARAMETERS | | TEST CONDITION | | $V_{CCB}$ | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 0.8V | 1.2V | 1.5V | 1.8V | 2.5V | 3.3V | |
| | | | | TYP | TYP | TYP | TYP | TYP | TYP | |
| $t_{pd}$ | Propagation delay | $V_{CCA}$=0.8V | A to B | 23.2 | 14.5 | 13.1 | 12.5 | 12.0 | 12.2 | ns |
| | | | B to A | 29.0 | 22.8 | 21.6 | 21.1 | 20.3 | 20.0 | |
| | | $V_{CCA}$=1.2V | A to B | 20.4 | 11.1 | 9.3 | 8.5 | 7.7 | 7.5 | |
| | | | B to A | 17.9 | 12.1 | 10.9 | 10.3 | 9.7 | 9.3 | |
| | | $V_{CCA}$=1.5V | A to B | 19.2 | 10.0 | 8.3 | 7.4 | 6.6 | 6.1 | |
| | | | B to A | 16.2 | 10.2 | 8.9 | 8.3 | 7.7 | 7.3 | |
| | | $V_{CCA}$=1.8V | A to B | 18.7 | 9.5 | 7.7 | 6.8 | 6.0 | 5.5 | |
| | | | B to A | 15.5 | 9.3 | 8.0 | 7.3 | 6.7 | 6.4 | |
| | | $V_{CCA}$=2.5V | A to B | 18.1 | 8.9 | 7.1 | 6.2 | 5.3 | 4.9 | |
| | | | B to A | 15.1 | 8.3 | 7.0 | 6.3 | 5.7 | 5.3 | |
| | | $V_{CCA}$=3.3V | A to B | 17.7 | 8.6 | 6.7 | 5.9 | 4.9 | 4.5 | |
| | | | B to A | 15.3 | 7.9 | 6.6 | 5.9 | 5.2 | 4.9 | |
| $t_{dis}$ | Disable time | $V_{CCA}$=0.8V | DIR to A | 26.6 | 26.8 | 27 | 27.5 | 27.7 | 27.2 | ns |
| | | | DIR to B | 36.6 | 22.2 | 19.4 | 18.4 | 17.6 | 18 | |
| | | $V_{CCA}$=1.2V | DIR to A | 12.2 | 11.9 | 12.3 | 12.3 | 12.4 | 12.1 | |
| | | | DIR to B | 28.2 | 16.1 | 13.4 | 12.3 | 10.6 | 10.3 | |
| | | $V_{CCA}$=1.5V | DIR to A | 9.1 | 8.8 | 9.1 | 8.9 | 9.1 | 9.3 | |
| | | | DIR to B | 24.3 | 15.0 | 12.0 | 11.0 | 9.1 | 8.8 | |
| | | $V_{CCA}$=1.8V | DIR to A | 7.6 | 7.6 | 7.7 | 7.6 | 8.0 | 7.9 | |
| | | | DIR to B | 22.4 | 14.4 | 11.4 | 10.4 | 8.4 | 7.9 | |
| | | $V_{CCA}$=2.5V | DIR to A | 5.4 | 5.7 | 5.6 | 5.7 | 5.8 | 5.8 | |
| | | | DIR to B | 18.7 | 14.0 | 10.9 | 8.2 | 7.8 | 7.1 | |
| | | $V_{CCA}$=3.3V | DIR to A | 4.9 | 5.1 | 5.0 | 5.1 | 5.1 | 5.1 | |
| | | | DIR to B | 17.1 | 13.1 | 10.9 | 9.1 | 7.6 | 7.0 | |

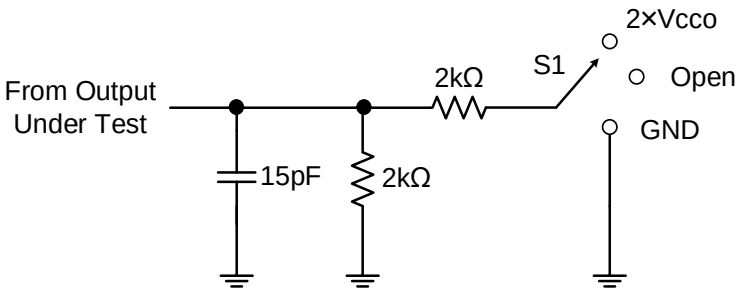
| PARAMETERS | | TEST CONDITION | | $V_{CCB}$ | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 0.8V | 1.2V | 1.5V | 1.8V | 2.5V | 3.3V | |
| | | | | TYP | TYP | TYP | TYP | TYP | TYP | |
| $t_{en}$(1) | Enable time | $V_{CCA}$=0.8V | DIR to A | 65.6 | 45 | 41 | 39.5 | 37.9 | 38 | ns |
| | | | DIR to B | 49.8 | 41.3 | 40.1 | 40 | 39.7 | 39.4 | |
| | | $V_{CCA}$=1.2V | DIR to A | 46.1 | 28.2 | 24.3 | 22.6 | 20.3 | 19.6 | |
| | | | DIR to B | 32.6 | 23 | 21.6 | 20.8 | 20.1 | 19.6 | |
| | | $V_{CCA}$=1.5V | DIR to A | 40.5 | 25.2 | 20.9 | 19.3 | 16.8 | 16.1 | |
| | | | DIR to B | 28.3 | 18.8 | 17.4 | 16.3 | 15.7 | 15.4 | |
| | | $V_{CCA}$=1.8V | DIR to A | 37.9 | 23.7 | 19.4 | 17.7 | 15.1 | 14.3 | |
| | | | DIR to B | 26.3 | 17.7 | 15.4 | 14.4 | 14 | 13.4 | |
| | | $V_{CCA}$=2.5V | DIR to A | 33.8 | 22.3 | 17.9 | 14.5 | 13.5 | 12.4 | |
| | | | DIR to B | 23.5 | 14.6 | 12.7 | 11.9 | 11.1 | 10.7 | |
| | | $V_{CCA}$=3.3V | DIR to A | 32.4 | 21 | 17.5 | 15 | 12.8 | 11.9 | |
| | | | DIR to B | 22.6 | 13.7 | 11.7 | 11 | 10 | 9.6 | |

（1）$t_{en}$ is a calculated value:

- $t_{en}$ (DIR to nA) = $t_{dis}$ (DIR to nB) + $t_{pd}$ (nB to nA)
- $t_{en}$ (DIR to nB) = $t_{dis}$ (DIR to nA) + $t_{pd}$ (nA to nB)

# Typical Characteristic

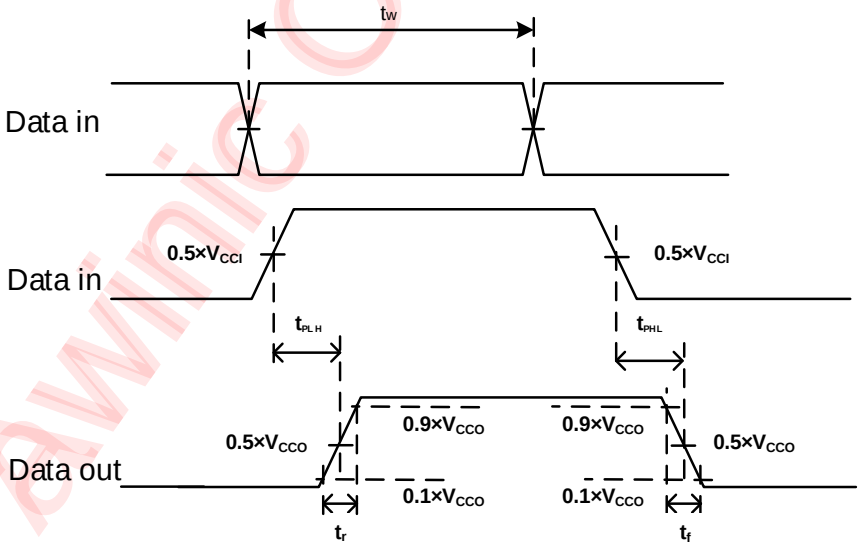
## TEST INFORMATION




| TEST | S1 |
|---|---|
| $t_{PZL}/t_{PLZ}$ | 2 × $V_{CCO}$ |
| $t_{PZH}/t_{PHZ}$ | GND |
| $t_{PLH}/t_{PHL}$ | Open |

1. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
2. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
3. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
4. VCCI is the VCC associated with the input port.
5. VCCO is the VCC associated with the output port.
6. The resistance and Capacitance values at output notes above are the total effective values.

**Figure 7 Load Circuit for Enable Time ,Propagation Delay Time and Disable Time Measurement**



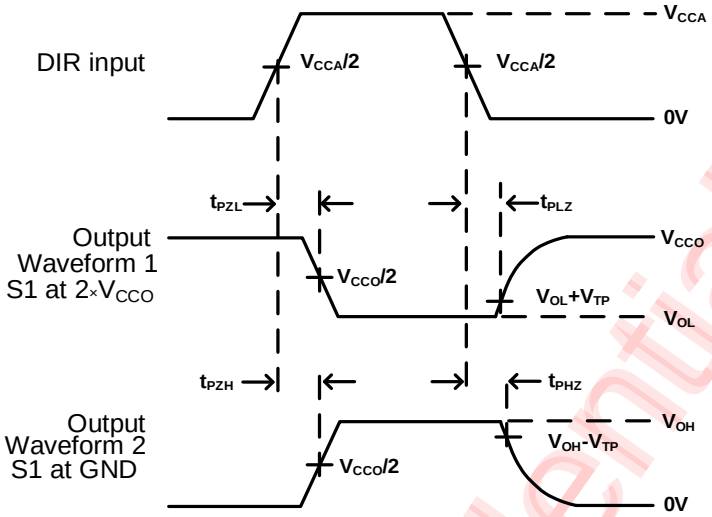

The input pulses should have the following characteristics:

1. PRR ≤10MHz.
2. dv/dt ≥ 1V/ns.
3. $Z_O$ = 50Ω

**Figure 8 Timing Parameter Definition**






1. The Waveform 1 is obtained under the condition that the input is low and S1 at 2*$V_{CCO}$.

2. The Waveform 2 is obtained under the condition that the input and S1 at GND.

3. The following table gives the value of $V_{TP}$ under different supply voltage：

| $V_{CCA}$, $V_{CCB}$ | $V_{TP}$ |
|---|---|
| 1.1V to 1.6V | 0.1V |
| 1.65V to 2.7V | 0.15V |
| 3.0V to 3.6V | 0.3V |

**Figure 9 Enable and Disable Times**



# Detailed Functional Description

AWS74AVC2T45TSR is a dual-bit, dual-supply high-performance voltage-level translator with direction control pin that enables bidirectional level translation. Both A pins and DIR pin are referenced to $V_{CCA}$ and accepts any supply voltage from 0.8 V to 3.6 V. B pins are referenced to $V_{CCB}$ and accepts any supply voltage from 0.8 V to 3.6 V. This allows for universal low-voltage bidirectional translation and level-shifting between any of the 0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V voltage nodes. The device transmits data from the A port to the B port when the DIR pin is HIGH. The device transmits data from the B port to the A port when the DIR pin is LOW. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess internal leakage of the CMOS.

The AWS74AVC2T45TSR is fully specified for partial power-down applications using off output current ($I_{OFF}$). The outputs for this device enter a high-impedance state when the device is powered down, preventing any damaging backflow current through the device. The $V_{CC}$ isolation feature ensures that if either $V_{CCA}$ or $V_{CCB}$ is at GND, both A and B ports are put in a high-impedance state.

## VCC Isolation

The $V_{CC}$ isolation feature ensures that if either $V_{CCA}$ or $V_{CCB}$ is at GND, both A and B ports are put in a high-impedance state($I_{OZ}$). This will prevent a false high or low logic being presented at the output.

## Partial-Power-Down Mode

The AWS74AVC2T45TSR is fully specified for partial-power-down applications using off output current ($I_{off}$). The outputs for this device enter a high-impedance state when the device is powered down, preventing any damaging backflow current through the device.

## DIR Control

The AWS74AVC2T45TSR's DIR pin can control the direction of data transfer. The DIR pin is referenced to $V_{CCA}$ and accepts any supply voltage from 0.8 V to 3.6 V. The DIR pin has a 8.2MΩ internal pull-down resistor to ensure that the data transmission direction is B to A when the DIR port is floating. The device transmits data from the A port to the B port when the DIR pin is HIGH. The device transmits data from the B port to the A port when the DIR pin is LOW.

## Functional Modes

If at least one of VCCA or VCCB is at GND, both A and B ports are put in a high-impedance state.

| VCCA, VCCB | DIR | nA | nB |
|---|---|---|---|
| 0.8V to 3.6V | L | nA = nB | input |
| 0.8V to 3.6V | H | input | nB = nA |
| GND | X | Hi-Z | Hi-Z |

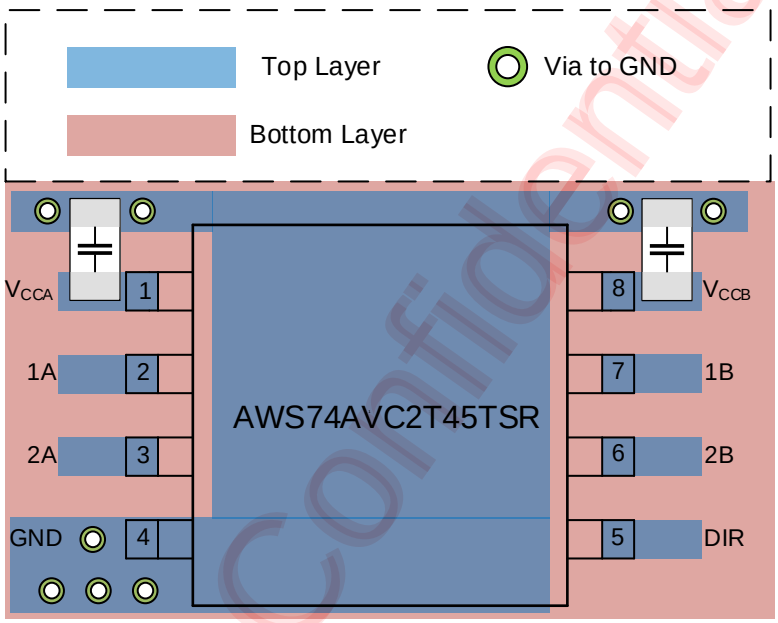


## PCB Layout Consideration

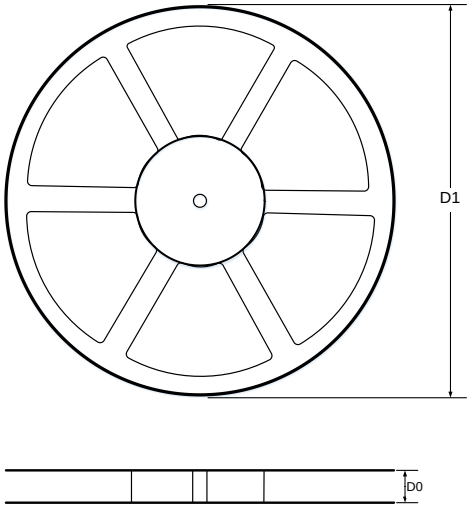
To obtain the optimal performance of AWS74AVC2T45TSR, PCB layout should be considered carefully. Here are some guidelines:

1. Bypass capacitors should be used on power supplies. Place the capacitors as close as possible to the VCCA, VCCB pin and GND pin. A 0.1 μF capacitor is recommended, but transient performance can be improved by having both 1 μF and 0.1 μF capacitors in parallel as bypass capacitors.
2. Routing and load conditions should be considered to prevent ringing.

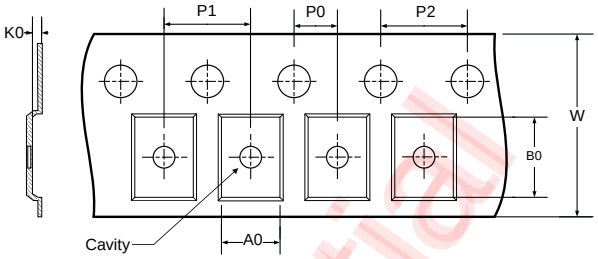


# Tape And Reel Information

REEL DIMENSIONS

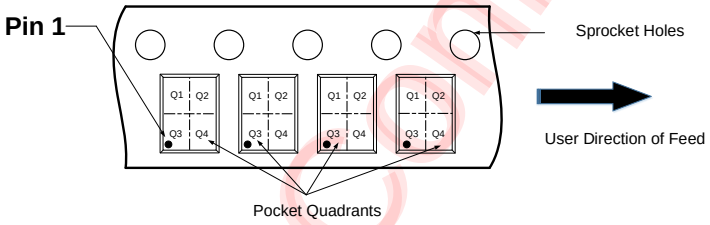



TAPE DIMENSIONS




A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

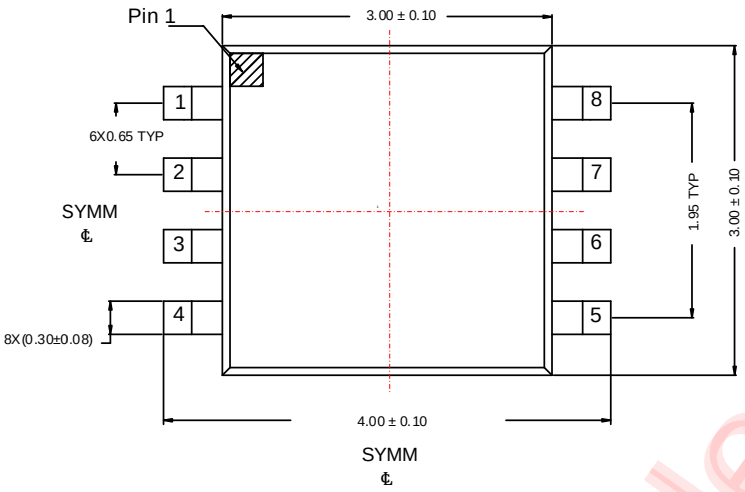
| D1 (mm) | D0 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|
| 330 | 12.4 | 3.35 | 4.45 | 1.45 | 2 | 4 | 4 | 12 | Q3 |

**All dimensions are nominal**

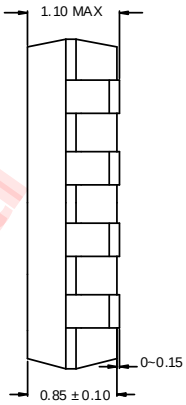


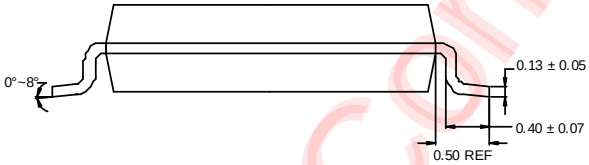
## Package Description




Top View




Side View



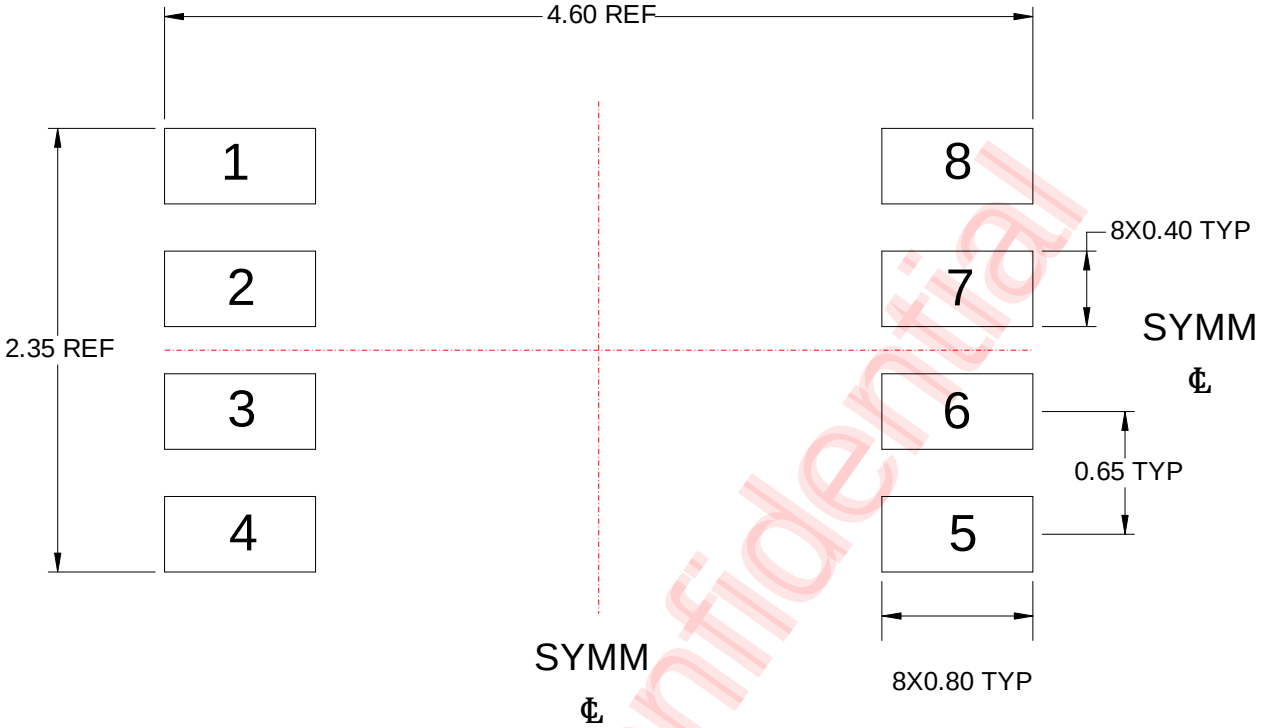

Side View

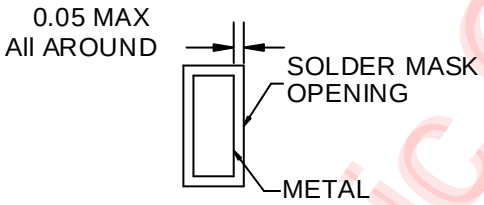
Unit:mm



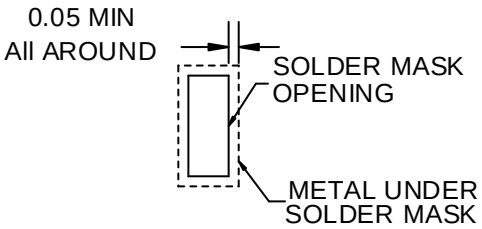
 

## Land Pattern Data




NON SOLDER MASK DEFINED




SOLDER MASK DEFINED

Unit:mm

# Revision History

| Version | Date | Change Record |
|---|---|---|
| V1.0 | Feb. 2022 | Officially released |
| V1.1 | Mar. 2023 | Updated maximum data rates description (P1) |

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