High Sensitivity Micropower Linear Hall-effect Sensor

Features

- Ratiometric linear hall effect magnetic sensor.
- Analog output with VREF / 2 quiescent offset
- High-impedance output during sleep mode.
- Operates from 2.5V and 5.5V power supplies
- Less than 1.5μA power consumption in the sleep mode.
- Sensitivity selection

  AW86561CDNR: 2.50mV/Gs
- Reference voltage (VREF pin).
- Temperature-stable quiescent voltage output and sensitivity
- Wide operating temperature range: -40℃ to 125℃
- WBDFN 3mm X 2mm X 0.75mm-6L package

Applications

- Accurate position detection
- Industrial automation robot
- Handheld gaming consoles
- Bluetooth headset
- Medical facility
- Domestic appliance

General Description

The AW86561CDNR are linear Hall effect IC that respond proportionally to magnetic flux density.. The quiescent output voltage of these devices is 50 % nominal of the ratiometric supply reference voltage applied to the VREF pin of the device.

The AW86561CDNR consume 2.6 mA of current in the active mode. minimize current consumption to less than 1.5 μA through the addition of a user-selectable sleep mode.

The AW86561CDNR features magnet temperature compensation to counteract how magnets drift for linear performance across a wide –40°C to +125°C temperature range. Device options for no temperature compensation of magnet drift are also available.

The AW86561CDNR are available in 6 pin DFN and are rated over –40°C to +125°C. The package is available in a lead (Pb)free version.

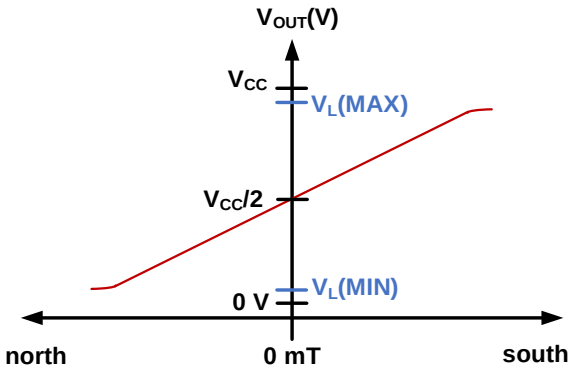


Figure 1 V_{OUT} versus Magnetic Field (V_{CC}=V_{REF})

Typical Application Circuit

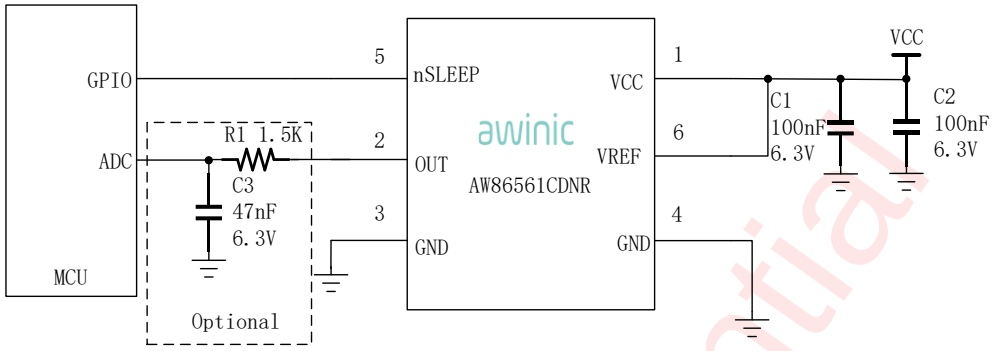
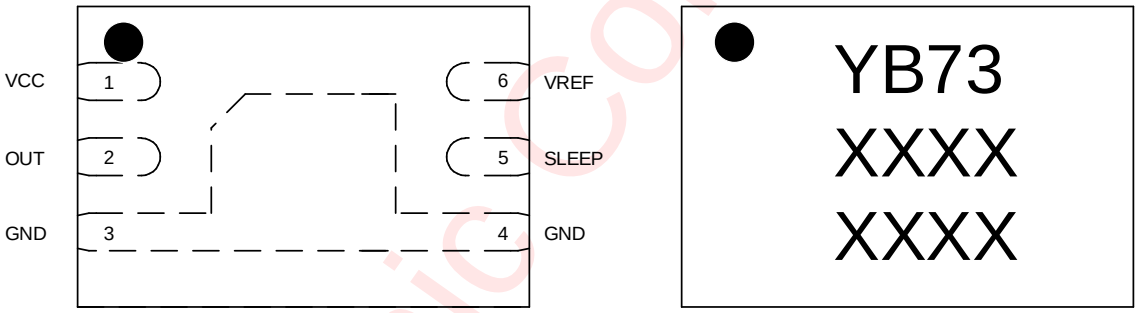


Figure 2 Typical Application Circuit of AW86561CDNR

Pin Configuration And Top Mark

AW86561CDNR
(Top View)

AW86561CDNR Marking
(Top View)



YB73 – AW86561CDNR
XXXX/XXXX – Production Tracing Code

Figure 3 Pin Configuration And Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	VCC	Power Supply
2	OUT	Analog Output
3	GND	Ground
4	GND	Ground
5	nSLEEP	Toggle sleep mode
6	VREF	Supply for ratiometric reference

Functional Block Diagram

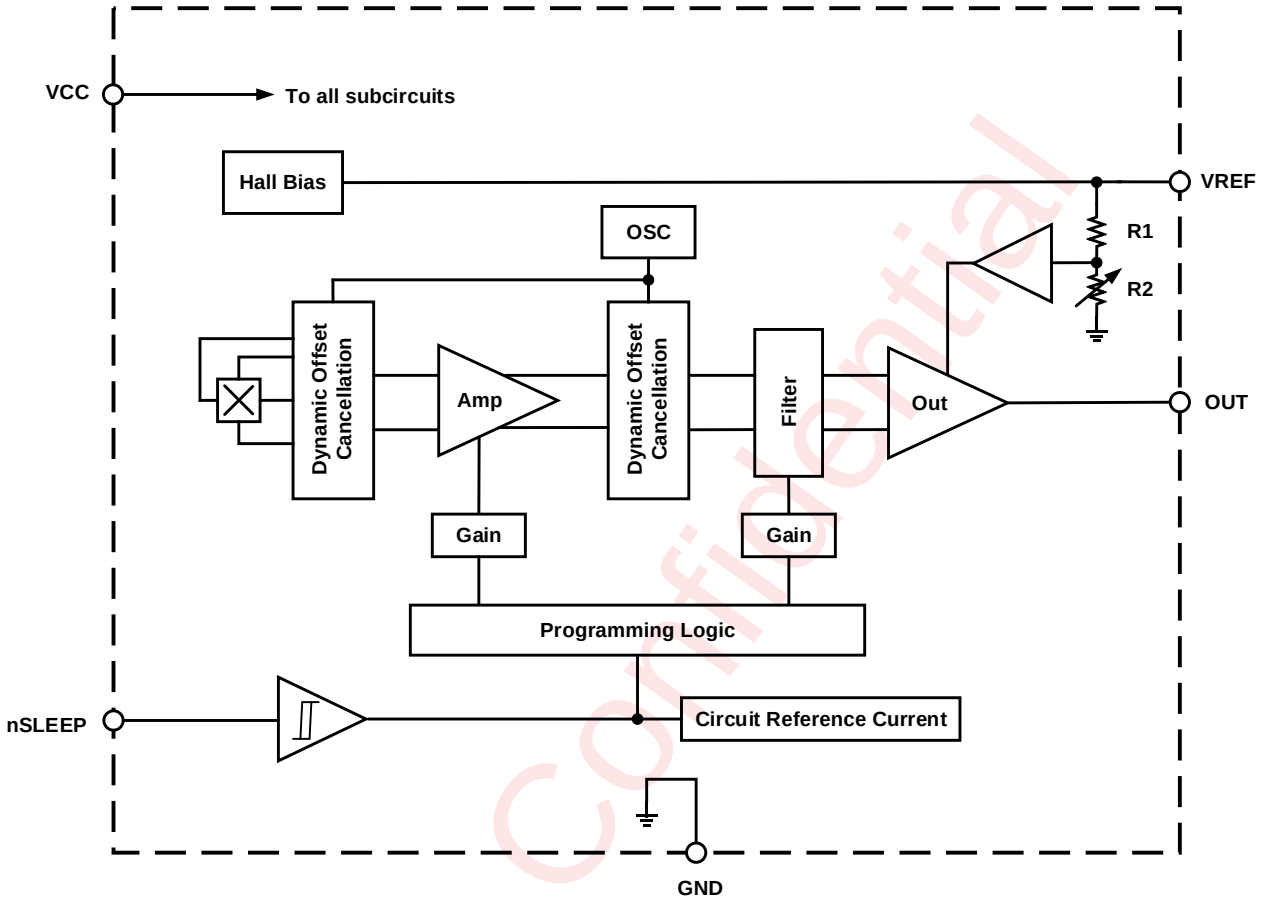


Figure 4 Functional Block Diagram

Typical Application Circuits

Device Supply Ratiometry Application Circuit

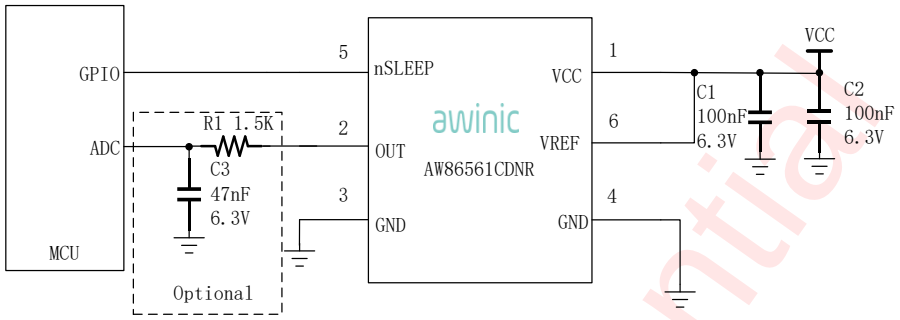


Figure 5 Showing microprocessor-controlled sleep mode and output ratiometric

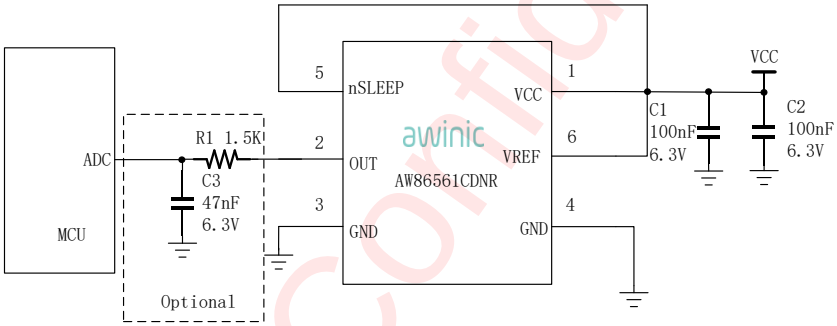


Figure 6 Showing sleep mode disabled and output ratiometric

Figures 5 and 6 present applications where the VCC pin is connected together with the VREF pin of the AW86561CDNR. Both of these pins are connected to VCC. In this case, the device output will be ratiometric with respect to the VCC voltage.

In figure 5, the nSLEEP pin is toggled by the microprocessor; therefore, the device is selectively and periodically toggled between active mode and sleep mode.

In figure 6, the nSLEEP pin is connected to the VCC potential, so the device is always in the active mode.

In both figures, the device output is connected to the input of an A-to-D converter. In this configuration, the converter reference voltage is VCC.

It is strongly recommended that an external bypass capacitor be connected, in close proximity to the AW86561CDNR device, between the VCC and GND pins of the device to reduce both external noise and noise generated by the chopper-stabilization circuits inside of the AW86561CDNR.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW86561CDNR	-40℃~125℃	WBDFN 3mmX2mm-6L	YB73	MSL1	ROHS+HF	3000 units/ Tape and Reel

Detailed Function Description

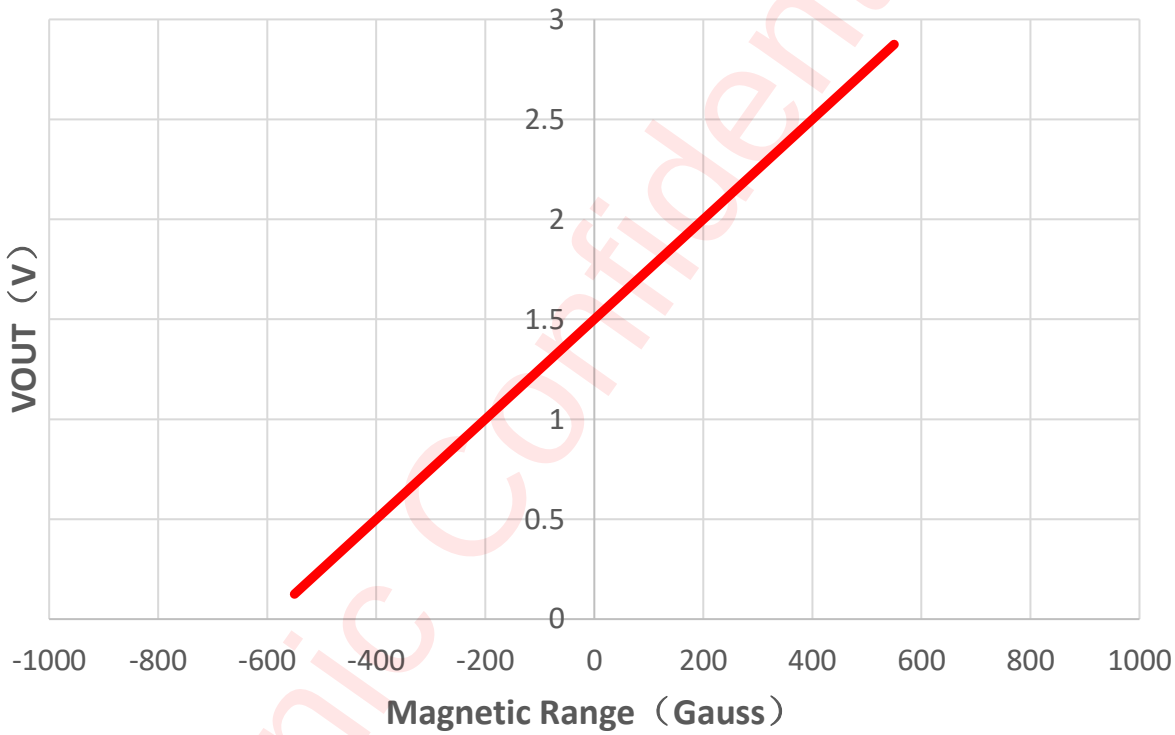


Figure 7 V_{OUT} versus Magnetic Field (V_{CC}=V_{REF}=3V)

Absolute Maximum Ratings

PARAMETERS	RANGE
Supply Voltage V_{CC}	-0.1V to 6V
Ratiometric Supply Reference Voltage V_{REF}	-0.1V to 6V
Logic Supply Voltage V_{SLEEP}	-0.1V to 6V
Output Voltage V_{OUT}	VCC + 0.1V
Reverse-Output Voltage V_{ROUT}	-0.1V
Operating Ambient Temperature T_A	－40 to 125℃
Junction Temperature T_J(MAX)	150℃
StorageTemperature T_{stg}	－65 to 150℃
Lead temperature (soldering 10 seconds)	260°C
ESD Rating(NOTE2 3)	
Human Body Model (HBM) ESD capability	±6kV
Charged-device model (CDM) ESD capability	±1.5kV
Latch-up	
Test Condition: JESD78E	＋IT: 200mA －IT: 200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2:The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS -001-2017.

NOTE3:Charge Device Model test method: ESDA/JEDEC JS-002-2018.

Electrical Characteristics

T_A = 25°C, V_{CC} = V_{REF} = V_{CCN} for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP[1]	MAX	UNIT
V_{CC}	Supply Voltage		2.5	–	5.5	V
V_{CCN}	Nominal Supply Voltage		–	3.0	–	V
V_{REF}	Ratiometric Reference Voltage[2]		2.5	–	V_{CC}	V
V_{nSLEEP}	nSLEEP Input Voltage		–0.1		V_{CC} + 0.1V	V
V_{INH}	nSLEEP Input Threshold	For active mode	–	0.45 × V_{CC}	–	V
V_{INL}		For sleep mode	–	0.20 ×V_{CC}	–	V
R_{REF}[5]	Ratiometric Reference Input Resistance	V_{SLEEP} > V_{INH}	140	–	–	kΩ
		V_{SLEEP} < V_{INL}	–	1	–	MΩ
f_C	Chopper Stabilization Chopping Frequency	V_{CC} = V_{CCN}	–	200	–	kHz
I_{CC}	Supply Current[3]	V_{SLEEP} < V_{INL}	–	1.5	–	μA
		V_{SLEEP} > V_{INH}	–	3	–	mA
I_{SLEEP}	nSLEEP Input Current	V_{SLEEP} = 3 V	–	1	–	μA
PSR_{VOQ}	Quiescent Output Power Supply Rejection[4]	f_{AC} < 1 kHz	–	-60	–	dB

[1]Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions, such as T_A = 25°C. Performance

may vary for individual units, within the specified maximum and minimum limits.

[2] Voltage applied to the VREF pin. Note that the VREF voltage must be less than or equal to Vcc. Degradation in device accuracy will occur with applied

voltages of less than 2.5 V.

[3] If the VREF pin is tied to the VCC pin, the supply current would be IVcc + VREF / RREF

[4] f_{AC} is any ac component frequency that exists on the supply line.

[5] Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

Output Characteristics

T_A = 25°C, V_{CC} = V_{REF} = V_{CCN} for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP[1]	MAX	UNIT
V_{OUTH}	Output Voltage Saturation Limits[2]	B = ***X***	–	V_{CC} – 0.1	–	V
V_{OUTL}		B = –***X***	–	0.1	–	V
V_{OUTMAX}[6]	Maximum Voltage Applied to Output	V_{SLEEP} < V_{INL}	–	–	V_{CC} + 0.1	V
Sens	Sensitivity[3]	C_{Bypass}=100nF	–	2.50	–	mV/Gs
V_{OUTQ}	Quiescent Output	B = 0 Gs		0.5 × V_{REF}		V
R_{OUT}	Output Resistance[4]	f_{out} = 1 kHz, V_{SLEEP} > V_{INH}, Active mode	–	20	–	Ω
		f_{out} = 1 kHz, V_{SLEEP} < V_{INL}, Sleep mode	–	1M	–	Ω
R_L[6]	Output Load Resistance	Output to ground	15	–	–	kΩ
C_L[6]	Output Load Capacitance		–	–	1	nF
BW	Output Bandwidth	–3 dB point, V_{CC} = V_{CCN}, V_{OUT} = 1 V_{pp} sinusoidal	–	10	–	kHz
V_{rms}	Noise[5]	C_{Bypass}=100nF R_{filter}=1.5KΩ C_{filter}=47nF	–	0.96	–	mVrms
S_{TC}	Sensitivity temperature compensation for magnets	-40°C ≤ T_A ≤ 125°C	0.12			%/°C
S_{LE}	Sensitivity linear error	within the Output Voltage Saturation Range		±1		%

[1]Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions, such as TA = 25°C. Performance

may vary for individual units, within the specified maximum and minimum limits.

[2]This test requires positive and negative magnetic fields sufficient to swing the output driver between fully OFF and saturated (ON), respectively. The

value of vector X is NOT intended to indicate a range of linear operation.

[3]For VREF values other than VREF = VCCN , the sensitivity can be derived from the following equation: 0.416 × VREF.

[4]f OUT is the output signal frequency

[5]Noise specification includes digital and analog noise.

[6] Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

Output Timing Characteristics

PARAMETER[1]		TEST CONDITION	MIN	TYP[2]	MAX	UNIT
t_{PON}	Power-On Time[3]	T_A = 25°C	–	40	–	μs
t_{POFF}	Power-Off Time[4]	T_A = 25°C	–	1	–	μs

[1]See figure 10 for explicit timing delays.

[2]Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions, such as T_A = 25°C. Performance may vary for individual units, within the specified maximum and minimum limits.

[3]Power-On Time is the elapsed time after the voltage on the nSLEEP pin exceeds the active mode threshold voltage, V_{INH}, until the time the device output reaches 90% of its value. When the device output is loaded with the maximum capacitance of 1 nF, the Power-On Time range is guaranteed for input nSLEEP pin frequencies less than 10 Hz.

[4]Power-Off Time is the duration of time between when the signal on the nSLEEP pin switches from HIGH to LOW and when I_{CC} drops to under 100 μA. During this time period, the output goes into the HIGH impedance state.

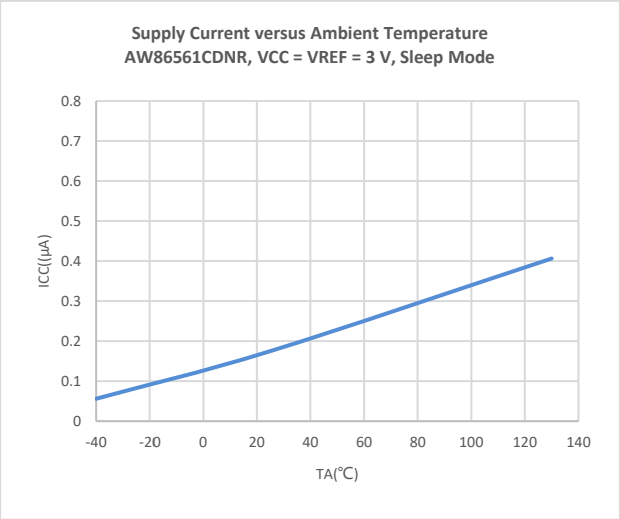
Magnetic Characteristics

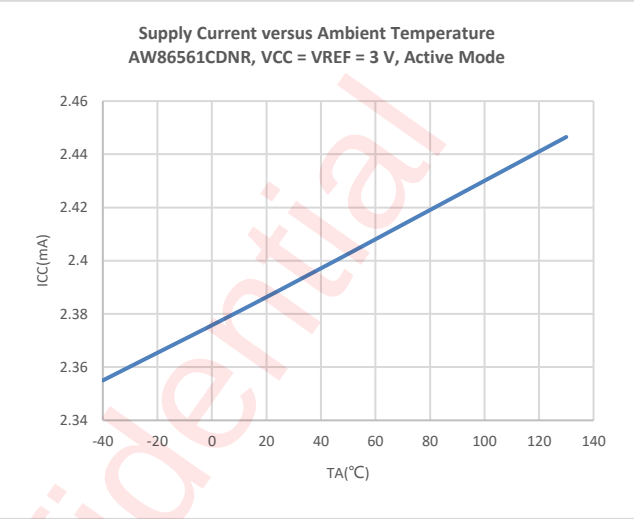
PARAMETER		TEST CONDITION	MIN	TYP*	MAX	UNIT
$\Delta V_{OUTQ(\Delta V)}$	Ratiometry		–	99.5	–	%
$\Delta Sens_{(\Delta V)}$	Ratiometry		–	99.5	–	%
Lin+	Positive Linearity		–	99.0	–	%
Lin-	Negative Linearity		–	99.0	–	%
Sym	Symmetry		–	98.0	–	%

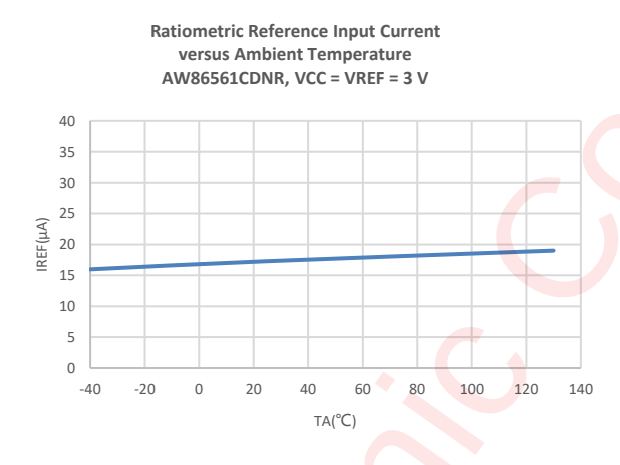
*Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions, such as TA = 25°C. Performance may vary for individual units, within the specified maximum and minimum limits.

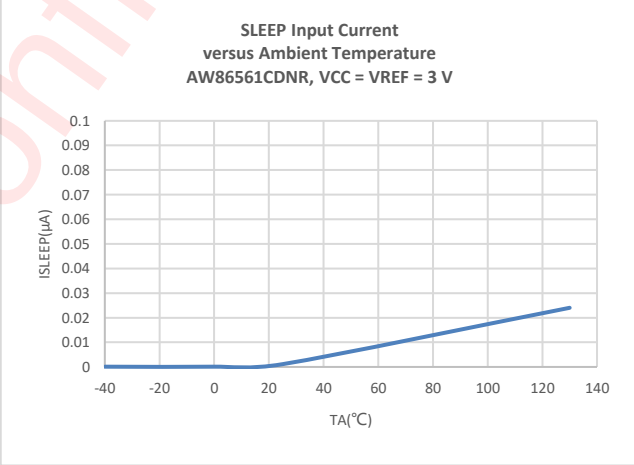
Typical Characteristics

Electrical Characteristic Data

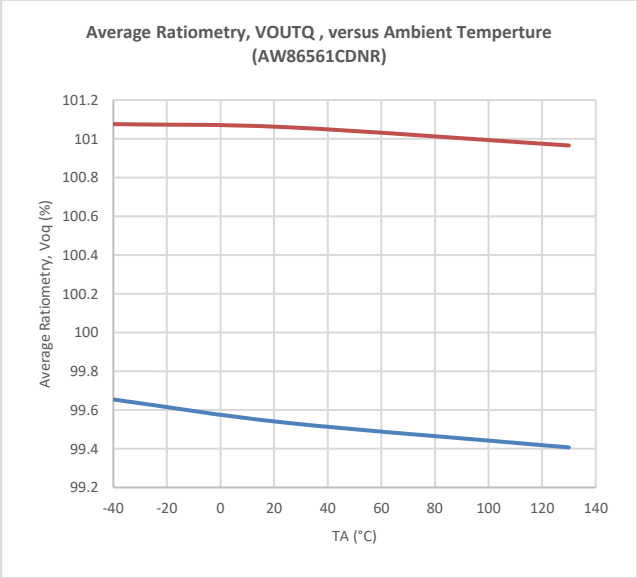


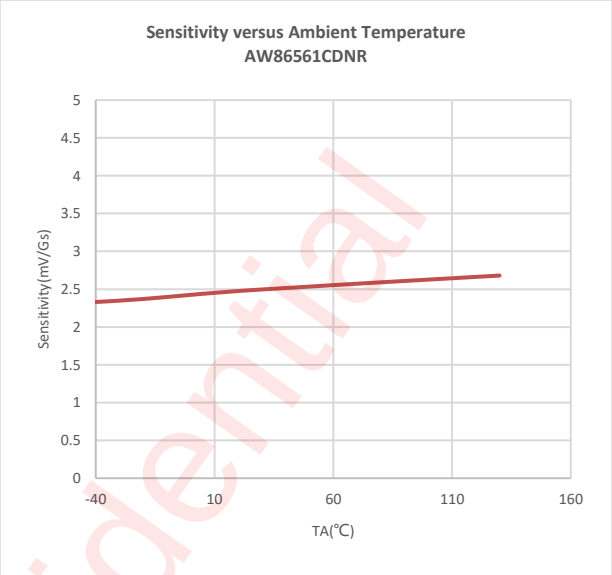


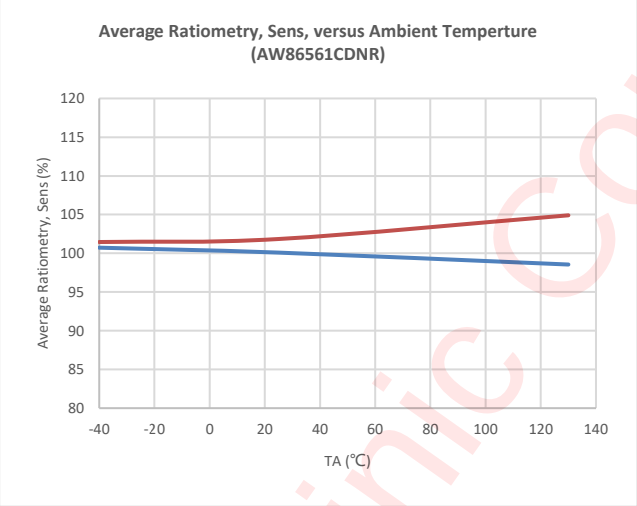


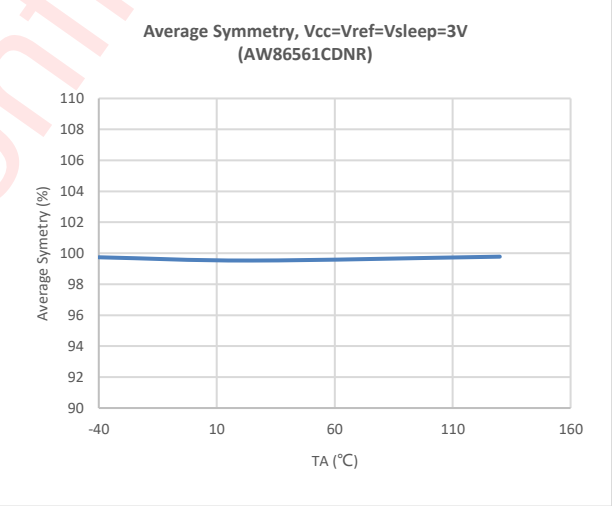


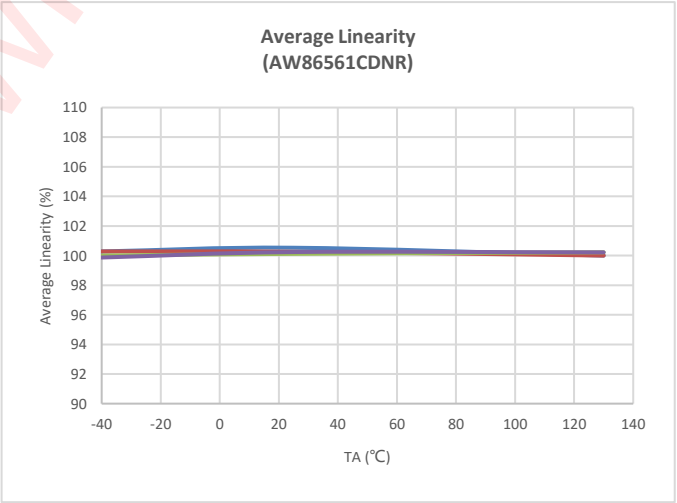
Magnetic Characteristic Data











Characteristics Definitions

Ratiometric. The AW86561CDNR devices feature ratiometric output. The quiescent voltage output and sensitivity are proportional to the ratiometric supply reference voltage. The percent ratiometric change in the quiescent voltage output is defined as:

$$\Delta V_{OUTQ(\Delta V)} = \frac{\Delta V_{OUTQ(VREF)} \div \Delta V_{OUTQ(3V)}}{V_{REF} \div 3V} \times 100\% \quad (1)$$

and the percent ratiometric change in sensitivity is defined as:

$$\Delta Sens_{(\Delta V)} = \frac{\Delta Sens_{(VREF)} \div \Delta Sens_{(3V)}}{V_{REF} \div 3V} \times 100\% \quad (2)$$

Linearity and Symmetry. The on-chip output stage is designed to provide a linear output with maximum supply voltage of V_{CCN}. Although application of very high magnetic fields will not damage these devices, it will force the output into a non-linear region. Linearity in percent is measured and defined as:

$$Lin+ = \frac{V_{OUT(+B)} - V_{OUTQ}}{2 \times (V_{OUT(+B/2)} - V_{OUTQ})} \times 100\% \quad (3)$$

$$Lin- = \frac{V_{OUT(-B)} - V_{OUTQ}}{2 \times (V_{OUT(-B/2)} - V_{OUTQ})} \times 100\% \quad (4)$$

and output symmetry as:

$$sym = \frac{V_{OUT(+B)} - V_{OUTQ}}{V_{OUTQ} - V_{OUT(-B)}} \times 100\% \quad (5)$$

The Parameter S_{LE} defines the linear error as the difference in sensitivity between any positive B values and any negative B values when the output is within the Output Voltage Saturation range.

$$S_{LE} = \frac{sen_+ - sen_-}{0.5 \times (sen_+ + sen_-)} \times 100\% \quad (6)$$

Detailed Functional Description

AW86561CDNR are low-power Hall effect sensor ICs that are perfect for power sensitive customer applications. The current consumption of these devices is typically 2.6 mA, while the device is in the active mode, and less than 1 μA when the device is in the sleep mode. Toggling the logic level signal connected to the nSLEEP pin drives the device into either the active mode or the sleep mode. A logic low sleep signal drives the device into the sleep mode, while a logic high sleep signal drives the device into the active mode.

In the case in which the VREF pin is powered before the VCC pin, the device will not operate within the specified limits until the supply voltage is equal to the reference voltage. When the device is switched from the sleep mode to the active mode, a time defined by t_{PON} must elapse before the output of the device is valid. The device output transitions into the high impedance state approximately t_{POFF} seconds after a logic low signal is applied to the nSLEEP pin (see Figure 8).

If possible, it is recommended to power-up the device in the sleep mode. However, if the application requires that the device be powered on in the active mode, then a 10 kΩ resistor in series with the nSLEEP pin is recommended. This resistor will limit the current that flows into the nSLEEP pin if certain semiconductor junctions become forward biased before the ramp up of the voltage on the VCC pin. Note that this current limiting resistor is not required if the user connects the nSLEEP pin directly to the VCC pin. The same precautions are advised if the device supply is powered-off while power is still applied to the nSLEEP pin.

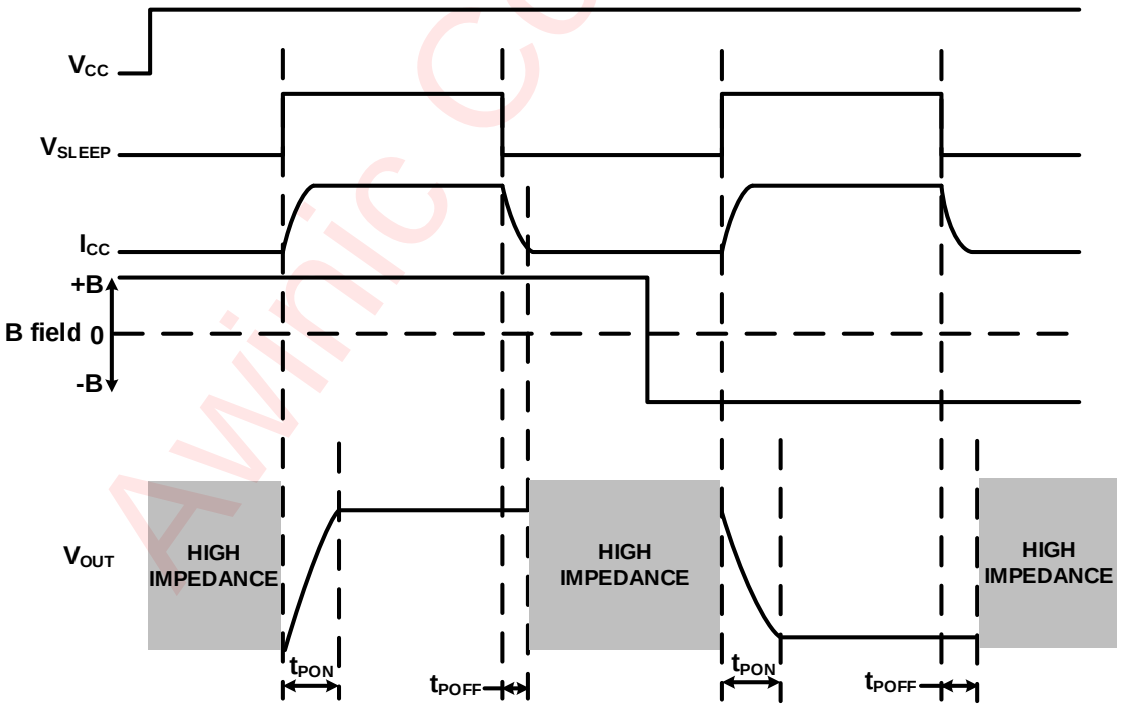
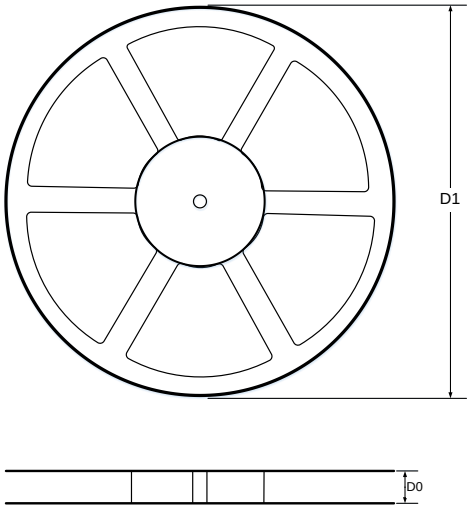


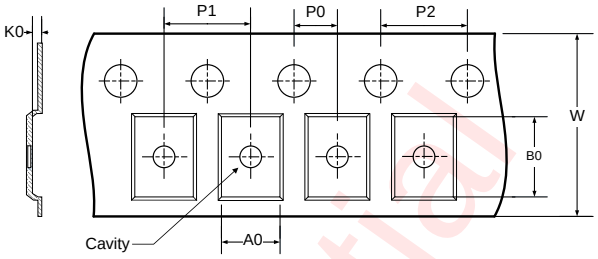
Figure 8 AW86561CDNR Timing Diagram

Tape And Reel Information

REEL DIMENSIONS

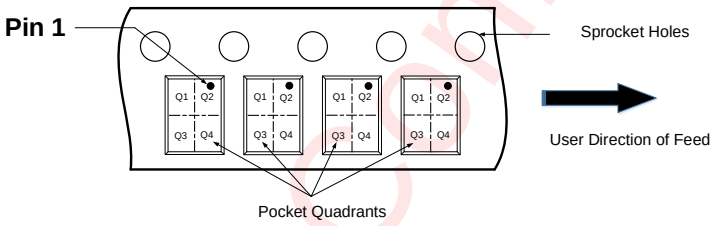


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



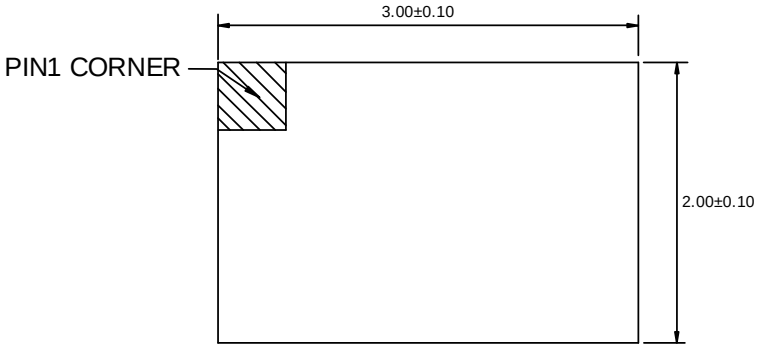
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

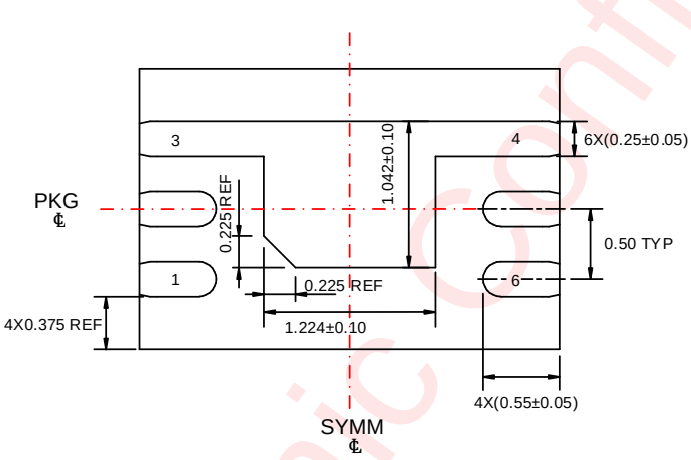
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2.3	3.2	1	2	4	4	8	Q2

All dimensions are nominal

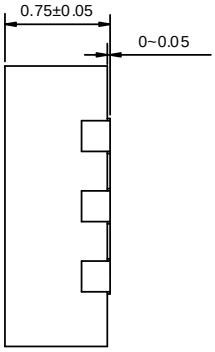
Package Description



Top View



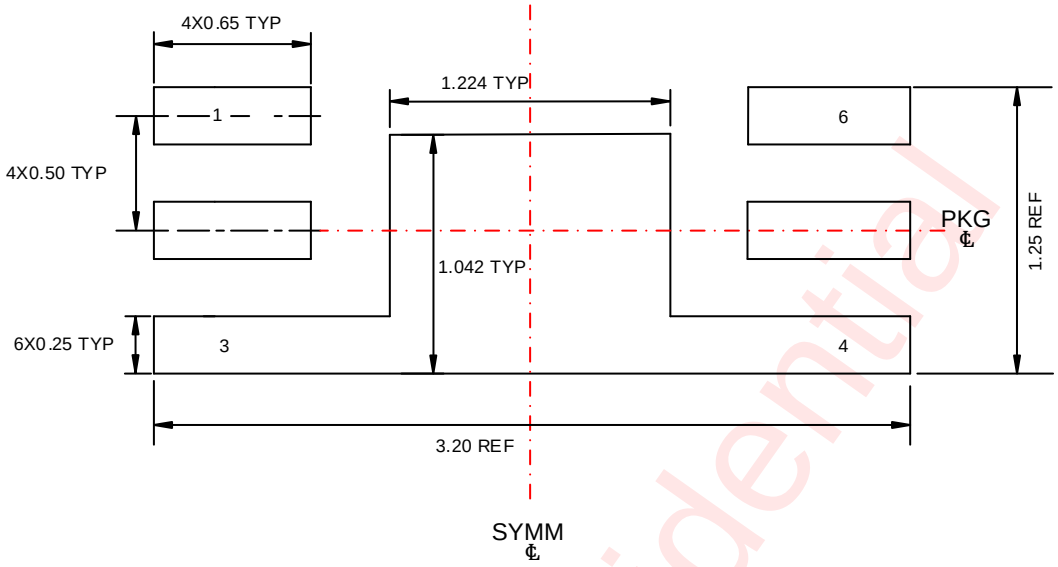
Bottom View

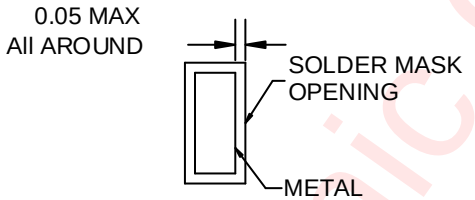


Side View

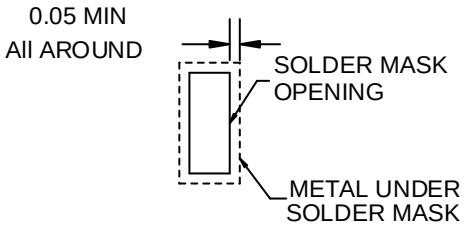
Unit: mm

Land Pattern Data





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Feb. 2025	Official released

Disclaimer

All trademarks are the property of their respective owners. Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.