36V, 12MHz, 19V/μs Op Amps

Features

- Supply Voltage: 4.5V to 36V
- Supply Current: Maximum 2150μA per channel
- Differential Input Voltage Range to Supply Rail
- Input Rail to V-, Rail to Rail Output
- Fast Response:12MHz Bandwidth, 19V/μs Slew Rate,60ns Overload Recovery
- Low Offset Voltage:±150μV Maximum at 25°C
- Very Low THD+N: 0.0005%
- 4KV HBM, 1KV CDM, ±200mA Latch Up
- -40°C to 125°C Operation Temperature Range

Applications

- Sensor Interface
- Motor Control
- Industrial Control
- Audio

General Description

The AWS7227X is newest high supply voltage amplifier with low offset, stable high frequency response. It incorporates AWINIC's proprietary and patented design techniques to achieve very good AC performance with 12MHz bandwidth,19V/μs slew rate and low distortion.

The input common-mode voltage range extends to V-, and the outputs swing rail-to-rail. The AWS7227X can be used as plug-in replacements for many commercially available op-amps to reduce offset and improve input/output range and performance.

The combination of features makes the AWS7227X ideal choices for industrial control, motor control and portable audio amplification, sound ports, and other consumer audio.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AWS72272	SOIC - 8L	3.9mm ×4.9mm
AWS72274	SOIC - 14L	3.9mm ×8.65mm

Typical Application Circuit

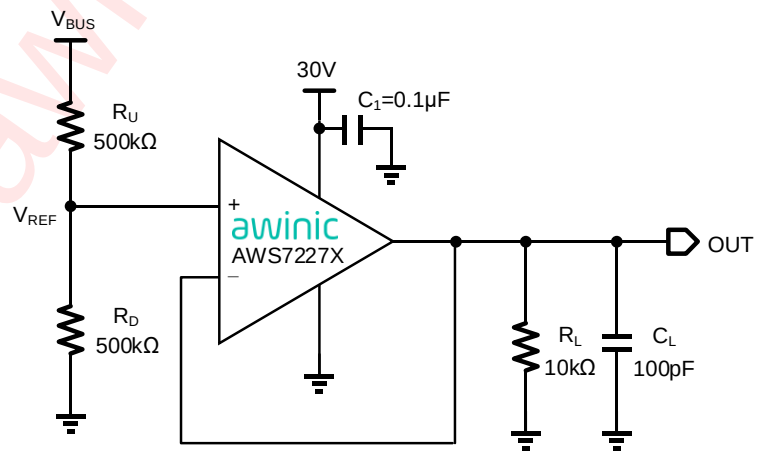
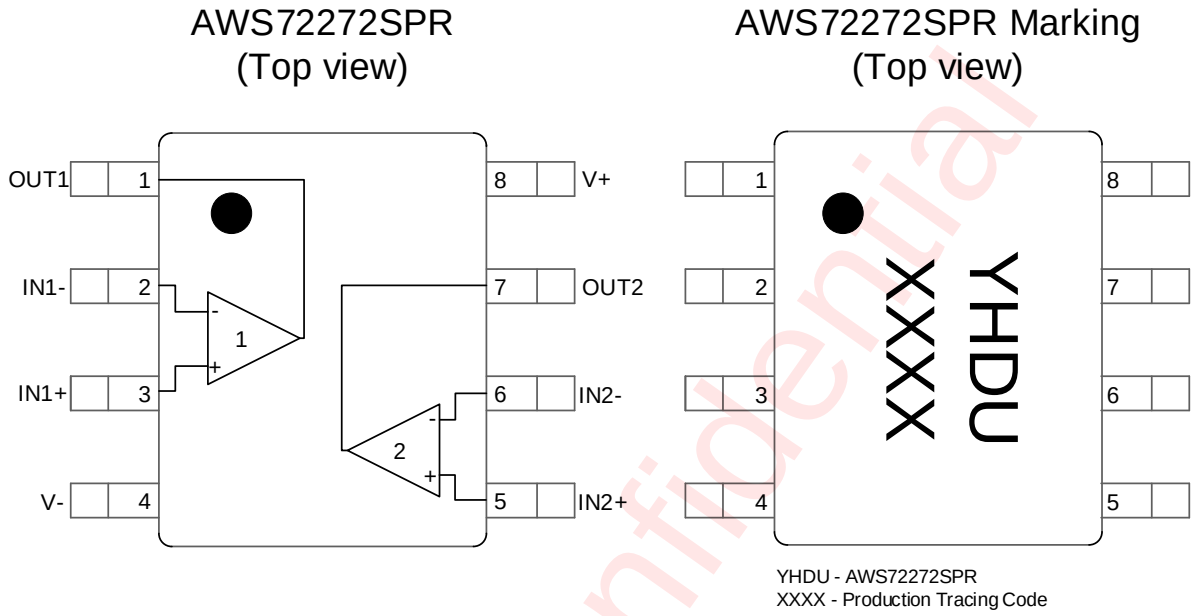


Figure 1 Typical Application of AWS7227X

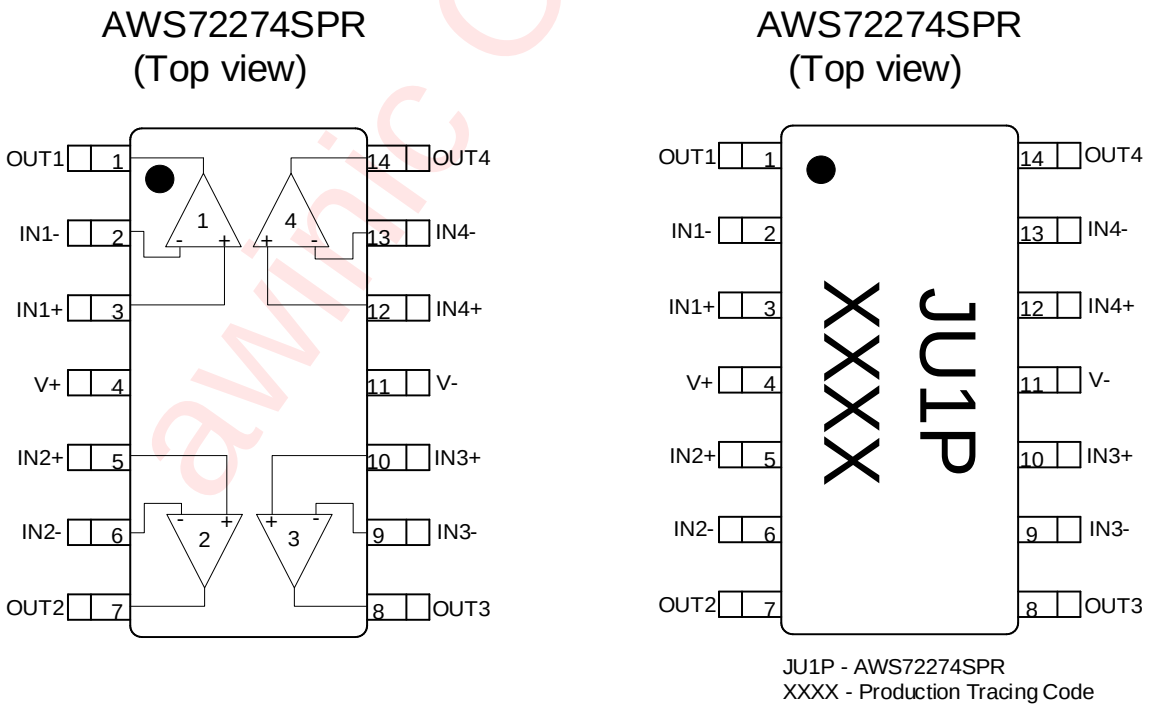
Pin Configuration And Top Mark

SOIC - 8L



YHDU - AWS72272SPR
XXXX - Production Tracing Code

SOIC - 14L



JU1P - AWS72274SPR
XXXX - Production Tracing Code

Figure 2 Pin Configuration

Pin Definition

SOIC - 8L

No.	NAME	DESCRIPTION
1	OUT1	Channel 1 output
2	IN1-	Channel 1 inverting input
3	IN1+	Channel 1 noninverting input
4	V-	Negative (low) supply or ground (for single-supply operation)
5	IN2+	Channel 2 noninverting input
6	IN2-	Channel 2 inverting input
7	OUT2	Channel 2 output
8	V+	Positive (high) supply

SOIC - 14L

No.	NAME	DESCRIPTION
1	OUT1	Channel 1 output
2	IN1-	Channel 1 inverting input
3	IN1+	Channel 1 noninverting input
4	V+	Positive (high) supply
5	IN2+	Channel 2 noninverting input
6	IN2-	Channel 2 inverting input
7	OUT2	Channel 2 output
8	OUT3	Channel 3 output
9	IN3-	Channel 3 inverting input
10	IN3+	Channel 3 noninverting input
11	V-	Negative (low) supply or ground (for single-supply operation)
12	IN4+	Channel 4 noninverting input
13	IN4-	Channel 4 inverting input
14	OUT4	Channel 4 output

Functional Block Diagram

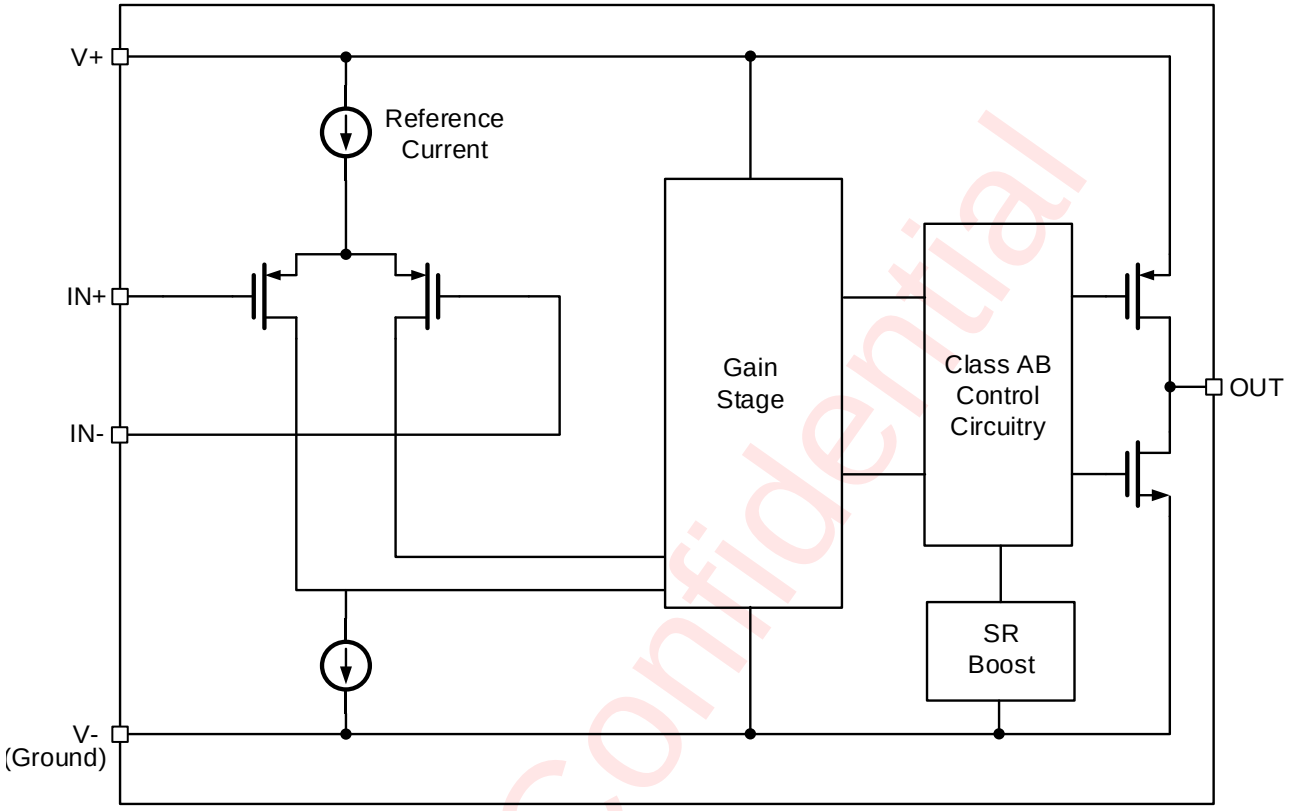


Figure 3 Functional Block Diagram

Typical Application Circuits

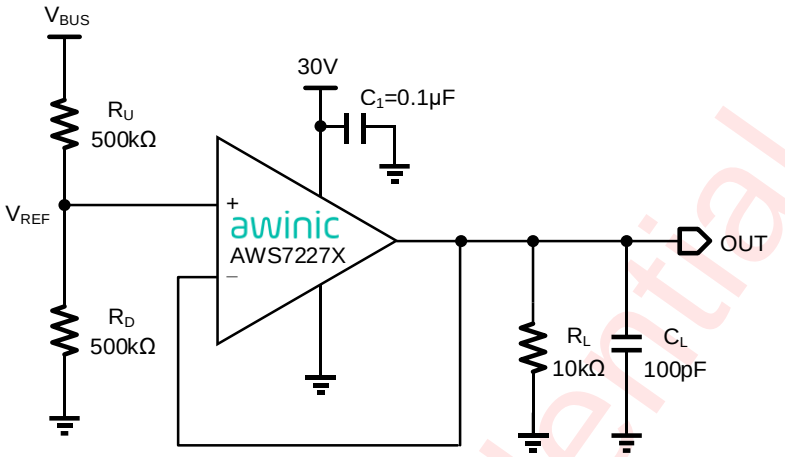


Figure 4 AWS7227X Application Circuit

- ***Notice for typical application circuits:***

1. Bypass capacitors C_1 is used to reduce the coupled noise by providing a low-impedance path to ground. So low-ESR, 0.1μF ceramic bypass capacitors are necessary between each supply pin and ground, placed close to the device, but far away from input traces.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWS72272SPR	-40°C ~ 125°C	SOIC - 8L	YHDU	MSL3	RoHS+HF	3000units/ Tape and Reel
AWS72274SPR	-40°C ~ 125°C	SOIC - 14L	JU1P	MSL3	RoHS+HF	2500units/ Tape and Reel

Absolute Maximum Ratings (NOTE1)

PARAMETERS		RANGE
Supply voltage, V_S = (V+) - (V-)		-0.3V to 40V
Signal input pins	Common-mode voltage (NOTE 2)	(V-) - 0.3V to (V+) + 0.3V
	Differential voltage (NOTE 2)	(+V_S)- (-V_S)
	Current (NOTE 2)	-10mA to 10mA
Output short-circuit (NOTE 3)		Continuous
Operating free-air temperature range T_A		-40°C to 125°C
Maximum operating junction temperature T_{JMAX}		150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: *Input pins are diode-clamped to each power supply. Input signals that may extend more than 0.5V beyond the supply rails must be current limited to 10mA or less.*

NOTE3: *A heat sink may be required to keep the junction temperature below the absolute maximum.*

ESD Rating and Latch Up

PARAMETERS	VALUE	UNIT
HBM (Human Body Model) (NOTE 4)	±4	kV
CDM (NOTE 5)	±1	kV
Latch-Up (NOTE 6)	+IT: 200 -IT: -200	mA

NOTE4: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2023*

NOTE5: Test method: ESDA/JEDEC JS-002-2022

NOTE6: Test method: JESD78F

Thermal Information

THERMAL METRICS		AWS7227X		UNIT
		SOIC		
SYMBOL	PARAMETER	8PIN	14PIN	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	89.49	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	47.03	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	TBD	45.76	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	TBD	14.15	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	TBD	42.34	°C/W

Electrical Characteristics

All test condition is V_S =30V, T_A = 25°C, R_L = 10kΩ connected to V_S/2, Unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	T_A	MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_S	Specified voltage range			4.5 (±2.25)		36 (±18)	V
I_Q	Quiescent current per channel	V_S = 30V, I_O = 0A			1560	2150	μA
			-40~125°C			2300	μA
		V_S = 5V, I_O = 0A			1420	2000	μA
			-40~125°C			2150	μA
PSRR	Power-supply rejection ratio	V_S =4.5V to 36V		90	130		dB
			-40~125°C	80			dB
INPUT CHARACTERISTICS							
V_{OS}	Input offset voltage	V_S = 30V, V_{CM}=0V to 28V		-150		150	μV
		V_S = 30V, V_{CM}=28.5V		-150		150	μV
		V_S = 5V, V_{CM}=2.5V		-150		150	μV
V_{OS} TC	Input offset voltage Drift		-40~125°C		2		μV/°C
I_B	Input bias current				15		pA
			-40~125°C		1000		pA
I_{OS}	Input offset current				15		pA
C_{IN}	Input Capacitance	Differential Mode			5		pF
		Common Mode			2.5		pF
Av	Open-loop Voltage Gain			105	120		dB
			-40~125°C	100			dB
V_{CMR}	Common-mode Input Voltage Range			(V-)		(V+) –1.5	V
CMRR	Common Mode Rejection Ratio	V_{CM} = 0V to 28V		90	130		dB
			-40~125°C	80			dB
OUTPUT CHARACTERISTICS							
V_{OH}		R_L = 10kΩ to V_S/2			100	200	mV

SYMBOL	PARAMETER	TEST CONDITION	T_A	MIN	TYP	MAX	UNIT
	Output Swing from Positive Rail		-40~125°C			300	mV
		R_L = 2kΩ to V_S/2			450	650	mV
			-40~125°C			750	mV
V_{OL}	Output Swing from Negative Rail	R_L = 10kΩ to V_S/2			140	200	mV
			-40~125°C			250	mV
		R_L = 2kΩ to V_S/2			450	650	mV
			-40~125°C			750	mV
I_{SC}	Output Short-Circuit Current			25	35		mA
AC SPECIFICATIONS							
GBW	Gain-bandwidth product				12		MHz
SR	Slew rate	G=1,10V step			19		V/μs
t_{OR}	Overload recovery time	V_{IN} × gain > V_S			60		ns
t_S	Settling Time, 0.1%	G = -1, 10V step			0.8		μs
	Settling time, 0.01%				2		μs
PM	Phase margin	V_S = 36V, R_L=10K, C_L=100pF			65		°
NOISE PERFORMANCE							
E_N	Input Voltage Noise	f = 0.1Hz to 10Hz			1.5		μV_{RMS}
e_N	Input Voltage Noise Density	f = 1kHz			40		nV/ √Hz
THD+N	Total harmonic distortion + noise	f = 1kHz, G =1, R_L = 10kΩ, V_{OUT}= 6VRMS			0.0005		%

Typical Characteristics

VS = ±15V, VCM = 0V, RL = 10kΩ, unless otherwise specified.

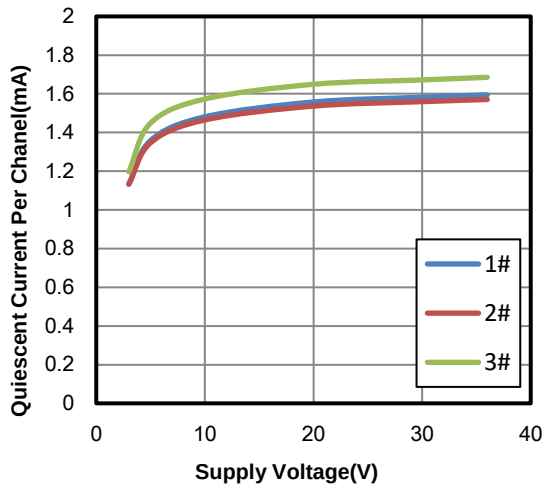


Figure 5 Quiescent Current vs. Supply Voltage

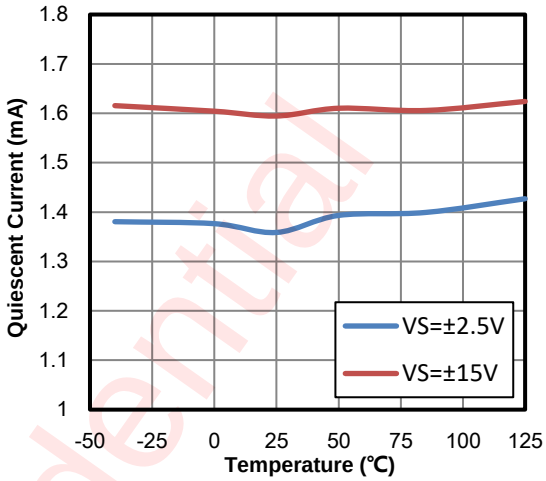


Figure 6 Quiescent Current vs. Temperature

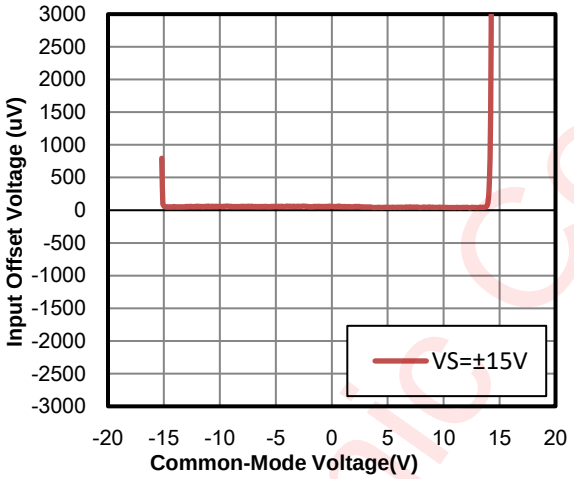


Figure 7 Input Offset Voltage vs. V_{CM}

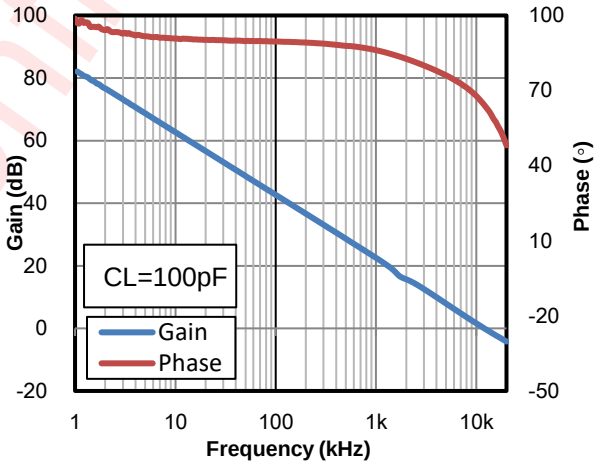


Figure 8 A_{OL} and Phase vs. Frequency

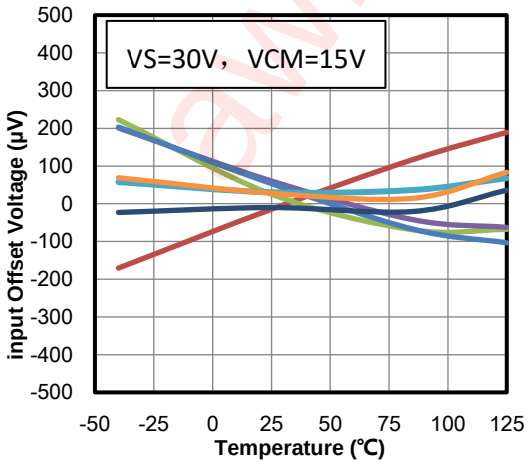


Figure 9 Offset Voltage vs. Temperature

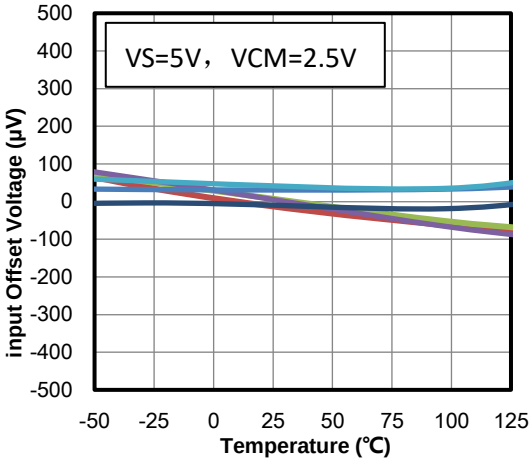


Figure 10 Offset Voltage vs. Temperature

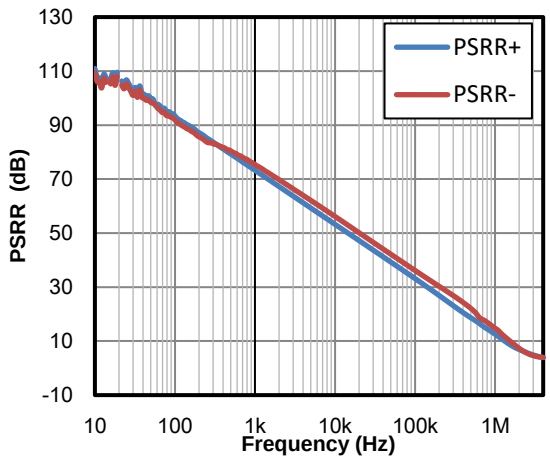


Figure 11 PSRR vs. Frequency

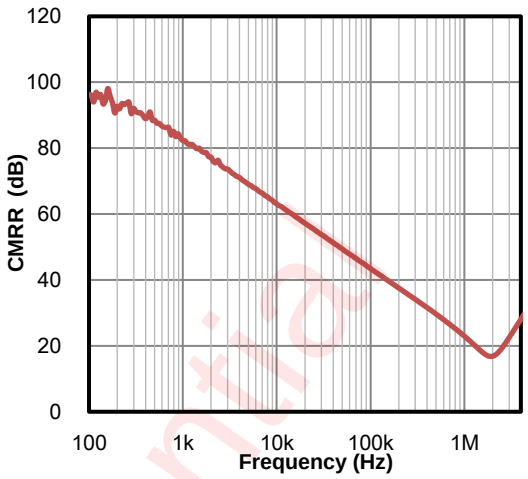


Figure 12 CMRR vs. Frequency

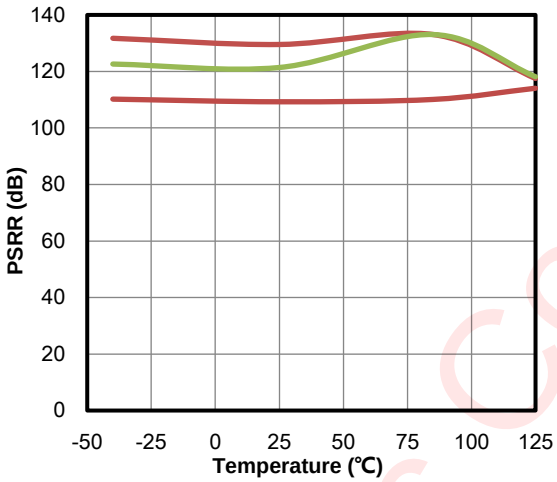


Figure 13 PSRR vs. Temperature

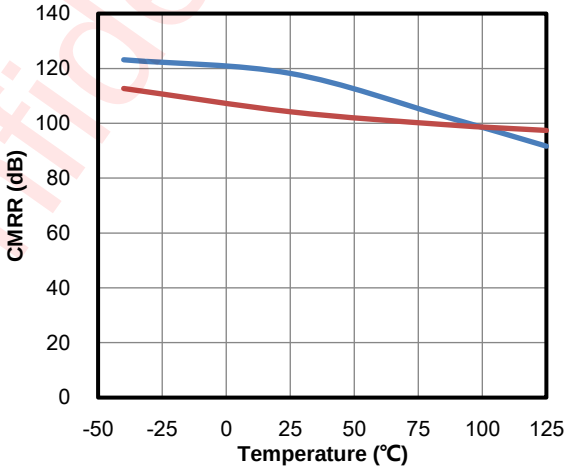


Figure 14 CMRR vs. Temperature

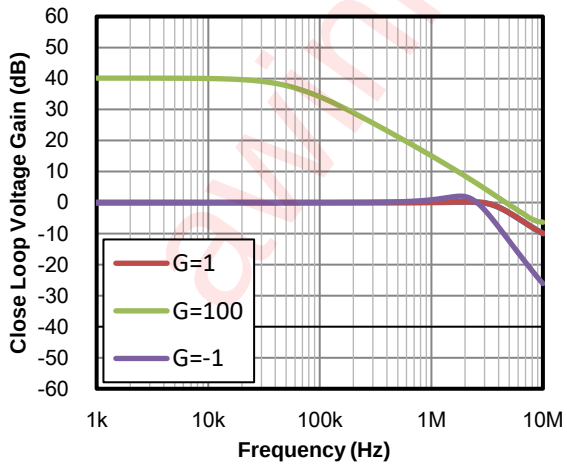


Figure 15 Close Loop Gain vs. Frequency

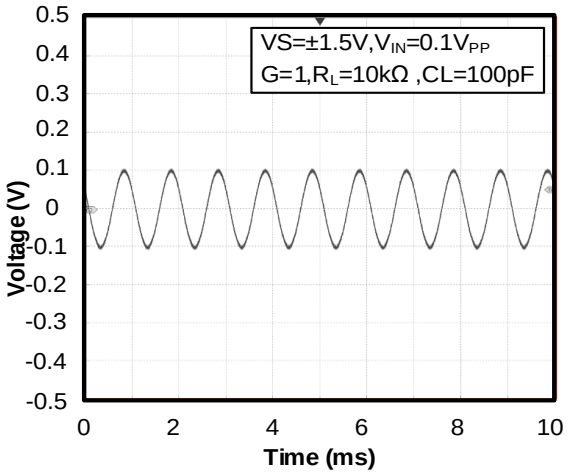


Figure 16 Waveform under 3V Supply Voltage

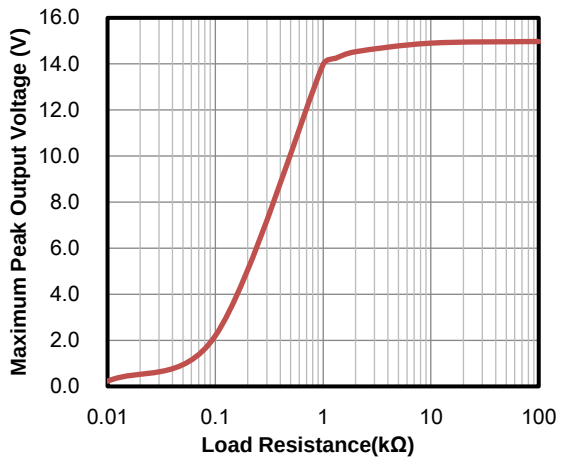


Figure 17 Maximum Output Voltage vs. Load Resistance

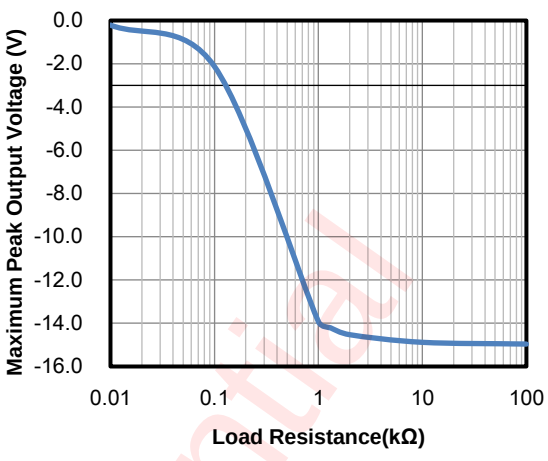


Figure 18 Maximum Peak Output Voltage vs. Load Resistance

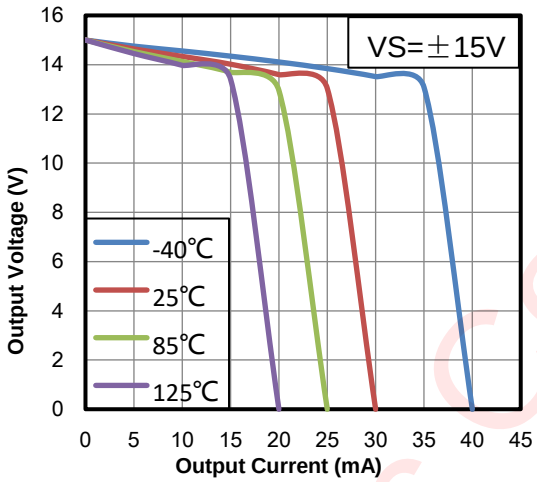


Figure 19 Output Voltage vs. Output Current

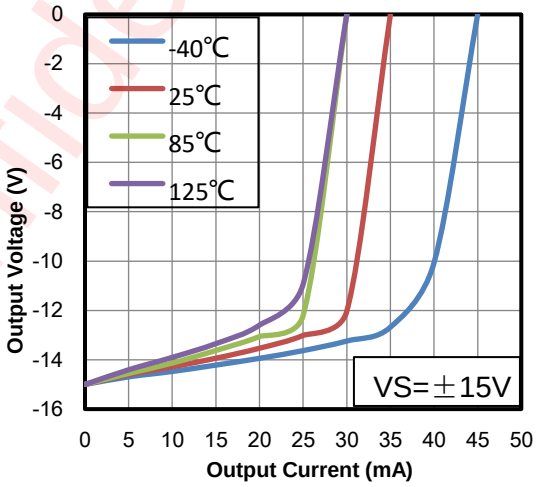


Figure 20 Output Voltage vs. Output Current

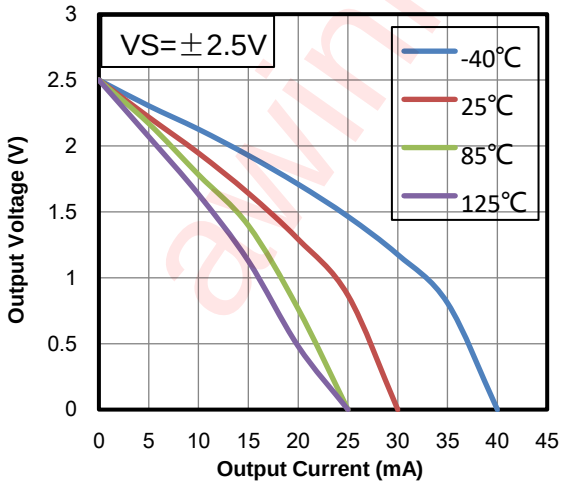


Figure 21 Output Voltage vs. Output Current

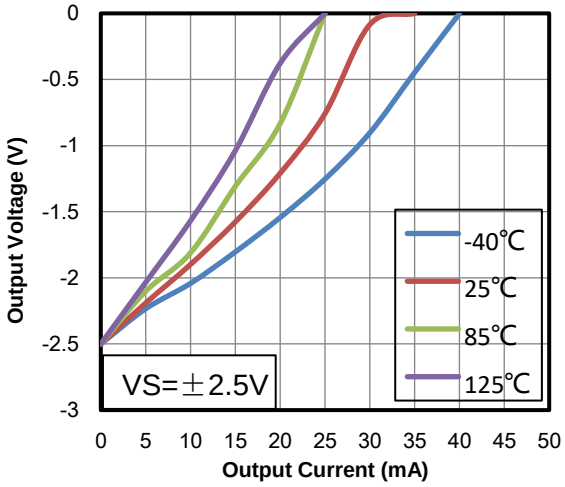


Figure 22 Output Voltage vs. Output Current

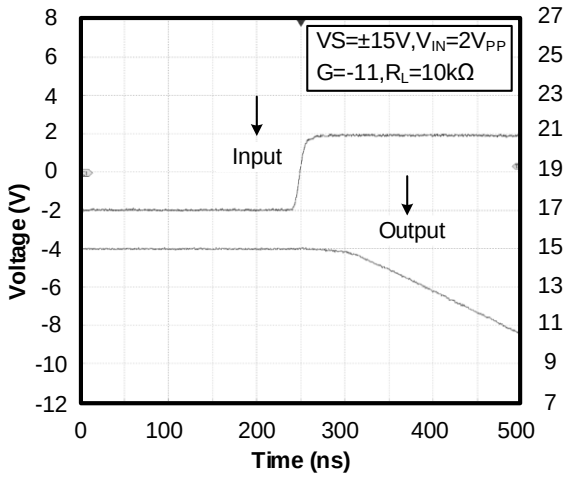


Figure 23 Positive Overload Recovery

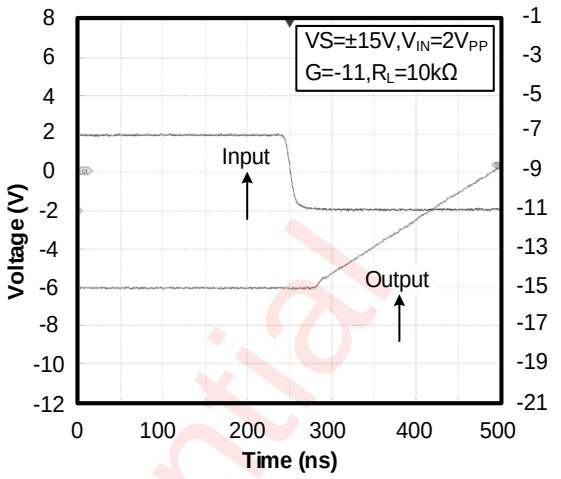


Figure 24 Negative Overload Recovery

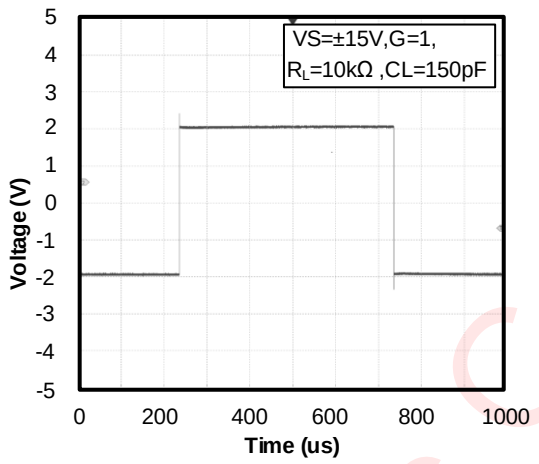


Figure 25 4V Signal Step Response

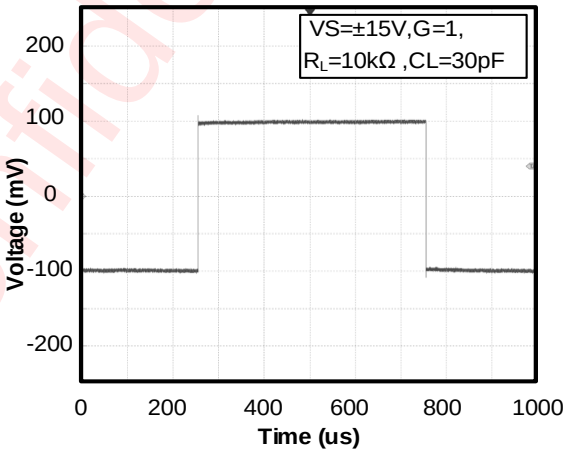


Figure 26 200mV Signal Step Response

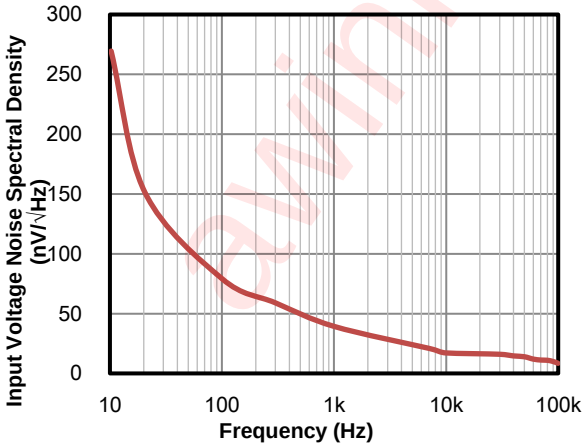


Figure 27 Voltage Noise Spectral Density vs. Frequency

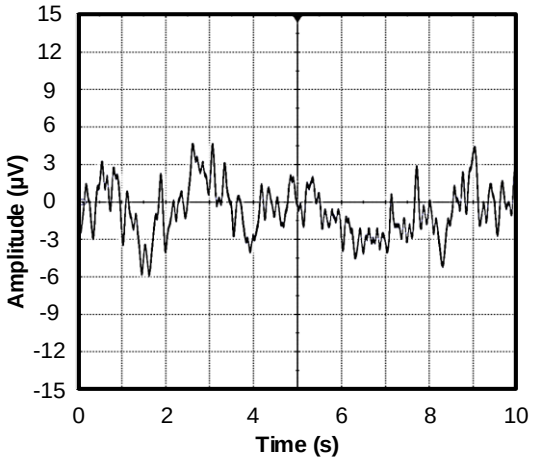


Figure 28 0.1-Hz to 10-Hz Integrated Voltage Noise

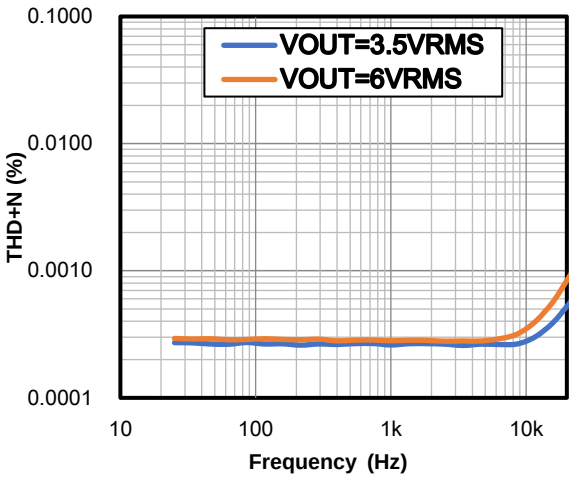


Figure 29 THD + N vs. Frequency

PCB Layout Consideration

For the optimal performance of the device, good PCB layout practices are needed, here are some guidelines:

1. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground. So low-ESR, 0.1μF ceramic bypass capacitors are necessary between each supply pin and ground, placed close to the device, but far away from input traces.
2. R_I is a balance resistor equals to R_G || R_F to reduce the influence of the input bias current on R_G and R_F, which can be shorted when unnecessary.
3. Separate grounding for analog and digital portions of circuitry for better noise suppression. Devote one or more layers on multilayer PCBs to ground planes, which help distribute heat and reduces EMI noise.
4. Run the input traces far away from the Vs supply or output traces to reduce the parasitic coupling. If not, cross these sensitive traces at a 90 degree instead of being parallel with the noisy trace.
5. The input traces are the most sensitive part of the circuit, so keep the length of input traces as short as possible. Place the external resistors and capacitors as close to device as possible, especially the R_F and R_G should be close to the inverting input to minimize the parasitic capacitance.
6. In differential applications, the trace of the inverting input and the non-inverting input should be symmetrical including the same layer, same length, same width and same line spacing.
7. Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process.

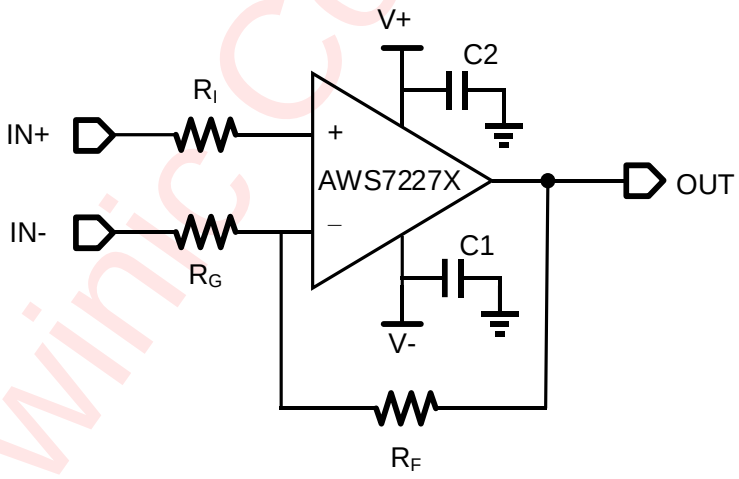
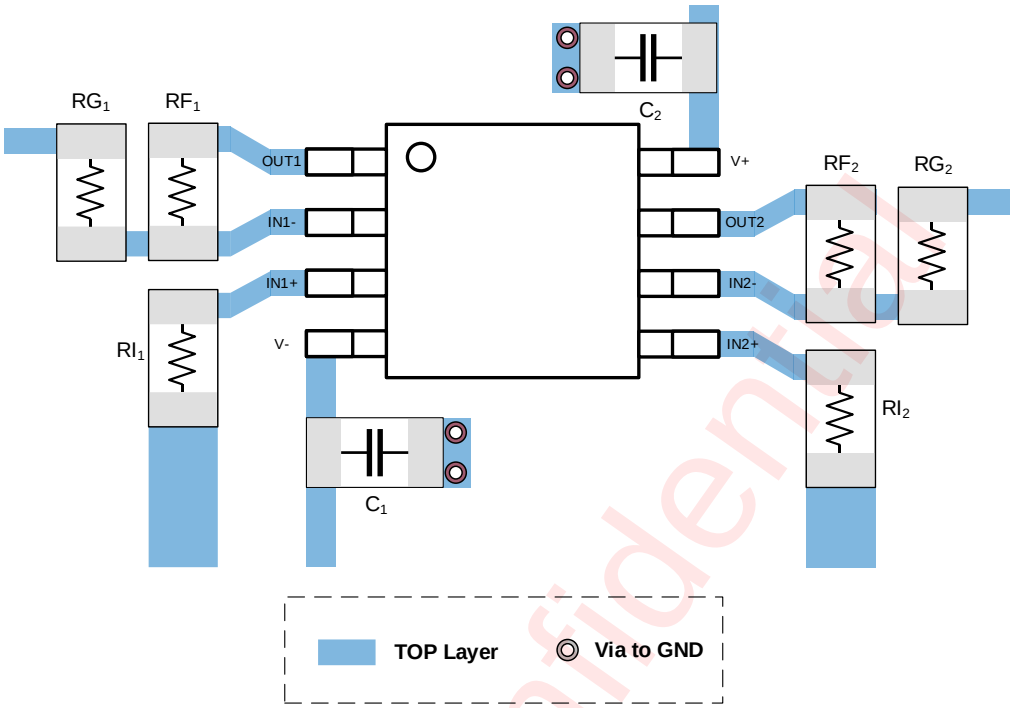


Figure 37 AWS7227X Schematic Example

SOIC - 8L



SOIC - 14L

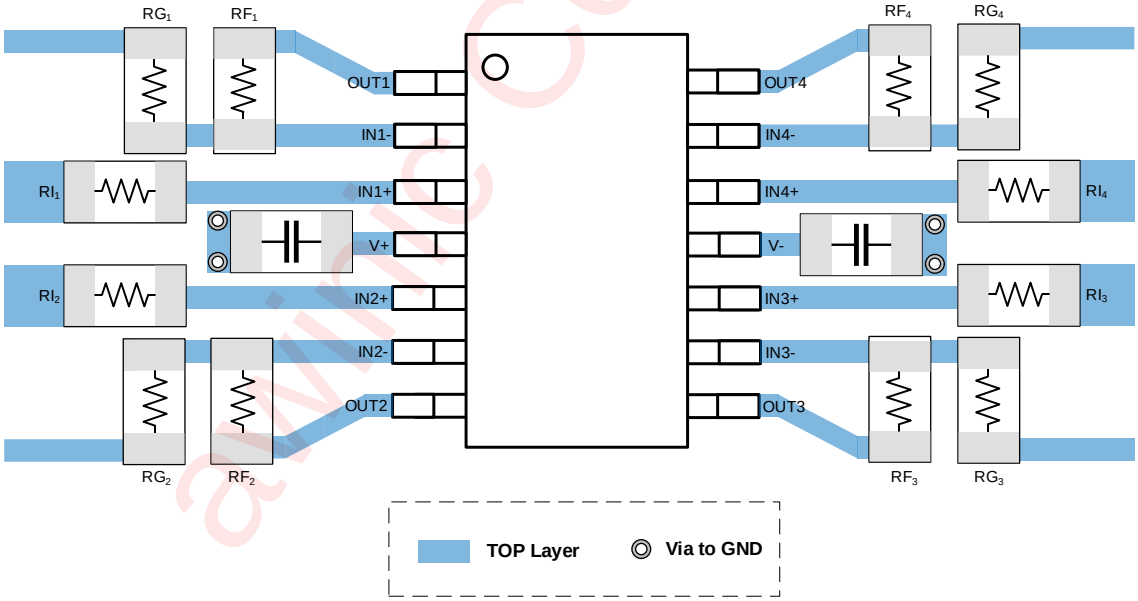


Figure 31 AWS7227X Layout Example

PCB Surface Leakage Current

In high precision applications where input bias current is critically concerned, the leakage current on PCB surface caused by dust or humidity may badly reduce the output accuracy. In this case, a multi-layer PCB is recommended for routing the input traces under the PCB surface. In addition, the usage of a guard ring can significantly reduce the leakage current to sensitive node. A conductive ring surrounding the inputs should be connected to a low impendence node with the same voltage as the inputs, so this ring will absorb the leakage current from high voltage nodes around the inputs.

For non-inverting gain application，connect the IN+ to the input with traces not touching the PCB surface, for example, routing in second layer in Figure 32. Then surround the IN+ pin with a guard ring which is connected to IN-, thus biasing the guard ring with the same voltage of the common mode input voltage.

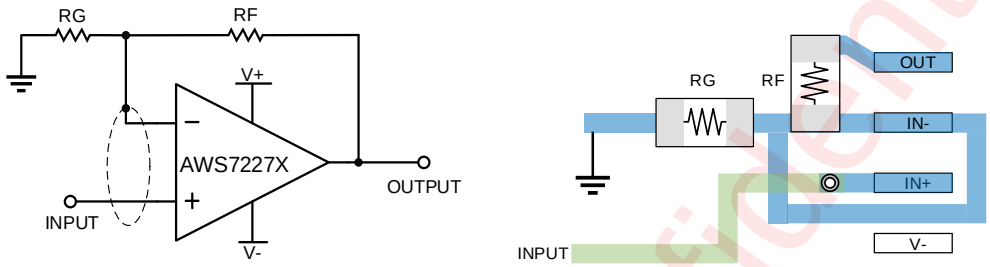


Figure 32 Non-inverting Gain Application Schematic and Layout Example

Similarly, for inverting gain application, connect the IN- to the input with traces not touching the PCB surface, for example, striding over with the input resistor in Figure 33. Then surround the IN- pin with a guard ring which is connected to IN+, thus biasing the guard ring with the reference voltage of AWS7227X.

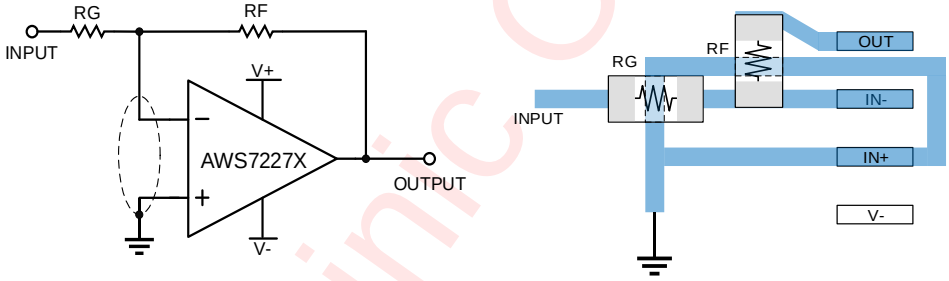
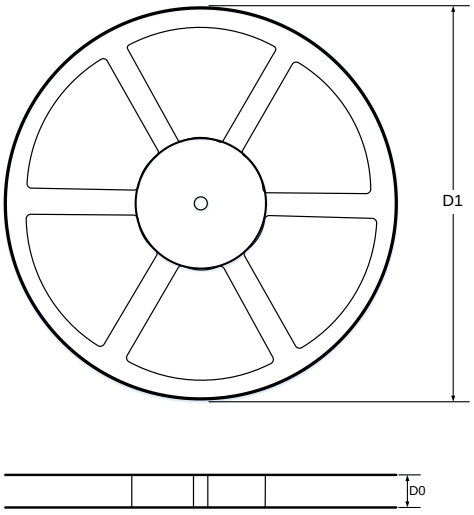


Figure 33 Inverting Gain Application Schematic and Layout Example

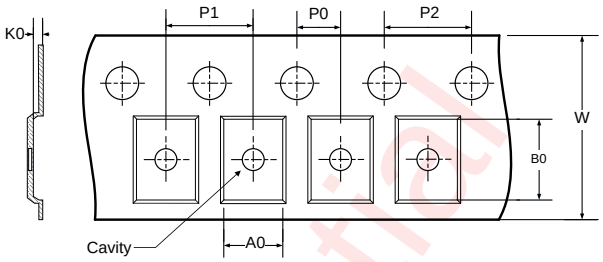
Tape And Reel Information

SOIC - 8L

REEL DIMENSIONS

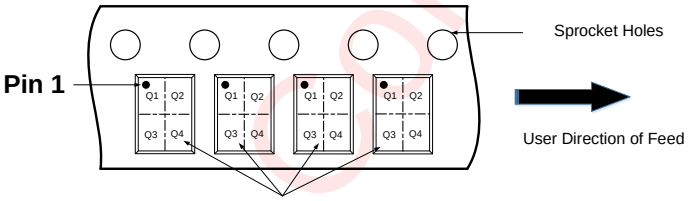


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

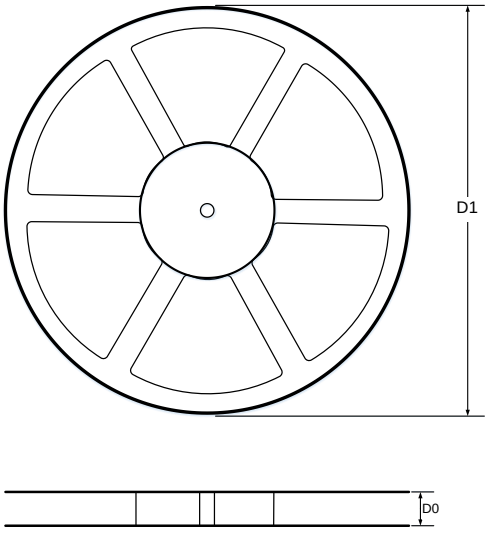
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	6.6	5.3	1.9	2	8	4	12	Q1

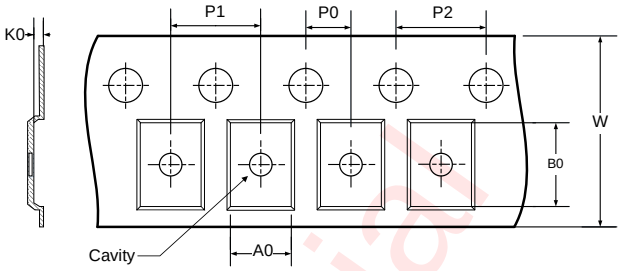
All dimensions are nominal

SOIC - 14L

REEL DIMENSIONS

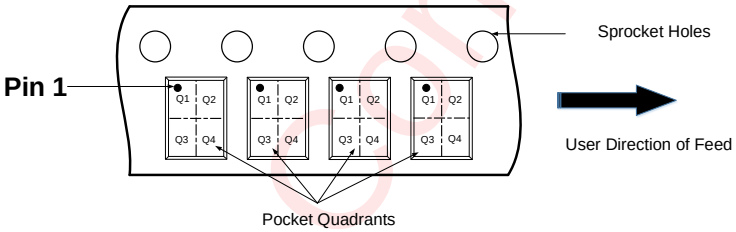


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

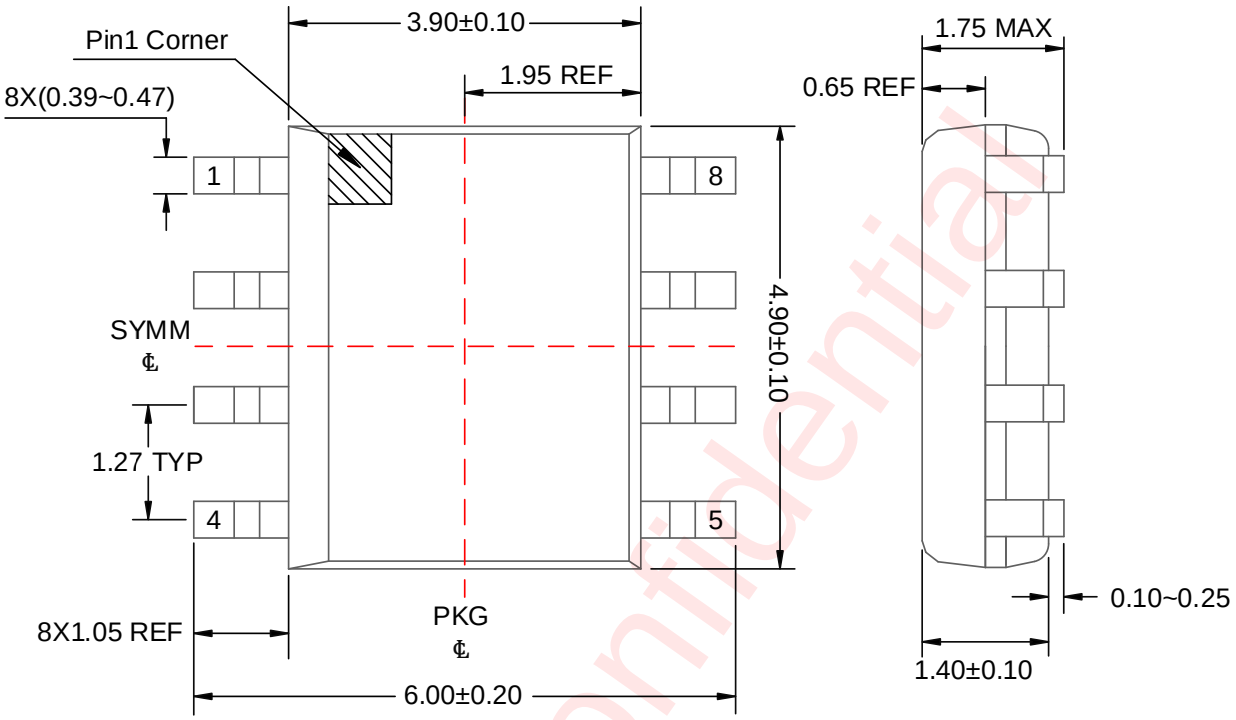
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	16.4	6.5	9.3	2	2	8	4	16	Q1

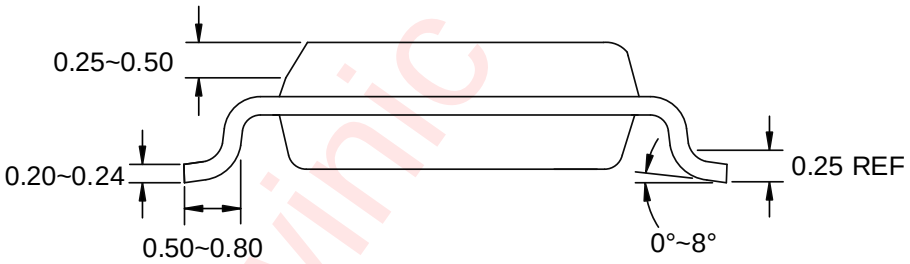
All dimensions are nominal

Package Description

SOIC - 8L



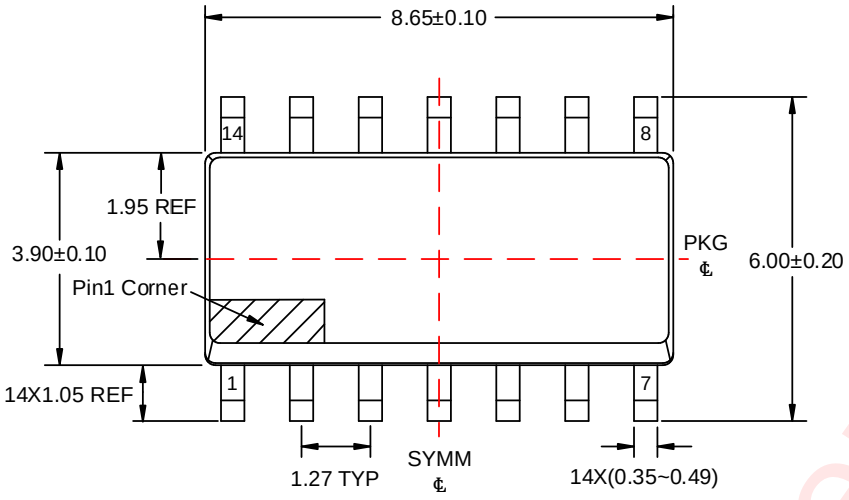
Top View **Side View**



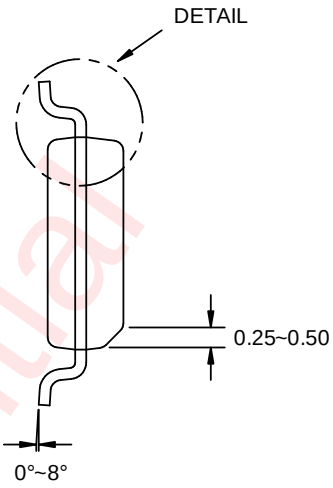
Side View

Unit: mm

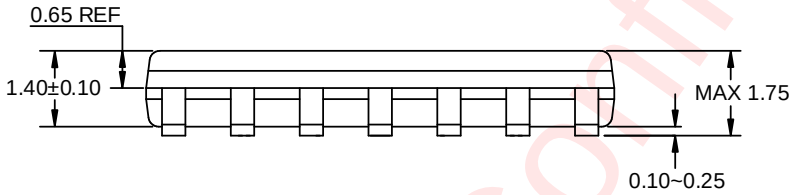
SOIC - 14L



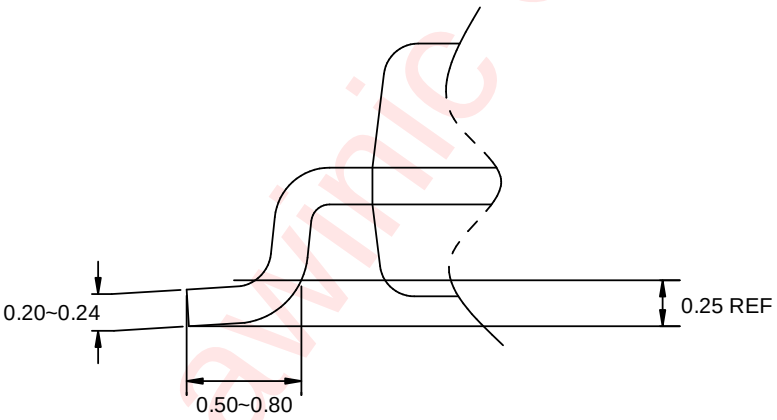
TOP VIEW



SIDE VIEW



SIDE VIEW

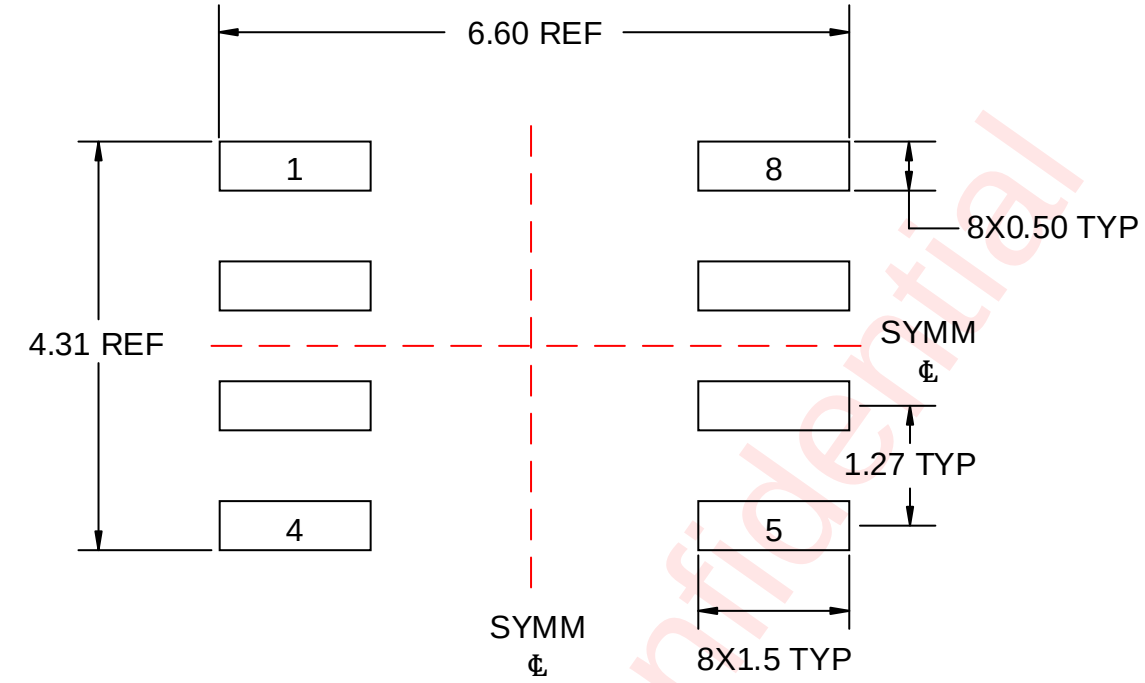


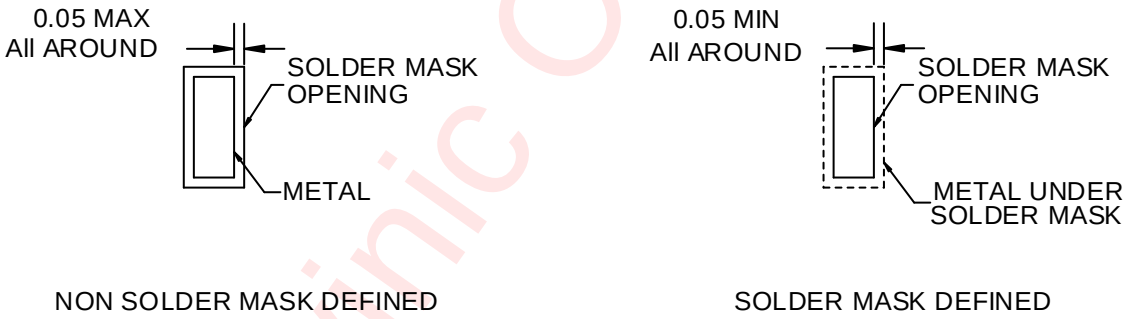
DETAIL

Unit: mm

Land Pattern Data

SOIC - 8L



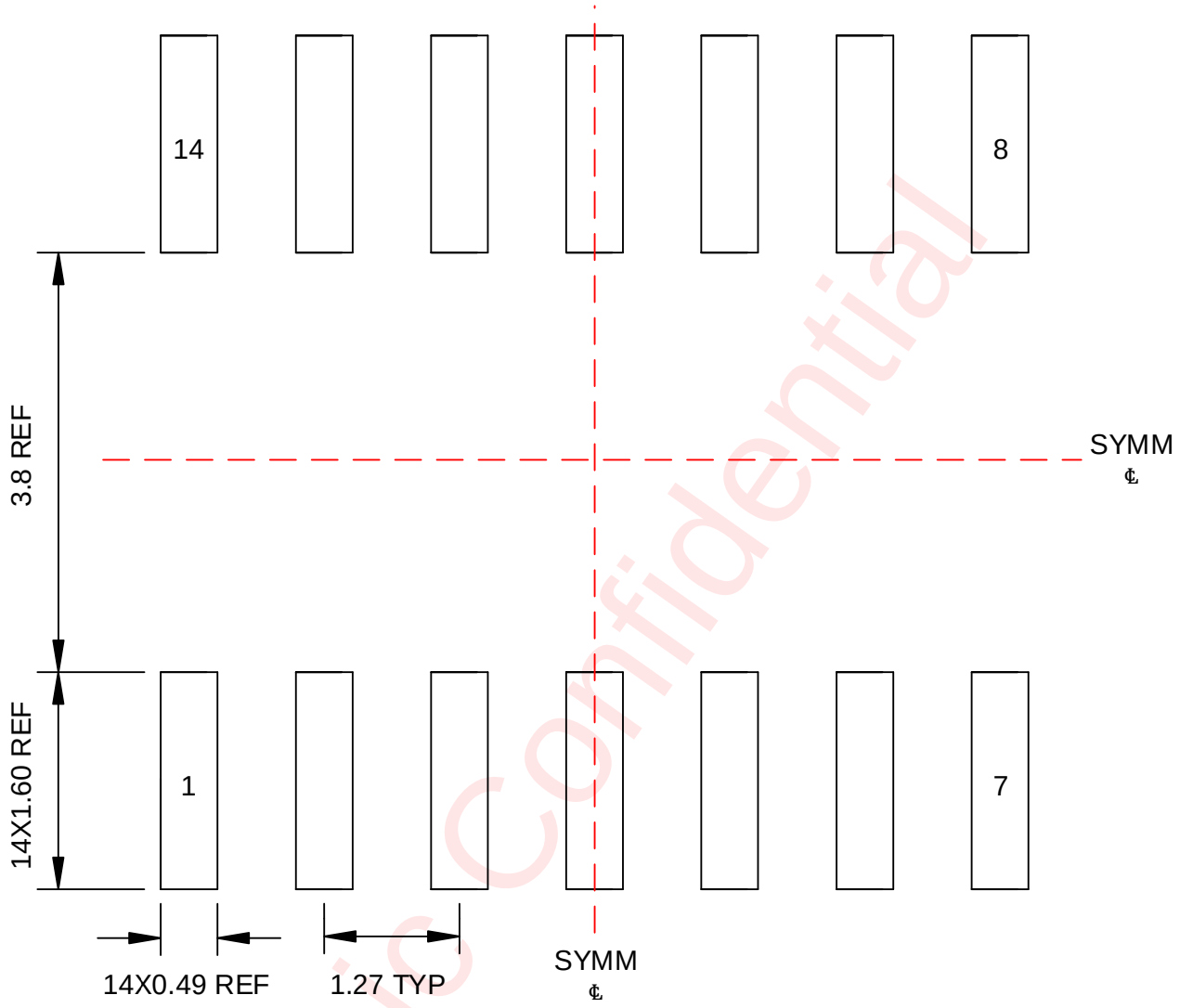


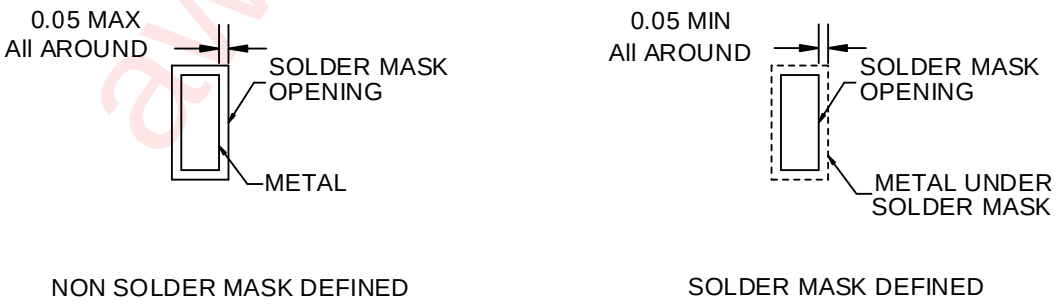
NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit：mm

SOIC - 14L





NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit：mm

Revision History

Version	Date	Change Record
V1.0	Jun. 2023	Official released
V1.1	Jan.2024	1. Update SR in *title*.(P1) 2. Added *Device Information.*(P1) 3. Update some parameters in *Features*.(P1) 4. Update some parameters in *General Description*.(P1) 5. Update channels connections in *Pin Configuration And Top Mark*.(P2) 6. Update ESD and Latch-up in *ESD Rating and Latch Up*.(P6) 7. Update some parameters in *Electrical Characteristics*.(P8/P9) 8. Update Figure 8 in *Typical Characteristics*.(P10) 9. Update Figure 12 in *Typical Characteristics*.(P11) 10. Update Figure 19/20/21/22 in *Typical Characteristics*.(P12)
V1.2	Mar.2024	1. Update all AWS72274 to AWS7227X in *Datasheet* 2. Added AWS72272 in *Device Information.*(P1) 3. Added AWS72272 in *Pin Configuration And Top Mark*.(P2) 4. Added AWS72272 in *Pin Definition*.(P3) 5. Added AWS72272 in *Ordering Information*.(P5) 6. Added AWS72272 in *Thermal Information*.(P7) 7. Added AWS72272 in *PCB Layout Consideration*.(P16) 8. Added SOIC - 8L in *Tape And Reel Information*.(P18) 9. Added SOIC - 8L in *Package Description*.(P20) 10. Added SOIC - 8L in *Land Pattern Data*.(P23)

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