

0.1-9.3GHz SPDT Switch for 3G/4G/5G RX

Features

- Broadband frequency range: 0.1 to 9.3GHz
- Low insertion loss: 0.41dB@4.2GHz
- High isolation: 32dB@4.2GHz
- Integrated logic
- DFN 1.1X0.7-6L package

Applications

- Cellular 3G/4G/5G RX and WLAN
- Cellular modems , tablets and USB Devices
- UWB Application
- Other RF front-end modules

General Description

The AW13012VDNR is a SPDT switch with low insertion loss and high Isolation. It can be used to support band switching and mode switching for cellular 3G/4G/5G, data cards and tablets. It is also WLAN compatible.

The symmetrical design of internal ports makes it convenient for PCB routing and adjustment of receiving and transmitting signals. The band/mode switching is realized by the GPIO pins as referenced in the chip block diagram and the control logic.

The AW13012VDNR is provided in a compact DFN 1.1X0.7-6L package.

Typical Application Circuit

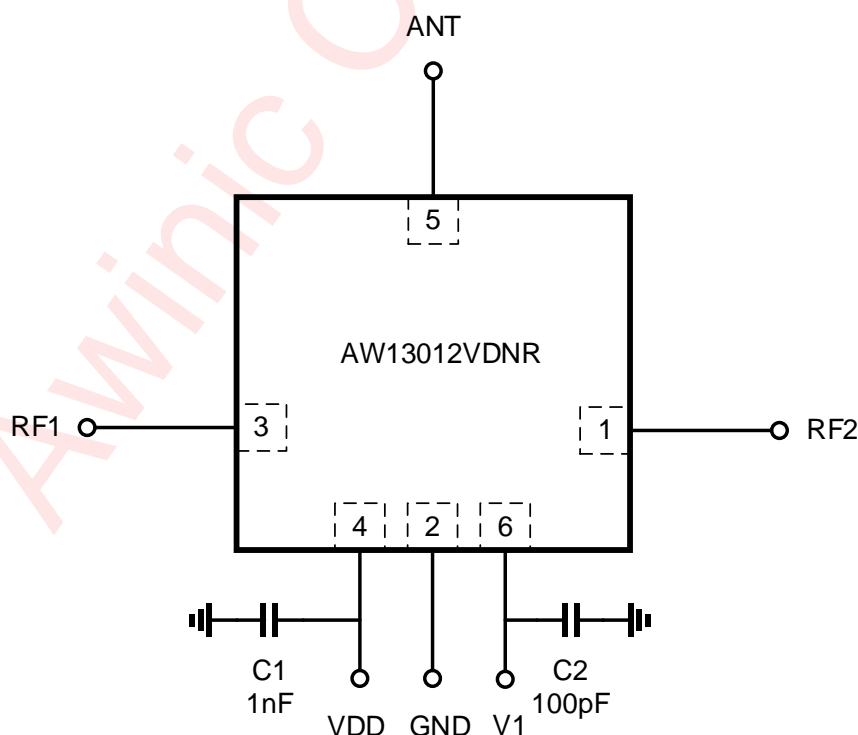
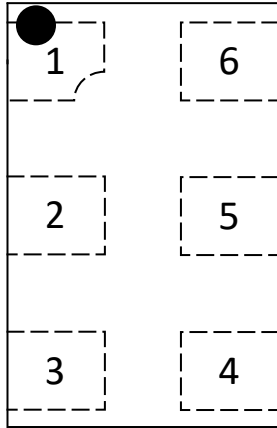


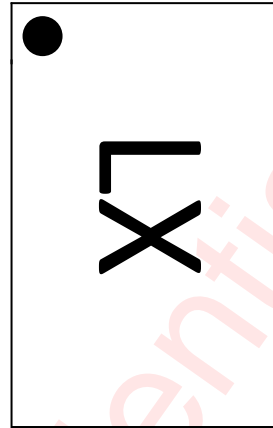
Figure 1 Typical Application Circuit of AW13012VDNR

Pin Configuration And Top Mark

AW13012VDNR
(Top View)



AW13012VDNR Marking
(Top View)



L – AW13012VDNR
X – Production Tracing Code

Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	RF2	RF I/O path 2
2	GND	Ground
3	RF1	RF I/O path 1
4	VDD	DC power supply
5	ANT	Antenna port
6	V1	DC control voltage 1

Functional Block Diagram

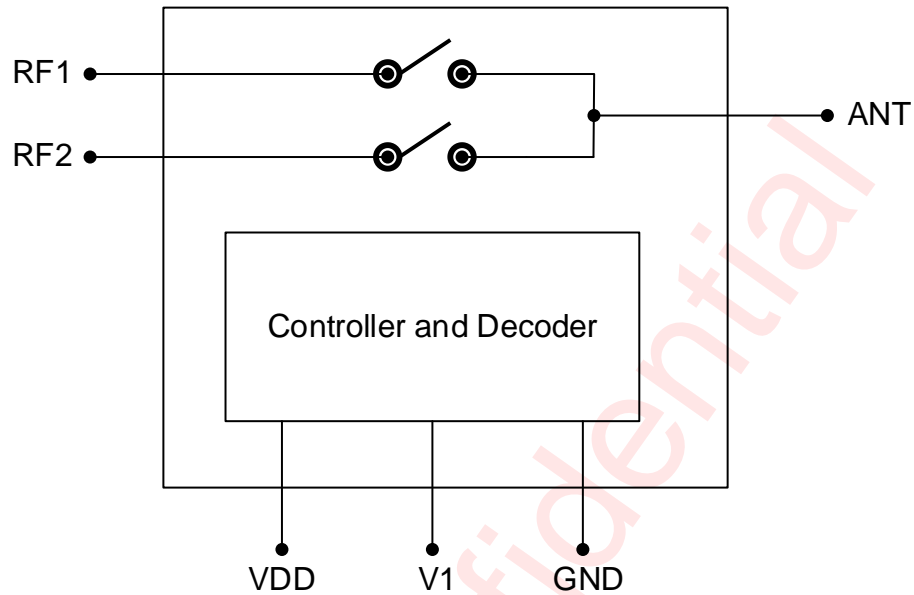


Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW13012VDNR	-40°C~105°C	DFN 1.1X0.7-6L	L	MSL1	ROHS+HF	9000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE	
Supply Voltage Range VDD		-0.3V to 5.0V	
Control Voltage Range	V1	-0.3V to 5.0V	
RF input power(RF1/RF2)		VDD=1.8V	31.5dBm
		VDD=2.8V	32.5dBm
Operating Free-air Temperature Range		-40°C to 105°C	
Storage Temperature T _{STG}		-65°C to 150°C	
Lead Temperature (Soldering 10 Seconds)		260°C	
ESD (NOTE 2)			
HBM		±1000V	
CDM		±500V	

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

HBM Test method: ESDA/JEDEC JS-001-2024. CDM Test method: ESDA/JEDEC JS-002-2025.

Electrical Characteristics

DC Characteristics

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
VDD	Supply Voltage		1.65		3.6	V
IDD	Supply Current	VDD=1.8V		20	40	μA
		VDD= 2.8V		35	70	μA
VCTL_H	Control logic High	VDD=1.8V or 2.8V	0.85		VDD	V
VCTL_L	Control logic Low	VDD=1.8V or 2.8V	0		0.45	V
ICTL	Control Current	VDD=1.8V or 2.8V		1	5	μA

VDD=2.8~3.6V, V1=0/VDD, PIN=0dBm, TEMP=+25°C, Z₀=50Ω. (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
T _{sw}	Switching On/Off Time	50% of final control voltage to 10%/90% of final RF power, switching between RF1/2		120	300	ns
IL	Insertion loss(ANT pin to RF1/RF2)	0.1-0.96GHz		0.28	0.38	dB
		0.96-2.2GHz		0.34	0.45	dB
		2.3-2.7GHz		0.37	0.48	dB
		3.3-4.2GHz		0.41	0.55	dB
		4.4-5GHz		0.43	0.60	dB
		5.15-5.925GHz		0.5	0.70	dB
		5.925-7.125GHz		0.57	0.85	dB
ISO	Isolation (ANT pin to RF1/RF2)	0.1-0.96GHz	42	47		dB
		0.96-2.2GHz	30	35		dB
		2.3-2.7GHz	29	34		dB
		3.3-4.2GHz	27	32		dB
		4.4-5GHz	24	29		dB
		5.15-5.925GHz	20	25		dB
		5.925-7.125GHz	18	23		dB
RL ^[1]	Input return loss (ANT pin to RF1/RF2)	0.1-0.96GHz	26	33		dB
		0.96-2.2GHz	22	28		dB
		2.3-2.7GHz	20	26		dB
		3.3-4.2GHz	16	24		dB
		4.4-5GHz	15	23		dB
		5.15-5.925GHz	13	21		dB
		5.925-7.125GHz	11	17		dB
2f ₀ ^[1]	Second harmonics (ANT pin to RF1/RF2)	PIN=+24dBm, 2400MHz		-63	-53	dBm
		PIN=+24dBm, 2400MHz		-69	-59	dBm
2f ₀ ^[1]	Second harmonics (ANT pin to RF1/RF2)	PIN=+24dBm, 5800MHz		-63	-53	dBm

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$3f_0^{[1]}$	Third harmonics (ANT pin to RF1/RF2)	PIN=+24dBm, 5800MHz		-65	-55	dBm
$P_{0.1dB}^{[1]}$	0.1dB Compression Point (ANT pin to RF1/RF2)	25% DC		31		dBm

[1] Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

VDD=1.8V, V1=0/1.8V, PIN=0dBm, TEMP=+25°C, Z₀=50Ω. (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT		
T _{sw}	Switching On/Off Time	50% of final control voltage to 10%/90% of final RF power, switching between RF1/2		160	300	ns		
IL	Insertion loss(ANT pin to RF1/RF2)	0.1-0.96GHz		0.37	0.47	dB		
		0.96-2.2GHz		0.44	0.57	dB		
		2.3-2.7GHz		0.47	0.60	dB		
		3.3-4.2GHz		0.51	0.65	dB		
		4.4-5GHz		0.53	0.68	dB		
		5.15-5.925GHz		0.60	0.85	dB		
		5.925-7.125GHz		0.69	1.00	dB		
ISO	Isolation (ANT pin to RF1/RF2)	7.125-9.3GHz		0.98	1.30	dB		
		0.1-0.96GHz	41	46		dB		
		0.96-2.2GHz	30	35		dB		
		2.3-2.7GHz	29	34		dB		
		3.3-4.2GHz	26	31		dB		
		4.4-5GHz	23	28		dB		
		5.15-5.925GHz	19	24		dB		
RL ^[1]	Input return loss (ANT pin to RF1/RF2)	5.925-7.125GHz	17	22		dB		
		7.125-9.3GHz	13	18		dB		
		0.1-0.96GHz	23	30		dB		
		0.96-2.2GHz	21	27		dB		
		2.3-2.7GHz	19	25		dB		
		3.3-4.2GHz	16	24		dB		
		4.4-5GHz	15	23		dB		
$2f_0^{[1]}$	Second harmonics (ANT pin to RF1/RF2)	5.15-5.925GHz	13	20		dB		
		5.925-7.125GHz	11	17		dB		
		7.125-9.3GHz	10	15		dB		
		PIN=+24dBm, 2400MHz		-59	-49	dBm		
		$3f_0^{[1]}$	Third harmonics (ANT pin to RF1/RF2)	PIN=+24dBm, 2400MHz		-61	-51	dBm
		$2f_0^{[1]}$	Second harmonics (ANT pin to RF1/RF2)	PIN=+24dBm, 5800MHz		-61	-51	dBm
		$3f_0^{[1]}$	Third harmonics (ANT pin to RF1/RF2)	PIN=+24dBm, 5800MHz		-56	-46	dBm
$P_{0.1dB}^{[1]}$	0.1dB Compression Point (ANT pin to RF1/RF2)	25% DC		30		dBm		

[1] Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

Timing Diagram (Power ON and OFF sequence)

It is very important that the user adheres to the correct power-on/off sequence in order to avoid damaging the device. The control signal V1 should be set to 0V unless VDD is set in the operating voltage range.

Power ON:

- 1) Apply voltage supply --- VDD
- 2) Set Controls---V1
- 3) Apply RF input

Change switch position from one RF port to another:

- 1) Remove RF input
- 2) Change control voltages V1 to set the switch to desired RF port
- 3) Apply RF input

Power OFF:

- 1) Remove RF input
- 2) Remove control voltages-V1
- 3) Remove VDD input

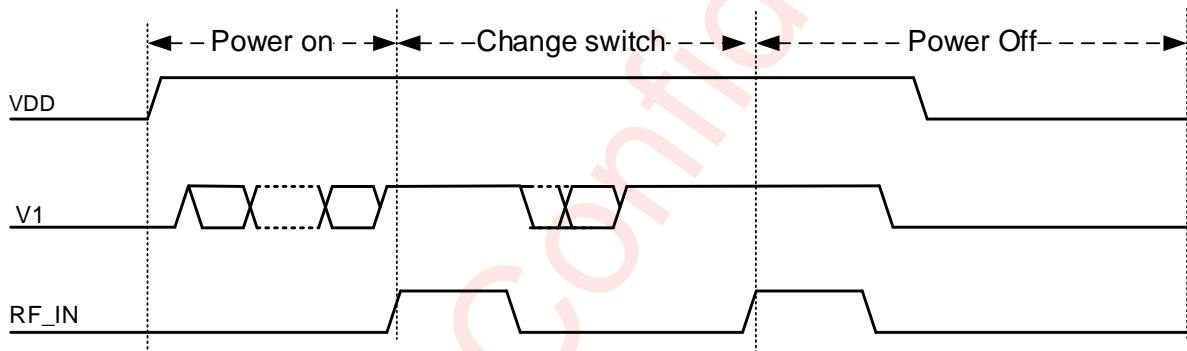
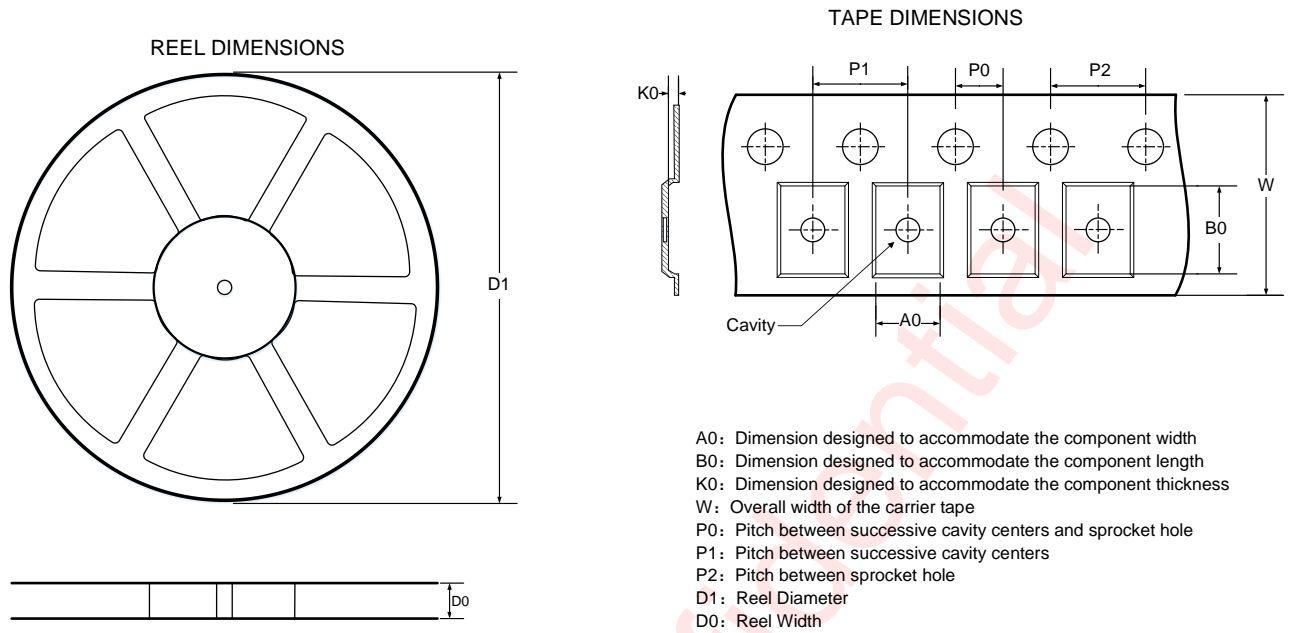


Figure 4 Power on/Change switch/Power off sequence

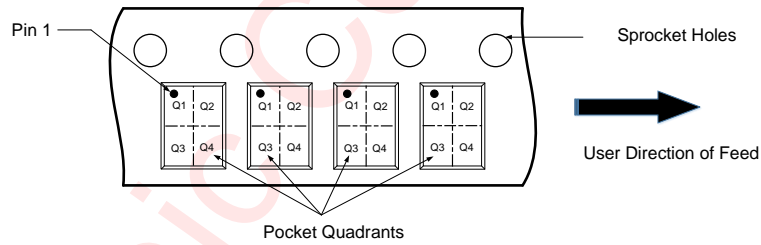
Control Logic

State	Active Path	V1
0	ANT to RF1	0
1	ANT to RF2	1

Tape and Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

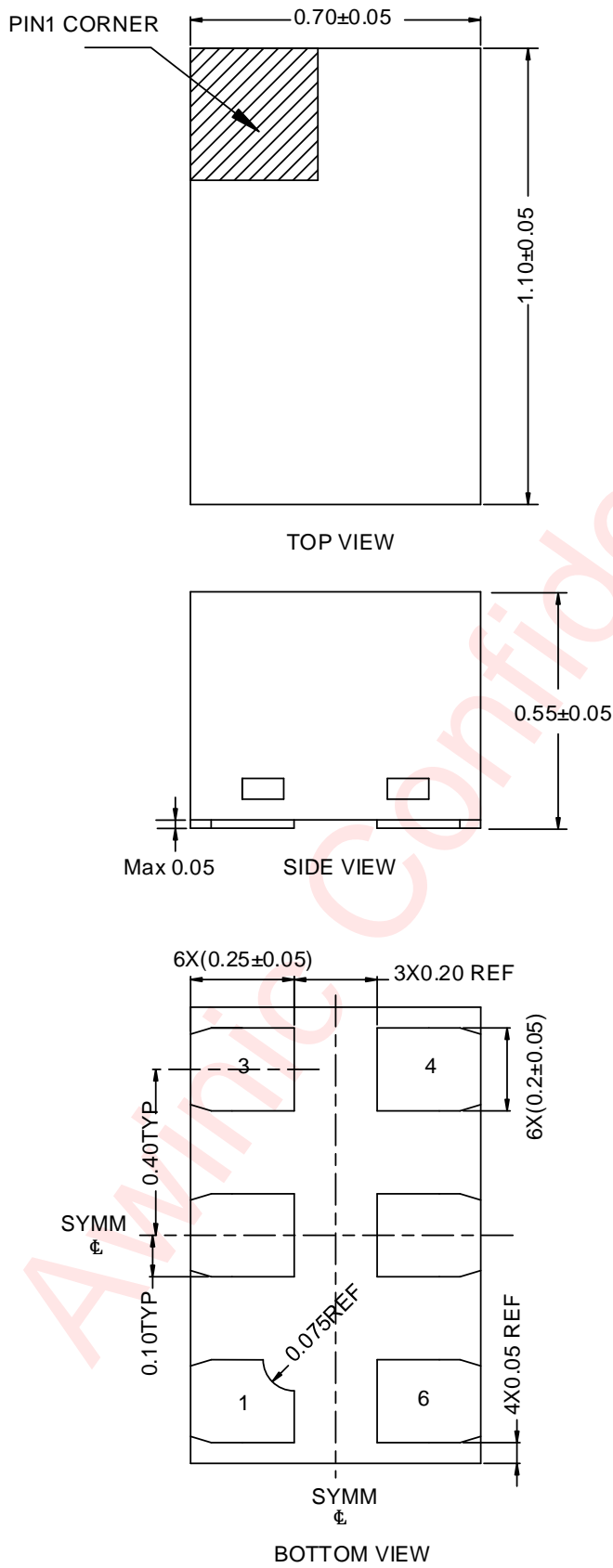


All dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	9.5	0.82	1.22	0.66	2	2	4	8	Q1

Figure 5 Tape and Reel

Package Description



Unit: mm

Figure 6 Package Outline

Land Pattern Data

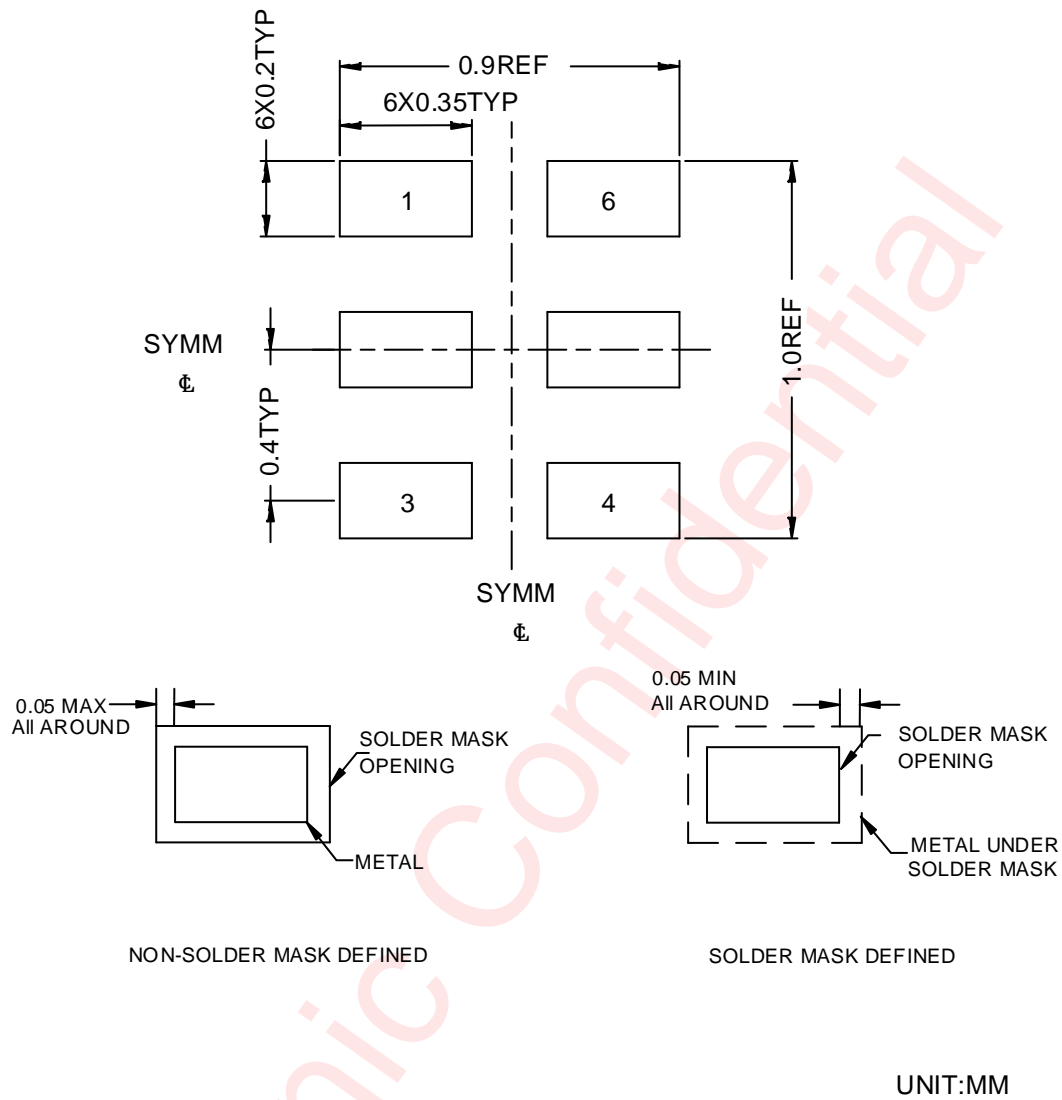


Figure 7 Land Pattern

Revision History

Version	Date	Change Record
V1.0	Oct 2025	Officially Released

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