General Description

The AGM40N20F combines proprietary New Planar Technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

This device is ideal for load switch and battery protection applications.

Features

- Proprietary New Planar Technology
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance
- 100% Avalanche tested
- 100% DVDS tested

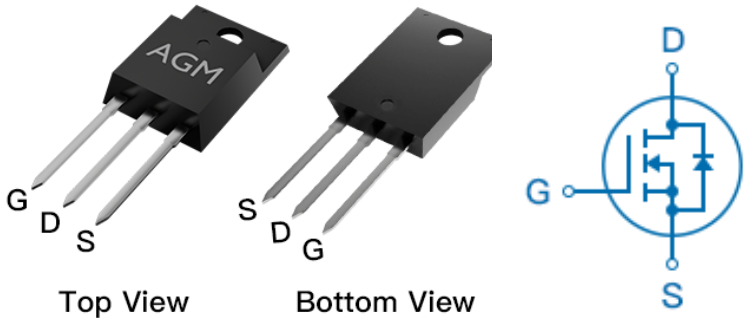
Application

- MB/VGA Vcore
- SMPS 2nd Synchronous Rectifier
- POL application
- BLDC Motor driver

Product Summary

BVDSS	RDSON	ID
200V	47mΩ	40A

TO-220F Pin Configuration



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AGM40N20F	AGM40N20F	TO-220F	----	----	1000

Table 1. Absolute Maximum Ratings (TA=25℃)

Symbol	Parameter	Value	Unit
VDS	Drain-Source Voltage (VGS=0V)	200	V
VGS	Gate-Source Voltage (VDS=0V)	±20	V
ID	Drain Current-Continuous(Tc=25℃) **(Note 1)**	40	A
	Drain Current-Continuous(Tc=100℃)	24	A
IDM (pluse)	Drain Current-Pulsed **(Note 2)**	160	A
PD	Maximum Power Dissipation(Tc=25℃)	100	w
	Maximum Power Dissipation(Tc=100℃)	50	w
EAS	Avalanche energy **(Note 3)**	1105	mJ
TJ,TSTG	Operating Junction and Storage Temperature Range	-55 To 150	℃

Table 2. Thermal Characteristic

Symbol	Parameter	Typ	Max	Unit
RθJA	Thermal Resistance Junction-ambient (Steady State)[1]	---	62	℃/W
RθJC	Thermal Resistance Junction-Case[1]	---	1.0	℃/W

Table 3. Electrical Characteristics (TJ=25℃unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BVDSS	Drain-Source Breakdown Voltage	VGS=0V ID=250μA	200	--	--	V
IDSS	Zero Gate Voltage Drain Current	VDS=200V,VGS=0V	--	--	1	μA
IGSS	Gate-Body Leakage Current	VGS=±20V,VDS=0V	--	--	±100	nA
VGS(th)	Gate Threshold Voltage	VDS=VGS,ID=250μA	2	--	4	V
gFS	Forward Transconductance	VDS=10V,ID=15A	--	65	--	S
RDS(on)	Drain-Source On-State Resistance	VGS=10V, ID=20A	--	47	62	mΩ
Dynamic Characteristics						
Ciss	Input Capacitance	VDS=40V,VGS=0V, F=1MHZ	--	2800	--	pF
Coss	Output Capacitance		--	260	--	pF
Crss	Reverse Transfer Capacitance		--	85	--	pF
Rg	Gate resistance	VGS=0V, VDS=0V,f=1.0MHz	--	0.5	--	Ω
Switching Times						
td(on)	Turn-on Delay Time	VGS=10V,VDS=100V, ID=20A,RGEN=3.9Ω	--	20	--	nS
tr	Turn-on Rise Time		--	30	--	nS
td(off)	Turn-Off Delay Time		--	65	--	nS
tf	Turn-Off Fall Time		--	25	--	nS
Qg	Total Gate Charge	VGS=10V, VDS=100V, ID=20A	--	97	--	nC
Qgs	Gate-Source Charge		--	14	--	nC
Qgd	Gate-Drain Charge		--	39	--	nC
Source-Drain Diode Characteristics						
ISD	Source-Drain Current(Body Diode)		--	--	40	A
VSD	Forward on Voltage	VGS=0V,IS=20A	--	--	1.3	V
trr	Reverse Recovery Time	IF=20A , dI/dt=100A/μs , TJ=25℃	--	280	--	ns
Qrr	Reverse Recovery Charge		--	420	--	nc

Notes 1.The maximum current rating is package limited.

Notes 2.Repetitive Rating: Pulse width limited by maximum junction temperature

Notes 3.EAS condition: TJ=25℃,VDD=50V,Vgs=10V,ID=47A, L=1mH,RG=25ohm

Typical Characteristics

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

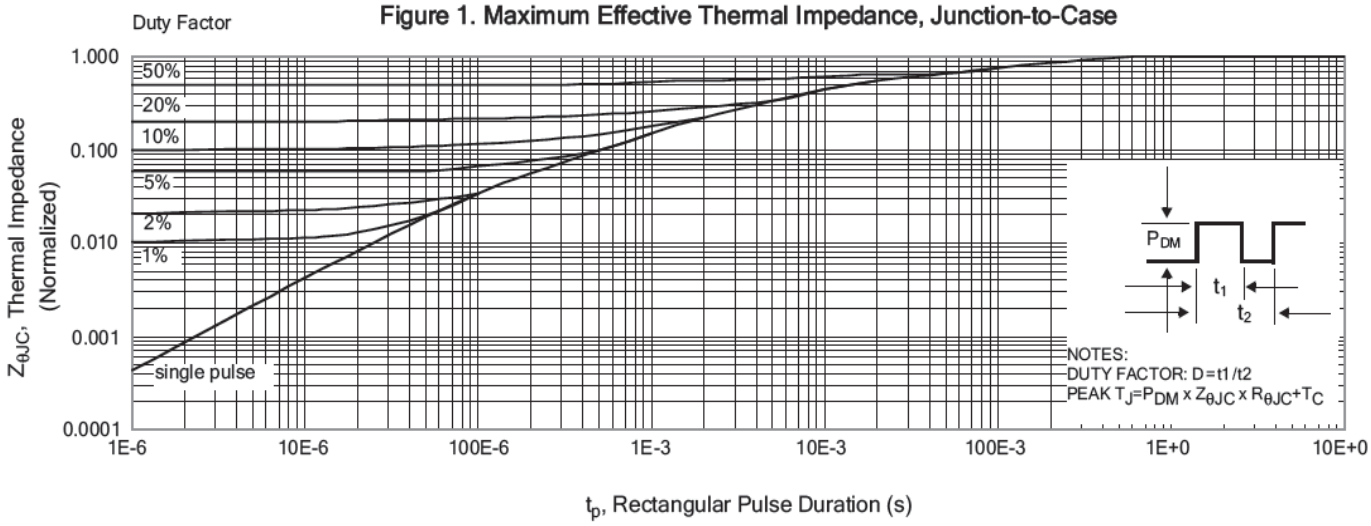


Figure 2. Maximum Power Dissipation vs Case Temperature

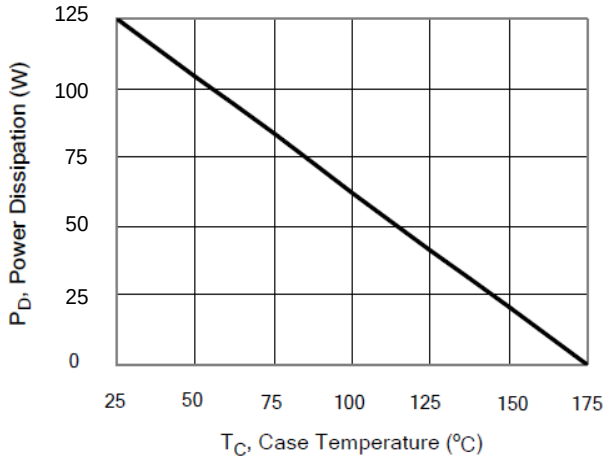


Figure3. Maximum Continuous Drain Current vs Case Temperature

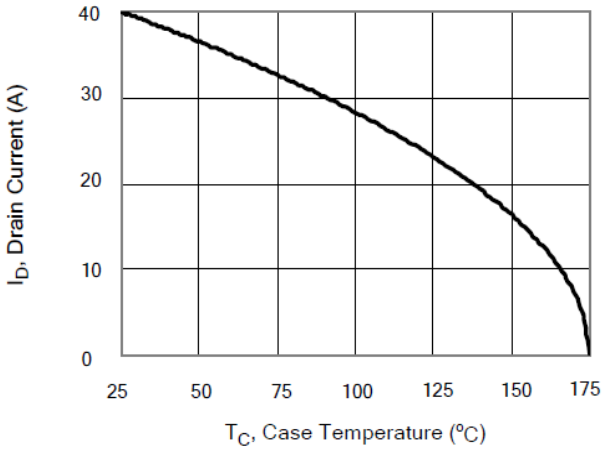


Figure 4. Typical Output Characteristics

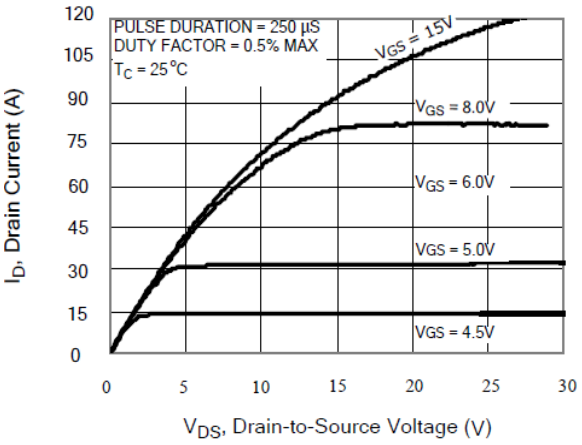
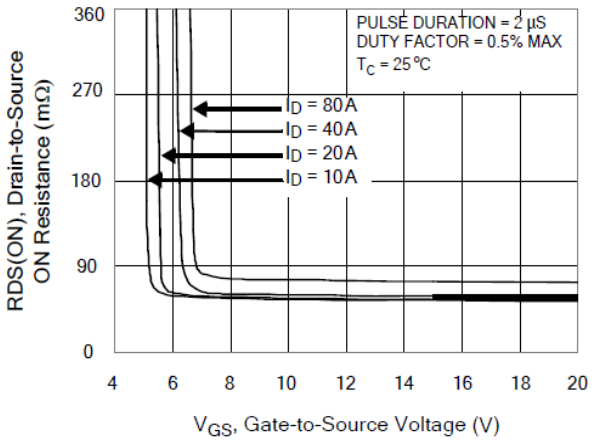


Figure 5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current



Typical Characteristics(Cont.)

Figure 6. Maximum Peak Current Capability

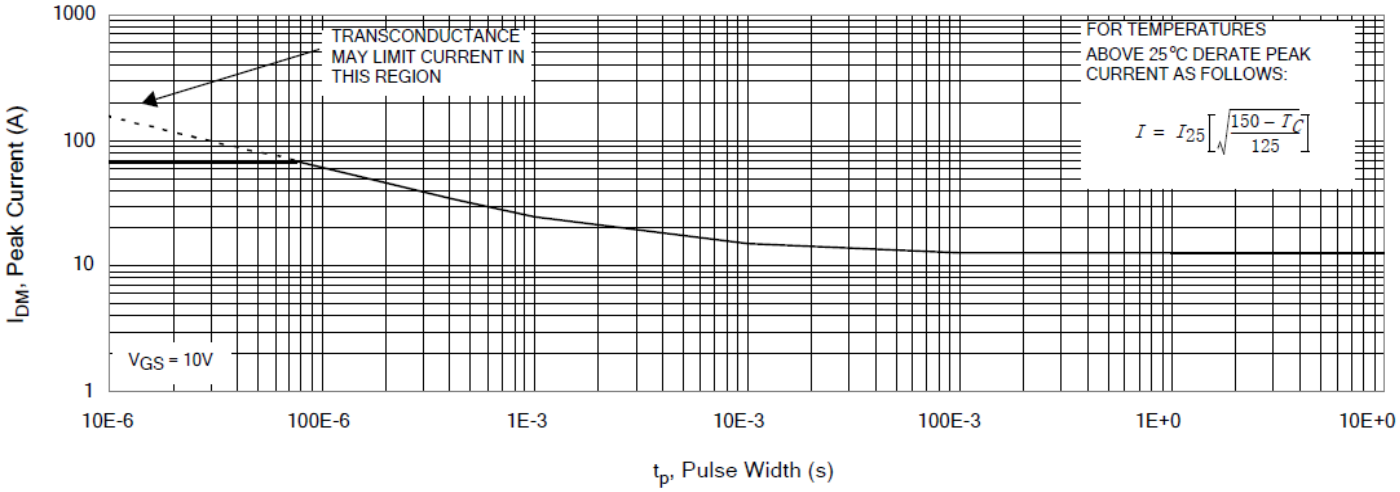


Figure 7. Typical Transfer Characteristics

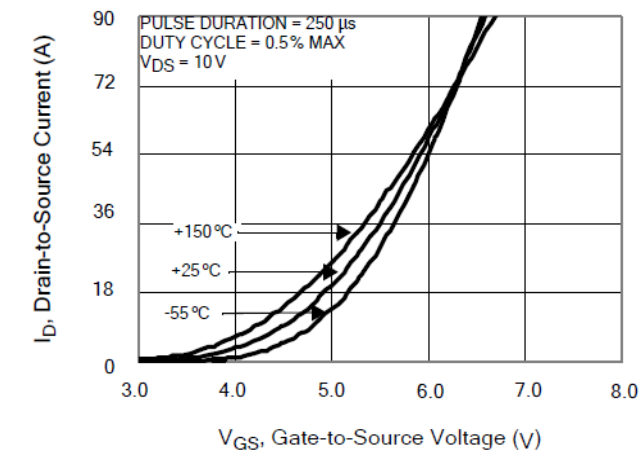


Figure 8. Unclamped Inductive Switching Capability

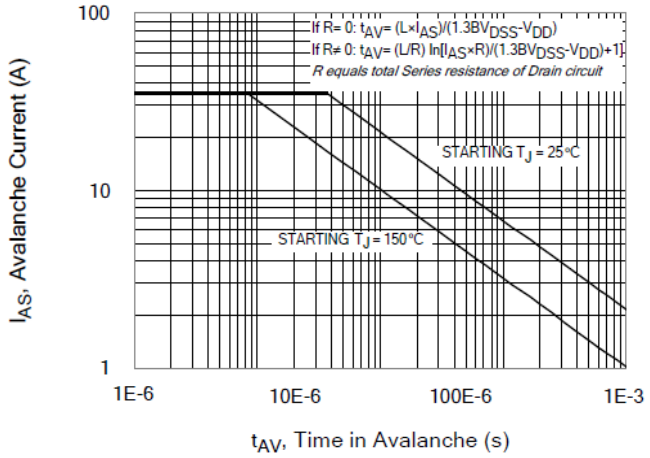


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

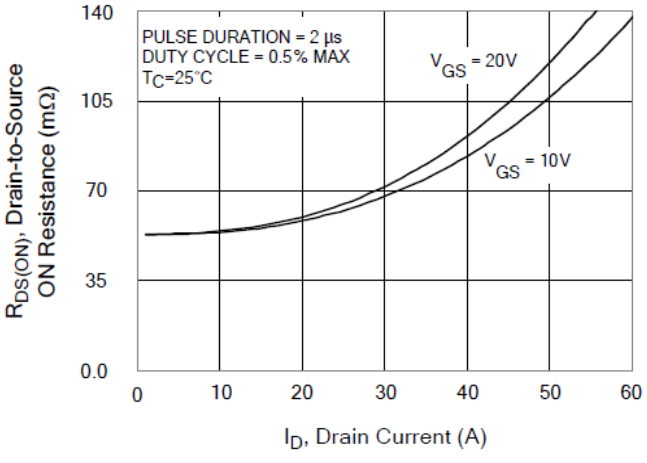
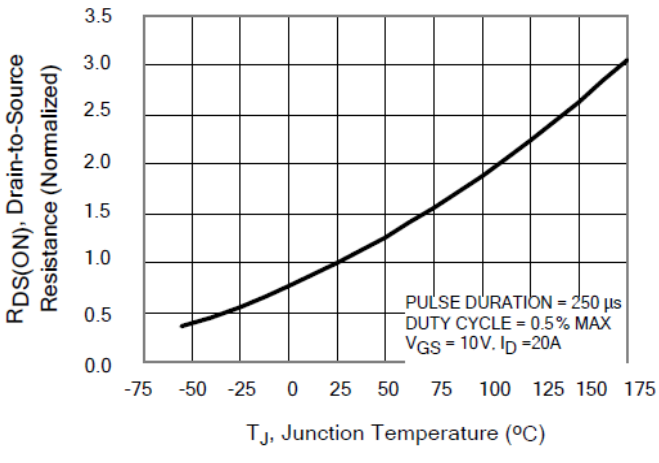


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature



Typical Characteristics(Cont.)

Figure 11. Typical Breakdown Voltage vs Junction Temperature

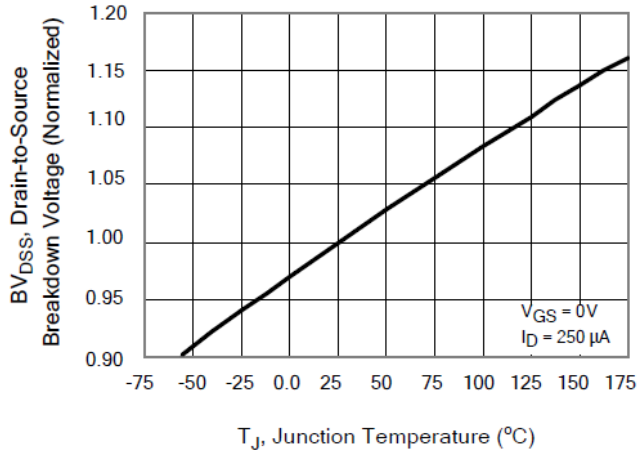


Figure 12. Typical Threshold Voltage vs Junction Temperature

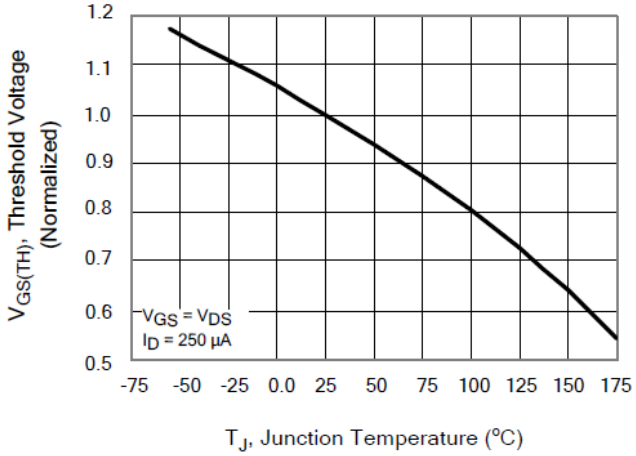


Figure 13. Maximum Forward Bias Safe Operating Area

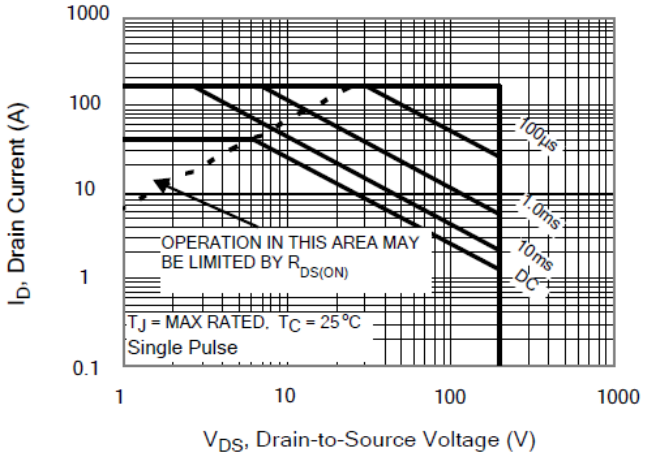


Figure 14. Typical Capacitance vs Drain-to-Source Voltage

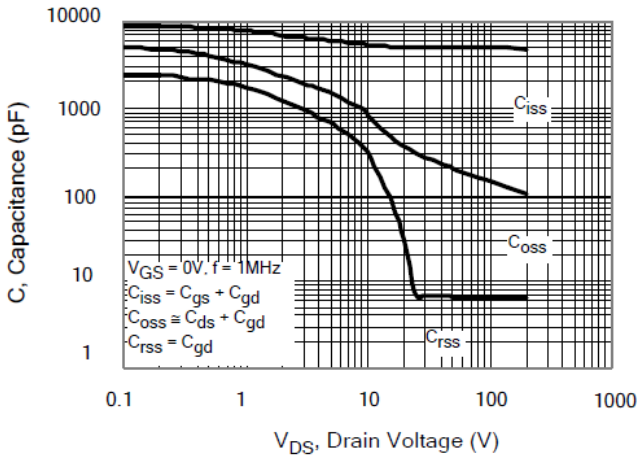


Figure 15 .Typical Gate Charge

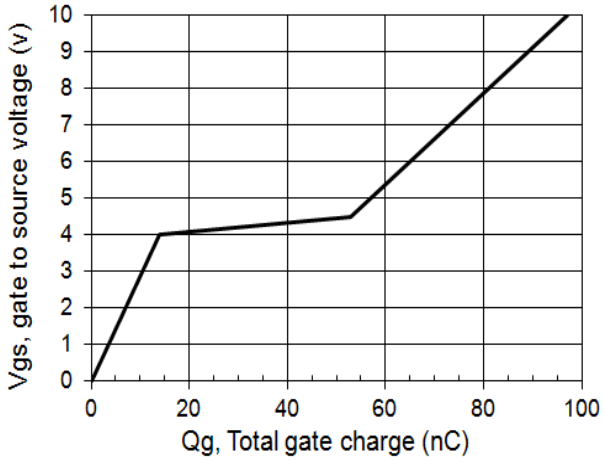
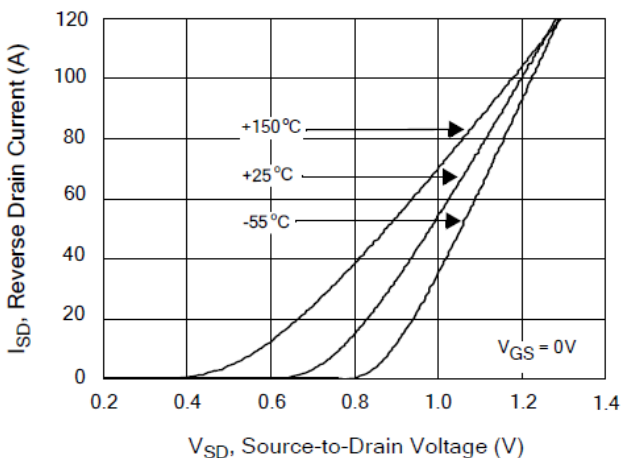


Figure 16. Typical Body Diode Transfer Characteristics



Test Circuits and Waveforms

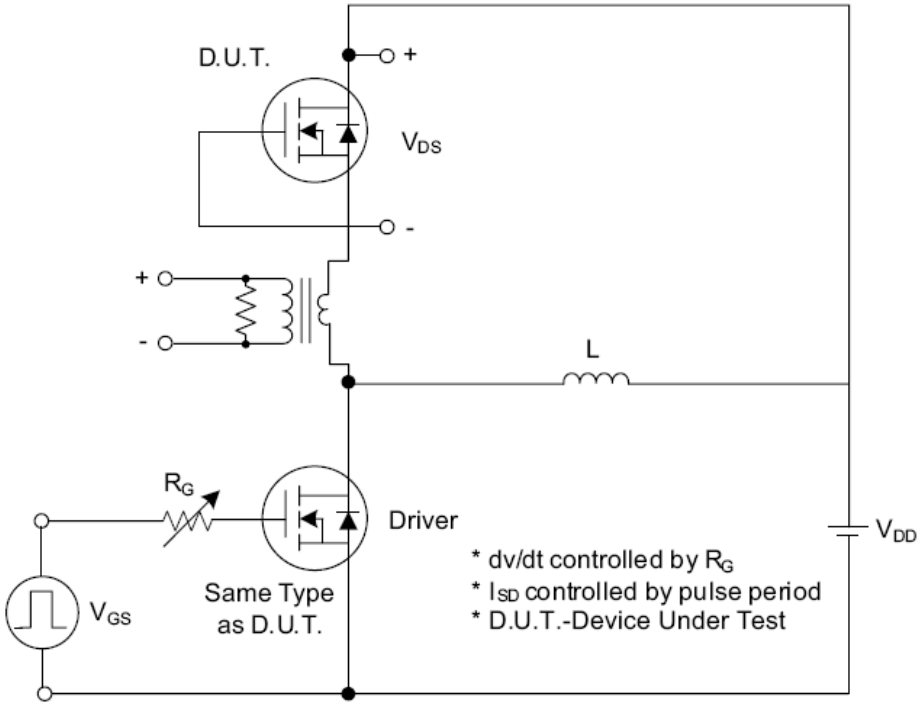


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

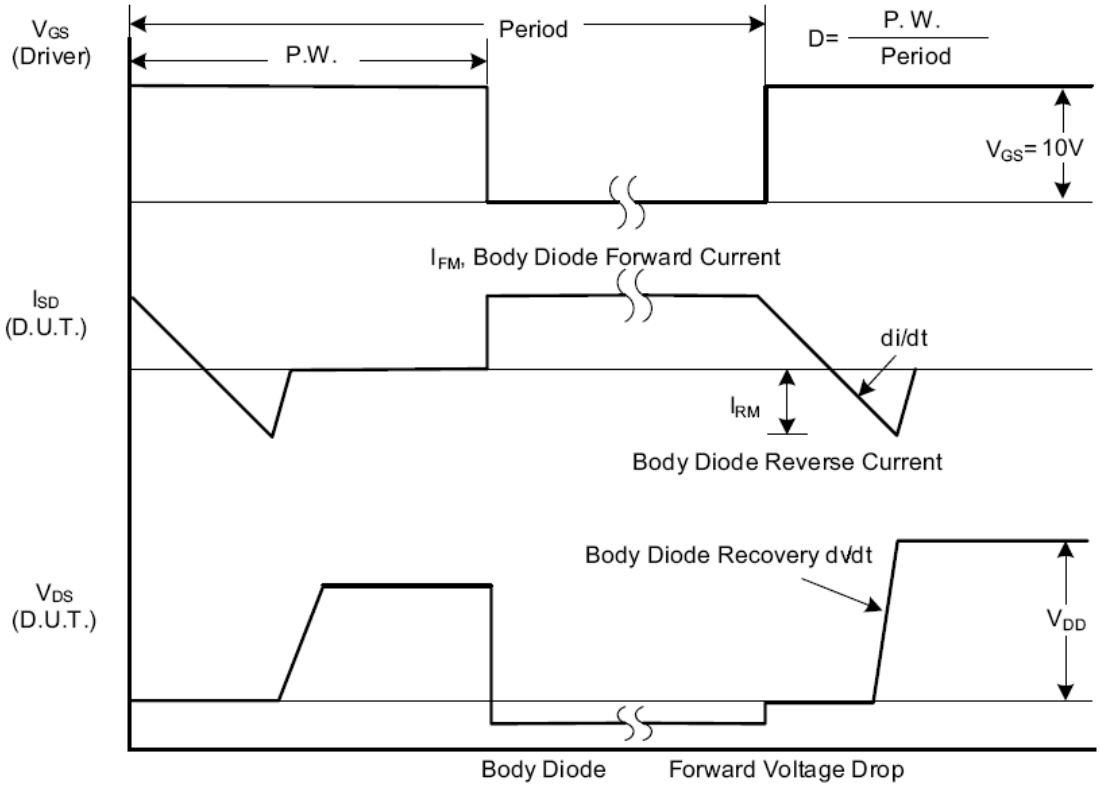


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms

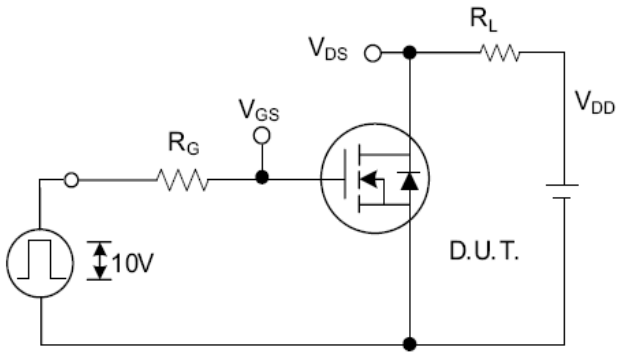


Fig. 2.1 Switching Test Circuit

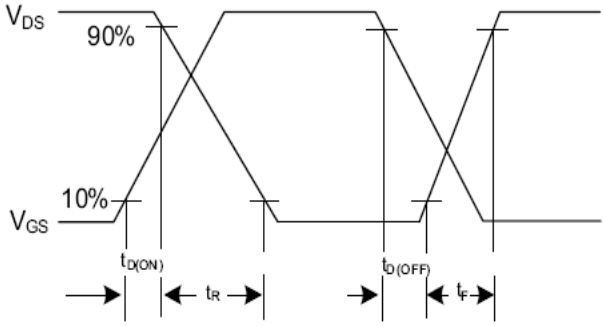


Fig. 2.2 Switching Waveforms

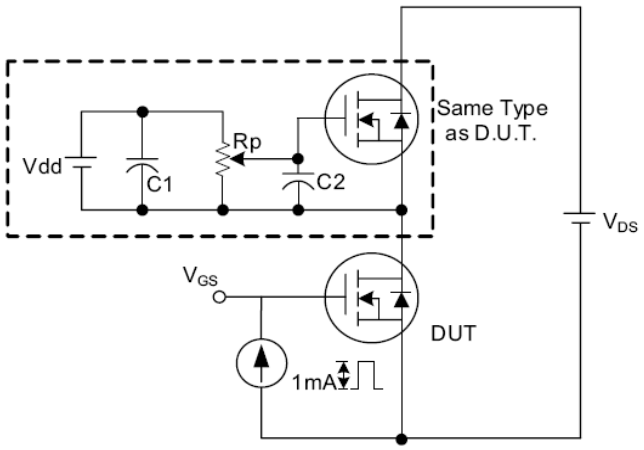


Fig. 3 . 1 Gate Charge Test Circuit

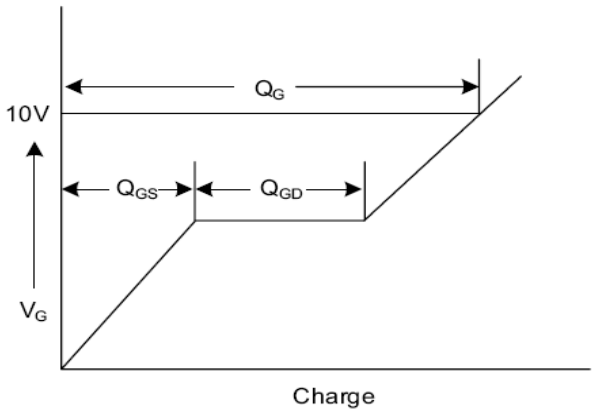


Fig. 3 . 2 Gate Charge Waveform

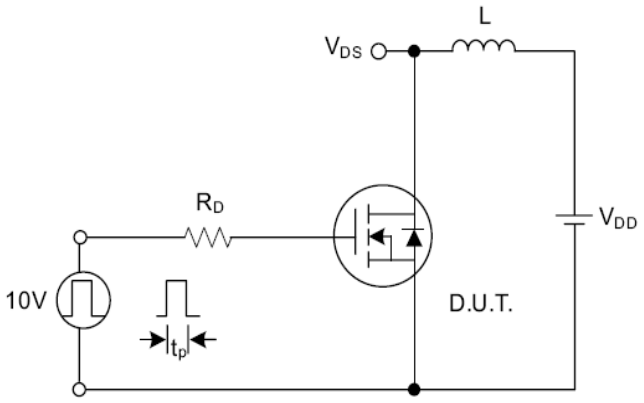


Fig. 4.1 Unclamped Inductive Switching Test Circuit

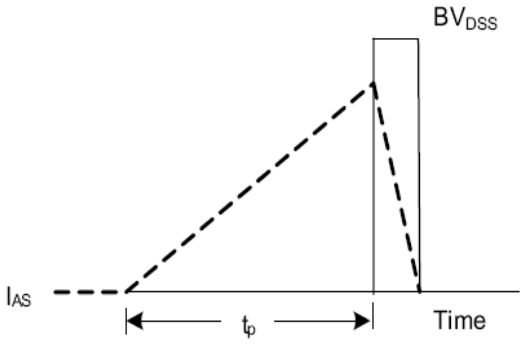
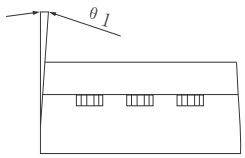
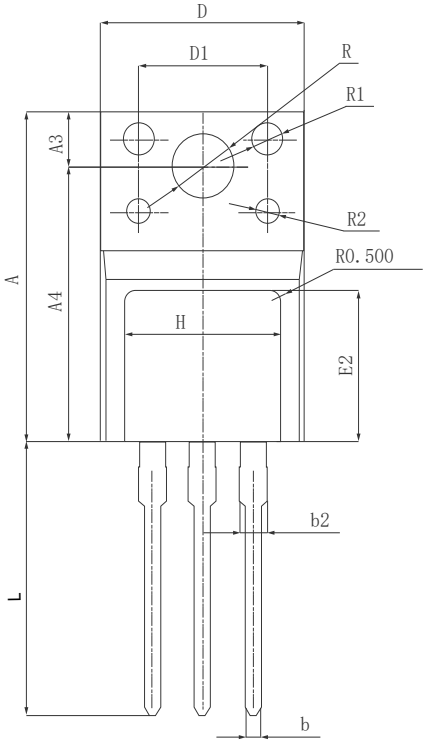
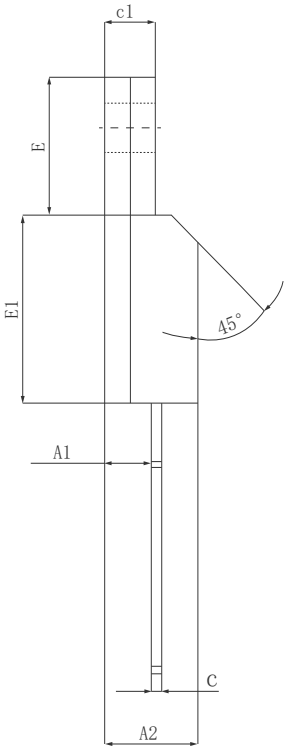


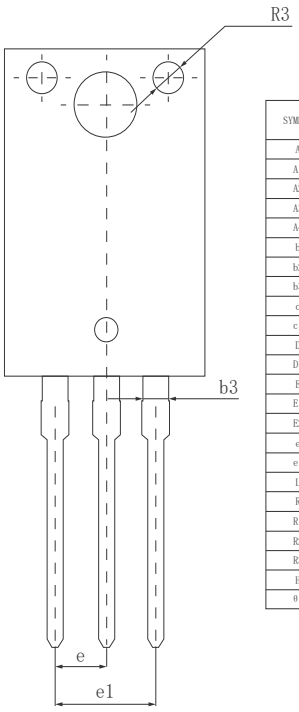
Fig. 4.2 Unclamped Inductive Switching Waveforms

●Dimensions（TO-220F）

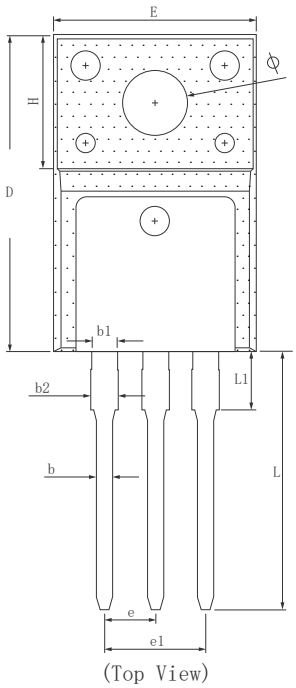




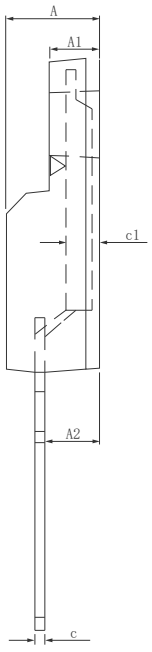


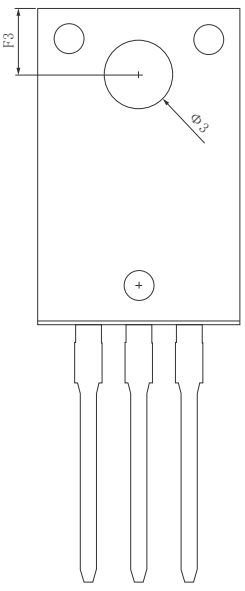


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	15.670	15.870	16.070
A1	2.150	2.350	2.550
A2	4.500	4.700	4.900
A3	3.100	3.300	3.500
A4	12.270	12.570	12.870
b	0.770	0.800	0.830
b2	1.200	1.300	1.400
b3	1.200BSC		
c	0.400	0.500	0.600
c1	2.440	2.540	2.640
D	9.860	10.160	10.460
D1	6.900	7.000	7.100
E	6.480	6.680	6.880
E1	8.990	9.190	9.390
E2	7.100	7.300	7.500
e	2.540BSC		
e1	5.080BSC		
L	13.140	13.340	13.540
R	3.100	3.300	3.500
R1	1.500REF.		
R2	1.200REF.		
R3	1.500REF.		
H	7.600	7.800	8.000
θ1	4°	4.5°	5°



(Top View)



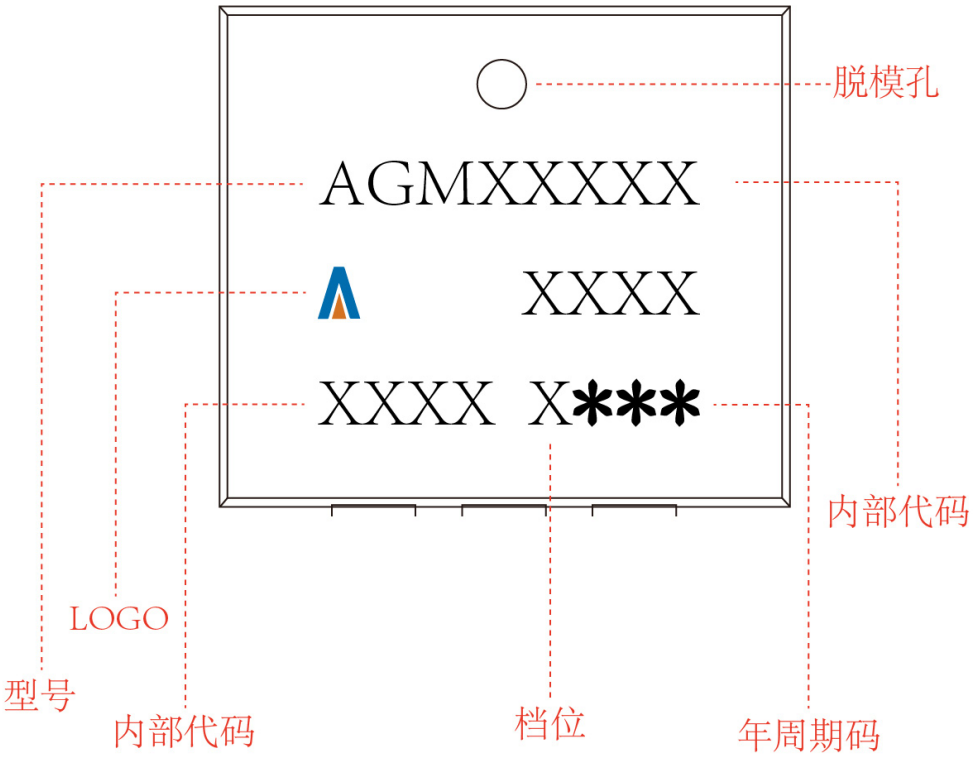


(Bottom View)

SYMBOL	MILLIMETER		
	MIN	Typ.	MAX
A	4.500	4.700	4.900
A1	2.340	2.540	2.740
A2	2.560	2.760	2.960
b	0.700	0.800	0.950
b1	1.180	1.280	1.430
b2	1.250	1.350	1.550
c	0.400	0.500	0.650
c1	1.200	1.300	1.350
D	15.570	15.870	16.170
H	6.700 REF		
E	9.960	10.160	10.360
e	2.540 BSC		
e1	5.080 BSC		
L	12.680	12.980	13.280
L1	2.780	2.930	3.080
F3	3.150	3.300	3.450
Φ	3.030	3.180	3.450
Φ3	3.150	3.450	3.650

(注：全尺寸测量时c1不测)

TO-220F
Marking Instructions:



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This document is the fifth version issued on June 20th, 2025. This document replaces all previously provided information.