钍地半导体
Tudi Semiconductor

Product Specification

TUDI-TPS3705/ TPS3707

具有电源故障检测功能的处理器监控电路

网址 www.sztdbdt.com

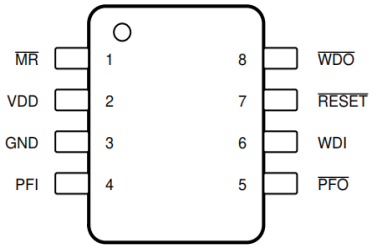
用芯智造·卓越品质

semiconductor device manufacturer

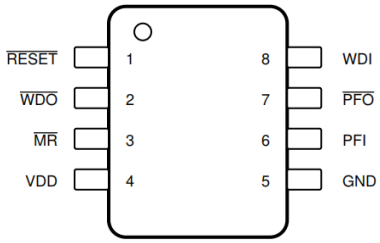
- Design
- research and development
- production
- and sales

特性

●具有 200ms 固定延时时间的上电复位发生器（无需 外部电容器）
●精密电源电压监控器：2.5V、3V、3.3V 和 5V
● 与 MAX705 至 MAX708 系列引脚对引脚兼容
●集成看门狗时间（仅限 TPS3705-xx）
●用于电源故障或低电池电量警告的电压监控器
●50μA 最大电源电流
● 8 引脚 MSOP 和 8 引脚 SOIC 封装
●温度范围：-40°C 至 85°C
（TPS3705-33 为-40°C 至 125°C）



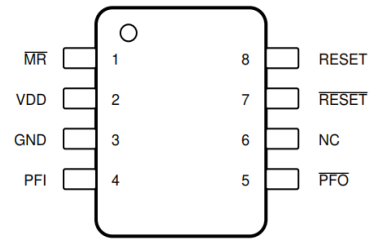
TPS3705-xx D Package 8-Pin SOIC Top View6



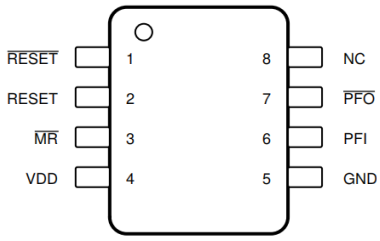
TPS3705-xx DGN Package 8-Pin MSOP-PowerPAD Top View

应用

●使用 DSP、微控制器或微处理器的设计
● 工业设备
● 可编程控制
●汽车系统
● 便携式或电池供电类设备
● 智能仪表
● 无线通信系统
●笔记本电脑或台式机



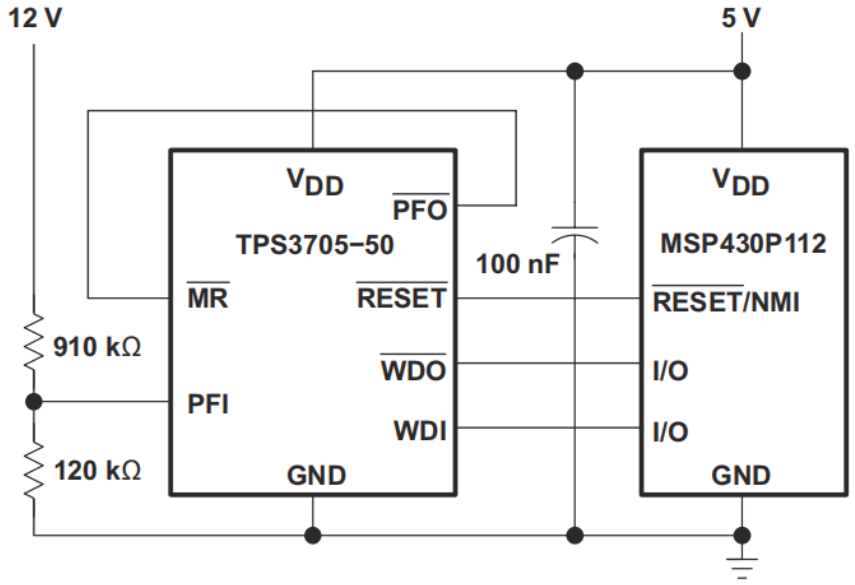
TPS3707-xx D Package 8-Pin SOIC Top View



TPS3707-xx DGN Package 8-Pin MSOP-PowerPAD Top View

说明

TPS370x-xx 系列微处理器电源电压监控器主要为DSP 以及基于其他处理器的系统提供电路初始化和时 序监控。 上电期间，如果电源电压 VDD 大于 1.1V，RESET 就 会生效。因此，只要 VDD 保持在阈值电压 VIT + 以下， 电源电压监控器就会监测 VDD，并使 RESET 保持有效 状态。当电源电压降到阈值电压 VIT – 以下时，输出再 次变为有效状态（低电平）。无需外部组件。该系列中 的所有器件均具有一个通过内部分压器设定的固定检测 阈值电压 VIT – 。
该产品系列专为 2.5V、3V、3.3V 以及 5V 电源电压而 设计。这些电路采用 8 引脚 MSOP 或标准 SOIC 封装。TPS370x-xx 器件的额定工作温度范围为 -40°C 至 85°C。



MSP430 典型应用

6.1 Pin Functions

PIN					I/O	DESCRIPTION
NAME	TPS3705-xx		TPS3707-xx			
	SOIC	MSOP-PowerPAD	SOIC	MSOP-PowerPAD		
GND	3	5	3	5	—	Ground
$\overline{MR}$	1	3	1	3	I	Manual reset
NC	—	—	6	8	—	No internal connection
PFI	4	6	4	6	I	Power-fail comparator input
$\overline{PFO}$	5	7	5	7	O	Power-fail comparator output
$\overline{RESET}$	7	1	7	1	O	Active-low reset output
RESET	—	—	8	2	O	Active-high reset output
V_{DD}	2	4	2	4	—	Supply voltage
WDI	6	8	—	—	I	Watchdog timer input
$\overline{WDO}$	8	2	—	—	O	Watchdog timer output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{DD} (2)		7	V
PFI voltage range, V_{PFI}	−0.3	V_{DD} + 0.3	V
All other pins(2)	−0.3	7	V
Maximum low output current, I_{OL}		5	mA
Maximum high output current, I_{OH}		−5	mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})		±20	mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD})		±20	mA
Continuous total power dissipation	See 节7.9		
Soldering temperature		260	°C
Operating temperature, T_A	−40	85	°C
Operating temperature, T_A for TPS3705-33 only	−40	125	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than t = 1000h continuously.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	2		6	V
V_I	Input voltage	0		V_{DD} + 0.3	V
V_{IH}	High-level input voltage	0.7 × V_{DD}			V
V_{IL}	Low-level input voltage			0.3 × V_{DD}	V
$\Delta t/\Delta V$	Input transition rise and fall rate at $\overline{MR}$ or WDI			100	ns/V
T_A	Operating free-air temperature	−40		85	°C
T_A	Operating free-air temperature for TPS3705-33 only	−40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS3705-xx D (SOIC) 8 PINS	TPS3707-xx DGN (MSOP-PowerPAD) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.2	66.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.4	62.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.5	45.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.8	7.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57.9	44.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	18.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.8 Switching Characteristics

at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{t(out)}$	Watchdog time out	$V_{DD} \geq V_{IT+}$ + 0.2 V, see 图 7-1	1.1	1.6	2.3	s
t_d	Delay time	$V_{DD} \geq V_{IT+}$ + 0.2 V, see 图 7-1	140	200	280	ms
t_{PHL}	Propagation (delay) time, high-to-low-level output	$\overline{MR}$ to $\overline{RESET}$ delay, $V_{DD} \geq V_{IT+}$ + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}		50	250	ns
t_{PLH}	Propagation (delay) time, low-to-high-level output	$\overline{MR}$ to RESET delay (TPS3707-xx only) $V_{DD} \geq V_{IT+}$ + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}		50	250	ns
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{RESET}$ delay		3	5	µs
t_{PLH}	Propagation (delay) time, low-to-high-level output	V_{DD} to RESET delay (TPS3707-xx only)		3	5	µs
t_{PHL}	Propagation (delay) time, high-to-low-level output	PFI to $\overline{PFO}$ delay, V_{DD} = 2 V to 6 V		0.5	1	µs
t_{PLH}	Propagation (delay) time, low-to-high-level output	PFI to $\overline{PFO}$ delay, V_{DD} = 2 V to 6 V		0.5	1	µs

7.9 Dissipation Ratings

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DGN	2.14 W	17.1 mW/°C	1.37 W	1.11 W
D	725 mW	5.8 mW/°C	464 mW	377 mW

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	TPS370x-xx, V_{DD} = 1.1 V, I_{OH} = – 4 μA	0.8			V
		TPS3707-25, TPS370x-30, TPS370x-33, V_{DD} = V_{IT+} + 0.2 V, I_{OH} = – 500 μA	0.7 × V_{DD}			
		TPS370x-50, V_{DD} = V_{IT+} + 0.2 V, I_{OH} = – 800 μA	V_{DD} – 1.5			
		TPS370x-xx, V_{DD} = 6 V, I_{OH} = – 800 μA	V_{DD} – 1.5			
V_{OL}	Low-level output voltage	TPS3707-25, TPS370x-30, TPS370x-33, V_{DD} = V_{IT+} + 0.2 V, I_{OL} = 1 mA			0.3	V
		TPS370x-50, V_{DD} = V_{IT+} + 0.2 V, I_{OL} = 2.5 mA			0.4	
		TPS370x-xx, V_{DD} = 6 V, I_{OL} = 3 mA			0.4	
	Power-up reset voltage(1)	V_{DD} ⩾ 1.1 V, I_{OL} = 50 μA			0.3	V
V_{IT-}	Negative-going input threshold voltage(2)	TPS3707-25, T_A = 0°C to 85°C	2.2	2.25	2.3	V
		TPS370x-30, T_A = 0°C to 85°C	2.57	2.63	2.68	
		TPS370x-33, T_A = 0°C to 85°C	2.87	2.93	2.98	
		TPS370x-50, T_A = 0°C to 85°C	4.45	4.55	4.63	
		TPS3707-25, T_A = – 40°C to 85°C	2.2	2.25	2.32	
		TPS370x-30, T_A = – 40°C to 85°C	2.57	2.63	2.7	
		TPS370x-33, T_A = – 40°C to 85°C	2.87	2.93	3	
		TPS370x-50, T_A = – 40°C to 85°C	4.45	4.55	4.65	
	Negative-going input threshold voltage, PFI(2)	TPS370x-xx, V_{DD} ⩾ 2 V, T_A = – 40°C to 85°C	1.2	1.25	1.3	
V_{hys}	Hysteresis, V_{DD}	TPS3707-25		40		mV
		TPS370x-30		50		
		TPS370x-33		50		
		TPS370x-50		70		
	Hysteresis, PFI	TPS370x-xx		10		
$I_{IH(AV)}$	Average high-level input current, WDI	WDI = V_{DD} = 6 V, time average (dc = 88%)		100	150	μA
$I_{IL(AV)}$	Average low-level input current, WDI	WDI = 0 V, V_{DD} = 6 V, time average (dc = 12%)		– 15	– 20	μA
I_{IH}	High-level input current, WDI	WDI = V_{DD} = 6 V		120	170	μA
	High-level input current, $\overline{MR}$	$\overline{MR}$ = 0.7 × V_{DD}, V_{DD} = 6 V		– 130	– 180	
I_{IL}	Low-level input current, WDI	WDI = 0 V, V_{DD} = 6 V		– 120	– 170	μA
	Low-level input current, $\overline{MR}$	$\overline{MR}$ = 0 V, V_{DD} = 6 V		– 430	– 600	
I_I	Input current, PFI	V_{DD} = 6 V, 0 V ⩽ V_I ⩽ V_{DD}	– 1	0	1	μA
I_{DD}	Supply current	TPS3705-xx, V_{DD} = 2 V to 6 V, $\overline{MR}$ = V_{DD}, $\overline{MR}$, WDI and outputs unconnected		30	50	μA
		TPS3707-xx, V_{DD} = 2 V to 6 V, $\overline{MR}$ = V_{DD}, $\overline{MR}$, WDI and outputs unconnected		20	50	
C_i	Input capacitance	V_I = 0 V to V_{DD}		5		pF

(1) The lowest supply voltage at which $\overline{RESET}$ becomes active, $t_{r,VDD}$ ⩾ 15 μs/V
(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed near to the supply terminals

7.6 Electrical Characteristics for TPS3705-33 Only

over operating free-air temperature range -40 to 125C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} = 1.1 V, I_{OH} = – 4 μA	0.8			V
		V_{DD} = V_{IT+} + 0.2 V, I_{OH} = – 500 μA	0.7 × V_{DD}			
		V_{DD} = 6 V, I_{OH} = – 800 μA	V_{DD} – 1.5			
V_{OL}	Low-level output voltage	V_{DD} = V_{IT+} + 0.2 V, I_{OL} = 1 mA			0.3	V
		V_{DD} = 6 V, I_{OL} = 3 mA			0.4	
	Power-up reset voltage(1)	V_{DD} ⩾ 1.1 V, I_{OL} = 50 μA			0.3	V
V_{IT-}	Negative-going input threshold voltag	T_A = 0°C to 125°C	2.87	2.93	3	V
		T_A = – 40°C to 125°C	2.87	2.93	3.02	
	Negative-going input threshold voltage, PFI(2)	V_{DD} ⩾ 2 V	1.2	1.25	1.3	
V_{hys}	Hysteresis, V_{DD}			50		mV
	Hysteresis, PFI			10		
$I_{IH(AV)}$	Average high-level input current, WDI	WDI = V_{DD} = 6 V, time average (dc = 88%)		100	150	μA
$I_{IL(AV)}$	Average low-level input current, WDI	WDI = 0 V, V_{DD} = 6 V, time average (dc = 12%)		– 15	– 20	μA
I_{IH}	High-level input current, WDI	WDI = V_{DD} = 6 V		120	170	μA
	High-level input current, $\overline{MR}$	$\overline{MR}$ = 0.7 × V_{DD}, V_{DD} = 6 V		– 130	– 180	
I_{IL}	Low-level input current, WDI	WDI = 0 V, V_{DD} = 6 V		– 120	– 170	μA
	Low-level input current, $\overline{MR}$	$\overline{MR}$ = 0 V, V_{DD} = 6 V		– 430	– 600	
I_I	Input current, PFI	V_{DD} = 6 V, 0 V ⩽ V_I ⩽ V_{DD}	– 1	0	1	μA
I_{DD}	Supply current	V_{DD} = 2 V to 6 V, $\overline{MR}$ = V_{DD}, $\overline{MR}$, WDI and outputs unconnected		30	50	μA
C_i	Input capacitance	V_I = 0 V to V_{DD}		5		pF

7.7 Timing Requirements

at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_w	Pulse width	At V_{DD}, V_{DD} = V_{IT+} + 0.2 V, V_{DD} = V_{IT-} – 0.2 V	6			μs
		At $\overline{MR}$ and WDI, V_{DD} ⩾ V_{IT+} + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}	100			ns

7.10 Timing Diagram

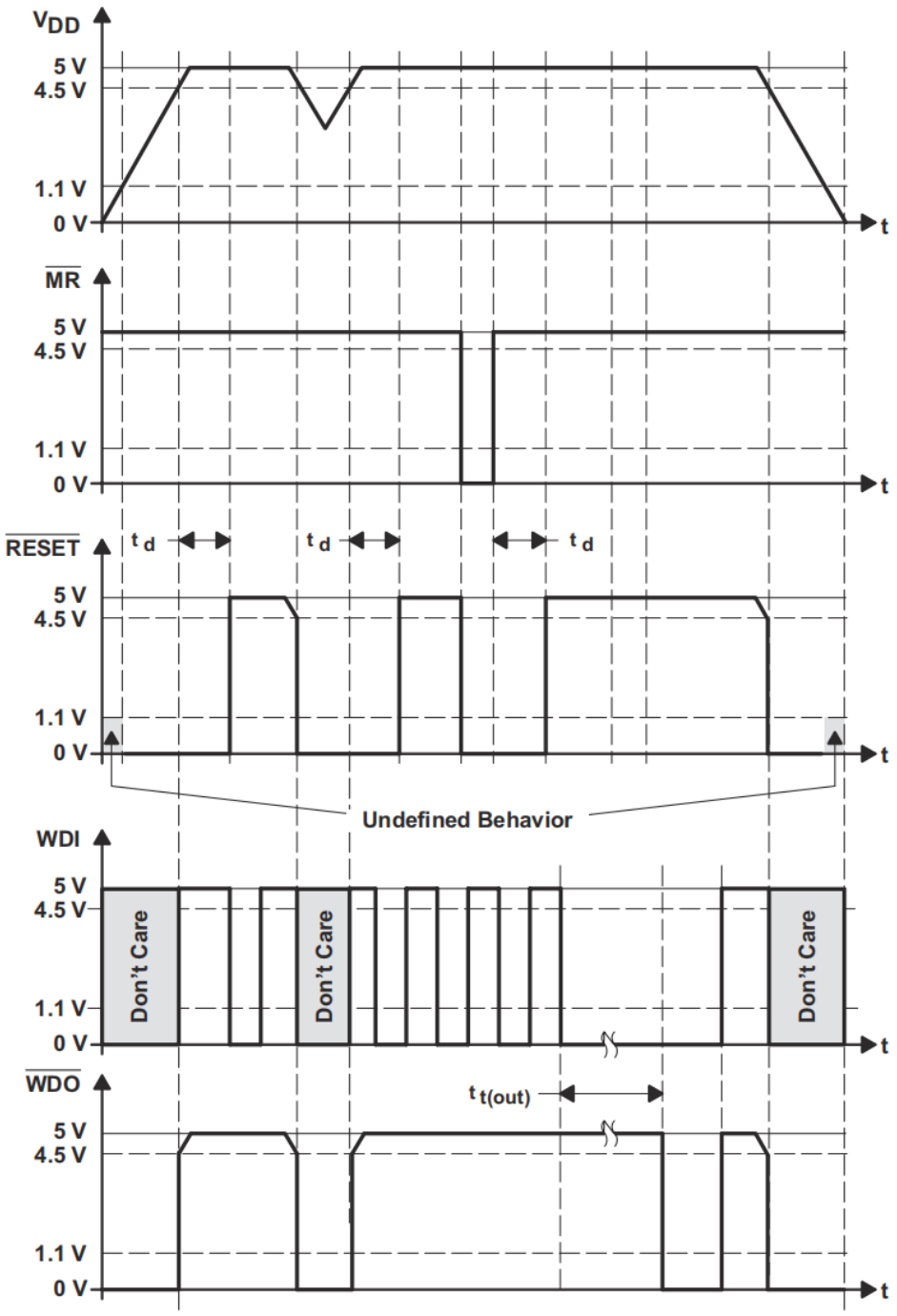


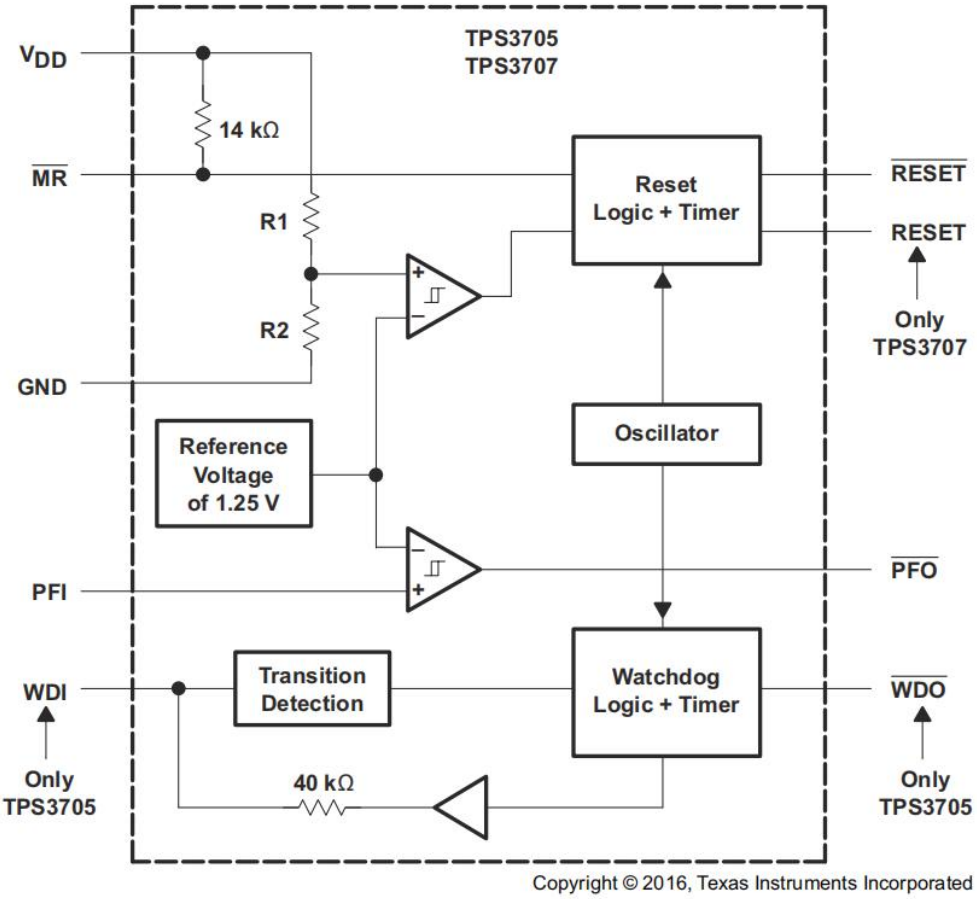
图 7-1. Timing Diagrams

8 Detailed Description

8.1 Overview

The TPS370x-xx family of supervisors feature an integrated reference and comparator for V_{DD} supervision, an additional power-fail supervisor, and a manual reset input. The TPS3705-xx devices feature a watchdog timer, where the TPS3707-xx devices feature a complimentary RESET output.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Manual Reset Input

The TPS370x-xx devices incorporate a manual reset input, $\overline{MR}$. A low level at $\overline{MR}$ causes $\overline{RESET}$ to become active.

8.3.2 Power-Fail Comparator

The TPS370x-xx family integrates a power-fail comparator which can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply.

8.3.3 Watchdog Timer

The TPS3705-xx devices have a watchdog timer that is periodically triggered by a positive or negative transition at WDI. When the supervising system fails to retrigger the watchdog circuit within the timeout interval, $t_{t(out)}$ = 1.6 s, $\overline{WDO}$ becomes active. This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog.

The TPS3707-xx devices do not have the watchdog function, but include a high-level output RESET.

8.4 Device Functional Modes

8.4.1 V_{DD} < 1.1 V

When V_{DD} is less than 1.1 V, the status of the outputs cannot be determined.

8.4.2 1.1 V < V_{DD} ⩽ 2 V

When V_{DD} is greater than 1.1 V but less than 2 V, the output states are valid. However, the specifications in 节 7.5 do not apply.

8.4.3 2 V < V_{DD} < 6 V

When V_{DD} is greater than 2 V but less than 6 V, the device is within the recommended operating conditions (see 节 7.3). See 表 8-1, 表 8-2, and 表 8-3 for corresponding truth tables.

表 8-1. TPS3705 Truth Table

$\overline{MR}$	$V_{DD} > V_{IT}$	$\overline{RESET}$	TYPICAL DELAY
H → L	1	H → L	30 ns
L → H	1	L → H	200 ms
H	1 → 0	H → L	3 µs
H	0 → 1	L → H	200 ms

表 8-2. TPS3707 Truth Table

$\overline{MR}$	$V_{DD} > V_{IT}$	$\overline{RESET}$	RESET	TYPICAL DELAY
H → L	1	H → L	L → H	30 ns
L → H	1	L → H	H → L	200 ms
H	1 → 0	H → L	L → H	3 µs
H	0 → 1	L → H	H → L	200 ms

表 8-3. TPS370x Truth Table

PFI > V_{IT}	$\overline{PFO}$	TYPICAL DELAY
0 → 1	L → H	0.5 µs
1 → 0	H → L	0.5 µs

9.1 Application Information

The TPS370x-xx family of devices offers several options for power monitoring. The TPS3705-xx offers a watchdog supervisor, V_{DD} rail monitoring, and a power-fail interrupt monitor. The TPS3707-xx offers V_{DD} rail monitoring with complimentary outputs and a power-fail interrupt monitor.

9.2 Typical Application

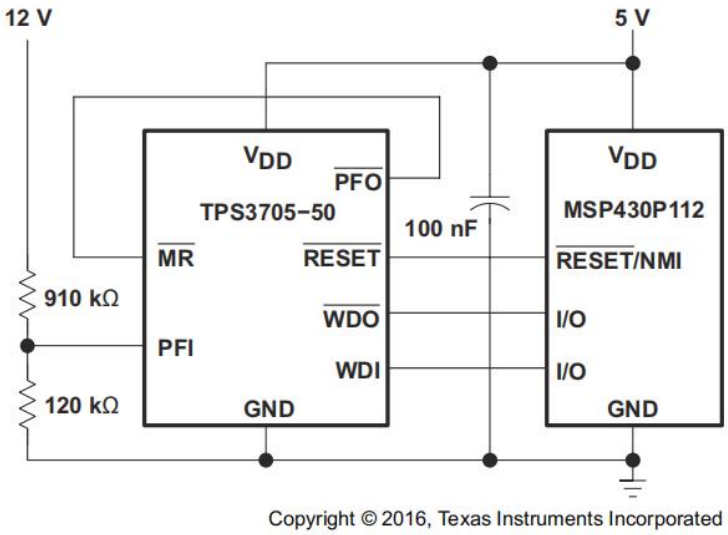


图 9-1. Typical MSP430 Application

9.2.1 Design Requirements

表 9-1 lists the required design parameters for 图 9-1.

表 9-1. Application Parameters

DESIGN PARAMETER	VALUE
Monitored voltage 1	5 V
Monitored voltage 2	12 V

9.2.2 Detailed Design Procedure

To create two voltage monitoring rails, the PFI input can be used along with the MR pin to create a single output. The 5-V monitor is created by selecting a 5-V device option, giving threshold of 4.55 V. The PFI input is configured to any adjustable rail with a voltage divider. Use 方程式 1 to select resistors.

$$V_{TH} = \frac{R_1 + R_2}{R_2} \times V_{IT-} = \frac{910\,k + 120\,k}{120\,k} \times 1.25 = 10.73\ V \quad (1)$$

11 Layout

11.1 Layout Guidelines

Place a 0.1-μF decoupling capacitor as close to the device as possible.

If a resistor divider is used, place the resistors as close to the device as possible to minimize noise coupling.

11.2 Layout Example

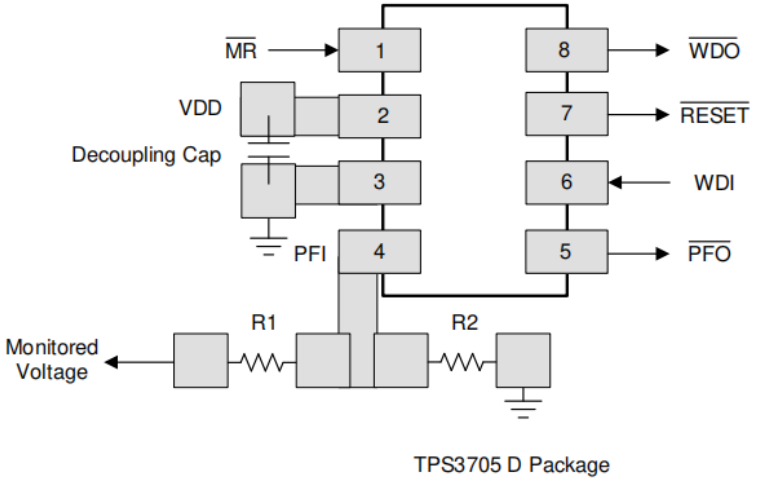
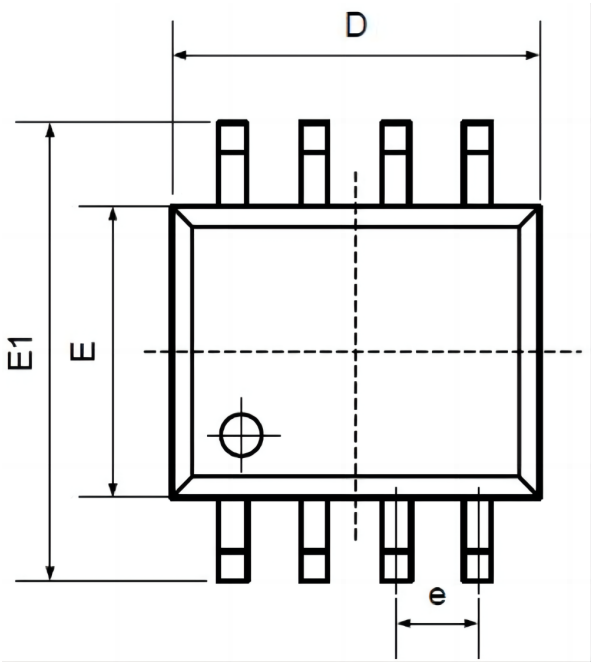


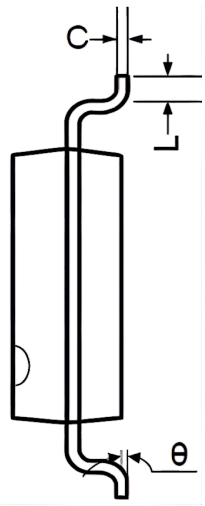
图 **11-1. TPS3705 Layout**

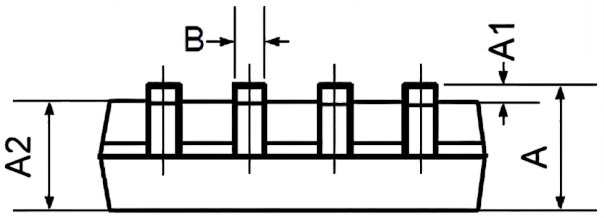
ORDERING INFORMATION

Order Number	Package	Package Quantity	Marking On The park
TPS3705-30DR-TUDI	SOP8	Tape,Reel,2500	70530
TPS3705-33DR-TUDI	SOP8	Tape,Reel,2500	70533
TPS3705-50DR-TUDI	SOP8	Tape,Reel,2500	70550
TPS3707-30DR-TUDI	SOP8	Tape,Reel,2500	70730
TPS3707-50DR-TUDI	SOP8	Tape,Reel,2500	70750

Package SOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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