



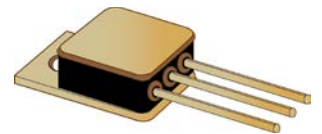
## N-CHANNEL MOSFET

Qualified per MIL-PRF-19500/592

Qualified Levels:  
JAN, JANTX, and  
JANTXV

### DESCRIPTION

This family of switching transistors is military qualified up to the JANTXV level for high-reliability applications. These devices are also available in a low profile U surface mount package. Microsemi also offers numerous other transistor products to meet higher and lower power ratings with various switching speed requirements in both through-hole and surface-mount packages.



**TO-254AA Package**


**Important:** For the latest information, visit our website <http://www.microsemi.com>.

### FEATURES

- JEDEC registered 2N7224, 2N7225, 2N7227 and 2N7228 number series.
- JAN, JANTX, and JANTXV qualifications are available per MIL-PRF-19500/592. (See [part nomenclature](#) for all available options.)
- RoHS compliant by design.

Also available in:

**U (SMD-1 or TO-267AB) package**  
(surface mount)

 [2N7224U & 2N7228U](#)

### APPLICATIONS / BENEFITS

- Low-profile design.
- Military and other high-reliability applications.

### MAXIMUM RATINGS @ T<sub>A</sub> = +25°C unless otherwise stated

Parameters / Test Conditions	Symbol	Value	Unit					
Operating & Storage Junction Temperature Range	T <sub>J</sub> & T <sub>stg</sub>	-55 to +150	°C					
Thermal Resistance Junction-to-Case	R <sub>θJC</sub>	0.83	°C/W					
Total Power Dissipation @ T <sub>A</sub> = +25 °C @ T <sub>C</sub> = +25 °C <sup>(1)</sup>	P <sub>T</sub>	4 150	W					
Gate-Source Voltage, dc	V <sub>GS</sub>	± 20	V					
Drain Current, dc @ T <sub>C</sub> = +25 °C <sup>(2)</sup>	I <sub>D1</sub>	2N7224 2N7225 2N7227 2N7228	34.0 27.4 14.0 12.0	A				
Drain Current, dc @ T <sub>C</sub> = +100 °C <sup>(2)</sup>		I <sub>D2</sub>	2N7224 2N7225 2N7227 2N7228		21 17 9 8	A		
Off-State Current (Peak Total Value) <sup>(3)</sup>			I <sub>DM</sub>		2N7224 2N7225 2N7227 2N7228		136 110 56 48	A (pk)
Source Current					I <sub>S</sub>		2N7224 2N7225 2N7227 2N7228	

**NOTES:**

1. Derated linearly by 1.2 W/°C for T<sub>C</sub> > +25 °C.
2. The following formula derives the maximum theoretical ID limit. ID is limited by package and internal wires and may also be limited by pin diameter:

$$I_D = \sqrt{\frac{T_J(\max) - T_C}{R_{\theta JC} \times R_{DS(on)} @ T_J(\max)}}$$

3. I<sub>DM</sub> = 4 x I<sub>D1</sub> as calculated in note 2.

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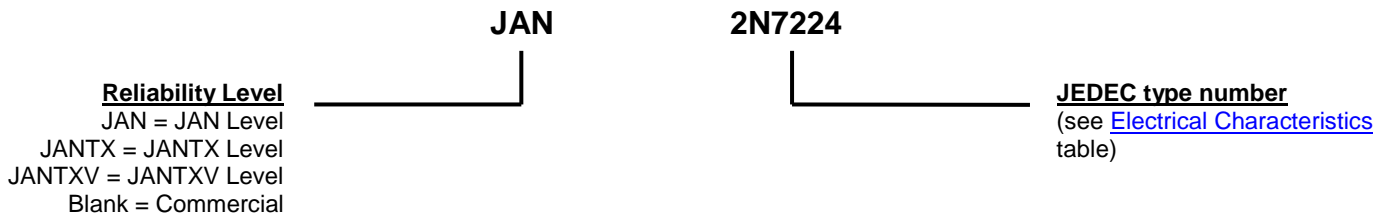
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[www.microsemi.com](http://www.microsemi.com)

**MECHANICAL and PACKAGING**

- CASE: Ceramic and gold over nickel plated steel.
- TERMINALS: Gold over nickel plated tungsten/copper.
- MARKING: Part number, date code, and polarity symbol.
- WEIGHT: 6.5 grams.
- See [Package Dimensions](#) on last page.

**PART NOMENCLATURE**

**SYMBOLS & DEFINITIONS**

Symbol	Definition
$di/dt$	Rate of change of diode current while in reverse-recovery mode, recorded as maximum value.
$I_F$	Forward current
$R_G$	Gate drive impedance
$V_{DD}$	Drain supply voltage
$V_{DS}$	Drain source voltage, dc
$V_{GS}$	Gate source voltage, dc

**ELECTRICAL CHARACTERISTICS @  $T_A = +25^\circ\text{C}$ , unless otherwise noted**

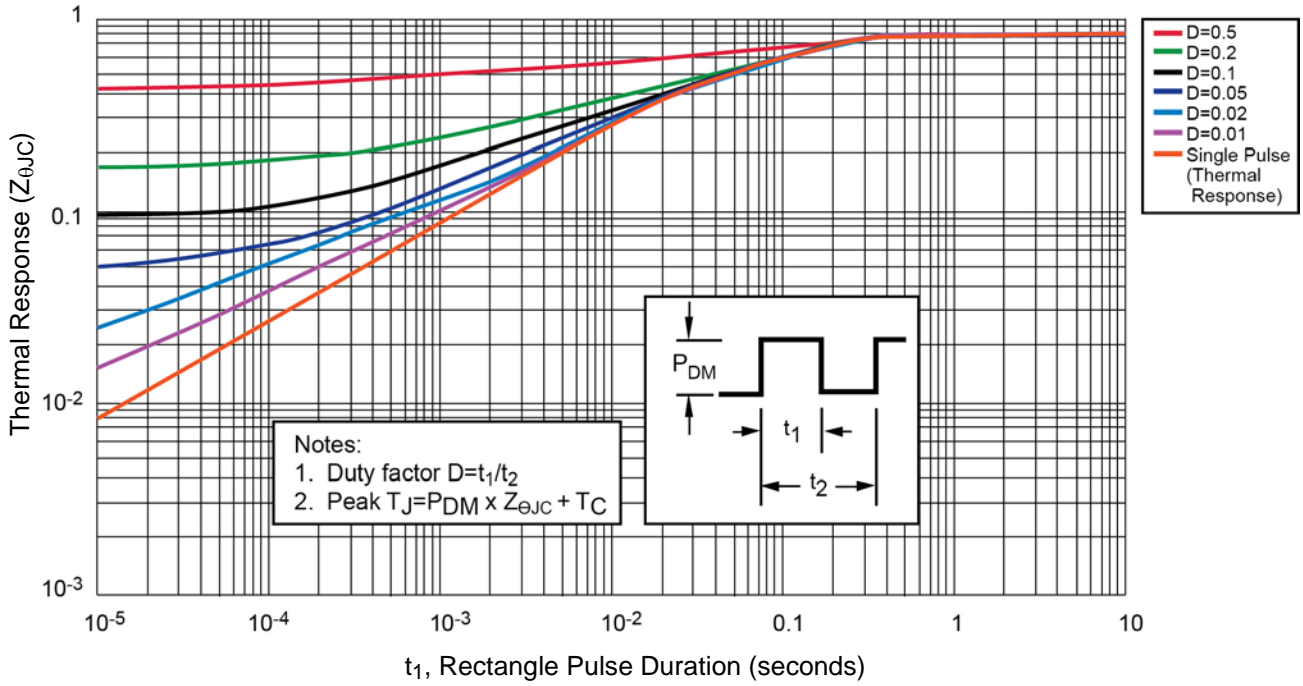
Parameters / Test Conditions	Symbol	Min.	Max.	Unit
<b>OFF CHARACTERISTICS</b>				
Drain-Source Breakdown Voltage $V_{GS} = 0\text{ V}, I_D = 1.0\text{ mA}$	2N7224 2N7225 2N7227 2N7228 $V_{(BR)DSS}$	100 200 400 500		V
Gate-Source Voltage (Threshold) $V_{DS} \geq V_{GS}, I_D = 0.25\text{ mA}$ $V_{DS} \geq V_{GS}, I_D = 0.25\text{ mA}, T_J = +125^\circ\text{C}$ $V_{DS} \geq V_{GS}, I_D = 0.25\text{ mA}, T_J = -55^\circ\text{C}$	$V_{GS(th)1}$ $V_{GS(th)2}$ $V_{GS(th)3}$	2.0 1.0	4.0 5.0	V
Gate Current $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}, T_J = +125^\circ\text{C}$	$I_{GSS1}$ $I_{GSS2}$		$\pm 100$ $\pm 200$	nA
Drain Current $V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$ $V_{GS} = 0\text{ V}, V_{DS} = 160\text{ V}$ $V_{GS} = 0\text{ V}, V_{DS} = 320\text{ V}$ $V_{GS} = 0\text{ V}, V_{DS} = 400\text{ V}$	2N7224 2N7225 2N7227 2N7228 $I_{DSS1}$		25	$\mu\text{A}$
Drain Current $V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}, T_J = +125^\circ\text{C}$ $V_{GS} = 0\text{ V}, V_{DS} = 160\text{ V}, T_J = +125^\circ\text{C}$ $V_{GS} = 0\text{ V}, V_{DS} = 320\text{ V}, T_J = +125^\circ\text{C}$ $V_{GS} = 0\text{ V}, V_{DS} = 400\text{ V}, T_J = +125^\circ\text{C}$	2N7224 2N7225 2N7227 2N7228 $I_{DSS2}$		0.25	mA
Static Drain-Source On-State Resistance $V_{GS} = 10\text{ V}, I_D = 21.0\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 17.0\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 9.0\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 8.0\text{ A pulsed}$	2N7224 2N7225 2N7227 2N7228 $r_{DS(on)1}$		0.070 0.100 0.315 0.415	$\Omega$
Static Drain-Source On-State Resistance $V_{GS} = 10\text{ V}, I_D = 34.0\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 27.4\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 14.0\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 12.0\text{ A pulsed}$	2N7224 2N7225 2N7227 2N7228 $r_{DS(on)2}$		0.081 0.105 0.415 0.515	$\Omega$
Static Drain-Source On-State Resistance $T_J = +125^\circ\text{C}$ $V_{GS} = 10\text{ V}, I_D = 21.0\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 17.0\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 9.0\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 8.0\text{ A pulsed}$	2N7224 2N7225 2N7227 2N7228 $r_{DS(on)3}$		0.11 0.17 0.68 0.90	$\Omega$
Diode Forward Voltage $V_{GS} = 0\text{ V}, I_D = 34.0\text{ A pulsed}$ $V_{GS} = 0\text{ V}, I_D = 27.4\text{ A pulsed}$ $V_{GS} = 0\text{ V}, I_D = 14.0\text{ A pulsed}$ $V_{GS} = 0\text{ V}, I_D = 12.0\text{ A pulsed}$	2N7224 2N7225 2N7227 2N7228 $V_{SD}$		1.8 1.9 1.7 1.7	V

**ELECTRICAL CHARACTERISTICS @  $T_A = +25\text{ }^\circ\text{C}$ , unless otherwise noted (continued)**
**DYNAMIC CHARACTERISTICS**

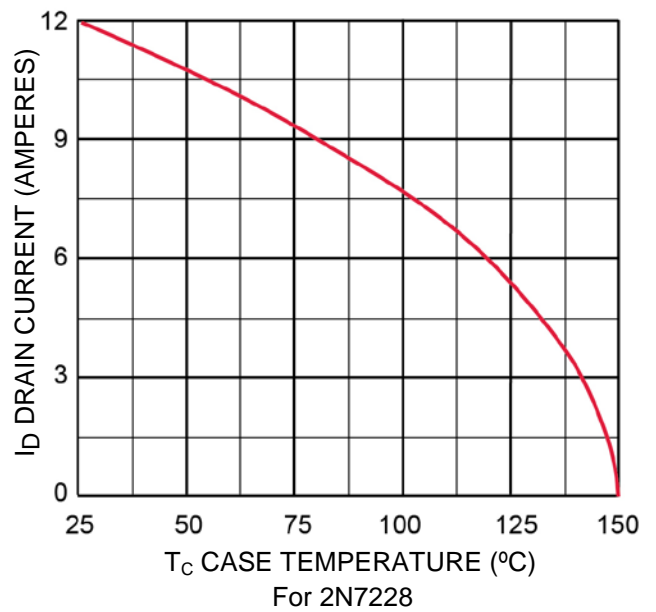
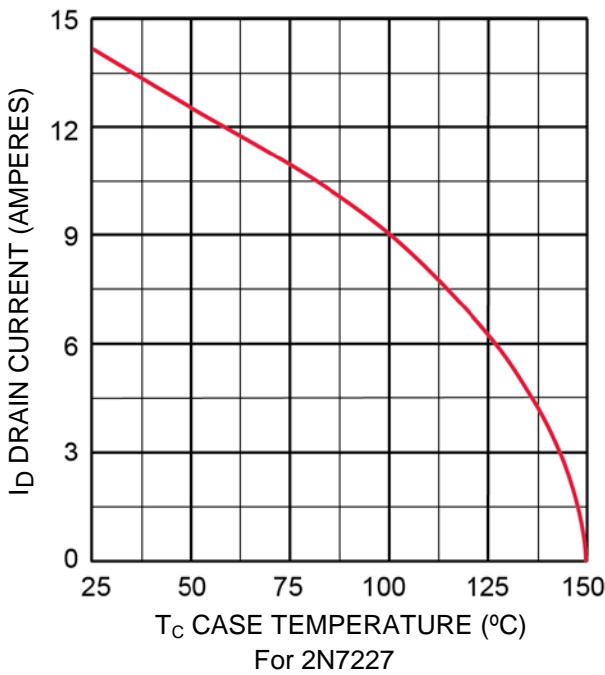
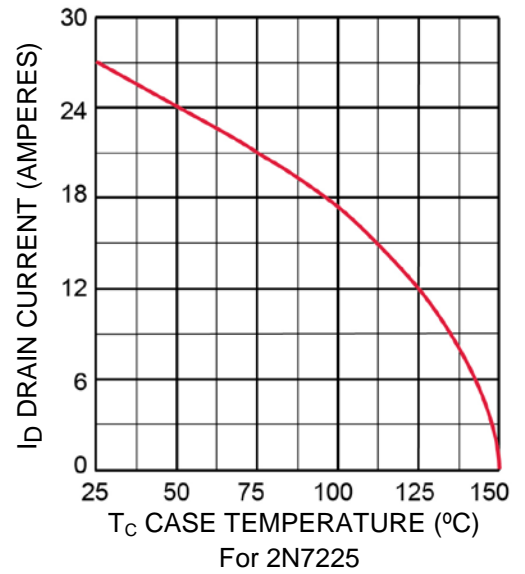
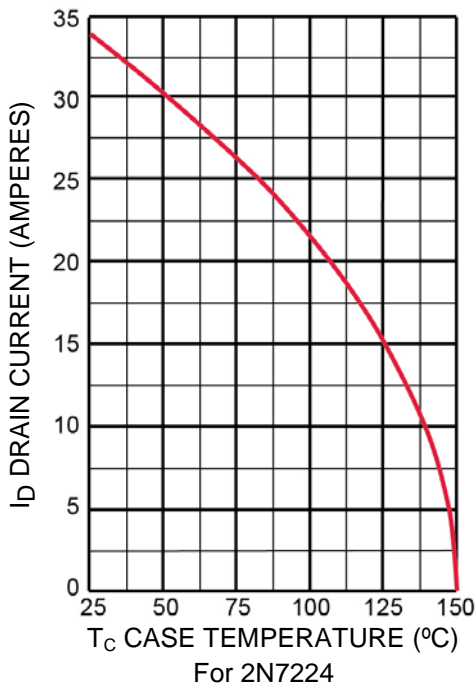
Parameters / Test Conditions	Symbol	Min.	Max.	Unit
<b>Gate Charge:</b>				
On-State Gate Charge				
$V_{GS} = 10\text{ V}, I_D = 34.0\text{ A}, V_{DS} = 50\text{ V}$ 2N7224	$Q_{g(on)}$		125	nC
$V_{GS} = 10\text{ V}, I_D = 27.4\text{ A}, V_{DS} = 50\text{ V}$ 2N7225		115		
$V_{GS} = 10\text{ V}, I_D = 14.0\text{ A}, V_{DS} = 50\text{ V}$ 2N7227		110		
$V_{GS} = 10\text{ V}, I_D = 12.0\text{ A}, V_{DS} = 50\text{ V}$ 2N7228		120		
Gate to Source Charge				
$V_{GS} = 10\text{ V}, I_D = 34.0\text{ A}, V_{DS} = 50\text{ V}$ 2N7224	$Q_{gs}$		22	nC
$V_{GS} = 10\text{ V}, I_D = 27.4\text{ A}, V_{DS} = 50\text{ V}$ 2N7225		22		
$V_{GS} = 10\text{ V}, I_D = 14.0\text{ A}, V_{DS} = 50\text{ V}$ 2N7227		18		
$V_{GS} = 10\text{ V}, I_D = 12.0\text{ A}, V_{DS} = 50\text{ V}$ 2N7228		19		
Gate to Drain Charge				
$V_{GS} = 10\text{ V}, I_D = 34.0\text{ A}, V_{DS} = 50\text{ V}$ 2N7224	$Q_{gd}$		65	nC
$V_{GS} = 10\text{ V}, I_D = 27.4\text{ A}, V_{DS} = 50\text{ V}$ 2N7225		60		
$V_{GS} = 10\text{ V}, I_D = 14.0\text{ A}, V_{DS} = 50\text{ V}$ 2N7227		65		
$V_{GS} = 10\text{ V}, I_D = 12.0\text{ A}, V_{DS} = 50\text{ V}$ 2N7228		70		

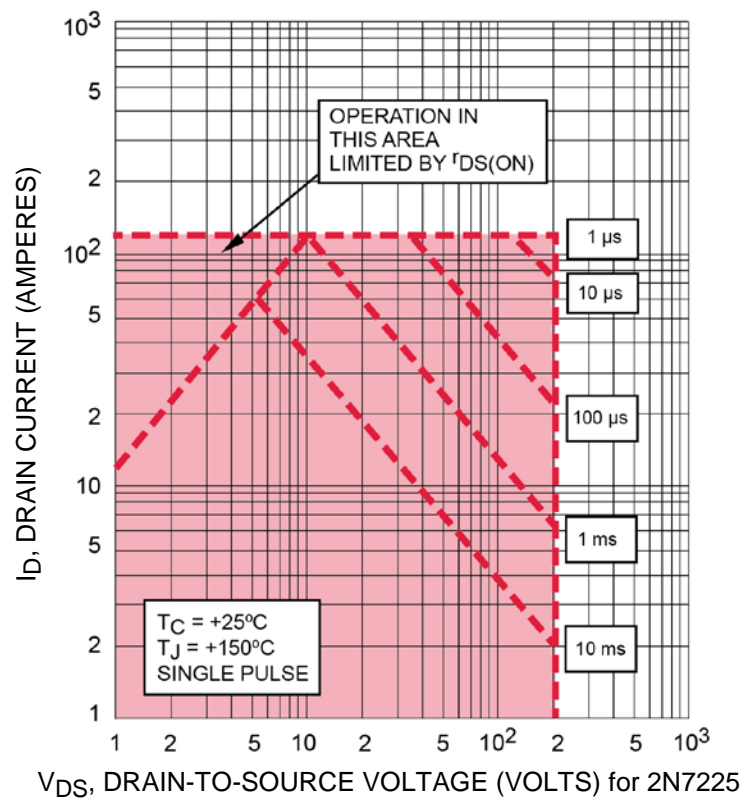
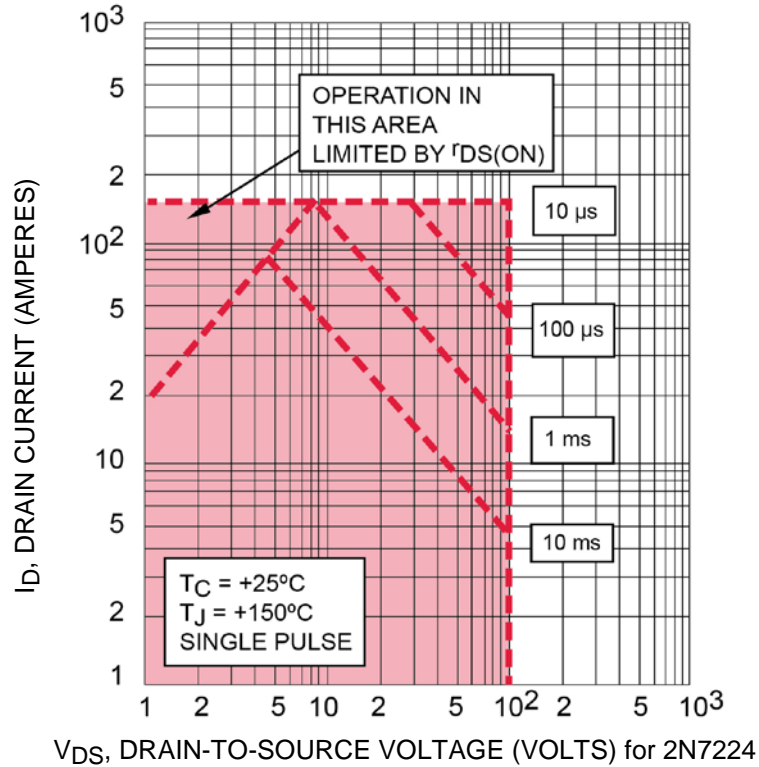
**SWITCHING CHARACTERISTICS**

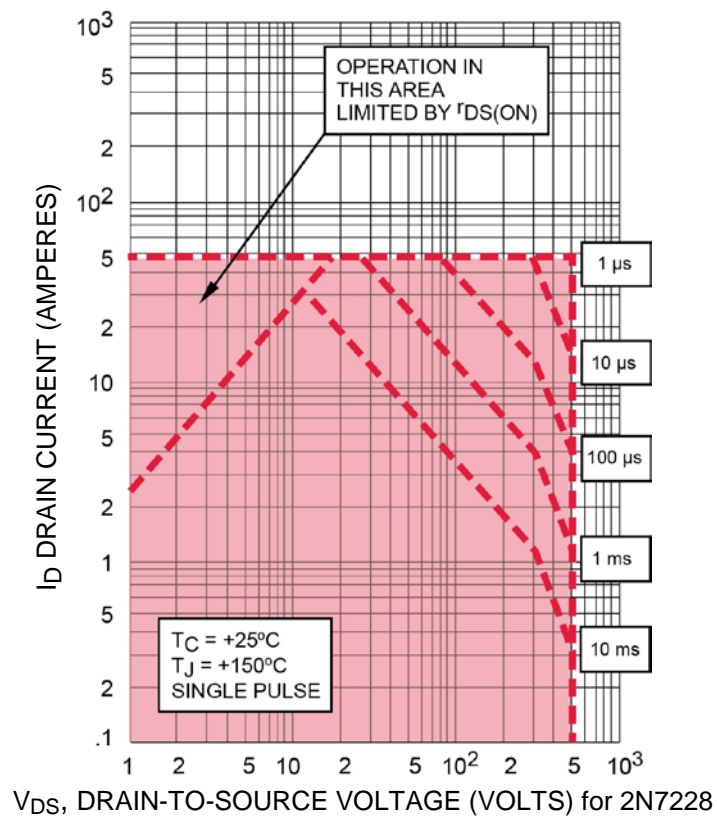
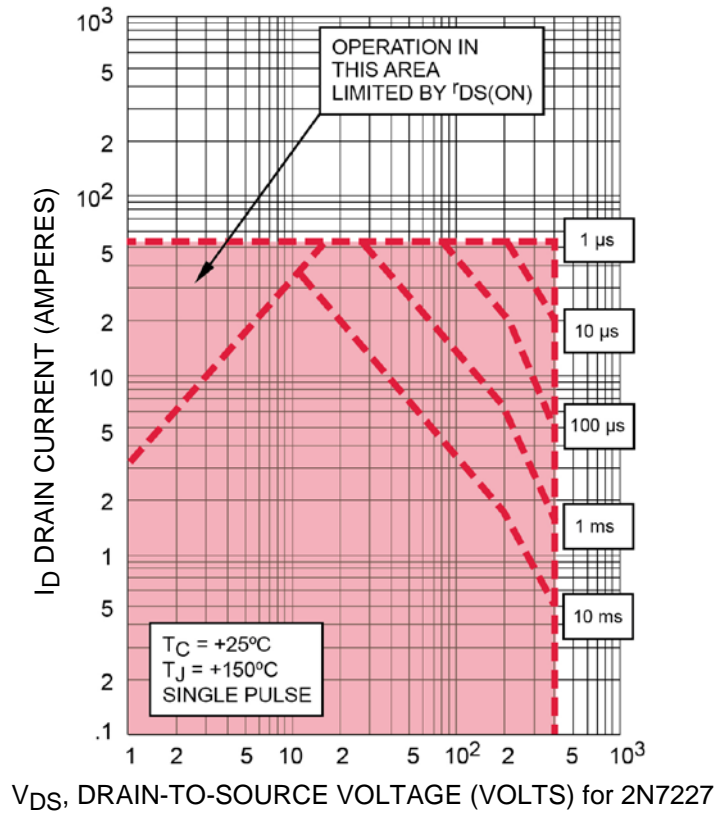
Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Turn-on delay time				
$I_D = 34.0\text{ A}, V_{GS} = 10\text{ V}, R_G = 2.35\ \Omega, V_{DD} = 50\text{ V}$ 2N7224	$t_{d(on)}$		35	ns
$I_D = 27.4\text{ A}, V_{GS} = 10\text{ V}, R_G = 2.35\ \Omega, V_{DD} = 100\text{ V}$ 2N7225				
$I_D = 14.0\text{ A}, V_{GS} = 10\text{ V}, R_G = 2.35\ \Omega, V_{DD} = 200\text{ V}$ 2N7227				
$I_D = 12.0\text{ A}, V_{GS} = 10\text{ V}, R_G = 2.35\ \Omega, V_{DD} = 250\text{ V}$ 2N7228				
Rinse time				
$I_D = 34.0\text{ A}, V_{GS} = 10\text{ V}, R_G = 2.35\ \Omega, V_{DD} = 50\text{ V}$ 2N7224	$t_r$		190	ns
$I_D = 27.4\text{ A}, V_{GS} = 10\text{ V}, R_G = 2.35\ \Omega, V_{DD} = 100\text{ V}$ 2N7225				
$I_D = 14.0\text{ A}, V_{GS} = 10\text{ V}, R_G = 2.35\ \Omega, V_{DD} = 200\text{ V}$ 2N7227				
$I_D = 12.0\text{ A}, V_{GS} = 10\text{ V}, R_G = 2.35\ \Omega, V_{DD} = 250\text{ V}$ 2N7228				
Turn-off delay time				
$I_D = 34.0\text{ A}, V_{GS} = 10\text{ V}, R_G = 2.35\ \Omega, V_{DD} = 50\text{ V}$ 2N7224	$t_{d(off)}$		170	ns
$I_D = 27.4\text{ A}, V_{GS} = 10\text{ V}, R_G = 2.35\ \Omega, V_{DD} = 100\text{ V}$ 2N7225				
$I_D = 14.0\text{ A}, V_{GS} = 10\text{ V}, R_G = 2.35\ \Omega, V_{DD} = 200\text{ V}$ 2N7227				
$I_D = 12.0\text{ A}, V_{GS} = 10\text{ V}, R_G = 2.35\ \Omega, V_{DD} = 250\text{ V}$ 2N7228				
Fall time				
$I_D = 34.0\text{ A}, V_{GS} = 10\text{ V}, R_G = 2.35\ \Omega, V_{DD} = 50\text{ V}$ 2N7224	$t_f$		130	ns
$I_D = 27.4\text{ A}, V_{GS} = 10\text{ V}, R_G = 2.35\ \Omega, V_{DD} = 100\text{ V}$ 2N7225				
$I_D = 14.0\text{ A}, V_{GS} = 10\text{ V}, R_G = 2.35\ \Omega, V_{DD} = 200\text{ V}$ 2N7227				
$I_D = 12.0\text{ A}, V_{GS} = 10\text{ V}, R_G = 2.35\ \Omega, V_{DD} = 250\text{ V}$ 2N7228				
Diode Reverse Recovery Time				
$di/dt \leq 100\text{ A}/\mu\text{s}, V_{DD} \leq 30\text{ V}, I_F = 34.0\text{ A}$ 2N7224	$t_{rr}$		500	ns
$di/dt \leq 100\text{ A}/\mu\text{s}, V_{DD} \leq 30\text{ V}, I_F = 27.4\text{ A}$ 2N7225		950		
$di/dt \leq 100\text{ A}/\mu\text{s}, V_{DD} \leq 30\text{ V}, I_F = 14.0\text{ A}$ 2N7227		1200		
$di/dt \leq 100\text{ A}/\mu\text{s}, V_{DD} \leq 30\text{ V}, I_F = 12.0\text{ A}$ 2N7228		1600		

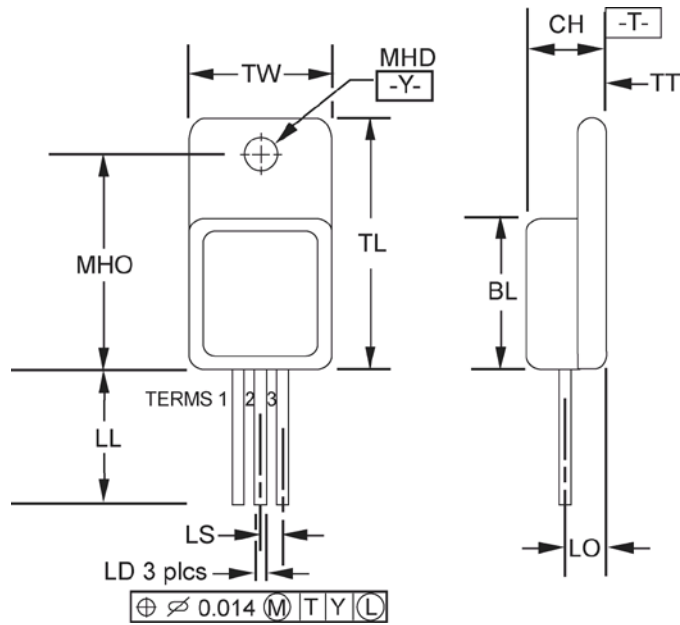
**GRAPHS**


**FIGURE 1**  
Thermal Impedance Curves

**GRAPHS (continued)**
**FIGURE 2 – Maximum Drain Current vs Case Temperature Graphs**


**GRAPHS (continued)**
**FIGURE 3 – Maximum Safe Operating Area**


**GRAPHS (continued)**


**PACKAGE DIMENSIONS**

**NOTES:**

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Glass meniscus included in dimension D and E.
4. All terminals are isolated from case.
5. In accordance with ASME Y14.5M, diameters are equivalent to  $\Phi$ x symbology.

Ltr	Dimensions				Notes
	Inch		Millimeters		
	Min	Max	Min	Max	
<b>BL</b>	.535	.545	13.59	13.84	
<b>CH</b>	.249	.260	6.32	6.60	
<b>LD</b>	.035	.045	0.89	1.14	
<b>LL</b>	.510	.570	12.95	14.48	
<b>LO</b>	.150 BSC		3.81 BSC		
<b>LS</b>	.150 BSC		3.81 BSC		
<b>MHD</b>	.139	.149	3.53	3.78	
<b>MHO</b>	.665	.685	16.89	17.40	
<b>TL</b>	.790	.800	20.07	20.32	3, 4
<b>TT</b>	.040	.050	1.02	1.27	
<b>TW</b>	.535	.545	13.59	13.84	3, 4
<b>Term 1</b>	Drain				
<b>Term 2</b>	Source				
<b>Term 3</b>	Gate				