

# 256-Kbit (32K × 8) Serial (SPI) nvSRAM

## Features

- 256-Kbit nonvolatile static random access memory (nvSRAM)
  - Internally organized as 32K × 8
  - STORE to QuantumTrap nonvolatile elements initiated automatically on power-down (AutoStore) or by user using HSB pin (Hardware STORE) or SPI instruction (Software STORE)
  - RECALL to SRAM initiated on power-up (Power-Up RECALL) or by SPI instruction (Software RECALL)
  - Automatic STORE on power-down with a small capacitor (except for CY14B256Q1)
- High reliability
  - Infinite read, write, and RECALL cycles
  - 1 million STORE cycles to QuantumTrap
  - Data retention: 20 years
- High-speed serial peripheral interface (SPI)
  - 40-MHz clock rate
  - Supports SPI mode 0 (0, 0) and mode 3 (1, 1)
- Write protection
  - Hardware protection using Write Protect ( $\overline{WP}$ ) pin
  - Software protection using Write Disable instruction
  - Software block protection for 1/4, 1/2, or entire array
- Low power consumption
  - Single 3 V +20%, -10% operation
  - Average active current of 10 mA at 40-MHz operation

## Industry standard configurations

- Industrial temperature
- CY14B256Q1 has identical pin configuration to industry standard 8-pin NV memory
- 8-pin dual flat no-lead (DFN) package and 16-pin small outline integrated circuit (SOIC) package
- Restriction of hazardous substances (RoHS) compliant

## Functional Description

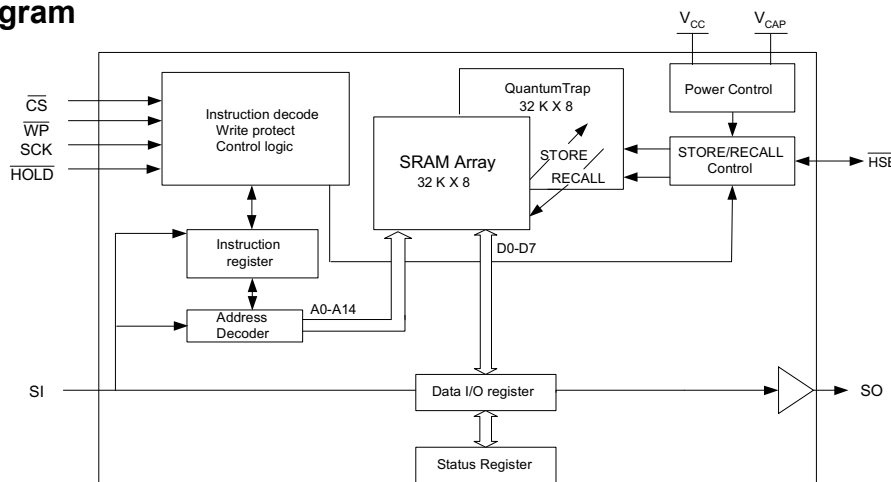
The Cypress CY14B256Q1/CY14B256Q2/CY14B256Q3 combines a 256-Kbit nvSRAM<sup>[1]</sup> with a nonvolatile element in each memory cell with serial SPI interface. The memory is organized as 32K words of 8 bits each. The embedded nonvolatile elements incorporate the QuantumTrap technology, creating the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, while the QuantumTrap cell provides highly reliable nonvolatile storage of data. Data transfers from SRAM to the nonvolatile elements (STORE operation) takes place automatically at power-down (except for CY14B256Q1). On power-up, data is restored to the SRAM from the nonvolatile memory (RECALL operation). The STORE and RECALL operations can also be initiated by the user through SPI instruction.

For a complete list of related documentation, click [here](#).

## Configuration

Feature	CY14B256Q1	CY14B256Q2	CY14B256Q3
AutoStore	No	Yes	Yes
Software STORE	Yes	Yes	Yes
Hardware STORE	No	No	Yes

## Logic Block Diagram



### Note

1. This device will be referred to as nvSRAM throughout the document.

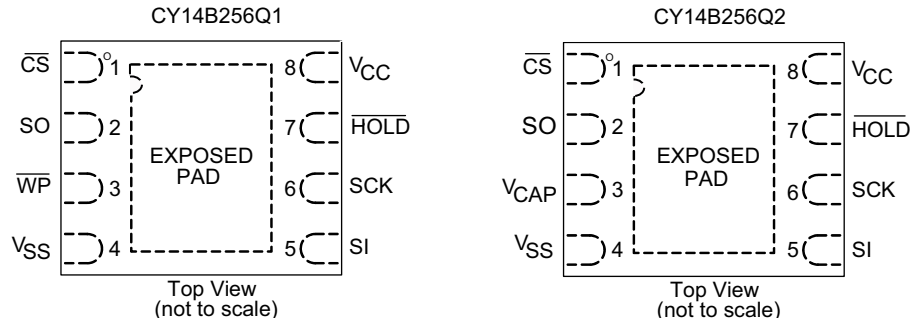


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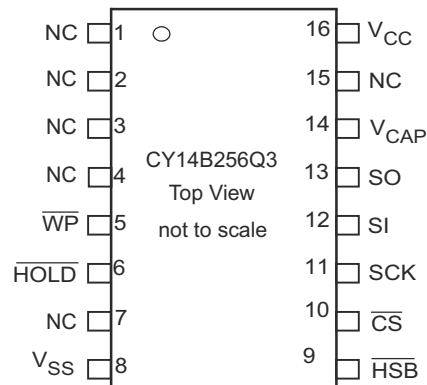
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## Pinouts

**Figure 1. 8-pin DFN pinout** [2, 3, 4]



**Figure 2. 16-pin SOIC pinout**



### Notes

2. HSB pin is not available in 8-pin DFN packages.
3. CY14B256Q1 part does not have V<sub>CAP</sub> pin and does not support AutoStore.
4. CY14B256Q2 part does not have WP pin.



## Pin Definitions

Pin Name	I/O Type	Description
$\overline{\text{CS}}$	Input	<b>Chip select.</b> Activates the device when pulled LOW. Driving this pin HIGH puts the device in low-power standby mode.
SCK	Input	<b>Serial clock.</b> Runs at speeds up to maximum of $f_{\text{SCK}}$ . Serial input is latched at the rising edge of this clock. Serial output is driven at the falling edge of the clock.
SI	Input	<b>Serial input.</b> Pin for input of all SPI instructions and data.
SO	Output	<b>Serial output.</b> Pin for output of data through SPI.
$\overline{\text{WP}}$	Input	<b>Write protect.</b> Implements hardware write protection in SPI.
$\overline{\text{HOLD}}$	Input	<b>HOLD pin.</b> Suspends serial operation.
HSB	Input/output	<b>Hardware STORE busy:</b> Output: Indicates busy status of nvSRAM when LOW. After each hardware and software STORE operation HSB is driven HIGH for a short time ( $t_{\text{HHHD}}$ ) with standard output high current and then a weak internal pull-up resistor keeps this pin HIGH (external pull-up resistor connection optional). Input: Hardware STORE implemented by pulling this pin LOW externally.
$V_{\text{CAP}}$	Power supply	<b>AutoStore capacitor.</b> Supplies power to the nvSRAM during power loss to STORE data from the SRAM to nonvolatile elements. If AutoStore is not needed, this pin must be left as No Connect. It must never be connected to ground.
NC	No connect	<b>No connect:</b> This pin is not connected to the die.
$V_{\text{SS}}$	Power supply	Ground.
$V_{\text{CC}}$	Power supply	Power supply (2.7 V to 3.6 V).
EXPOSED PAD	No connect	The exposed pad on the bottom of 8-pin DFN package is not connected to the die. It is recommended to connect the exposed pad to $V_{\text{SS}}$ . Thermal vias can be used to increase thermal conductivity.



## Device Operation

CY14B256Q1/CY14B256Q2/CY14B256Q3 is a 256-Kbit nvSRAM memory with a nonvolatile element in each memory cell. All the reads and writes to nvSRAM happen to the SRAM which gives nvSRAM the unique capability to handle infinite writes to the memory. The data in SRAM is secured by a STORE sequence that transfers the data in parallel to the nonvolatile QuantumTrap cells. A small capacitor ( $V_{CAP}$ ) is used to AutoStore the SRAM data in nonvolatile cells when power goes down providing power-down data security. The QuantumTrap nonvolatile elements built in the reliable SONOS technology make nvSRAM the ideal choice for secure data storage.

The 256-Kbit memory array is organized as 32K words  $\times$  8 bits. The memory is accessed through a standard SPI interface that enables very high clock speeds up to 40 MHz with zero cycle delay read and write cycles. This device supports SPI modes 0 and 3 (CPOL, CPHA = 0, 0 and 1, 1) and operates as SPI slave. The device is enabled using the chip select ( $\overline{CS}$ ) pin and accessed through serial input (SI), serial output (SO), and serial clock (SCK) pins.

This device provides the feature for hardware and software write protection through the  $\overline{WP}$  pin and WRDI instruction respectively along with mechanisms for block write protection (one quarter, one half, or full array) using BP0 and BP1 pins in the Status Register. Further, the HOLD pin is used to suspend any serial communication without resetting the serial sequence.

CY14B256Q1/CY14B256Q2/CY14B256Q3 uses the standard SPI opcodes for memory access. In addition to the general SPI instructions for read and write, it provides four special instructions which enable access to four nvSRAM specific functions: STORE, RECALL, AutoStore Disable (ASDISB), and AutoStore Enable (ASENB).

The major benefit of nvSRAM over serial EEPROMs is that all reads and writes to nvSRAM are performed at the speed of SPI bus with zero cycle delay. Therefore, no wait time is required after any of the memory accesses. The STORE and RECALL operations need finite time to complete and all memory accesses are inhibited during this time. While a STORE or RECALL operation is in progress, the busy status of the device is indicated by the Hardware STORE Busy (HSB) pin and also reflected on the RDY bit of the Status Register.

The device is available in three different pin configurations that enable the user to choose a part which fits in best in their application. The feature summary is given in [Table 1](#).

**Table 1. Feature Summary**

Feature	CY14B256Q1	CY14B256Q2	CY14B256Q3
$\overline{WP}$	Yes	No	Yes

**Table 1. Feature Summary (continued)**

Feature	CY14B256Q1	CY14B256Q2	CY14B256Q3
$V_{CAP}$	No	Yes	Yes
HSB	No	No	Yes
AutoStore	No	Yes	Yes
Power-Up RECALL	Yes	Yes	Yes
Hardware STORE	No	No	Yes
Software STORE	Yes	Yes	Yes
Software RECALL	Yes	Yes	Yes

### SRAM Write

All writes to nvSRAM are carried out on the SRAM and do not use up any endurance cycles of the nonvolatile memory. This enables user to perform infinite write operations. A write cycle is performed through the WRITE instruction. The WRITE instruction is issued through the SI pin of the nvSRAM and consists of the WRITE opcode, two bytes of address, and one byte of data. Write to nvSRAM is done at SPI bus speed with zero cycle delay.

The device allows burst mode writes to be performed through SPI. This enables write operations on consecutive addresses without issuing a new WRITE instruction. When the last address in memory is reached in burst mode, the address rolls over to 0x0000 and the device continues to write.

The SPI write cycle sequence is defined in the section [Memory Access on page 13](#) of SPI Protocol Description.

### SRAM Read

A read cycle is performed at the SPI bus speed and the data is read out with zero cycle delay after the READ instruction is executed. The READ instruction is issued through the SI pin of the nvSRAM and consists of the READ opcode and two bytes of address. The data is read out on the SO pin.

This device allows burst mode reads to be performed through SPI. This enables reads on consecutive addresses without issuing a new READ instruction. When the last address in memory is reached in burst mode read, the address rolls over to 0x0000 and the device continues to read.

The SPI read cycle sequence is defined explicitly in the section [Memory Access on page 13](#) of SPI Protocol Description.

## STORE Operation

STORE operation transfers the data from the SRAM to the nonvolatile QuantumTrap cells. The device STOREs data to the nonvolatile cells using one of the three STORE operations: AutoStore, activated on device power-down; Software STORE, activated by a `STORE` instruction; and Hardware STORE, activated by the `HSB`. During the STORE cycle, an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. After a STORE cycle is initiated, `read/write` to CY14B256Q1/CY14B256Q2/CY14B256Q3 is inhibited until the cycle is completed.

The `HSB` signal or the `RDY` bit in the Status Register can be monitored by the system to detect if a STORE or Software RECALL cycle is in progress. The busy status of nvSRAM is indicated by `HSB` being pulled LOW or `RDY` bit being set to '1'. To avoid unnecessary nonvolatile STOREs, AutoStore and Hardware STORE operations are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle. However, software initiated STORE cycles are performed regardless of whether a write operation has taken place.

### AutoStore Operation

The AutoStore operation is a unique feature of nvSRAM which automatically stores the SRAM data to QuantumTrap cells during power-down. This STORE makes use of an external capacitor ( $V_{CAP}$ ) and enables the device to safely STORE the data in the nonvolatile memory when power goes down.

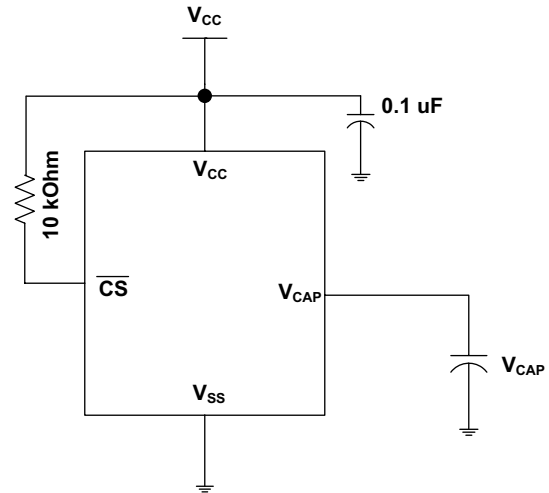
During normal operation, the device draws current from  $V_{CC}$  to charge the capacitor connected to the  $V_{CAP}$  pin. When the voltage on the  $V_{CC}$  pin drops below  $V_{SWITCH}$  during power-down, the device inhibits all memory accesses to nvSRAM and automatically performs a conditional STORE operation using the charge from the  $V_{CAP}$  capacitor. The AutoStore operation is not initiated if no write cycle has been performed since the last RECALL.

**Note** If a capacitor is not connected to  $V_{CAP}$  pin, AutoStore must be disabled by issuing the AutoStore Disable instruction specified in [AutoStore Enable \(ASENB\) instruction on page 15](#). If AutoStore is enabled without a capacitor on the  $V_{CAP}$  pin, the device attempts an AutoStore operation without sufficient charge to complete the STORE. This corrupts the data stored in the nvSRAM and Status Register. To resume normal functionality, the `WRSR` instruction must be issued to update the nonvolatile bits `BP0`, `BP1` and `WPEN` in the Status Register.

Figure 3 shows the proper connection of the storage capacitor ( $V_{CAP}$ ) for AutoStore operation. Refer to [DC Electrical Characteristics on page 17](#) for the size of the  $V_{CAP}$ .

**Note** CY14B256Q1 does not support AutoStore operation. The user must perform Software STORE operation by using the SPI STORE instruction to secure the data.

Figure 3. AutoStore Mode



### Software STORE Operation

Software STORE enables the user to trigger a STORE operation through a special SPI instruction. STORE operation is initiated by executing STORE instruction irrespective of whether a write has been performed since the last NV operation.

A STORE cycle takes  $t_{STORE}$  time to complete, during which all the memory accesses to nvSRAM are inhibited. The `RDY` bit of the Status Register or the `HSB` pin may be polled to find the ready or busy status of the nvSRAM. After the  $t_{STORE}$  cycle time is completed, the SRAM is activated again for read and write operations.

### Hardware STORE and HSB Pin Operation

The `HSB` pin in CY14B256Q3 is used to control and acknowledge STORE operations. If no STORE or RECALL is in progress, this pin can be used to request a Hardware STORE cycle. When the `HSB` pin is driven LOW, nvSRAM conditionally initiates a STORE operation after  $t_{DELAY}$  duration. An actual STORE cycle starts only if a write to the SRAM is performed since the last STORE or RECALL cycle. Reads and writes to the memory are inhibited for  $t_{STORE}$  duration or as long as `HSB` pin is LOW.

The `HSB` pin also acts as an open drain driver (internal 100 kOhm weak pull-up resistor) that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

**Note** After each Hardware and Software STORE operation `HSB` is driven HIGH for a short time ( $t_{HHHD}$ ) with standard output high current and then remains HIGH by an internal 100 kOhm pull-up resistor.

**Note** For successful last data byte STORE, a hardware store should be initiated at least one clock cycle after the last data bit `D0` is received.

Upon completion of the STORE operation, the nvSRAM memory access is inhibited for  $t_{LZHSB}$  time after `HSB` pin returns HIGH. The `HSB` pin must be left unconnected if not used.

**Note** CY14B256Q1/CY14B256Q2 do not have  $\overline{\text{HSB}}$  pin.  $\overline{\text{RDY}}$  bit of the SPI Status Register may be probed to determine the ready or busy status of nvSRAM.

### RECALL Operation

A RECALL operation transfers the data stored in the nonvolatile QuantumTrap elements to the SRAM. A RECALL may be initiated in two ways: Hardware RECALL, initiated on power-up; and Software RECALL, initiated by a SPI RECALL instruction.

Internally, RECALL is a two step procedure. First, the SRAM data is cleared. Next, the nonvolatile information is transferred into the SRAM cells. All memory accesses are inhibited while a RECALL cycle is in progress. The RECALL operation does not alter the data in the nonvolatile elements.

### Hardware RECALL (Power-Up)

During power-up, when  $V_{CC}$  crosses  $V_{SWITCH}$ , an automatic RECALL sequence is initiated, which transfers the content of nonvolatile memory on to the SRAM. The data would previously have been stored on the nonvolatile memory through a STORE sequence.

A Power-Up RECALL cycle takes  $t_{FA}$  time to complete and the memory access is disabled during this time. HSB pin is used to detect the ready status of the device.

### Software RECALL

Software RECALL enables the user to initiate a RECALL operation to restore the content of nonvolatile memory on to the SRAM. A Software RECALL is issued by using the SPI instruction for RECALL.

A Software RECALL takes  $t_{RECALL}$  time to complete during which all memory accesses to nvSRAM are inhibited. The controller must provide sufficient delay for the RECALL operation to complete before issuing any memory access instructions.

### Disabling and Enabling AutoStore

If the application does not require the AutoStore feature, it can be disabled by using the ASDISB instruction. If this is done, the nvSRAM does not perform a STORE operation at power-down.

AutoStore can be re-enabled by using the ASENB instruction. However, these operations are not nonvolatile and if the user needs this setting to survive the power cycle, a STORE operation must be performed following AutoStore Disable or Enable operation.

**Note** CY14B256Q2/CY14B256Q3 comes from the factory with AutoStore enabled and CY14B256Q1/CY14B256Q2/CY14B256Q3 comes from the factory with 0x00 written in all cells. In CY14B256Q1,  $V_{CAP}$  pin is not present and AutoStore option is not available. The

AutoStore Enable and Disable instructions to CY14B256Q1 are ignored.

**Note** If AutoStore is disabled and  $V_{CAP}$  is not required, then the  $V_{CAP}$  pin must be left open. The  $V_{CAP}$  pin must never be connected to ground. The Power-Up RECALL operation cannot be disabled in any case.

## Serial Peripheral Interface

### SPI Overview

The SPI is a four-pin interface with chip select ( $\overline{\text{CS}}$ ), serial input (SI), serial output (SO), and serial clock (SCK) pins. CY14B256Q1/CY14B256Q2/CY14B256Q3 provides serial access to nvSRAM through SPI interface. The SPI bus on this device can run at speeds up to 40 MHz.

The SPI is a synchronous serial interface which uses clock and data pins for memory access and supports multiple devices on the data bus. A device on SPI bus is activated using the  $\overline{\text{CS}}$  pin.

The relationship between chip select, clock, and data is dictated by the SPI mode. This device supports SPI modes 0 and 3. In both these modes, data is clocked into the nvSRAM on the rising edge of SCK starting from the first rising edge after  $\overline{\text{CS}}$  goes active.

The SPI protocol is controlled by opcodes. These opcodes specify the commands from the bus master to the slave device. After  $\overline{\text{CS}}$  is activated the first byte transferred from the bus master is the opcode. Following the opcode, any addresses and data are then transferred. The  $\overline{\text{CS}}$  must go inactive after an operation is complete and before a new opcode can be issued. The commonly used terms used in SPI protocol are as follows:

#### SPI Master

The SPI master device controls the operations on a SPI bus. A SPI bus may have only one master with one or more slave devices. All the slaves share the same SPI bus lines and the master may select any of the slave devices using the  $\overline{\text{CS}}$  pin. All the operations must be initiated by the master activating a slave device by pulling the  $\overline{\text{CS}}$  pin of the slave LOW. The master also generates the SCK and all the data transmission on SI and SO lines are synchronized with this clock.

#### SPI Slave

The SPI slave device is activated by the master through the chip select line. A slave device gets the SCK as an input from the SPI master and all the communication is synchronized with this clock. SPI slave never initiates a communication on the SPI bus and acts on the instruction from the master.

CY14B256Q1/CY14B256Q2/CY14B256Q3 operates as a SPI

### Chip Select ( $\overline{CS}$ )

For selecting any slave device, the master needs to pull-down the corresponding  $\overline{CS}$  pin. Any instruction can be issued to a slave device only while the  $\overline{CS}$  pin is LOW. When the device is not selected, data through the SI pin is ignored and the serial output pin (SO) remains in a high-impedance state.

**Note** A new instruction must begin with the falling edge of  $\overline{CS}$ . Therefore, only one opcode can be issued for each active chip select cycle.

### Serial Clock (SCK)

Serial clock is generated by the SPI master and the communication is synchronized with this clock after  $\overline{CS}$  goes LOW.

CY14B256Q1/CY14B256Q2/CY14B256Q3 enables SPI modes 0 and 3 for data communication. In both these modes, the inputs are latched by the slave device on the rising edge of SCK and outputs are issued on the falling edge. Therefore, the first rising edge of SCK signifies the arrival of the first bit (MSB) of SPI instruction on the SI pin. Further, all data inputs and outputs are synchronized with SCK.

### Data Transmission - SI and SO

SPI data bus consists of two lines, SI and SO, for serial data communication. The SI is also referred to as Master Out Slave In (MOSI) and SO is referred to as Master In Slave Out (MISO). The master issues instructions to the slave through the SI pin, while the slave responds through the SO pin. Multiple slave devices may share the SI and SO lines as described earlier.

CY14B256Q1/CY14B256Q2/CY14B256Q3 has two separate pins for SI and SO, which can be connected with the master as shown in Figure 4.

### Most Significant Bit (MSB)

The SPI protocol requires that the first bit to be transmitted is the most significant bit (MSB). This is valid for both address and data transmission.

The 256-Kbit serial nvSRAM requires a 2-byte address for any read or write operation. However, since the address is only 15-bits, it implies that the first MSB that is fed in is ignored by the device. Although this bit is 'don't care', Cypress recommends that this bit is treated as 0 to enable seamless transition to higher memory densities.

### Serial Opcode

After the slave device is selected with  $\overline{CS}$  going LOW, the first byte received is treated as the opcode for the intended operation. CY14B256Q1/CY14B256Q2/CY14B256Q3 uses the standard opcodes for memory accesses. In addition to the memory accesses, it provides additional opcodes for the nvSRAM specific functions: STORE, RECALL, AutoStore Enable, and AutoStore Disable. Refer to Table 2 on page 10 for details.

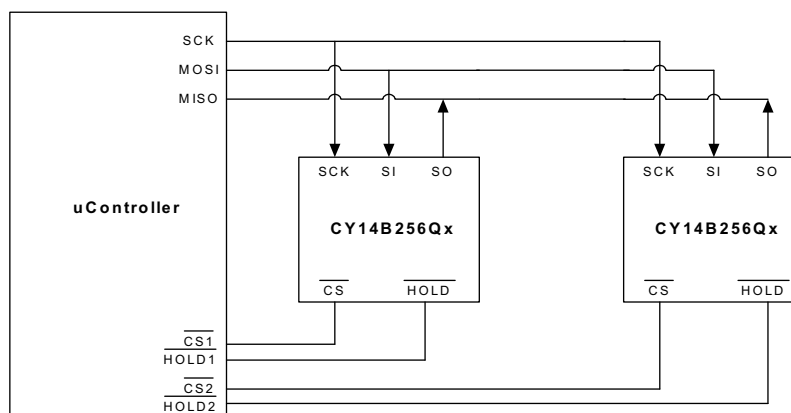
### Invalid Opcode

If an invalid opcode is received, the opcode is ignored and the device ignores any additional serial data on the SI pin till the next falling edge of  $\overline{CS}$  and the SO pin remains tristated.

### Status Register

CY14B256Q1/CY14B256Q2/CY14B256Q3 has an 8-bit Status Register. The bits in the Status Register are used to configure the SPI bus. These bits are described in the Table 4 on page 11.

Figure 4. System Configuration Using SPI nvSRAM





## SPI Modes

CY14B256Q1/CY14B256Q2/CY14B256Q3 may be driven by a microcontroller with its SPI peripheral running in either of the following two modes:

- SPI Mode 0 (CPOL = 0, CPHA = 0)
- SPI Mode 3 (CPOL = 1, CPHA = 1)

For both these modes, the input data is latched in on the rising edge of SCK starting from the first rising edge after CS goes active. If the clock starts from a HIGH state (in mode 3), the first rising edge after the clock toggles, is considered. The output data is available on the falling edge of SCK.

The two SPI modes are shown in Figure 5 and Figure 6. The status of clock when the bus master is in standby mode and not transferring data is:

- SCK remains at 0 for Mode 0
- SCK remains at 1 for Mode 3

CPOL and CPHA bits must be set in the SPI controller for the either Mode 0 or Mode 3. The device detects the SPI mode from the status of SCK pin when the device is selected by bringing the CS pin LOW. If SCK pin is LOW when the device is selected, SPI Mode 0 is assumed and if SCK pin is HIGH, it works in SPI Mode 3.

Figure 5. SPI Mode 0

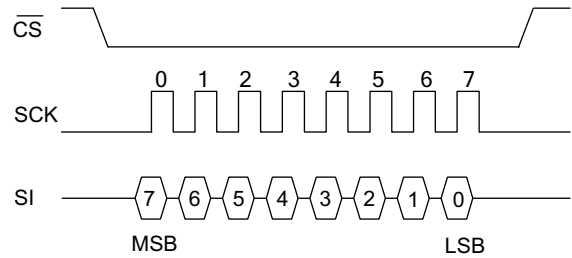
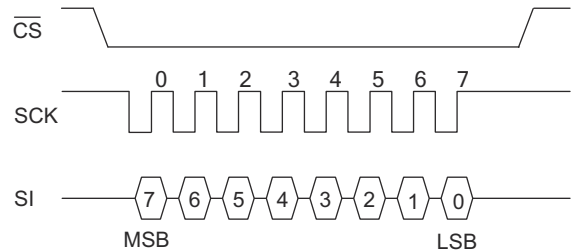


Figure 6. SPI Mode 3





## SPI Operating Features

### Power-Up

Power-up is defined as the condition when the power supply is turned on and  $V_{CC}$  crosses  $V_{switch}$  voltage. During this time, the  $\overline{CS}$  must be allowed to follow the  $V_{CC}$  voltage. Therefore,  $\overline{CS}$  must be connected to  $V_{CC}$  through a suitable pull-up resistor. As a built in safety feature,  $\overline{CS}$  is both edge sensitive and level sensitive. After power-up, the device is not selected until a falling edge is detected on  $\overline{CS}$ . This ensures that  $\overline{CS}$  must have been HIGH, before going LOW to start the first operation.

As described earlier, nvSRAM performs a Power-Up RECALL operation after power-up and therefore, all memory accesses are disabled for  $t_{FA}$  duration after power-up. The HSB pin can be probed to check the Ready or Busy status of nvSRAM after power-up.

### Power On Reset

A power on reset (POR) circuit is included to prevent inadvertent writes. At power-up, the device does not respond to any instruction until the  $V_{CC}$  reaches the POR threshold voltage ( $V_{SWITCH}$ ). After  $V_{CC}$  transitions the POR threshold, the device is internally reset and performs a Power-Up RECALL operation. During Power-Up RECALL all device accesses are inhibited. The device is in the following state after POR:

- Deselected (after power-up, a falling edge is required on  $\overline{CS}$  before any instructions are started).
- Standby power mode
- Not in the HOLD condition
- Status Register state:
  - Write Enable (WEN) bit is reset to '0'.
  - WPEN, BP1, BP0 unchanged from previous STORE operation
  - Don't care bits 4–6 are reset to '0'.

The WPEN, BP1, and BP0 bits of the Status Register are nonvolatile bits and remain unchanged from the previous STORE operation.

Before selecting and issuing instructions to the memory, a valid and stable  $V_{CC}$  voltage must be applied. This voltage must remain valid until the end of the instruction transmission.

### Power-Down

At power-down (continuous decay of  $V_{CC}$ ), when  $V_{CC}$  drops from the normal operating voltage and below the  $V_{SWITCH}$  threshold voltage, the device stops responding to any instruction sent to it. If a write cycle is in progress and the last data bit D0 has been received when the power goes down, it is allowed  $t_{DELAY}$  time to complete the write. After this, all memory accesses are inhibited and a conditional AutoStore operation is performed (AutoStore is not performed if no writes have happened since the last RECALL cycle). This feature prevents inadvertent writes to nvSRAM from happening during power-down.

However, to completely avoid the possibility of inadvertent writes during power-down, ensure that the device is deselected and is in standby power mode, and the  $\overline{CS}$  follows the voltage applied on  $V_{CC}$ .

## Active Power and Standby Power Modes

When  $\overline{CS}$  is LOW, the device is selected and is in the active power mode. The device consumes  $I_{CC}$  current, as specified in [DC Electrical Characteristics on page 17](#). When  $\overline{CS}$  is HIGH, the device is deselected and the device goes into the standby power mode if a STORE or RECALL cycle is not in progress. If a STORE or RECALL cycle is in progress, the device goes into the standby power mode after the STORE or RECALL cycle is completed. In the standby power mode, the current drawn by the device drops to  $I_{SB}$ .

## SPI Functional Description

The CY14B256Q1/CY14B256Q2/CY14B256Q3 uses an 8-bit instruction register. Instructions and their operation codes are listed in [Table 2](#). All instructions, addresses, and data are transferred with the MSB first and start with a HIGH to LOW  $\overline{CS}$  transition. There are, in all, 10 SPI instructions that provide access to most of the functions in nvSRAM. Further, the WP, HOLD and HSB pins provide additional functionality driven through hardware.

**Table 2. Instruction Set**

Instruction Category	Instruction Name	Opcode	Operation
Status Register control instructions	WREN	0000 0110	Set write enable latch
	WRDI	0000 0100	Reset write enable latch
	RDSR	0000 0101	Read Status Register
	WRSR	0000 0001	Write Status Register
SRAM Read/Write instructions	READ	0000 0011	Read data from memory array
	WRITE	0000 0010	Write data to memory array
Special NV instructions	STORE	0011 1100	Software STORE
	RECALL	0110 0000	Software RECALL
	ASENB	0101 1001	AutoStore Enable
	ASDISB	0001 1001	AutoStore Disable
Reserved	- Reserved -	0001 1110	

The SPI instructions are divided based on their functionality in the following types:

- Status Register access: RDSR and WRSR instructions
- Write protection functions: WREN and WRDI instructions along with WP pin and WEN, BP0, and BP1 bits
- SRAM memory access: READ and WRITE instructions
- nvSRAM special instructions: STORE, RECALL, ASENB, and ASDISB



## Status Register

The Status Register bits are listed in Table 3. The Status Register consists of a Ready bit (RDY) and data protection bits BP1, BP0, WEN, and WPEN. The RDY bit can be polled to check the Ready or Busy status while a nvSRAM STORE or Software RECALL cycle is in progress. The Status Register can be modified by

WRSR instruction and read by RDSR instruction. However, only the WPEN, BP1, and BP0 bits of the Status Register can be modified by using the WRSR instruction. The WRSR instruction has no effect on WEN and RDY bits. The default value shipped from the factory for WEN, BP0, BP1, bits 4–6 and WPEN bits is '0'.

**Table 3. Status Register Format**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN (0)	X (0)	X (0)	X (0)	BP1 (0)	BP0 (0)	WEN (0)	RDY

**Table 4. Status Register Bit Definition**

Bit	Definition	Description
Bit 0 (RDY)	Ready	Read only bit indicates the ready status of device to perform a memory access. This bit is set to '1' by the device while a STORE or Software RECALL cycle is in progress.
Bit 1 (WEN)	Write Enable	WEN indicates if the device is write enabled. This bit defaults to '0' (disabled) on power-up. WEN = '1' --> Write enabled WEN = '0' --> Write disabled
Bit 2 (BP0)	Block Protect bit '0'	Used for block protection. For details see Table 5 on page 13.
Bit 3 (BP1)	Block Protect bit '1'	Used for block protection. For details see Table 5 on page 13.
Bit 4-6	Don't care	Bits are writable and volatile. On power-up, bits are written with '0'.
Bit 7 (WPEN)	Write Protect Enable bit	Used for enabling the function of Write Protect Pin ( $\overline{WP}$ ). For details see Table 6 on page 13.

### Read Status Register (RDSR) Instruction

The Read Status Register (RDSR) instruction provides access to the status register. This instruction is used to probe the write enable status of the device or the Ready status of the device. RDY bit is set by the device to '1' whenever a STORE or Software RECALL cycle is in progress. The block protection and WPEN bits indicate the extent of protection employed.

This instruction is issued after the falling edge of  $\overline{CS}$  using the opcode for RDSR.

### Write Status Register (WRSR) Instruction

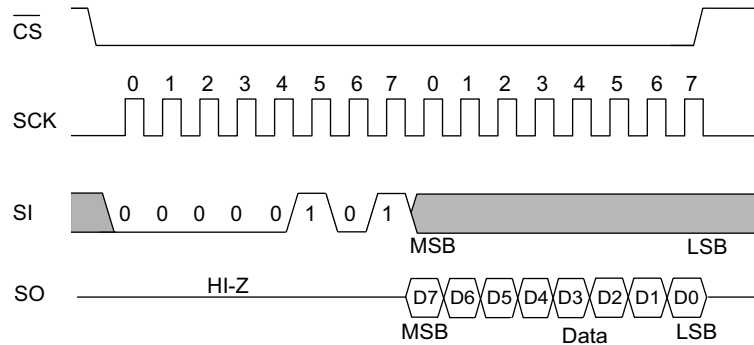
The WRSR instruction enables the user to write to the Status Register. However, this instruction cannot be used to modify bit 0 and bit 1 (RDY and WEN). The BP0 and BP1 bits can be used to select one of four levels of block protection. Further, WPEN bit must be set to '1' to enable the use of Write Protect ( $\overline{WP}$ ) pin.

WRSR instruction is a write instruction and needs writes to be enabled (WEN bit set to '1') using the WREN instruction before it is issued. The instruction is issued after the falling edge of  $\overline{CS}$  using the opcode for WRSR followed by 8 bits of data to be stored in the Status Register. Since only bits 2, 3, and 7 can be modified by WRSR instruction, it is recommended to leave the bits 4-6 as '0' while writing to the Status Register.

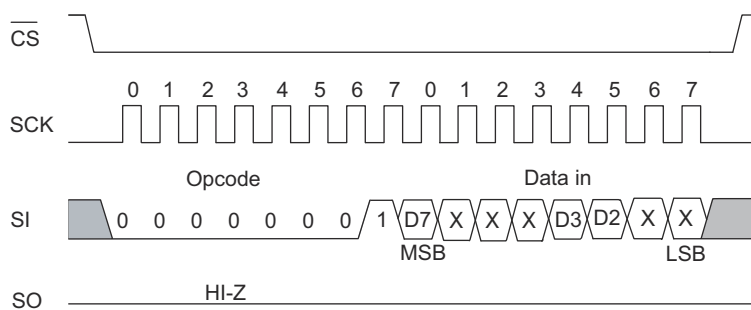
**Note** In CY14B256Q1/CY14B256Q2/CY14B256Q3, the values written to Status Register are saved to nonvolatile memory only after a STORE operation. If AutoStore is disabled (or while using CY14B256Q1), any modifications to the Status Register must be secured by performing a Software STORE operation.

**Note** CY14B256Q2 does not have  $\overline{WP}$  pin. Any modification to bit 7 of the Status Register has no effect on the functionality of CY14B256Q2.

**Figure 7. Read Status Register (RDSR) Instruction Timing**



**Figure 8. Write Status Register (WRSR) Instruction Timing**



## Write Protection and Block Protection

CY14B256Q1/CY14B256Q2/CY14B256Q3 provides features for both software and hardware write protection using WRDI instruction and WP. Additionally, this device also provides block protection mechanism through BP0 and BP1 pins of the Status Register.

The write enable and disable status of the device is indicated by WEN bit of the Status Register. The write instructions (WRSR and WRITE) and nvSRAM special instruction (STORE, RECALL, ASEN, and ASDISB) need the write to be enabled (WEN bit = 1) before they can be issued.

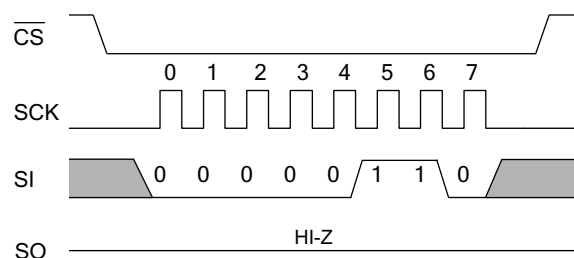
### Write Enable (WREN) Instruction

On power-up, the device is always in the write disable state. The following WRITE, WRSR, or nvSRAM special instruction (STORE, RECALL, ASEN, and ASDISB) must therefore be preceded by a Write Enable instruction. If the device is not write enabled (WEN = '0'), it ignores the write instructions and returns to the standby state when  $\overline{CS}$  is brought HIGH. A new  $\overline{CS}$  falling edge is required to re-initiate serial communication. The instruction is issued following the falling

edge of  $\overline{CS}$ . When this instruction is used, the WEN bit of Status Register is set to '1'. WEN bit defaults to '0' on power-up.

**Note** After completion of a write instruction (WRSR or WRITE) or nvSRAM special instruction (STORE, RECALL, ASEN, and ASDISB) instruction, WEN bit is cleared to '0'. This is done to provide protection from any inadvertent writes. Therefore, WREN instruction must be used before a new write instruction is issued.

**Figure 9. WREN Instruction**

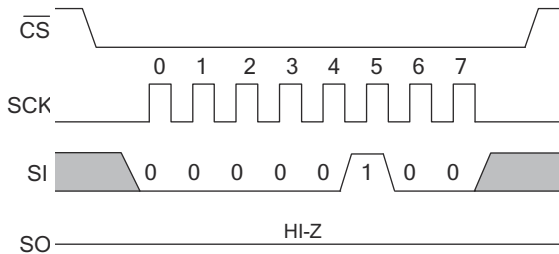




### Write Disable (WRDI) Instruction

Write Disable instruction disables the write by clearing the WEN bit to '0' in order to protect the device against inadvertent writes. This instruction is issued following the falling edge of  $\overline{CS}$  followed by opcode for WRDI instruction. The WEN bit is cleared on the rising edge of CS following a WRDI instruction.

Figure 10. WRDI Instruction



### Block Protection

Block protection is provided using the BP0 and BP1 pins of the Status Register. These bits can be set using WRSR instruction and probed using the RDSR instruction. The nvSRAM is divided into four array segments. One-quarter, one-half, or all of the memory segments can be protected. Any data within the protected segment is read only. Table 5 shows the function of Block Protect bits.

Table 5. Block Write Protect Bits

Level	Status Register Bits		Array Addresses Protected
	BP1	BP0	
0	0	0	None
1 (1/4)	0	1	0x6000–0x7FFF
2 (1/2)	1	0	0x4000–0x7FFF
3 (All)	1	1	0x0000–0x7FFF

### Write Protect ( $\overline{WP}$ ) Pin

The write protect pin ( $\overline{WP}$ ) is used to provide hardware write protection.  $\overline{WP}$  pin enables all normal read and write operations when held HIGH. When the  $\overline{WP}$  pin is brought LOW and WPEN bit is '1', all write operations to the Status Register are inhibited. The hardware write protection function is blocked when the WPEN bit is '0'. This enables the user to install the device in a system with the  $\overline{WP}$  pin tied to ground, and still write to the Status Register.

$\overline{WP}$  pin can be used along with WPEN and Block Protect bits (BP1 and BP0) of the Status Register to inhibit writes to memory. When  $\overline{WP}$  pin is LOW and WPEN is set to '1', any modifications to the Status Register are disabled. Therefore, the memory is protected by setting the BP0 and BP1 bits and the  $\overline{WP}$  pin inhibits any modification of the Status Register bits, providing hardware write protection.

**Note**  $\overline{WP}$  going LOW when  $\overline{CS}$  is still LOW has no effect on any of the ongoing write operations to the Status Register.

CY14B256Q2 does not have  $\overline{WP}$  pin and therefore does not provide hardware write protection.

Table 6 summarizes all the protection features of this device.

Table 6. Write Protection Operation

WPEN	$\overline{WP}$	WEN	Protected Blocks	Unprotected Blocks	Status Register
X	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	LOW	1	Protected	Writable	Protected
1	HIGH	1	Protected	Writable	Writable

### Memory Access

All memory accesses are done using the READ and WRITE instructions. These instructions cannot be used while a STORE or RECALL cycle is in progress. A STORE cycle in progress is indicated by the RDY bit of the Status Register and the HSB pin.

#### Read Sequence (READ) instruction

The read operations on this device are performed by giving the instruction on the SI pin and reading the output on SO pin. The following sequence needs to be followed for a read operation: After the CS line is pulled LOW to select a device, the read opcode is transmitted through the SI line followed by two bytes of address. The MSB bit (A15) of the address is a "don't care". After the last address bit is transmitted on the SI pin, the data (D7–D0) at the specific address is shifted out on the SO line on the falling edge of SCK starting with D7. Any other data on SI line after the last address bit is ignored.

CY14B256Q1/CY14B256Q2/CY14B256Q3 allows reads to be performed in bursts through SPI which can be used to read consecutive addresses without issuing a new READ instruction. If only one byte is to be read, the CS line must be driven HIGH after one byte of data comes out. However, the read sequence may be continued by holding the CS line LOW and the address is automatically incremented and data continues to shift out on SO pin. When the last data memory address (0x7FFF) is reached, the address rolls over to 0x0000 and the device continues to read.

#### Write Sequence (WRITE) instruction

The write operations on this device are performed through the SI pin. To perform a write operation, if the device is write disabled, then the device must first be write enabled through the WREN instruction. When the writes are enabled (WEN = '1'), WRITE instruction is issued after the falling edge of  $\overline{CS}$ . A WRITE instruction constitutes transmitting the WRITE opcode on SI line followed by 2 bytes of address and the data (D7–D0) which is to be written. The MSB bit (A15) of the address is a "don't care".

CY14B256Q1/CY14B256Q2/CY14B256Q3 enables writes to be performed in bursts through SPI which can be used to write consecutive addresses without issuing a new WRITE instruction. If only one byte is to be written, the CS line must be driven HIGH after the D0 (LSB of data) is transmitted. However, if more bytes are to be written, CS line must be held LOW and address is incremented automatically. The following bytes on the SI line are treated as data bytes and written in the successive addresses. When the last data memory address (0x7FFF) is reached, the

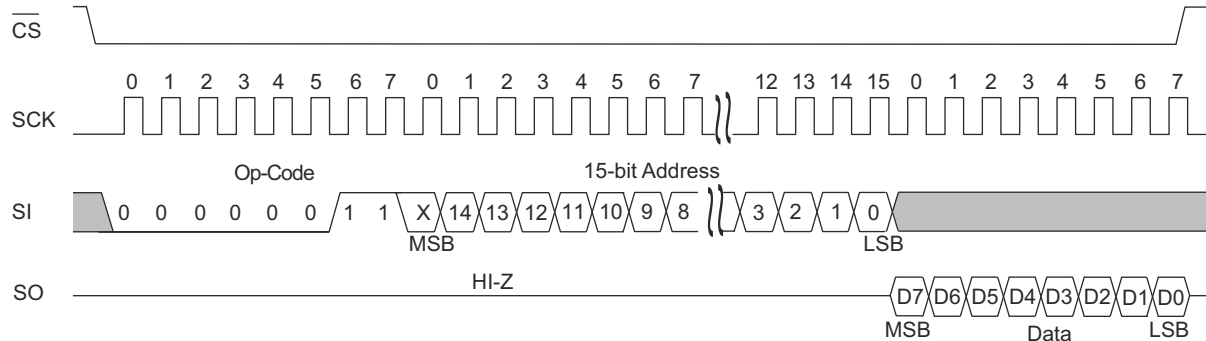


address rolls over to 0x0000 and the device continues to write. The WEN bit is reset to '0' on completion of a WRITE sequence.

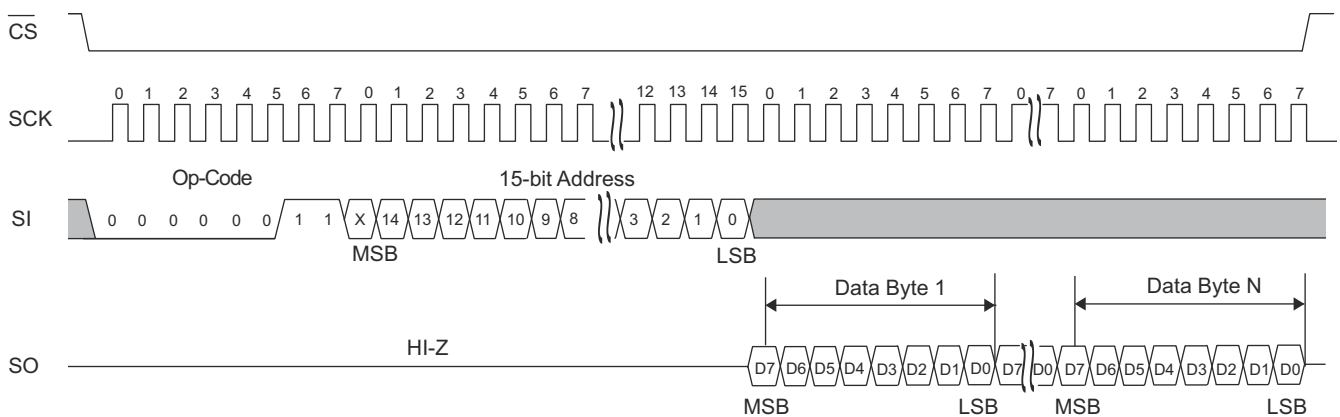
**Note** When a burst write reaches a protected block address, it continues the address increment into the protected space but

does not write any data to the protected memory. If the address roll over takes the burst write to unprotected space, it resumes writes. The same operation is true if a burst write is initiated within a write protected block.

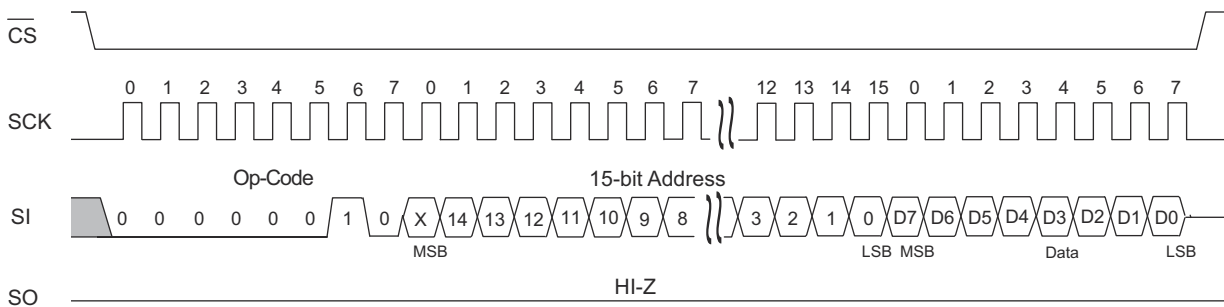
**Figure 11. Read Instruction Timing**

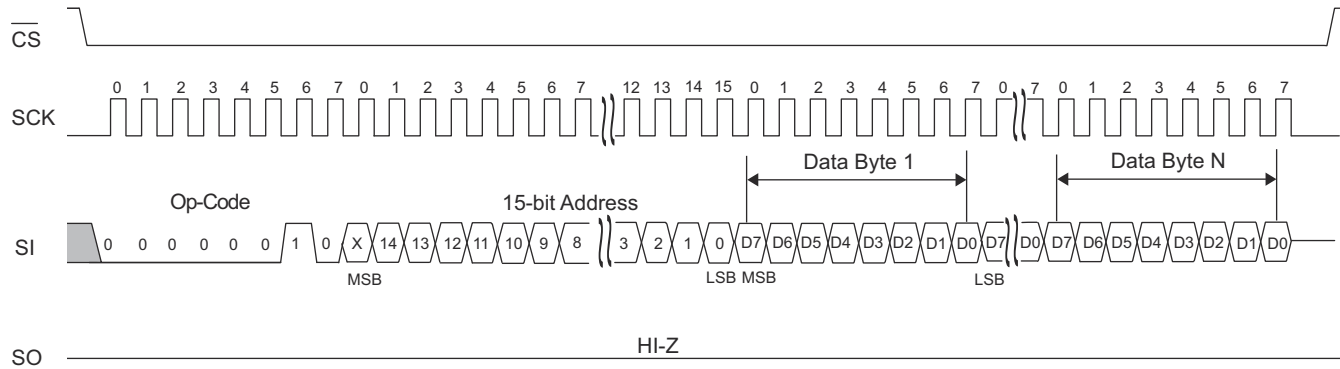


**Figure 12. Burst Mode Read Instruction Timing**



**Figure 13. Write Instruction Timing**



**Figure 14. Burst Mode Write Instruction Timing**


## nvSRAM Special Instructions

CY14B256Q1/CY14B256Q2/CY14B256Q3 provides four special instructions which enables access to the nvSRAM specific functions: STORE, RECALL, ASDISB, and ASENB. Table 7 lists these instructions.

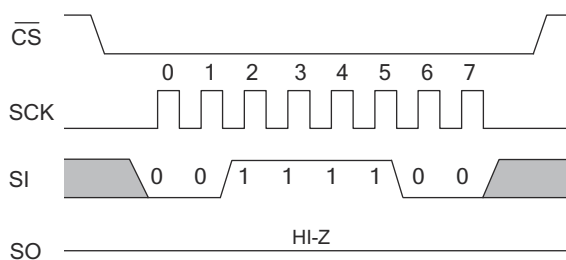
**Table 7. nvSRAM Special Instructions**

Function Name	Opcode	Operation
STORE	0011 1100	Software STORE
RECALL	0110 0000	Software RECALL
ASENB	0101 1001	AutoStore Enable
ASDISB	0001 1001	AutoStore Disable

### Software STORE (STORE) instruction

When a STORE instruction is executed, nvSRAM performs a Software STORE operation. The STORE operation is performed irrespective of whether a write has taken place since the last STORE or RECALL operation.

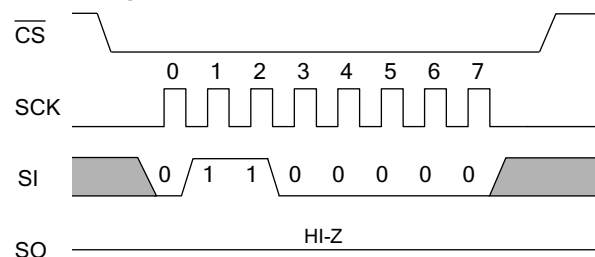
To issue this instruction, the device must be write enabled (WEN bit = '1'). The instruction is performed by transmitting the STORE opcode on the SI pin following the falling edge of CS. The WEN bit is cleared on the positive edge of CS following the STORE instruction.

**Figure 15. Software STORE Operation**


### Software RECALL (RECALL) instruction

When a RECALL instruction is executed, nvSRAM performs a Software RECALL operation. To issue this instruction, the device must be write enabled (WEN = '1').

The instruction is performed by transmitting the RECALL opcode on the SI pin following the falling edge of CS. The WEN bit is cleared on the positive edge of CS following the RECALL instruction.

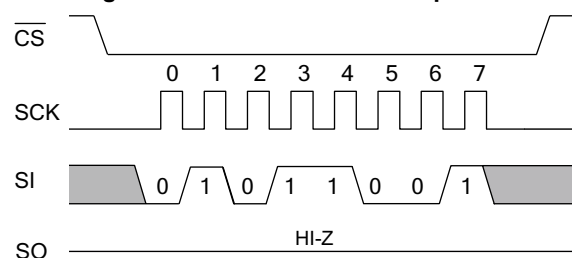
**Figure 16. Software RECALL Operation**


### AutoStore Enable (ASENB) instruction

The AutoStore Enable instruction enables the AutoStore on CY14B256Q1. This setting is not nonvolatile and needs to be followed by a STORE sequence if this is desired to survive the power cycle.

To issue this instruction, the device must be write enabled (WEN = '1'). The instruction is performed by transmitting the ASENB opcode on the SI pin following the falling edge of CS. The WEN bit is cleared on the positive edge of CS following the ASENB instruction.

**Note** If ASDISB and ASENB instructions are executed in CY14B256Q1, the device is busy for the duration of software sequence processing time ( $t_{SS}$ ). However, ASDISB and ASENB instructions have no effect on CY14B256Q1 as AutoStore is internally disabled.

**Figure 17. AutoStore Enable Operation**


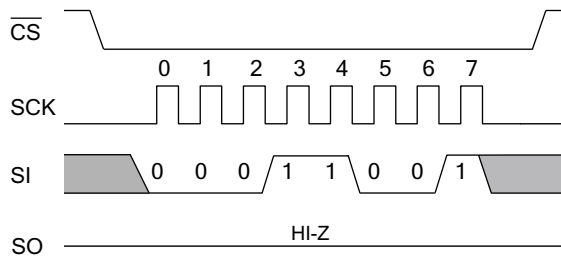


### AutoStore Disable (ASDISB) instruction

AutoStore is enabled by default in CY14B256Q2/CY14B256Q3. The ASDISB instruction disables the AutoStore. This setting is not nonvolatile and needs to be followed by a STORE sequence if this is desired to survive the power cycle.

To issue this instruction, the device must be write enabled (WEN = '1'). The instruction is performed by transmitting the ASDISB opcode on the SI pin following the falling edge of  $\overline{CS}$ . The WEN bit is cleared on the positive edge of  $\overline{CS}$  following the ASDISB instruction.

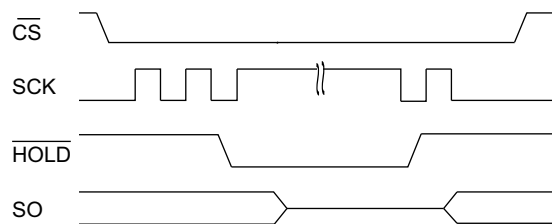
Figure 18. AutoStore Disable Operation



### $\overline{HOLD}$ Pin Operation

The  $\overline{HOLD}$  pin is used to pause the serial communication. When the device is selected and a serial sequence is underway,  $\overline{HOLD}$  is used to pause the serial communication with the master device without resetting the ongoing serial sequence. To pause, the  $\overline{HOLD}$  pin must be brought LOW when the SCK pin is LOW.  $\overline{CS}$  pin must remain LOW along with  $\overline{HOLD}$  pin to pause serial communication. While the device serial communication is paused, inputs to the SI pin are ignored and the SO pin is in the high impedance state. To resume serial communication, the  $\overline{HOLD}$  pin must be brought HIGH when the SCK pin is LOW (SCK may toggle during HOLD).

Figure 19.  $\overline{HOLD}$  Operation





## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C  
 Maximum accumulated storage time  
     At 150 °C ambient temperature ..... 1000 h  
     At 85 °C ambient temperature ..... 20 Years  
 Maximum junction temperature ..... 150 °C  
 Supply voltage on  $V_{CC}$  relative to  $V_{SS}$  ..... -0.5 V to +4.1 V  
 DC voltage applied to outputs  
 in high Z state ..... -0.5 V to  $V_{CC} + 0.5$  V  
 Input voltage ..... -0.5 V to  $V_{CC} + 0.5$  V

Transient voltage (< 20 ns)  
 on any pin to ground potential ..... -2.0 V to  $V_{CC} + 2.0$  V  
 Package power dissipation capability  
 ( $T_A = 25$  °C) ..... 1.0 W  
 Surface mount lead soldering temperature  
 (3 seconds) ..... +260 °C  
 DC output current  
 (1 output at a time, 1 s duration) ..... 15 mA  
 Static discharge voltage  
 (per MIL-STD-883, method 3015) ..... > 2001 V  
 Latch-up current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Industrial	-40 °C to +85 °C	2.7 V to 3.6 V

## DC Electrical Characteristics

Over the [Operating Range](#)

Parameter	Description	Test Conditions	Min	Typ <sup>[5]</sup>	Max	Unit
$V_{CC}$	Power supply voltage		2.7	3.0	3.6	V
$I_{CC1}$	Average $V_{CC}$ current	At $f_{SCK} = 40$ MHz. Values obtained without output loads ( $I_{OUT} = 0$ mA)	-	-	10	mA
$I_{CC2}$	Average $V_{CC}$ current during STORE	All inputs don't care, $V_{CC} = \text{Max}$ . Average current for duration $t_{STORE}$	-	-	10	mA
$I_{CC4}$	Average $V_{CAP}$ current during AutoStore cycle	All inputs don't care. Average current for duration $t_{STORE}$	-	-	5	mA
$I_{SB}$	$V_{CC}$ standby current	$\overline{CS} \geq (V_{CC} - 0.2 \text{ V})$ . $V_{IN} \leq 0.2 \text{ V}$ or $\geq (V_{CC} - 0.2 \text{ V})$ . Standby current level after nonvolatile cycle is complete. Inputs are static. $f = 0$ MHz	-	-	5	mA

### Note

5. Typical values are at 25 °C,  $V_{CC} = V_{CC(Typ)}$ . Not 100% tested.



## DC Electrical Characteristics

Over the [Operating Range](#)

Parameter	Description	Test Conditions	Min	Typ <sup>[5]</sup>	Max	Unit
I <sub>IX</sub> <sup>[6]</sup>	Input leakage current (except HSB)	V <sub>CC</sub> = Max, V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	-	+1	μA
	Input leakage current (for HSB)	V <sub>CC</sub> = Max, V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-100	-	+1	μA
I <sub>OZ</sub>	Off state output leakage current	V <sub>CC</sub> = Max, V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>	-1	-	+1	μA
V <sub>IH</sub>	Input HIGH voltage		2.0	-	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW voltage		V <sub>SS</sub> - 0.5	-	0.8	V
V <sub>OH</sub>	Output HIGH voltage	I <sub>OUT</sub> = -2 mA	2.4	-	-	V
V <sub>OL</sub>	Output LOW voltage	I <sub>OUT</sub> = 4 mA	-	-	0.4	V
V <sub>CAP</sub> <sup>[7]</sup>	Storage capacitor	Between V <sub>CAP</sub> pin and V <sub>SS</sub>	61	68	180	μF
V <sub>V<sub>CAP</sub></sub> <sup>[8, 9]</sup>	Maximum voltage driven on V <sub>CAP</sub> pin by the device	V <sub>CC</sub> = Max	-	-	V <sub>CC</sub>	V

### Notes

- The HSB pin has I<sub>OUT</sub> = -2 μA for V<sub>OH</sub> of 2.4 V when both active high and LOW drivers are disabled. When they are enabled standard V<sub>OH</sub> and V<sub>OL</sub> are valid. This parameter is characterized but not tested.
- Min V<sub>CAP</sub> value guarantees that there is a sufficient charge available to complete a successful AutoStore operation. Max V<sub>CAP</sub> value guarantees that the capacitor on V<sub>CAP</sub> is charged to a minimum voltage during a Power-Up RECALL cycle so that an immediate power-down cycle can complete a successful AutoStore. Therefore it is always recommended to use a capacitor within the specified min and max limits. Refer application note [AN43593](#) for more details on V<sub>CAP</sub> options.
- Maximum voltage on V<sub>CAP</sub> pin (V<sub>V<sub>CAP</sub></sub>) is provided for guidance when choosing the V<sub>CAP</sub> capacitor. The voltage rating of the V<sub>CAP</sub> capacitor across the operating temperature range should be higher than the V<sub>V<sub>CAP</sub></sub> voltage.
- These parameters are guaranteed by design and are not tested.



## Data Retention and Endurance

Over the [Operating Range](#)

Parameter	Description	Min	Unit
DATA <sub>R</sub>	Data retention	20	Years
NV <sub>C</sub>	Nonvolatile STORE operations	1,000	K

## Capacitance

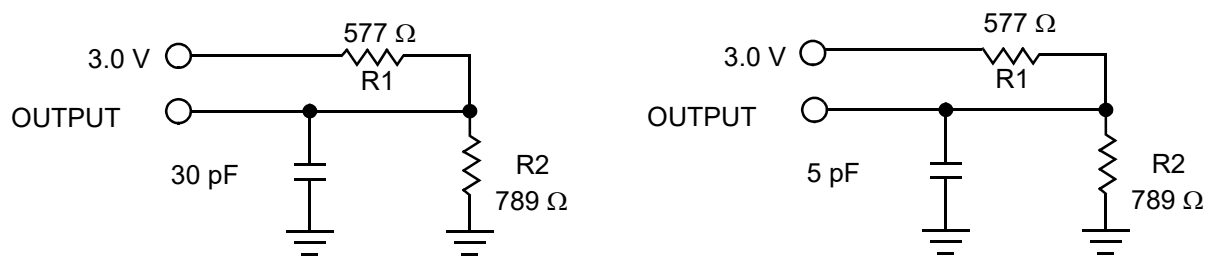
Parameter <sup>[10]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(Typ)</sub>	6	pF
C <sub>OUT</sub>	Output pin capacitance		8	pF

## Thermal Resistance

Parameter <sup>[10]</sup>	Description	Test Conditions	16-pin SOIC	8-pin DFN	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	55.17	17.7	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		2.64	18.8	°C/W

## AC Test Loads and Waveforms

Figure 20. AC Test Loads and Waveforms



## AC Test Conditions

Input pulse levels ..... 0 V to 3 V  
 Input rise and fall times (10% to 90%) ..... ≤ 3 ns  
 Input and output timing reference levels ..... 1.5 V

**Note**  
 10. These parameters are guaranteed by design and are not tested.



## AC Switching Characteristics

Over the [Operating Range](#)

Parameters <sup>[11]</sup>		Description	40 MHz		Unit
Cypress Parameter	Alt. Parameter		Min	Max	
f <sub>SCK</sub>	f <sub>SCK</sub>	Clock frequency, SCK	–	40	MHz
t <sub>CL</sub>	t <sub>WL</sub>	Clock pulse width LOW	11	–	ns
t <sub>CH</sub>	t <sub>WH</sub>	Clock pulse width HIGH	11	–	ns
t <sub>CS</sub>	t <sub>CE</sub>	$\overline{\text{CS}}$ high time	20	–	ns
t <sub>CSS</sub>	t <sub>CES</sub>	$\overline{\text{CS}}$ setup time	10	–	ns
t <sub>CSH</sub>	t <sub>CEH</sub>	$\overline{\text{CS}}$ hold time	10	–	ns
t <sub>SD</sub>	t <sub>SU</sub>	Data in setup time	5	–	ns
t <sub>HD</sub>	t <sub>H</sub>	Data in hold time	5	–	ns
t <sub>HH</sub>	t <sub>HD</sub>	HOLD hold time	5	–	ns
t <sub>SH</sub>	t <sub>CD</sub>	$\overline{\text{HOLD}}$ setup time	5	–	ns
t <sub>CO</sub>	t <sub>V</sub>	Output valid	–	9	ns
t <sub>HHZ</sub> <sup>[12]</sup>	t <sub>HZ</sub>	$\overline{\text{HOLD}}$ to output High-Z	–	15	ns
t <sub>HLZ</sub> <sup>[12]</sup>	t <sub>LZ</sub>	$\overline{\text{HOLD}}$ to output Low-Z	–	15	ns
t <sub>OH</sub>	t <sub>HO</sub>	Output hold time	0	–	ns
t <sub>HZCS</sub>	t <sub>DIS</sub>	Output disable time	–	25	ns

### Notes

11. Test conditions assume signal transition time of 3 ns or less, timing reference levels of V<sub>CC</sub>/2, input pulse levels of 0 to V<sub>CC</sub>(<sub>typ</sub>), and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and load capacitance shown in [Figure 20 on page 19](#).

12. These parameters are guaranteed by design and are not tested.



Switching Waveforms

Figure 21. Synchronous Data Timing (Mode 0)

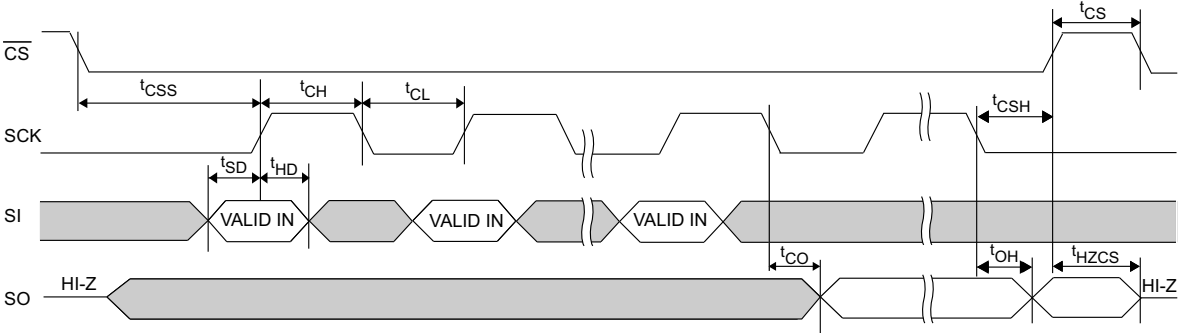
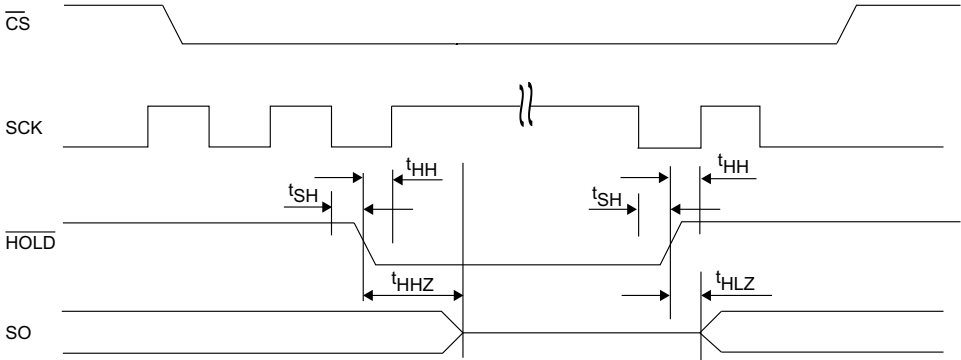


Figure 22. HOLD Timing





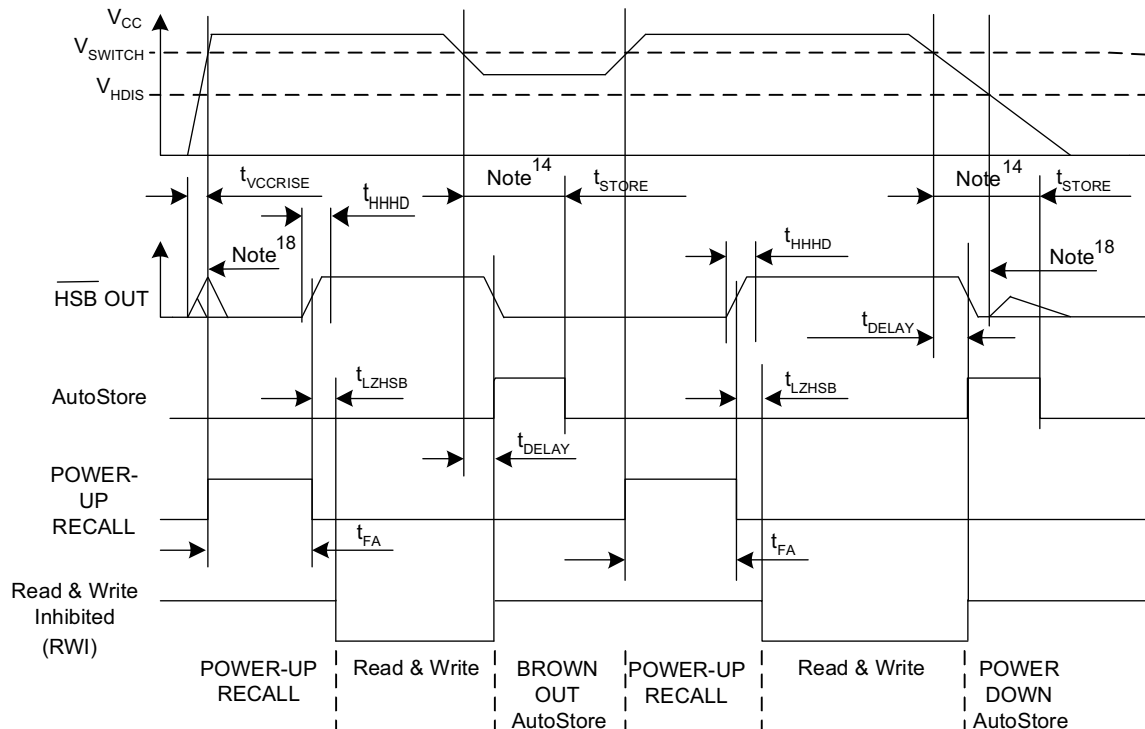
## AutoStore or Power-Up RECALL

Over the Operating Range

Parameter	Description	CY14B256Q1/ CY14B256Q2/ CY14B256Q3		Unit
		Min	Max	
$t_{FA}^{[13]}$	Power-Up RECALL duration	–	20	ms
$t_{STORE}^{[14]}$	STORE cycle duration	–	8	ms
$t_{DELAY}^{[15]}$	Time allowed to complete SRAM write cycle	–	25	ns
$V_{SWITCH}$	Low voltage trigger level	–	2.65	V
$t_{VCCRRISE}^{[16]}$	$V_{CC}$ rise time	150	–	$\mu$ s
$V_{HDIS}^{[16]}$	$\overline{HSB}$ output disable voltage	–	1.9	V
$t_{LZHSB}^{[16]}$	$\overline{HSB}$ high to nvSRAM active time	–	5	$\mu$ s
$t_{HHHD}^{[16]}$	$\overline{HSB}$ high active time	–	500	ns

## Switching Waveforms

Figure 23. AutoStore or Power-Up RECALL <sup>[17]</sup>



### Notes

13.  $t_{FA}$  starts from the time  $V_{CC}$  rises above  $V_{SWITCH}$ .
14. If an SRAM write has not taken place since the last nonvolatile cycle, AutoStore or Hardware STORE is not initiated.
15. On a Hardware STORE and AutoStore initiation, SRAM write operation continues to be enabled for time  $t_{DELAY}$ .
16. These parameters are guaranteed by design and are not tested.
17. Read and write cycles are ignored during STORE, RECALL, and while  $V_{CC}$  is below  $V_{SWITCH}$ .
18. During power-up and power-down,  $\overline{HSB}$  glitches when  $\overline{HSB}$  pin is pulled up through an external resistor.



## Software Controlled STORE and RECALL Cycles

Over the [Operating Range](#)

Parameter	Description	CY14B256Q1/ CY14B256Q2/ CY14B256Q3		Unit
		Min	Max	
$t_{\text{RECALL}}$	RECALL duration	–	200	$\mu\text{s}$
$t_{\text{SS}}^{[19, 20]}$	Soft sequence processing time	–	100	$\mu\text{s}$

## Switching Waveforms

Figure 24. Software STORE Cycle <sup>[20]</sup>

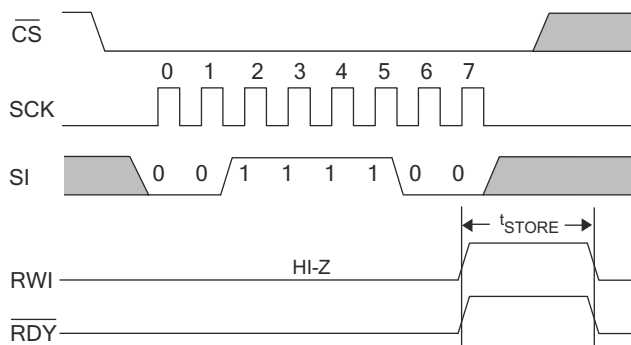


Figure 25. Software RECALL Cycle <sup>[20]</sup>

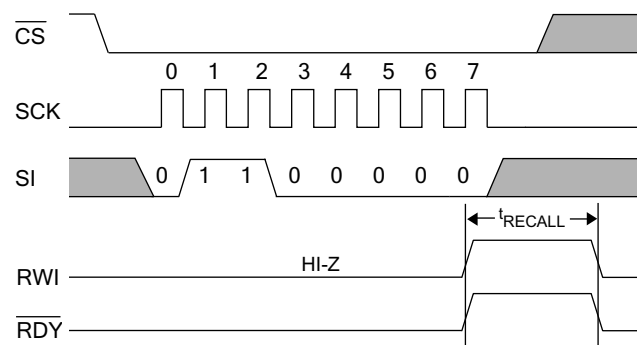


Figure 26. AutoStore Enable Cycle

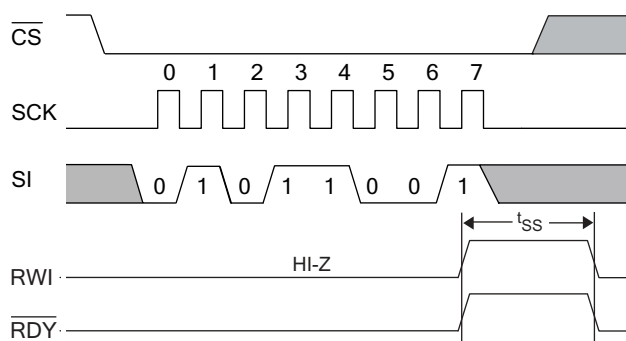
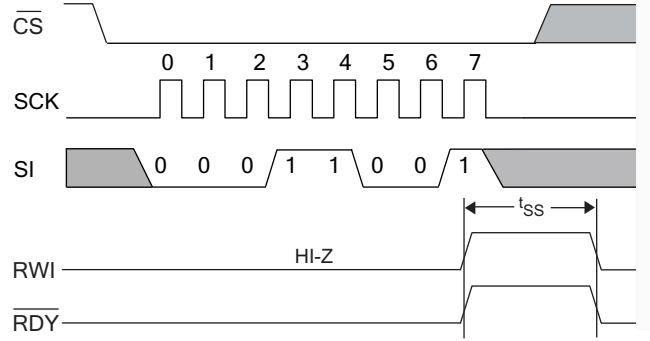


Figure 27. AutoStore Disable Cycle



### Notes

- This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain HIGH to effectively register command.
- Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.



### Hardware STORE Cycle

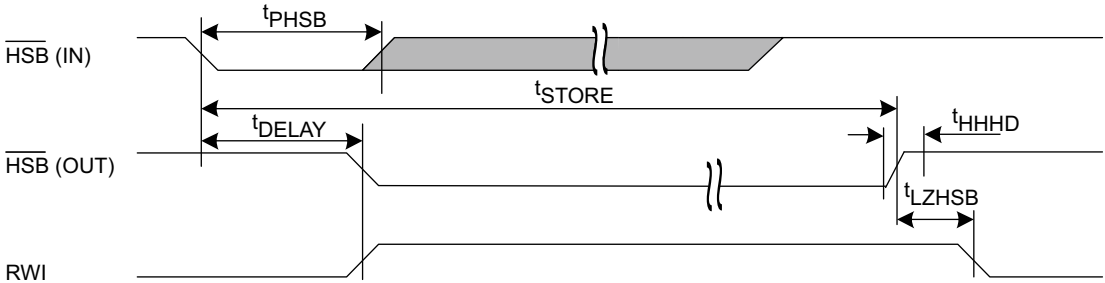
Over the [Operating Range](#)

Parameter	Description	CY14B256Q3		Unit
		Min	Max	
t <sub>PHSB</sub>	Hardware STORE pulse width	15	–	ns

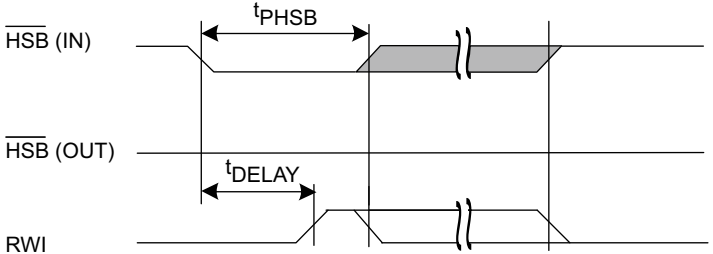
### Switching Waveforms

Figure 28. Hardware STORE Cycle [21]

#### Write Latch set



#### Write Latch not set



HSB pin is driven HIGH to V<sub>CC</sub> only by Internal 100 KΩ resistor, HSB driver is disabled  
 SRAM is disabled as long as HSB (IN) is driven LOW.

**Note**  
 21. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.



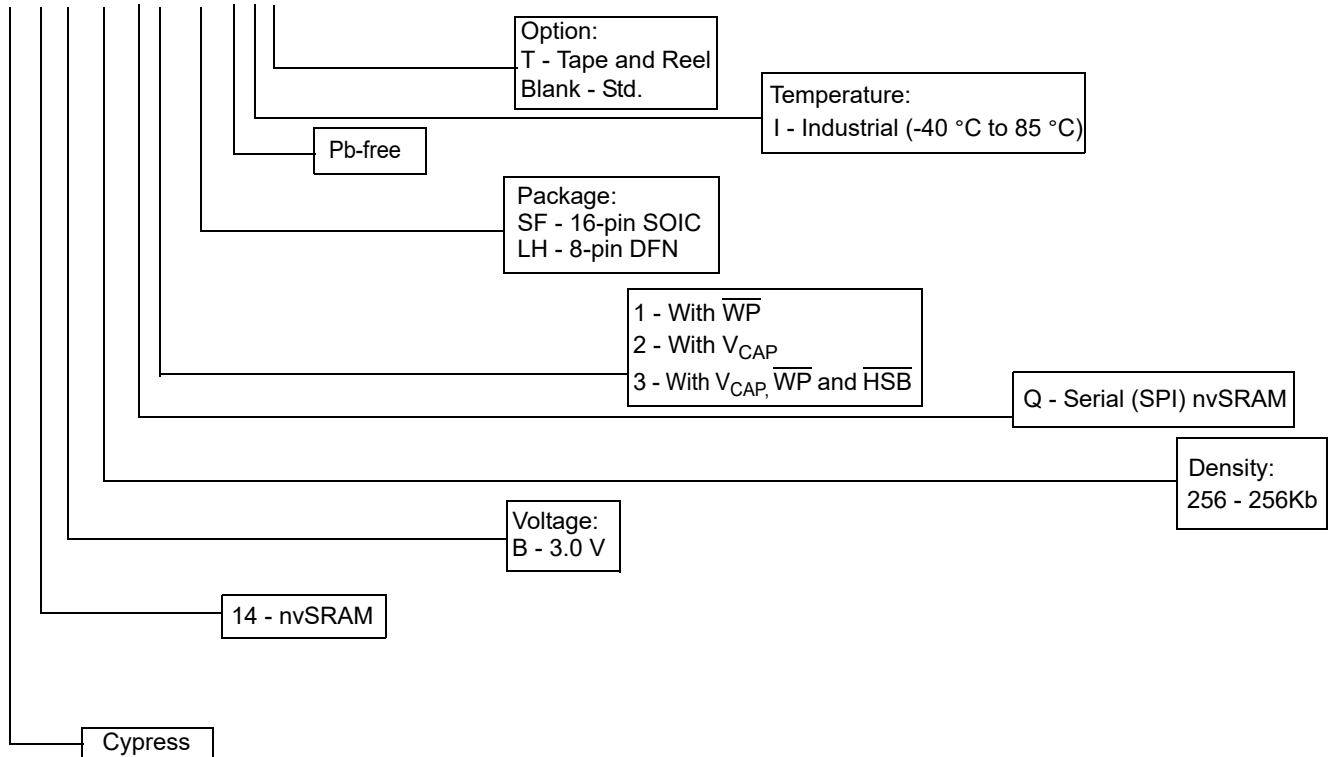
### Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
CY14B256Q2-LHXI	001-50671	8-pin DFN (with V <sub>CAP</sub> )	Industrial

All the above parts are Pb-free.

### Ordering Code Definitions

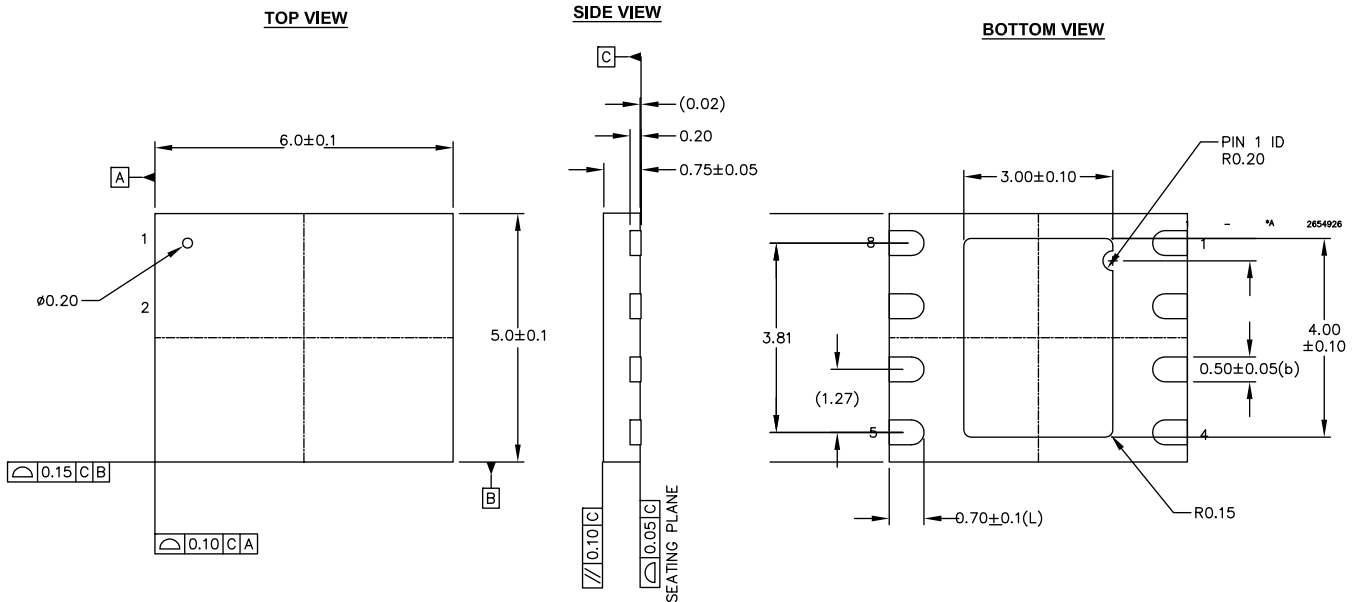
CY 14 B 256 Q 2 - LH X I T





Package Diagrams

Figure 29. 8-pin DFN ( $5 \times 6 \times 0.75$  mm) Package Outline, 001-50671



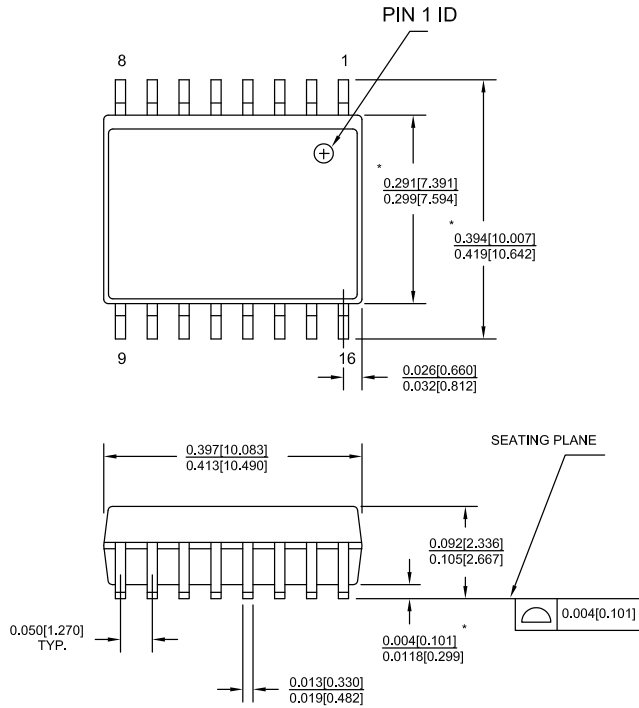
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. PACKAGE WEIGHT: TBD
3. BASED ON REF JEDEC # MO-240 EXCEPT DIMENSIONS (L) and (b)

001-50671 \*E

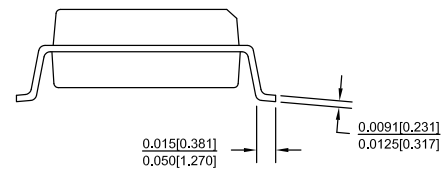
Package Diagrams (continued)

Figure 30. 16-pin SOIC (0.413 × 0.299 × 0.0932 inches) Package Outline, 51-85022



DIMENSIONS IN INCHES[MM]      MIN.  
 MAX.  
 REFERENCE JEDEC MO-119

PART #	
S16.3	STANDARD PKG.
SZ16.3	LEAD FREE PKG.



51-85022 \*E



## Acronyms

Acronym	Description
CPHA	Clock Phase
CPOL	Clock Polarity
DFN	Dual Flat No-lead
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIA	Electronic Industries Alliance
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
LSB	Least Significant Bit
MSB	Most Significant Bit
nvSRAM	non-volatile Static Random Access Memory
RWI	Read and Write Inhibit
RoHS	Restriction of Hazardous Substances
SPI	Serial Peripheral Interface
SONOS	Silicon-Oxide-Nitride-Oxide Semiconductor
SOIC	Small Outline Integrated Circuit
SRAM	Static Random Access Memory

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
KΩ	kilohm
Mbit	megabit
MHz	megahertz
μA	microampere
μF	microfarad
μs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt



## Document History Page

Document Title: CY14B256Q1/CY14B256Q2/CY14B256Q3, 256-Kbit (32K × 8) Serial (SPI) nvSRAM Document Number: 001-53882				
Rev.	ECN	Orig. of Change	Submission Date	Description of Change
**	2733272	GVCH / AESA	07/08/2009	New data sheet.
*A	2758444	GVCH	09/01/2009	Changed status from Preliminary to Final. Removed Commercial Temperature related information in all instances across the document. Updated <a href="#">Memory Access</a> : Updated <a href="#">Write Sequence (WRITE) instruction</a> : Updated description (Added Note at the end). Updated <a href="#">Thermal Resistance</a> : Added values for $\Theta_{JA}$ and $\Theta_{JC}$ parameters corresponding to 16-pin SOIC and 8-pin DFN package. Updated <a href="#">Ordering Information</a> : Updated part numbers.
*B	2839453	GVCH / PYRS	01/06/2010	Updated <a href="#">Features</a> : Replaced “200,000 STORE cycles to QuantumTrap” with “1 Million STORE cycles to QuantumTrap” under “High Reliability”. Updated <a href="#">Device Operation</a> : Updated <a href="#">AutoStore Operation</a> : Updated <a href="#">Figure 3</a> .
*C	3009761	GVCH	08/17/2010	Updated <a href="#">Pinouts</a> : Changed ground naming convention from GND to $V_{SS}$ . Updated <a href="#">Pin Definitions</a> : Updated details in “Description” column corresponding to $\overline{HSB}$ pin (Added more clarity on HSB pin operation). Updated <a href="#">Device Operation</a> : <a href="#">Hardware STORE and HSB Pin Operation</a> : Updated description (Added more clarity on $\overline{HSB}$ pin operation). Updated <a href="#">SPI Operating Features</a> : Updated <a href="#">Power On Reset</a> : Updated description. Updated <a href="#">Power-Down</a> : Updated description. Updated <a href="#">Status Register</a> : Updated <a href="#">Table 4</a> (Added “bits 4–6” and their corresponding details). Updated <a href="#">Write Status Register (WRSR) Instruction</a> : Updated <a href="#">Figure 8</a> . Updated <a href="#">Switching Waveforms</a> : Updated <a href="#">Figure 21</a> . Updated <a href="#">Figure 22</a> . Updated <a href="#">Switching Waveforms</a> : Updated <a href="#">Figure 23</a> . Updated Note 18. Updated <a href="#">Switching Waveforms</a> : Added <a href="#">Figure 26</a> . Added <a href="#">Figure 27</a> . Updated <a href="#">Hardware STORE Cycle</a> : Removed $t_{DHSB}$ parameter and its corresponding details. Updated <a href="#">Switching Waveforms</a> : Updated <a href="#">Figure 28</a> . Updated <a href="#">Package Diagrams</a> : spec 001-50671 – Changed revision from *A to *B. spec 51-85022 – Changed revision from *B to *C. Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> .



Document History Page (continued)

Document Title: CY14B256Q1/CY14B256Q2/CY14B256Q3, 256-Kbit (32K × 8) Serial (SPI) nvSRAM				
Document Number: 001-53882				
Rev.	ECN	Orig. of Change	Submission Date	Description of Change
*D	3054787	GVCH	10/11/2010	Added watermark "For Evaluation Samples only. Production will be supported with the next revision silicon in SOIC package." across the document. Updated <a href="#">nvSRAM Special Instructions</a> : Updated <a href="#">HOLD Pin Operation</a> : Updated description. Updated <a href="#">Figure 19</a> (to indicate that $\overline{CS}$ pin must remain LOW along with $\overline{HOLD}$ pin to pause serial communication). Updated <a href="#">Switching Waveforms</a> : Updated <a href="#">Figure 22</a> (to indicate that $\overline{CS}$ pin must remain LOW along with $\overline{HOLD}$ pin to pause serial communication).
*E	3143330	GVCH	01/17/2011	Updated <a href="#">Device Operation</a> : Updated <a href="#">Hardware STORE and HSB Pin Operation</a> : Updated description (Added more clarity on HSB pin operation). Updated <a href="#">AutoStore or Power-Up RECALL</a> : Updated details in "Description" column corresponding to $t_{LZHSB}$ parameter. Updated <a href="#">Switching Waveforms</a> : Updated <a href="#">Figure 23</a> (Fixed typo).
*F	3320699	GVCH	07/19/2011	Updated <a href="#">DC Electrical Characteristics</a> : Added Note 7 and referred the same note in $V_{CAP}$ parameter. Updated <a href="#">AC Switching Characteristics</a> : Added Note 11 and referred the same note in "Parameters" column. Completing Sunset Review.
*G	3510173	GVCH	01/27/2012	Removed "Best Practices". Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated <a href="#">Package Diagrams</a> : spec 001-50671 – Changed revision from *B to *C. spec 51-85022 – Changed revision from *C to *D.
*H	3666763	GVCH	07/05/2012	Updated <a href="#">DC Electrical Characteristics</a> : Added $V_{V_{CAP}}$ parameter and its details. Added Note 8 and referred the same note in $V_{V_{CAP}}$ parameter. Referred Note 9 in $V_{V_{CAP}}$ parameter. Completing Sunset Review.
*I	3710859	GVCH	08/13/2012	Updated <a href="#">Maximum Ratings</a> : Removed "Ambient temperature with power applied" and its corresponding details. Added "Maximum junction temperature" and its corresponding details.
*J	4011614	GVCH	05/27/2013	Removed watermark "For Evaluation Samples only. Production will be supported with the next revision silicon in SOIC package." across the document. Added watermark "Not Recommended for New Designs" across the document. Updated <a href="#">Package Diagrams</a> : spec 51-85022 – Changed revision from *D to *E. Completing Sunset Review.
*K	4557366	GVCH	11/05/2014	Updated <a href="#">Functional Description</a> : Added "For a complete list of related documentation, click <a href="#">here</a> ." at the end.
*L	6278065	GVCH	08/10/2018	Removed watermark "Not Recommended for New Designs" across the document. Updated <a href="#">Package Diagrams</a> : spec 001-50671 – Changed revision from *C to *E. Updated to new template.



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