GENERAL DESCRIPTION

The LW54XX Series is an ultra-low noise, high PSRR LDO with enable function that operates from 1.9V to 5.5V. It provides up to 500mA output current.

The features of low noise and high PSRR make LW54XX ideal for noise-sensitive and analog applications.

The LW54XX Series integrate current limit, short circuit, thermal shut down, that protecting IC from being damaged.

Output voltage is selectable from 1.2V to 5.0V which fixed by laser trimming technologies, Step=100mV.

The LW54XX Series is available in SOT23-5L, DFN1x1-4L and DFN2x2-6L packages.

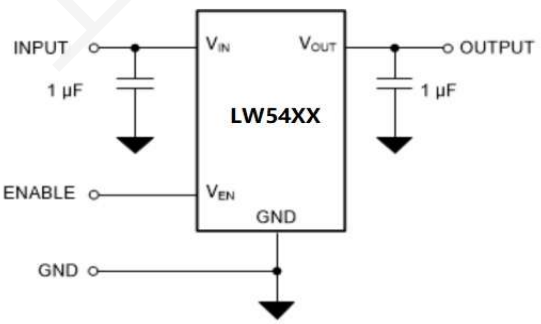
FEATURES

- Low Quiescent Current: 10μA(Typ.)
- Operating Voltage Range: from 1.9V to 5.5V
- Output Voltage Range: from 1.2V to 5.0V
- Maximum Output Current: 500mA
- Output Accuracy: ±1% @+25°C
- Low Dropout Voltage: 180mV@500mA/3.3V
- High PSRR: 90dB@1KHz,10mA
- Ultra-Low Noise: 5.3μV_{RMS}
- Inrush Current Limit: 250mA
- Current Limiting Protection
- Output Short-Circuit Protection
- Over-Temperature Protection
- Soft-Start Function
- Stable with 1μF Output Capacitor

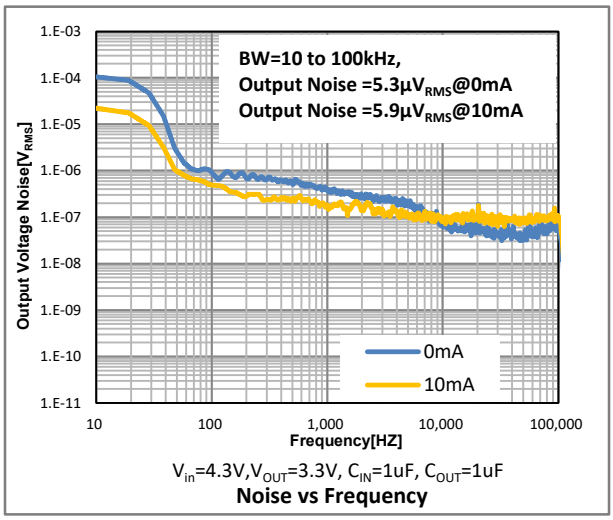
APPLICATIONS

- Mobile Phones, Tablets, Digital Cameras
- Audio Devices
- RF Modules
- Clock Generator: VCO, PLL, etc.
- Noise-Sensitive Devices: ADC, DAC

TYPICAL APPLICATION CIRCUIT



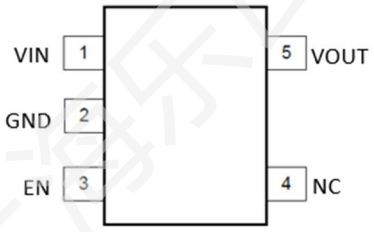
TYPICAL PERFORMANCE CHARACTERISTICS



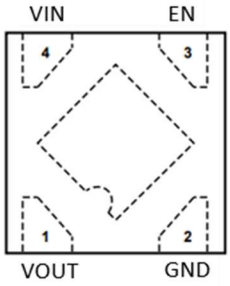
PIN DESCRIPTION:

PIN No			SYMBOL	DESCRIPTTION
SOT23-5L	DFN1x1-4L	DFN2x2-6		
1	4	6	VIN	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the Recommended Operating Conditions table and the Input and Output Capacitor Requirements section. Place the input capacitor as close to the output of the device as possible.
2	2	3	GND	Ground pin.
3	3	4	EN	Enable pin. Drive EN greater than $V_{EN(HI)}$ to turn on the regulator. Drive EN less than $V_{EN(LO)}$ to put the low-dropout regulator (LDO) into shutdown mode.
4	--	2,5	NC	No internal connection. Ground this pin for better thermal performance.
5	1	1	VOUT	Regulated output voltage pin. Connect a low-equivalent series resistance (ESR) capacitor to this pin. For best transient response, use the nominal recommended value or larger capacitor from OUT to GND. An internal pulldown resistor prevents a charge from remaining on OUT when the regulator is in shutdown mode ($V_{EN} < V_{EN\ (LOW)}$).
--	Thermal Pad	Thermal Pad	Pad	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

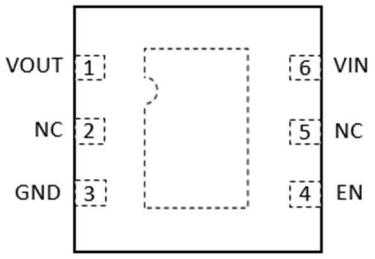
PIN ASSIGNMENT



SOT23-5L



DFN1x1-4L



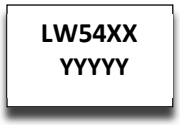
DFN2x2-6L

MARK INFORMATION:

SOT23-5L

XX: VOLTAGE

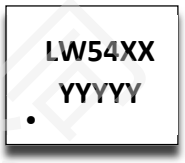
YY: DATE CODE



DFN2x2-6L

XX: VOLTAGE

YY: DATE CODE



DFN1X1-4L

X: VOLTAGE

1.2V	1.5V	1.8V	2.5V	2.8V	3.0V	3.3V	3.6V	4.2V	5.0V
C	D	G	H	J	L	M	P	S	T

ABSOLUTE MAXIMUM RATINGS (1):

(T_A =25℃, unless otherwise specified.)

SYMBOL	ITEM		RATING	UNIT
V_{IN}	Supply Voltage		-0.3~6.5	V
V_{EN}	EN Pin Voltage		-0.3~6.5	V
V_{OUT}	VOUT Pin Voltage		-0.3~6.0	V
$V_{(ESD)}$	ESD Susceptibility, HBM(2)		±4000	V
$R_{\theta JA}$	Junction-to-ambient Thermal Resistance(3)	SOT23-5L	188	℃/W
		DFN1x1-4L	180	
		DFN2x2-6L	73	
T_J	Junction Temperature Range		-40~150	℃
T_{STG}	Storage Temperature Range		-40~150	℃
T_{SOLDER}	Lead Temperature (Soldering)		260℃, 10s	

Note:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

2. per ANSI/ESDA/JEDEC JS-001

3. Device mounted on FR-4 PCB, Refer to JESD51-3 for detailed information on the board construction

RECOMMENDED OPERATING RANGE:

SYMBOL	ITEM	VALUE	UNIT
V_{IN}	VIN Supply Voltage	1.9~5.5	V
V_{EN}	EN Pin Voltage	0~5.5	V
V_{OUT}	V_{OUT} Pin Voltage	1.2~5.0	V
I_{OUT}	Output Current	0~500	mA
T_J	Junction Temperature Range	-40~125	℃

ELECTRICAL CHARACTERISTICS:

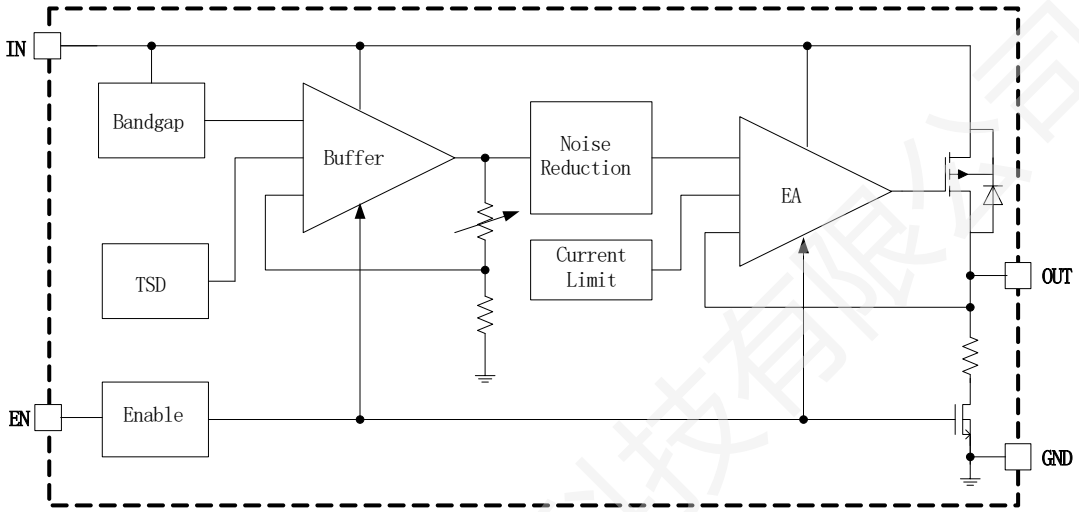
(V_{IN}=$V_{OUT(NOM)}$+1V or 2V, whichever is greater, C_{IN}= C_{OUT}=1μF, unless otherwise specified, typical values are at T_A = 25℃.)

Symbol	Parameter	Test Conditions		MIN	TYP	MAX	Units
V_{IN}	Input Voltage			1.9		5.5	V
V_{OUT}	Output Accuracy	I_{OUT}= 1mA		-1.0		+1.0	%
I_{LIM}	Current Limit(1)			550	700		mA
I_Q	Quiescent Current	V_{IN}= V_{EN}=V_{OUT}+1V, No Load			10	15	μA
I_{SHD}	Shutdown Current	V_{EN}=0V				0.1	μA
V_{DROP}	Dropout Voltage(1) (2)	I_{OUT}=100mA, V_{OUT}=1.2V			110		mV
		I_{OUT}=500mA, V_{OUT}=1.2V			510		
		I_{OUT}=100mA, V_{OUT}=3.3V			30		
		I_{OUT}=500mA, V_{OUT}=3.3V			180		
		I_{OUT}=100mA, V_{OUT}=5V			30		
		I_{OUT}=500mA, V_{OUT}=5V			160		
ΔV_{OUT}/ (ΔV_{IN}*$V_{OUT(NOM)}$)	Line Regulation	V_{IN}= V_{OUT} +1V to 5.5V, I_{OUT}=1mA			0.05	0.25	%/V
ΔV_{OUT}	Load Regulation	1mA≤I_{OUT}≤500mA			20	60	mV
I_{SHORT}	Short Current(1)	V_{OUT}=0V			50		mA
I_{EN}	EN Pull-Down Current	V_{IN}=V_{EN} =5.5V			0.15		μA
V_{ENH}	EN High Voltage	V_{IN}=1.9V to 5.5V, I_{OUT}=1mA		1.5			V
V_{ENL}	EN Low Voltage					0.5	V
PSRR	Power Supply Rejection Ratio	V_{IN}= 4.3V, V_{OUT}=3.3V C_{IN} =None, V_{PP}=0.5V I_{OUT}=10mA	f=217Hz		90		dB
			f=1KHz		90		
			f=10KHz		88		
			f=100KHz		60		
e_n	Output Voltage Noise	f=10Hz to 100kHz, V_{IN}=4.3V, V_{OUT}=3.3V	I_{OUT}=0mA		5.3		μV_{RMS}
			I_{OUT}=10mA		5.9		
T_{SD}	Thermal Shutdown	Temperature rising			160		℃
△T_{SD}	TSD Hysteresis	Temperature falling			20		℃
R_{DSCHG}	Output Discharge Resistance	V_{IN}=5.5V, V_{EN}=0V			60		Ω

NOTES:

1. Guaranteed by design
2. The dropout voltage is defined as V_{IN} - V_{OUT}, when V_{OUT} =95%*$V_{OUT(NOM)}$

SIMPLIFIED BLOCK DIAGRAM:



DETAIL OPERATION DESCRIPTION:

The LW54XX is a low noise, high PSRR LDO voltage regulator featuring high integration and multiple protection mechanisms. It utilizes a Bandgap reference and an Error Amplifier (EA) to ensure stable output. Key modules include a Buffer for driving, a Noise Reduction block for low noise performance, and a Current Limit function for safety. Additionally, it integrates an Enable control and a Thermal Shutdown (TSD) protection feature.

Error Amplifier

The Error Amplifier (EA) compares the internal reference voltage VREF with the output feedback voltage. Output of the error amplifier (EA) is used to control the gate voltage of P-MOSFET and ensures that the device provides good line and load regulation.

Current Limit and Short Circuit Protection

LW54XX provides current limit function to prevent the device from damaging during overload or shorted-circuit condition. The output current is limited to 700mA (typ.), and the output short circuit current is limited to 50mA(typ.)

Thermal Shutdown Protection

When the junction temperature exceeds 160°C(typ.), thermal shutdown is triggered and the device turns off. When the junction temperature falls below 140°C (typ.), the device turns on again.

Soft-Start and Inrush Current Limit

The inrush current protection circuit is built in the LW54XX. During appr.650μs(typ.) after the EN pin becomes "H", the inrush current is limited at appr.250 mA.

TYPICAL OPERATING CHARACTERISTICS:

（*Tested under* T_A *=25*°C, C_{IN}=C_{OUT}=1μF, unless otherwise specified）

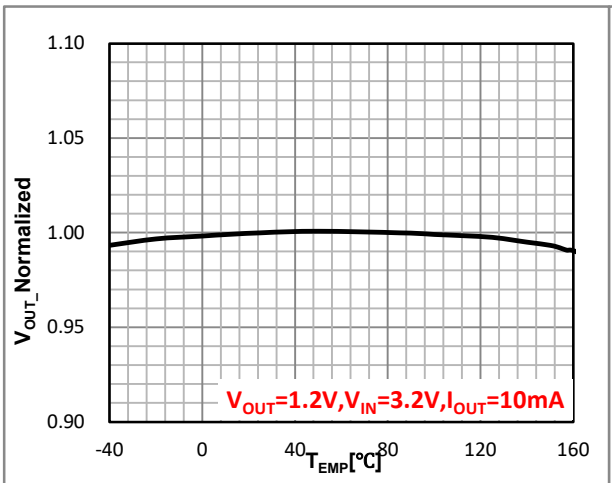


Figure 1. V_{OUT} vs Temperature

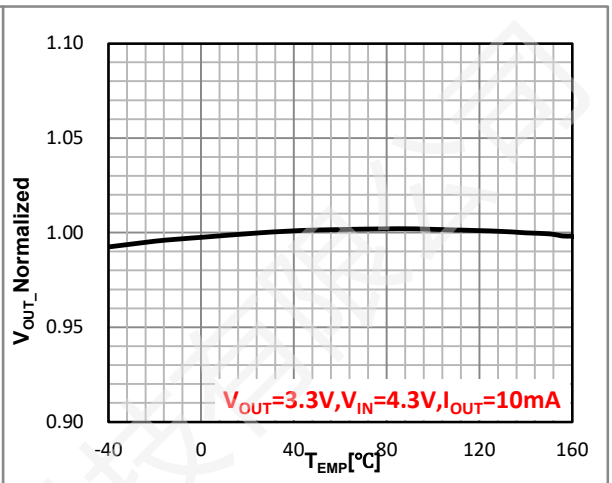


Figure 2. V_{OUT} vs Temperature

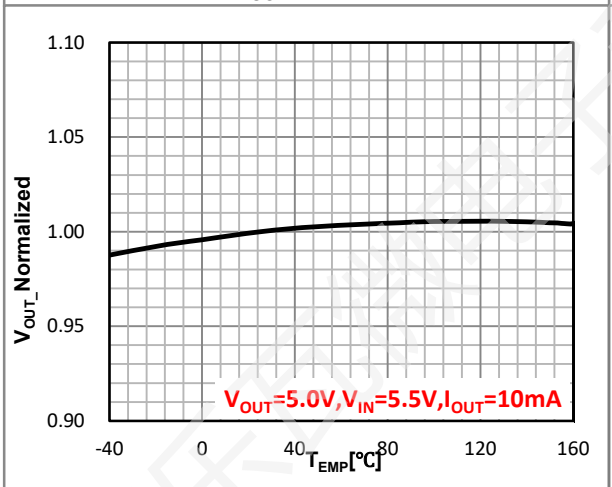


Figure 3. V_{OUT} vs Temperature

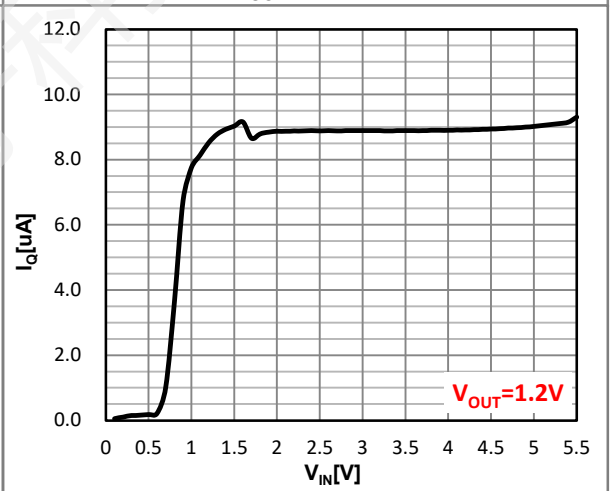


Figure 4. I_Q vs V_{IN}

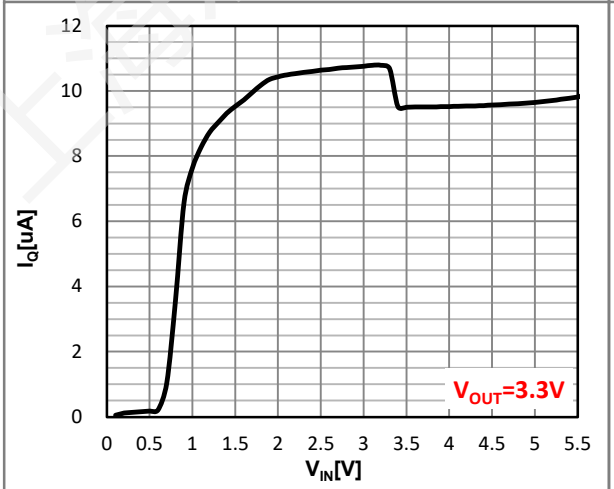


Figure 5. I_Q vs V_{IN}

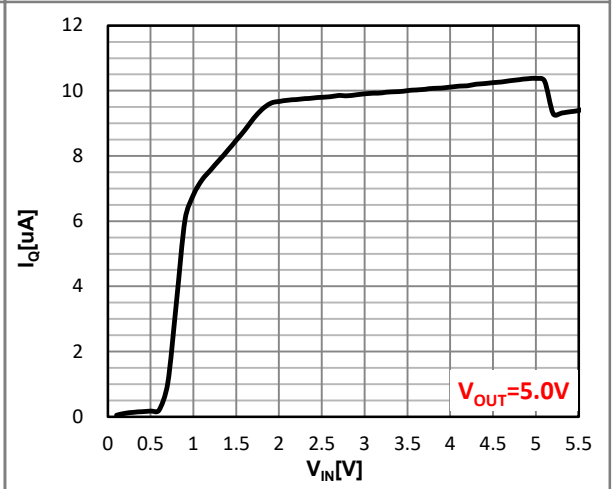


Figure 6. I_Q vs V_{IN}

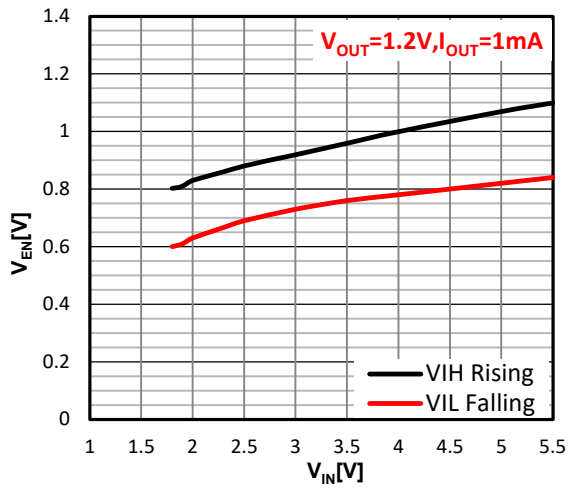


Figure 7. V_{EN} VS V_{IN}

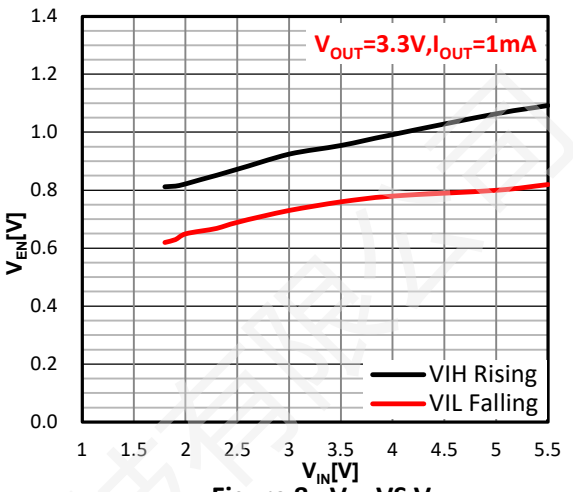


Figure 8. V_{EN} VS V_{IN}

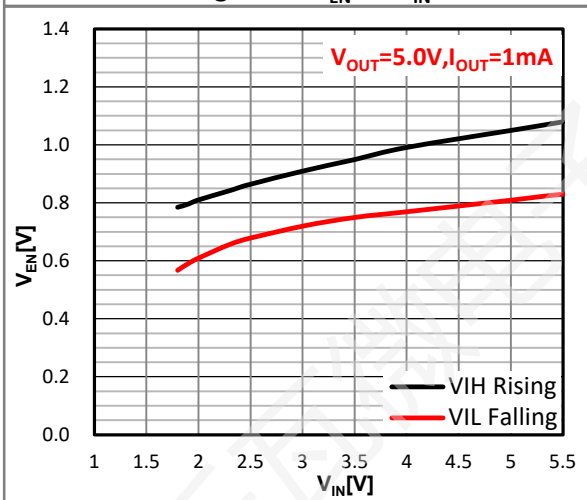


Figure 9. V_{EN} VS V_{IN}

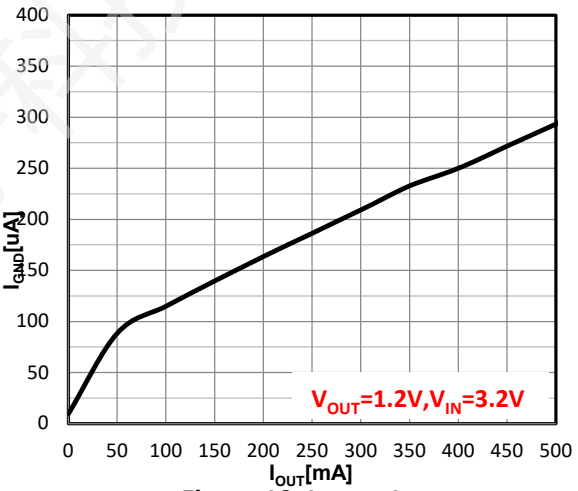


Figure 10. I_{GND} vs I_{OUT}

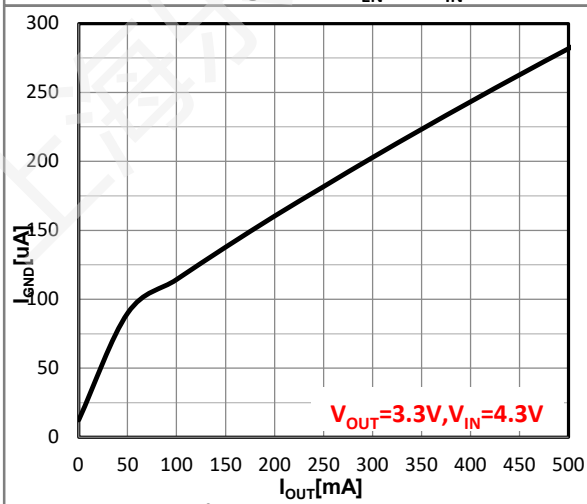


Figure 11. I_{GND} vs I_{OUT}

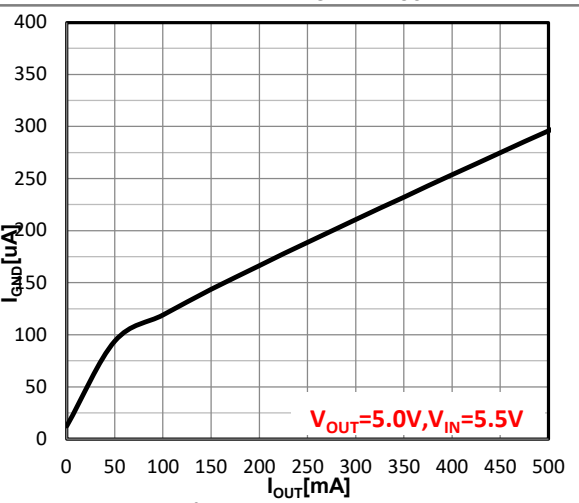


Figure 12. I_{GND} vs I_{OUT}

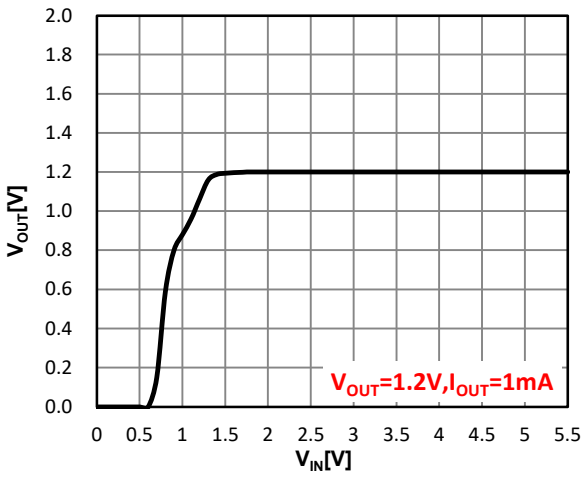


Figure 13. V_{OUT} vs V_{IN}

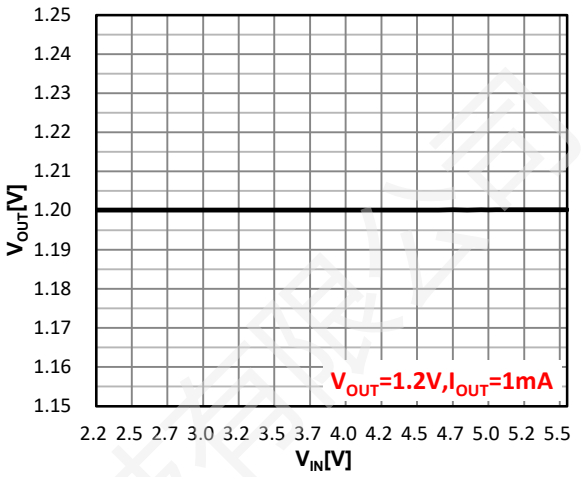


Figure 14. Line Regulation

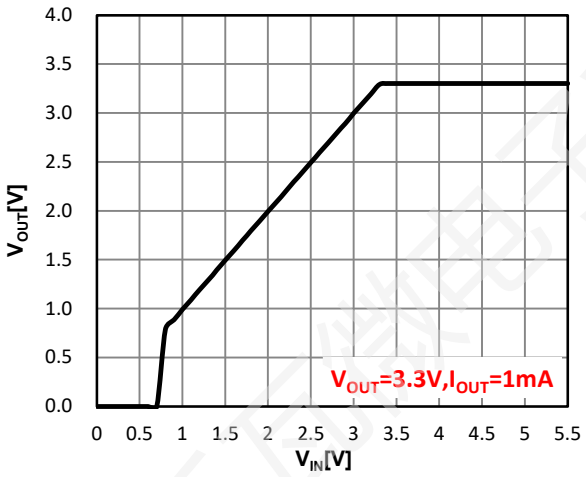


Figure 15. V_{OUT} vs V_{IN}

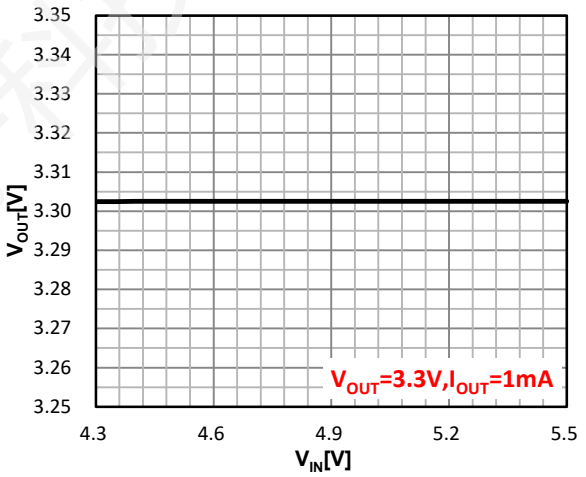


Figure 16. Line Regulation

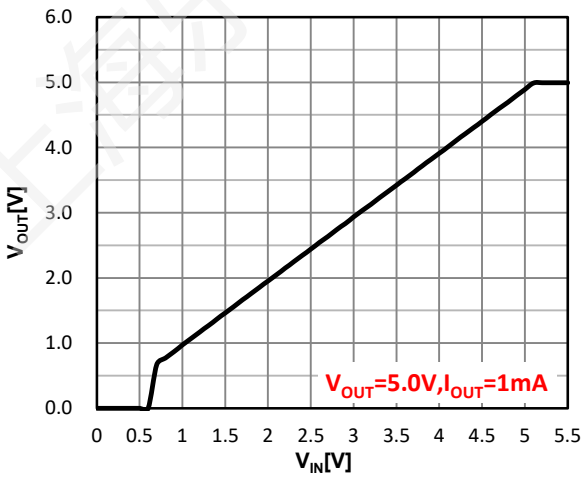


Figure 17. V_{OUT} vs V_{IN}

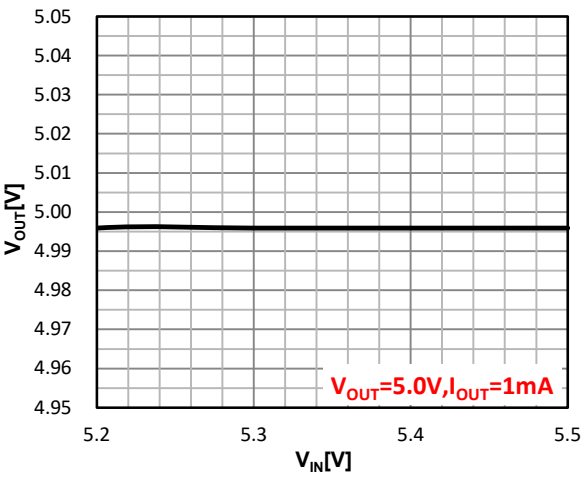


Figure 18. Line Regulation

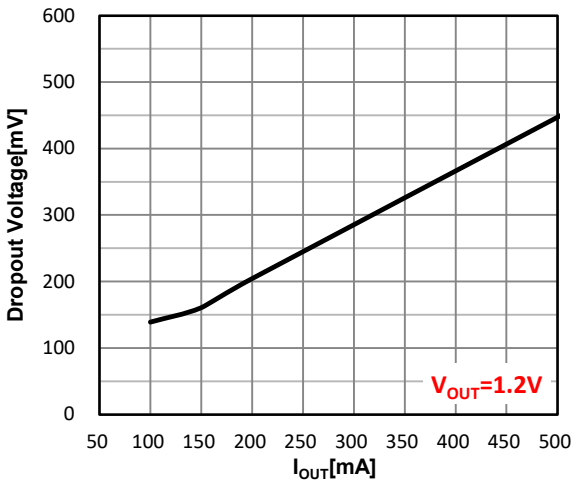


Figure 19. Dropout Voltage VS I_{OUT}

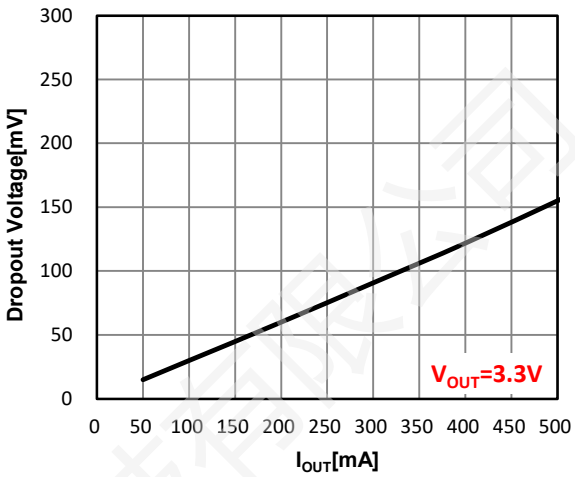


Figure 20. Dropout Voltage VS I_{OUT}

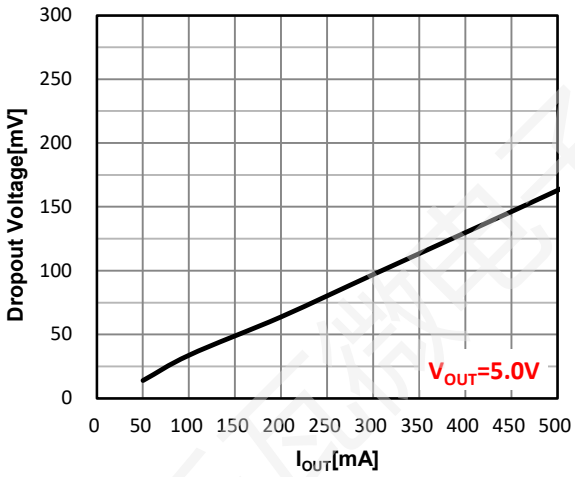


Figure 21. Dropout Voltage VS I_{OUT}

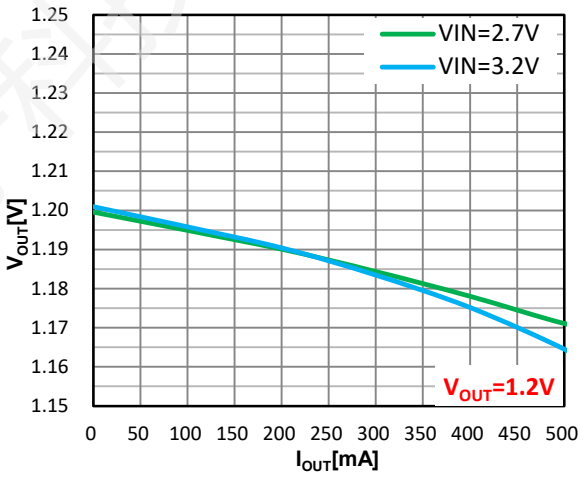


Figure 22. Load Regulation

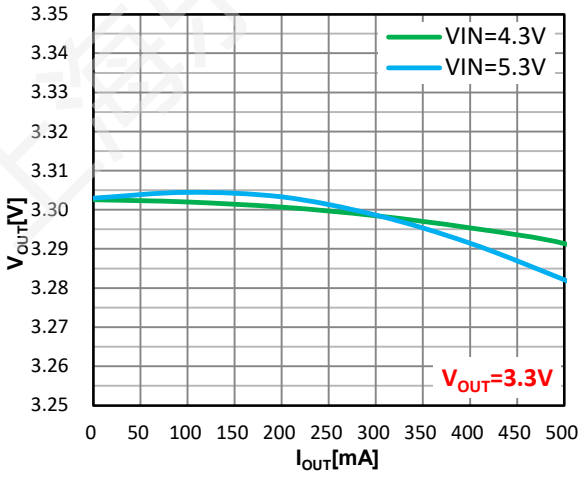


Figure 23. Load Regulation

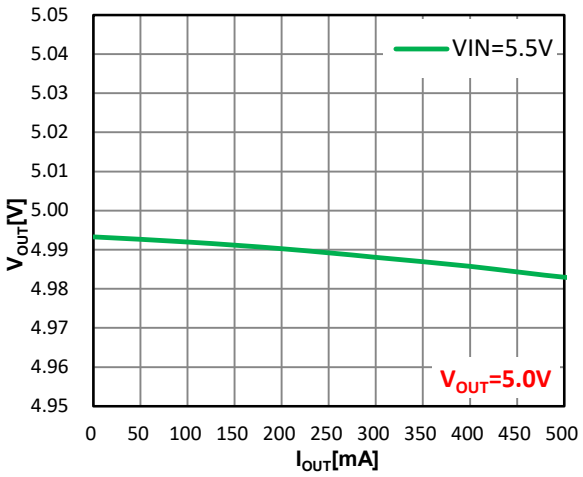
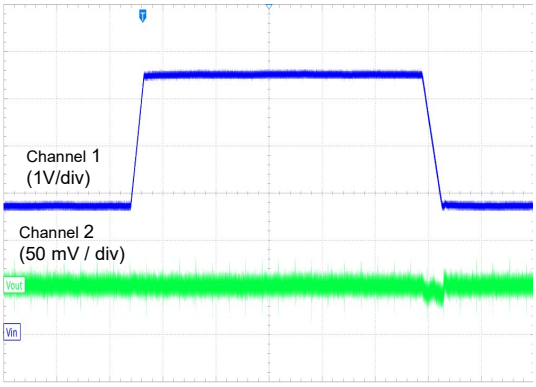


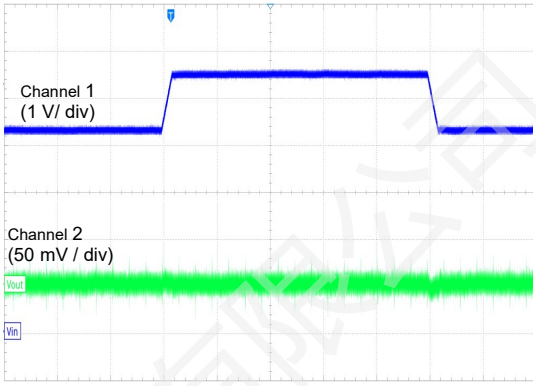
Figure 24. Load Regulation



Time (50 us / div)

Channel 1 = V_{IN}, Channel 2 =V_{OUT}, V_{IN}=2.7V→5.5V,Tr=Tf=10us, V_{OUT}=1.2V, I_{OUT}=10mA

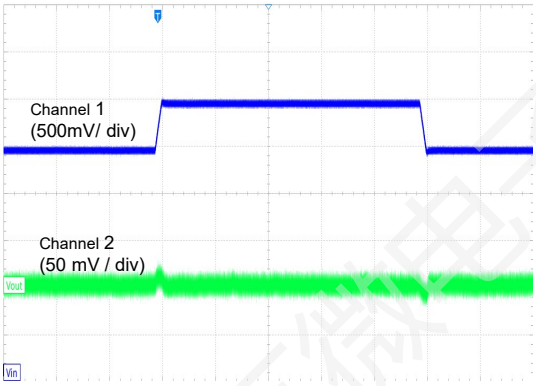
Figure 25. Line Transient



Time (50 us / div)

Channel 1 = V_{IN}, Channel 2 =V_{OUT}, V_{IN}=4.3V→5.5V,Tr=Tf=10us, V_{OUT}=3.3V, I_{OUT}=10mA

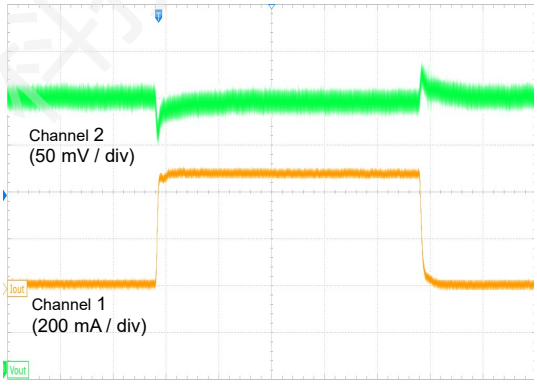
Figure 26. Line Transient



Time (100 us / div)

Channel 1 = V_{IN}, Channel 2 =V_{OUT}, V_{IN}=5.5V→6.0V,Tr=Tf=15us, V_{OUT}=5.0V, I_{OUT}=10mA

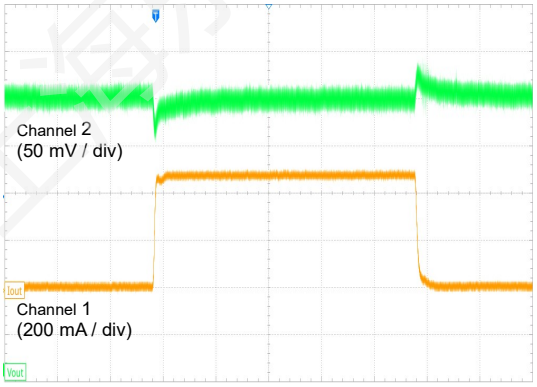
Figure 27. Line Transient



Time (200 us / div)

Channel 1 = I_{OUT}, Channel 2 =V_{OUT}, V_{IN}=3.0V, V_{OUT}=1.2V, C_{IN}= C_{OUT}=1uF

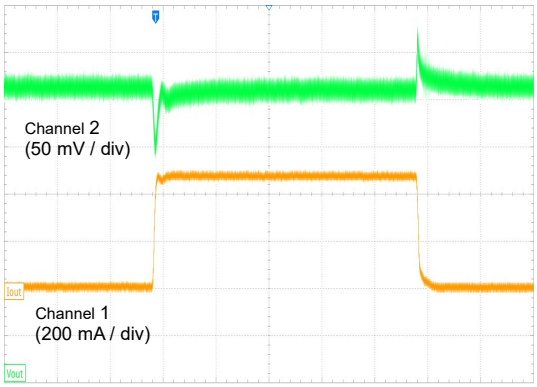
Figure 28. Load Transient (1 mA → 500 mA)



Time (200 us / div)

Channel 1 = I_{OUT}, Channel 2 =V_{OUT}, V_{IN}=4.3V, V_{OUT}=3.3V, C_{IN}= C_{OUT}=1uF

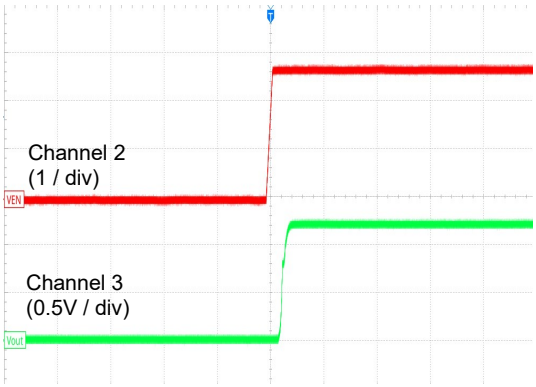
Figure 29. Load Transient (1 mA → 500 mA)



Time (200 us / div)

Channel 1 = I_{OUT}, Channel 2 =V_{OUT}, V_{IN}=5.5V, V_{OUT}=5.0V, C_{IN}= C_{OUT}=1uF

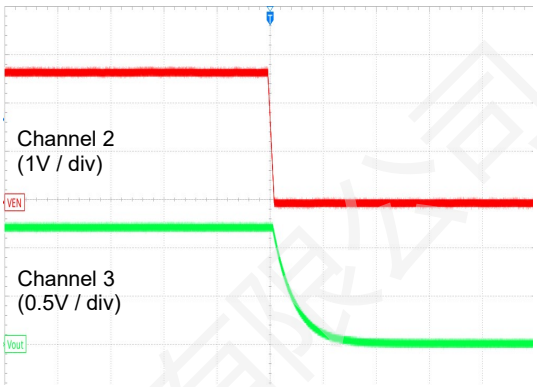
Figure 30. Load Transient (1 mA → 500 mA)



Time (200 us / div)

Channel 2 =EN, Channel 3 =V_{OUT} ,V_{IN}=2.7V, EN=0→2.7V, V_{OUT}=1.2V, C_{IN}= C_{OUT}=1uF, No Load

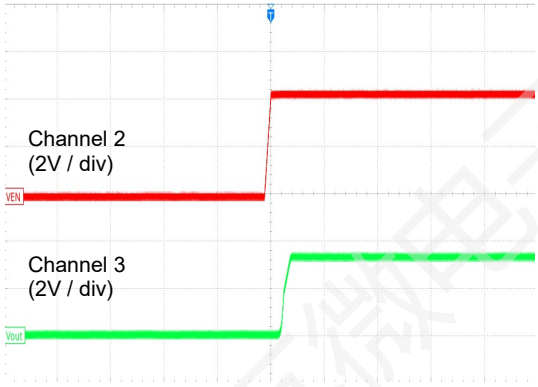
Figure 31. Start-Up with Enable



Time (200 us / div)

Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=2.7V, EN=2.7→0V, V_{OUT}=1.2V, C_{IN}= C_{OUT}=1uF,No Load

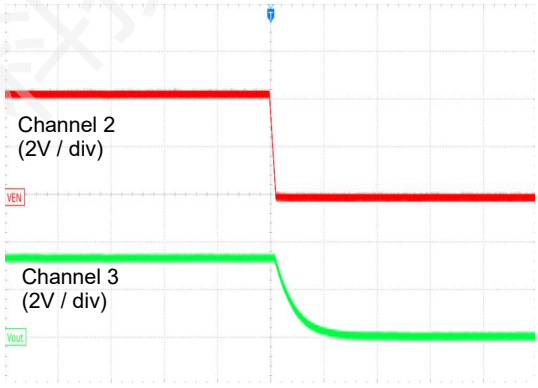
Figure 32. Shut-Down with Enable



Time (200 us / div)

Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=4.3V, EN=0→4.3V, V_{OUT}=3.3V, C_{IN}= C_{OUT}=1uF, No Load

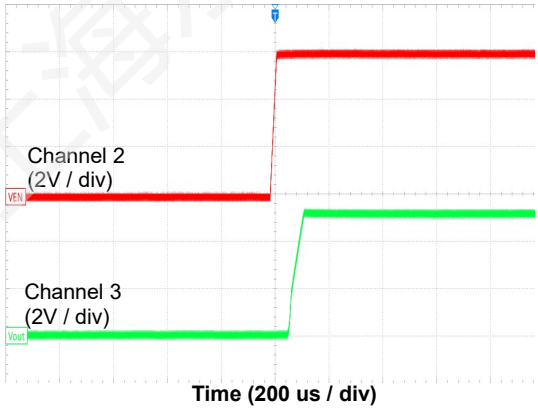
Figure 33. Start-Up with Enable



Time (200 us / div)

Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=4.3V, EN=4.3→0V, V_{OUT}=3.3V, C_{IN}= C_{OUT}=1uF, No Load

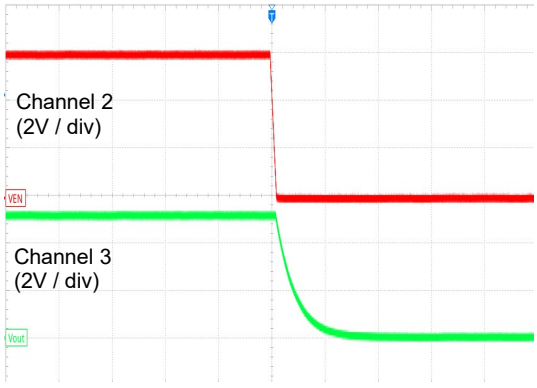
Figure 34. Shut-Down with Enable



Time (200 us / div)

Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=6.0V, EN=0→6.0V, V_{OUT}=5.0V, C_{IN}= C_{OUT}=1uF, No Load

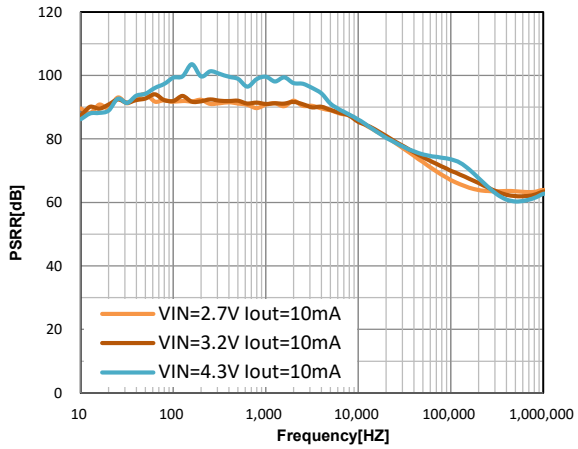
Figure 35. Start-Up with Enable



Time (200 us / div)

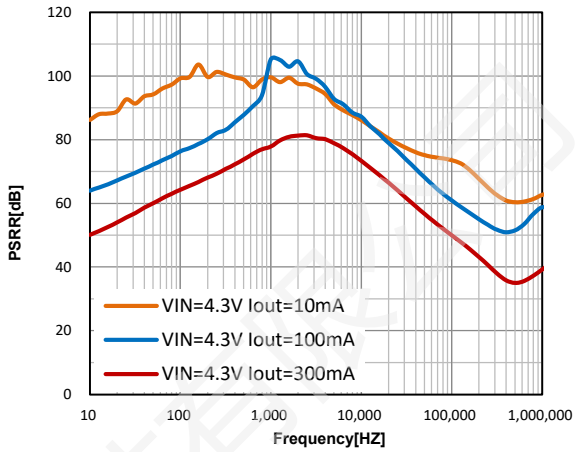
Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=6.0V, EN=6.0→0V, V_{OUT}=5.0V, C_{IN}= C_{OUT}=1uF, No Load

Figure 36. Shut-Down with Enable



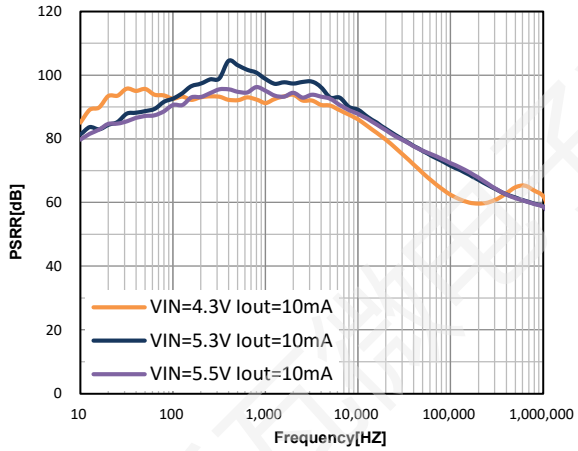
V_{OUT}=1.2V,V_{PP}=0.5V,C_{IN}=non,C_{OUT}=1uF,I_{OUT}=10mA

Figure 37. PSRR vs Frequency



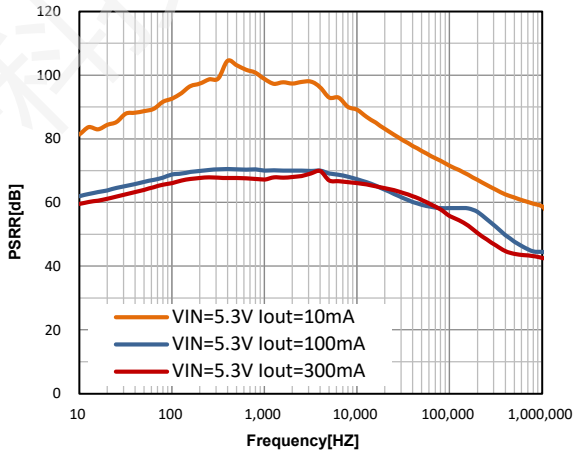
V_{OUT}=1.2V, V_{PP}=0.5V,C_{IN}=non,C_{OUT}=1uF,V_{IN}=4.3V

Figure 38. PSRR vs Frequency



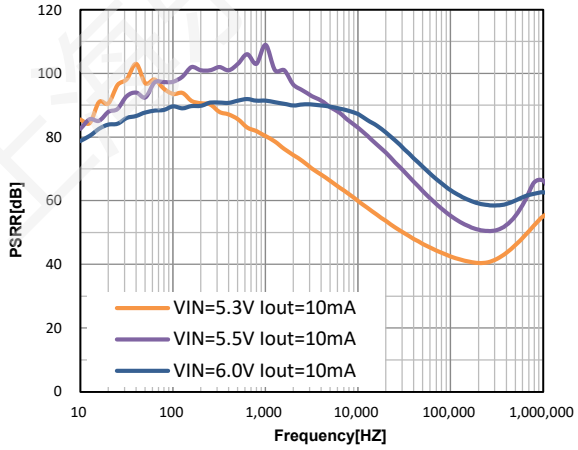
V_{OUT}=3.3V, V_{PP}=0.5V,C_{IN}=non, C_{OUT}=1uF,I_{OUT}=10mA

Figure 39. PSRR vs Frequency



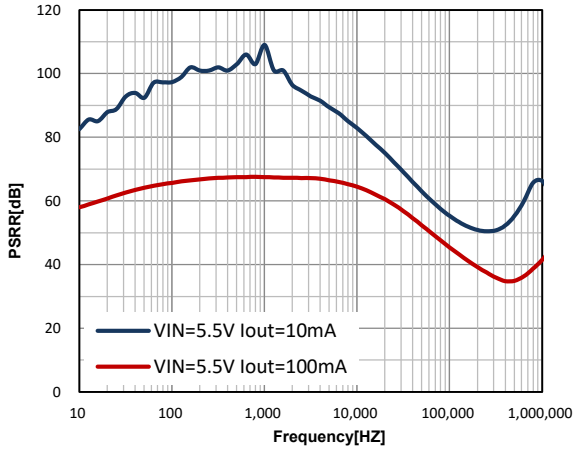
V_{OUT}=3.3V, V_{PP}=0.5V,C_{IN}=non, C_{OUT}=1uF,V_{IN}=5.3V

Figure 40. PSRR vs Frequency



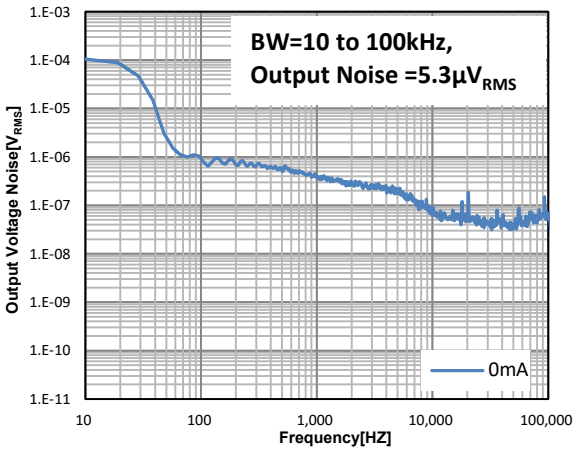
V_{OUT}=5.0V, V_{PP}=0.5V,C_{IN}=non, C_{OUT}=1uF,I_{OUT}=10mA

Figure 41. PSRR vs Frequency



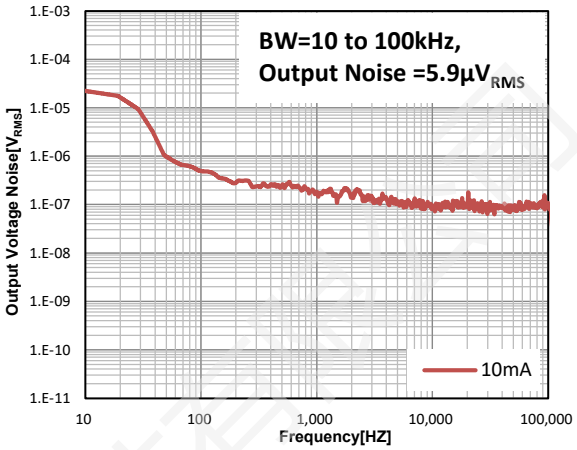
V_{OUT}=5.0V, V_{PP}=0.5V,C_{IN}=non, C_{OUT}=1uF,V_{IN}=5.5V

Figure 42. PSRR vs Frequency



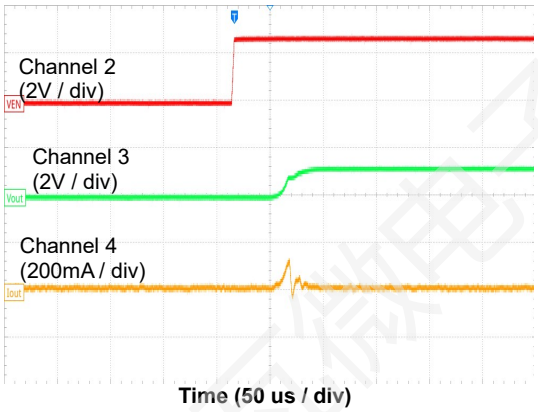
V_{in}=4.3V,V_{OUT}=3.3V, C_{IN}=1uF, C_{OUT}=1uF, I_{OUT}=0mA

Figure 43. Noise vs Frequency



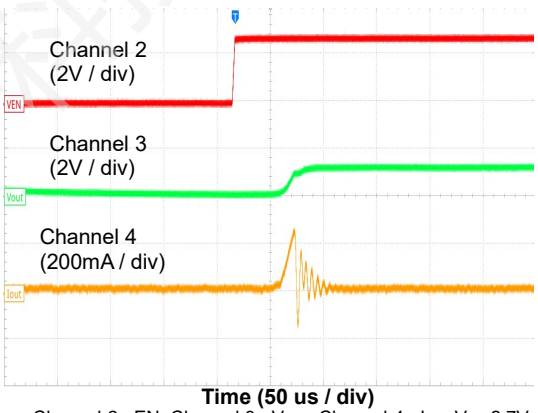
V_{in}=4.3V,V_{OUT}=3.3V, C_{IN}=1uF, C_{OUT}=1uF,I_{OUT}=10mA

Figure 44. Noise vs Frequency



Channel 2 =EN, Channel 3 =V_{OUT} ,Channel4 =I_{OUT},V_{IN}=2.7V,
EN=0→2.7V, V_{OUT}=1.2V, C_{IN}=1uF, C_{OUT}=1uF, No Load

Figure 45. Inrush Current

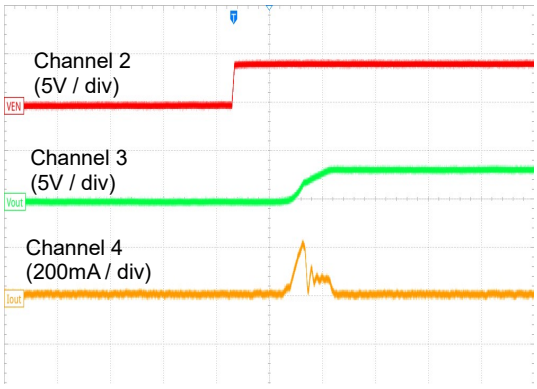


Channel 2 =EN, Channel 3 =V_{OUT} ,Channel 4 =I_{OUT},V_{IN}=2.7V,
EN=0→2.7V, V_{OUT}=1.2V, C_{IN}=1uF, C_{OUT}=2.2uF, No Load

Figure 46. Inrush Current

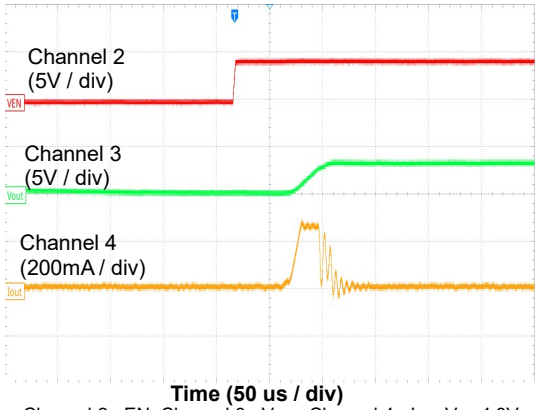
Channel 2 =EN, Channel 3 =V_{OUT} ,Channel 4 =I_{OUT},V_{IN}=2.7V,
EN=0→2.7V, V_{OUT}=1.2V, C_{IN}=1uF, C_{OUT}=10uF, No Load

Figure 47. Inrush Current



Channel 2 =EN, Channel 3 =V_{OUT} ,Channel 4 =I_{OUT} ,V_{IN}=4.3V,
EN=0→4.3V, V_{OUT}=3.3V, C_{IN}=1uF, C_{OUT}=1uF, No Load

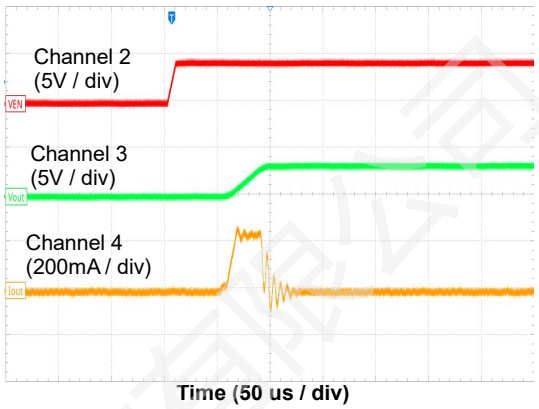
Figure 48. Inrush Current



Time (50 us / div)

Channel 2 =EN, Channel 3 =V_{OUT} ,Channel 4 =I_{OUT},V_{IN}=4.3V, EN=0→4.3V, V_{OUT}=3.3V, C_{IN}=1uF, C_{OUT}=2.2uF, No Load

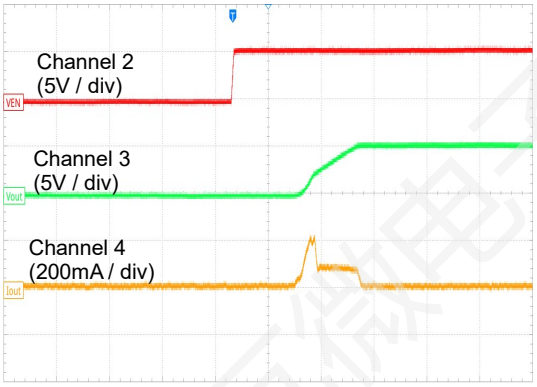
Figure 48. Inrush Current



Time (50 us / div)

Channel 2 =EN, Channel 3 =V_{OUT} ,Channel 4 =I_{OUT},V_{IN}=4.3V, EN=0→4.3V, V_{OUT}=3.3V, C_{IN}=1uF, C_{OUT}=10uF, No Load

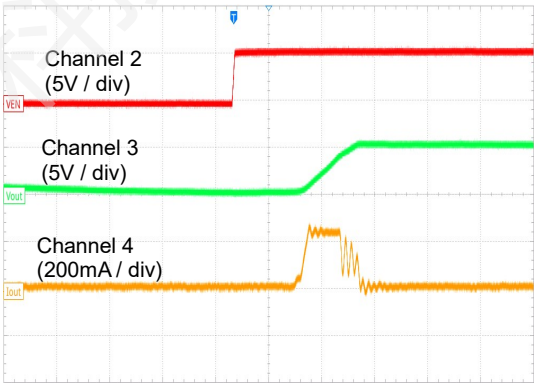
Figure 49. Inrush Current



Time (50 us / div)

Channel 2 =EN, Channel 3 =V_{OUT} ,Channel 4 =I_{OUT},V_{IN}=5.5V, EN=0→5.5V, V_{OUT}=5.0V, C_{IN}=1uF, C_{OUT}=1uF, No Load

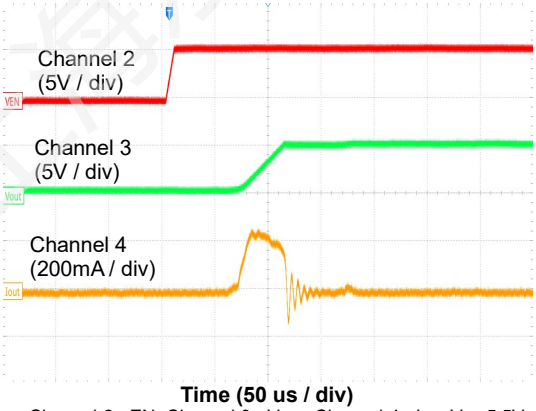
Figure 50. Inrush Current



Time (50 us / div)

Channel 2 =EN, Channel 3 =V_{OUT} ,Channel 4 =I_{OUT},V_{IN}=5.5V, EN=0→5.5V, V_{OUT}=5.0V, C_{IN}=1uF, C_{OUT}=2.2uF, No Load

Figure 51. Inrush Current



Time (50 us / div)

Channel 2 =EN, Channel 3 =V_{OUT} ,Channel 4 =I_{OUT},V_{IN}=5.5V, EN=0→5.5V, V_{OUT}=5.0V, C_{IN}=1uF, C_{OUT}=10uF, No Load

Figure 52. Inrush Current

APPLICATION INFORMATION:

- **Input Capacitor Selection**

Like any low-dropout regulator, the external capacitors used with the LW54XX Series must be carefully selected for regulator stability and performance. Using a capacitor whose value is >=1μF on the LW54XX Series input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance less than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

- **Output Capacitor Selection**

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LW54XX Series is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF on the LW54XX Series output ensures stability. An appropriate output capacitor can reduce noise and improve load transient response and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the LW54XX Series and returned to a clean analog ground.

- **Layout considerations**

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the PCB be designed with separate ground planes for VIN and VOUT, with each ground plane connected only at the GND pin of the device.

ORDER INFORMATION:

LW54①②③④⑤⑥

Designator	Item	Symbol	Description
①②	Output Voltage	12~50	e.g.1.2V→①=1,②=2
③④⑤⑥	Packages	A23E	SOT23-5L
		N11E	DFN1x1-4L
		N22G	DFN2x2-6L

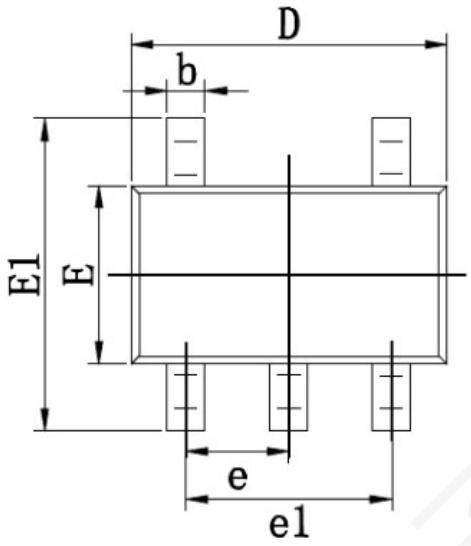
Part #	Output Voltage	Package	Shipping
LW5412A23E	1.2V	SOT23-5L	3000 Pcs/ Tape & Reel
LW5415A23E	1.5V		
LW5418A23E	1.8V		
LW5425A23E	2.5V		
LW5428A23E	2.8V		
LW5430A23E	3.0V		
LW5433A23E	3.3V		
LW5436A23E	3.6V		
LW5442A23E	4.2V		
LW5450A23E	5.0V		
LW5412N11E	1.2V	DFN1x1-4L	10000 Pcs/ Tape & Reel
LW5415N11E	1.5V		
LW5418N11E	1.8V		
LW5425N11E	2.5V		
LW5428N11E	2.8V		
LW5430N11E	3.0V		
LW5433N11E	3.3V		
LW5436N11E	3.6V		
LW5442N11E	4.2V		
LW5450N11E	5.0V		

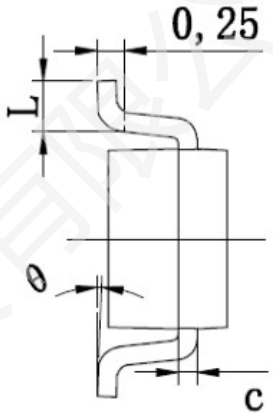
Part #	Output Voltage	Package	Shipping
LW5412N22G	1.2V	DFN2x2-6L	3000 Pcs/ Tape & Reel
LW5415N22G	1.5V		
LW5418N22G	1.8V		
LW5425N22G	2.5V		
LW5428N22G	2.8V		
LW5430N22G	3.0V		
LW5433N22G	3.3V		
LW5436N22G	3.6V		
LW5442N22G	4.2V		
LW5450N22G	5.0V		

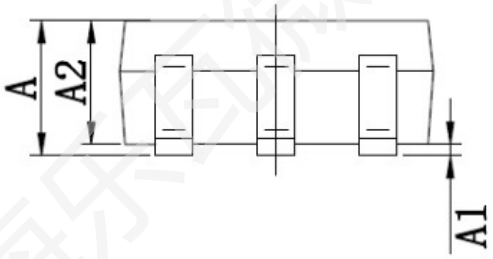
If customers have special output voltage requirements, please contact us.

PACKAGE OUTLINE:

SOT23-5L Package

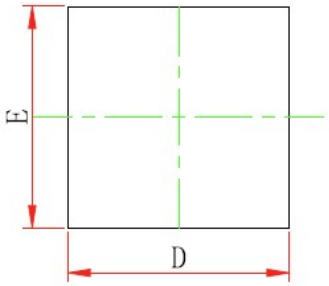




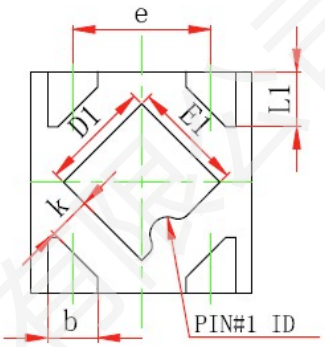


COMMON DIMENSION (MM)			
PKG	SOT23-5L		
Symbol	MIN	NOM	MAX
A	—	—	1.300
A1	0.010	—	0.150
A2	1.050	1.100	1.150
b	0.300	0.350	0.400
c	0.125	0.150	0.175
D	2.870	2.920	2.980
E	1.550	1.610	1.670
E1	2.650	2.850	3.000
e	0.95 BSC		
e1	1.800	1.900	2.000
L	0.300	0.450	0.600
θ	0°	4°	8°

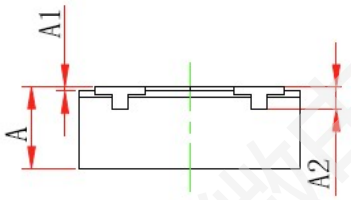
DFN1x1-4L Package



TOP VIEW
[顶视图]



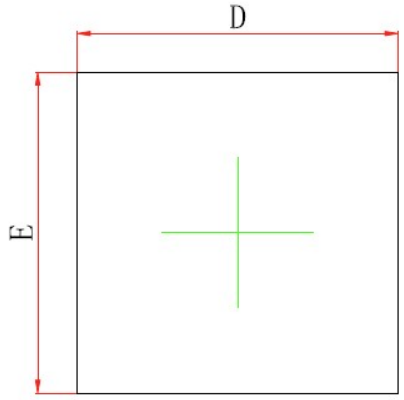
BOTTOM VIEW
[背视图]



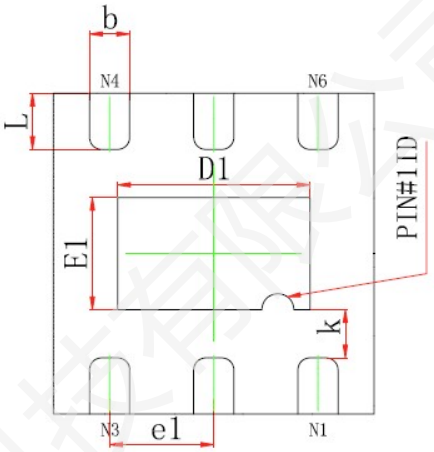
SIDE VIEW
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.335	0.405	0.013	0.016
A1	0.000	0.050	0.000	0.002
A2	0.100REF.		0.004REF.	
D	0.950	1.050	0.037	0.041
E	0.950	1.050	0.037	0.041
D1	0.450	0.550	0.018	0.022
E1	0.450	0.550	0.018	0.022
k	0.195REF.		0.0077REF.	
b	0.175	0.275	0.007	0.011
e	0.575	0.675	0.023	0.027
L1	0.200	0.300	0.008	0.012

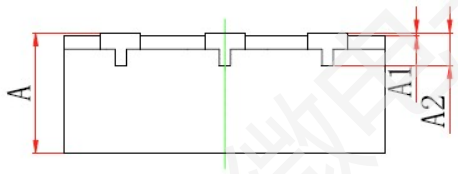
DFN2x2-6L Package



TOP VIEW
[顶视图]



BOTTOM VIEW
[背视图]



SIDE VIEW
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203REF.		0.008REF.	
D	1.924	2.076	0.076	0.082
E	1.924	2.076	0.076	0.082
D1	1.150	1.250	0.045	0.049
E1	0.650	0.750	0.026	0.030
b	0.200	0.300	0.008	0.012
e1	0.650TYP.		0.026TYP.	
k	0.200MIN.		0.008MIN.	
L	0.300	0.400	0.012	0.016

Revision History:

Revision	Date	Descriptions
Rev 1.0	Aug.2023	Released Version
Rev 1.1	Nov.2023	Update New Package (DFN2x2-6L)
Rev 1.2	May.2026	Update New Typical Operating Characteristics

DISCLAIMER:

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