钍地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65HVD10/ 65HVD11/ 65HVD12 /75HVD10/75HVD11/75HVD12

3.3V RS-485 transceiver

网址 www.sztdbdt.com

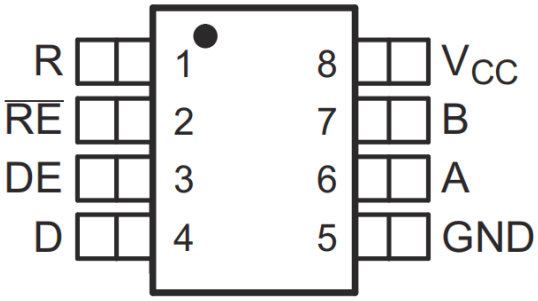
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- Powered by 3.3V supply
- Bus pin ESD protection exceeds 16kV HBM
- 1/8 unit option available (up to 256 nodes on the bus)
- Optional driver output slew rates of 11 Mbps, 10 Mbps, and 32
- Meets or exceeds ANSI TIA/EIA-485-A requirements
- – 7V to 12V bus pin short-circuit protection
- Low current standby mode: 1 μ A, typical
- Open-circuit, idle bus, and shorted bus fail-safe receivers
- Thermal shutdown protection
- Glitch-free power- and power-down protection for hot-plug applications ? SN75176 package



D, JD, or HKJ Package
8- Pin SOIC or PDIP
(Top View)

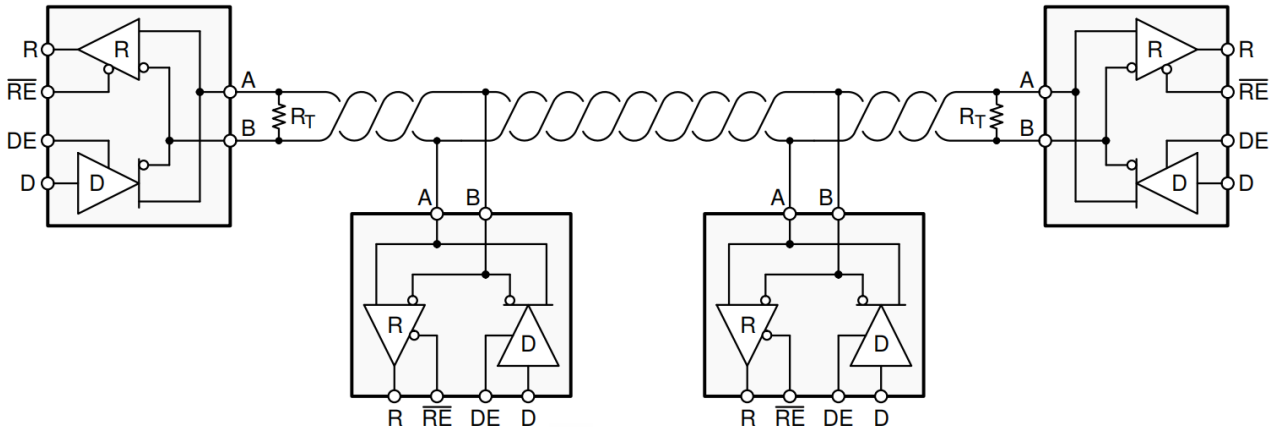
Applications

- Digital motor control
- Utility meters
- Chassis-to-chassis interconnects
- Electronic security stations
- Industrial process control
- Building
- Point-of-sale (POS) terminals and networks

Description

The SN65HVD10, SN75HVD10, SN65HVD11, SN5HVD11, SN65HVD12, and SN75HVD12 bus transceivers all integrate a three-state differential line driver and a input line receiver powered by a 3.3V single supply. These devices are designed for balanced transmission lines and meet or exceed ANSI standards TIA/EIA-48-A and ISO 8482:1993. These differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multi-point bus transmission. The drivers and receivers have active-high and active-low enable pins, which can be externally connected to be used for direction control. Extremely low device standby current can be achieved disabling the driver and receiver.

The driver differential outputs and receiver differential inputs are internally connected to form a differential input/output (I/O) bus port, which is designed to a minimal load to the bus when the driver is disabled or V_{CC} = 0. These devices have a wide positive and negative common-mode voltage range, making them suitable for coline applications.



典型应用图

表 **6-1. Pin Functions**

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Active-high driver enable
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Active-low receiver enable
V_{CC}	8	Supply	3-V to 3.6-V supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted (1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
	Voltage at A or B	–9	14	V
	Input voltage at D, DE, R, or $\overline{RE}$	–0.5	V_{CC} + 0.5	V
	Voltage input, transient pulse, A and B, through 100 Ω, see 图 8-12	–50	50	V
I_O	Receiver output current	–11	11	mA
	Continuous total power dissipation	See 节 7.10		
T_J	Junction temperature		170	°C
T_{stg}	Storage temperature	–55	145	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 7.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Pins 5, 6, and 7	±16000	V
			All pins	±4000	
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±1000	
		Electrical fast transient/burst(3)	Pins 5, 6, and 7	±4000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Tested in accordance with IEC 61000-4-4.

7.3 Recommended Operating Conditions

over operating free-air temperature range unless otherwise noted

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		3.6	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–7(1)		12	
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	
V_{IL}	Low-level input voltage	D, DE, $\overline{RE}$	0		0.8	
V_{ID}	Differential input voltage	See 图 8-8	–12		12	
I_{OH}	High-level output current	Driver	–60			mA
		Receiver	–8			
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
	Signaling rate	HVD10			32	Mbps
		HVD11			10	
		HVD12			1	
T_J (2)	Junction temperature				145	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

(2) See thermal characteristics table for information regarding this specification.

7.4 Thermal Information

THERMAL METRIC(1)		SNx5HVD1xx		UNIT
		D (SOIC)	P (PDIP)	
		8 Pins	8 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	84.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	65.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	62.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	31.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	60.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Driver Electrical Characteristics

Over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = − 18 mA		− 1.5			V
$\lvert V_{OD}\rvert$	Differential output voltage(2)		I_O = 0		2		V_{CC}	V
			R_L = 54 Ω, See 图 8-1		1.5			
			V_{test} = − 7 V to 12 V, See 图 8-2		1.5			
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage		See 图 8-1 and 图 8-2		− 0.2		0.2	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage		See 图 8-3			400		mV
$V_{OC(SS)}$	Steady-state common-mode output voltage				1.4		2.5	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage				− 0.05		0.05	V
I_{OZ}	High-impedance output current		See receiver input currents					
I_I	Input current	D			− 100		0	μA
		DE			0		100	
I_{OS}	Short-circuit output current		− 7 V ≤ V_O ≤ 12 V		− 250		250	mA
$C_{(OD)}$	Differential output capacitance		V_{OD} = 0.4 sin(4E6 π t) + 0.5 V, DE at 0 V			16		pF
I_{CC}	Supply current		$\overline{RE}$ at V_{CC}, D and DE at V_{CC}, No load	Receiver disabled and driver enabled		9	15.5	mA
			$\overline{RE}$ at V_{CC}, D at V_{CC}, DE at 0 V, No load	Receiver disabled and driver disabled (standby)		1	5	μA
			$\overline{RE}$ at 0 V, D and DE at V_{CC}, No load	Receiver enabled and driver enabled		9	15.5	mA

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) For T_A > 85°C, V_{CC} is ±5%.

7.6 Receiver Electrical Characteristics

Over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = －8 mA			－0.065	－0.01	V
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA		－0.2	－0.1		V
V_{hys}	Hysteresis voltage (V_{IT+} － V_{IT-})				35		mV
V_{IK}	Enable-input clamp voltage	I_I = －18 mA		－1.5			V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = －8 mA, see 图 8-8		2.4			V
V_{OL}	Low-level output voltage	V_{ID} = －200 mV, I_{OL} = 8 mA, see 图 8-8				0.4	V
I_{OZ}	High-impedance-state output current	V_O = 0 or V_{CC}, $\overline{RE}$ at V_{CC}		－1		1	μA
I_I	Bus input current	V_A or V_B = 12 V	HVD11, HVD12, Other inputs at 0 V		0.05	0.11	mA
		V_A or V_B = 12 V, V_{CC} = 0 V			0.06	0.13	
		V_A or V_B = －7 V		－0.1	－0.05		
		V_A or V_B = －7 V, V_{CC} = 0 V		－0.05	－0.04		
		V_A or V_B = 12 V	HVD10, Other inputs at 0 V		0.2	0.5	mA
		V_A or V_B = 12 V, V_{CC} = 0 V			0.25	0.5	
		V_A or V_B = －7 V		－0.4	－0.2		
		V_A or V_B = －7 V, V_{CC} = 0 V		－0.4	－0.15		
I_{IH}	High-level input current, $\overline{RE}$	V_{IH} = 2 V		－30		0	μA
I_{IL}	Low-level input current, $\overline{RE}$	V_{IL} = 0.8 V		－30		0	μA
C_{ID}	Differential input capacitance	V_{ID} = 0.4 sin(4E6 π t) + 0.5 V, DE at 0 V			15		pF
I_{CC}	Supply current	$\overline{RE}$ at 0 V, D and DE at 0 V, No load	Receiver enabled and driver disabled		4	8	mA
		$\overline{RE}$ at V_{CC}, D at V_{CC}, DE at 0 V, No load	Receiver disabled and driver disabled (standby)		1	5	μA
		$\overline{RE}$ at 0 V, D and DE at V_{CC}, No load	Receiver enabled and driver enabled		9	15.5	mA

(1) All typical values are at 25°C and with a 3.3-V supply.

7.7 Power Dissipation Characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_D	Device power dissipation	R_L= 60 Ω, C_L = 50 pF, DE at V_{CC}, $\overline{RE}$ at 0 V, Input to D is a 50% duty-cycle square wave at indicated signaling rate	HVD10 (32Mbps)		198	250	mW
			HVD11 (10Mbps)		141	176	
			HVD12 (500 kbps)		133	161	
T_A	Ambient air temperature(1)	High-K board, no airflow	D pkg	－40		116	°C
		No airflow(2)	P pkg	－40		123	
T_{JSD}	Thermal shutdown junction temperature(1)				165		°C

(1) See 节 12.3.1 section for an explanation of these parameters.
(2) JESD51−10, Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements.

7.8 Driver Switching Characteristics

Over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	HVD10	R_L = 54 Ω, C_L = 50 pF See 图 8-4	5	8.5	16	ns
		HVD11		18	25	40	
		HVD12		135	200	300	
t_{PHL}	Propagation delay time, high-to-low-level output	HVD10		5	8.5	16	ns
		HVD11		18	25	40	
		HVD12		135	200	300	
t_r	Differential output signal rise time	HVD10		3	4.5	10	ns
		HVD11		10	20	30	
		HVD12		100	170	300	
t_f	Differential output signal fall time	HVD10		3	4.5	10	ns
		HVD11		10	20	30	
		HVD12		100	170	300	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	HVD10				1.5	ns
		HVD11				2.5	
		HVD12				7	
$t_{sk(pp)}$ (2)	Part-to-part skew	HVD10				6	ns
		HVD11				11	
		HVD12				100	
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	HVD10	R_L = 110 Ω, $\overline{RE}$ at 0 V See 图 8-5			31	ns
		HVD11				55	
		HVD12				300	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	HVD10				25	ns
		HVD11				55	
		HVD12				300	
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	HVD10	R_L = 110 Ω, $\overline{RE}$ at 0 V See 图 8-6			26	ns
		HVD11				55	
		HVD12				300	
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	HVD10				26	ns
		HVD11				75	
		HVD12				400	
t_{PZH}	Propagation delay time, standby-to-high-level output		R_L = 110 Ω, $\overline{RE}$ at 3 V See 图 8-5			6	μs
t_{PZL}	Propagation delay time, standby-to-low-level output		R_L = 110 Ω, $\overline{RE}$ at 3 V See 图 8-6			6	μs

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

7.9 Receiver Switching Characteristics

Over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	HVD10	V_{ID} = – 1.5 V to 1.5 V C_L = 15 pF See 图 8-9	12.5	20	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output	HVD10		12.5	20	25	
t_{PLH}	Propagation delay time, low-to-high-level output	HVD11 HVD12		30	55	70	ns
t_{PHL}	Propagation delay time, high-to-low-level output	HVD11 HVD12		30	55	70	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	HVD10				1.5	ns
		HVD11				4	
		HVD12				4	
$t_{sk(pp)}$ (2)	Part-to-part skew	HVD10				8	ns
		HVD11				15	
		HVD12				15	
t_r	Output signal rise time		C_L = 15 pF See 图 8-9	1	2	5	ns
t_f	Output signal fall time			1	2	5	
t_{PZH} (1)	Output enable time to high level		C_L = 15 pF, DE at 3 V See 图 8-10			15	ns
t_{PZL} (1)	Output enable time to low level					15	
t_{PHZ}	Output disable time from high level					20	
t_{PLZ}	Output disable time from low level					15	
t_{PZH} (2)	Propagation delay time, standby-to-high-level output		C_L = 15 pF, DE at 0 See 图 8-11			6	μs
t_{PZL} (2)	Propagation delay time, standby-to-low-level output					6	

(1) All typical values are at 25°C and with a 3.3-V supply

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

7.10 Dissipation Ratings

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D(2)	597 mW	4.97 mW/°C	373 mW	298 mW	100 mW
D(3)	990 mW	8.26 mW/°C	620 mW	496 mW	165 mW
P	1290 mW	10.75 mW/°C	806 mW	645 mW	215 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

(2) Tested in accordance with the Low-K thermal metric definitions of EIA/JESD51-3.

(3) Tested in accordance with the High-K thermal metric definitions of EIA/JESD51-7.

8 Parameter Measurement Information

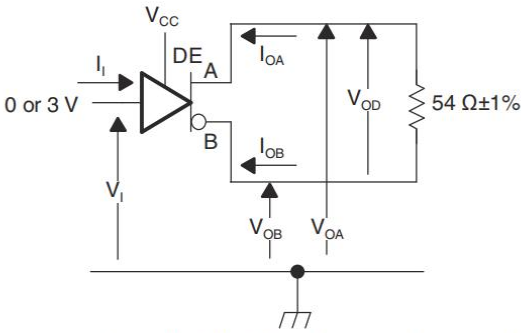


图 8-1. Driver V_{OD} Test Circuit and Voltage and Current Definitions

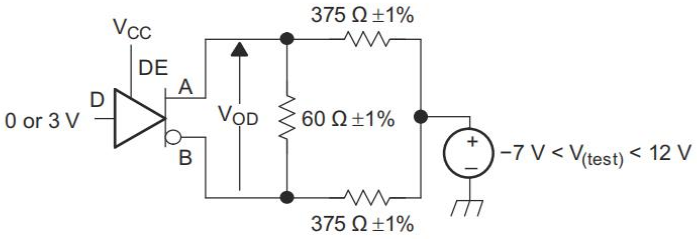
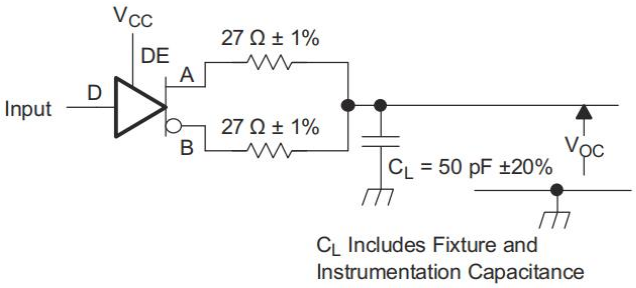
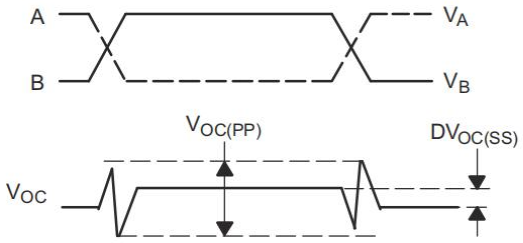


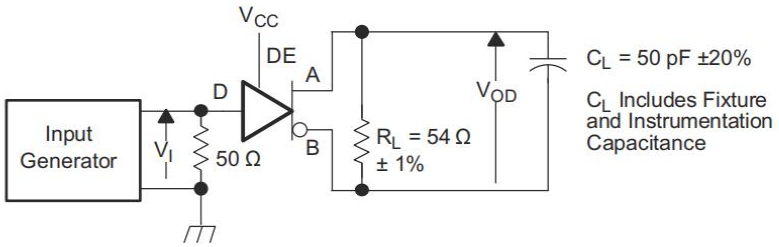
图 8-2. Driver V_{OD} With Common-Mode Loading Test Circuit

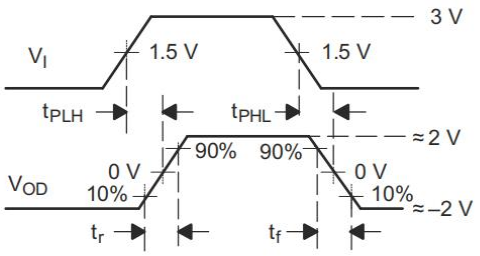




Input: PRR = 500 kHz, 50% Duty Cycle, t_r < 60 ns, t_f < 6 ns Z_O = 50 Ω

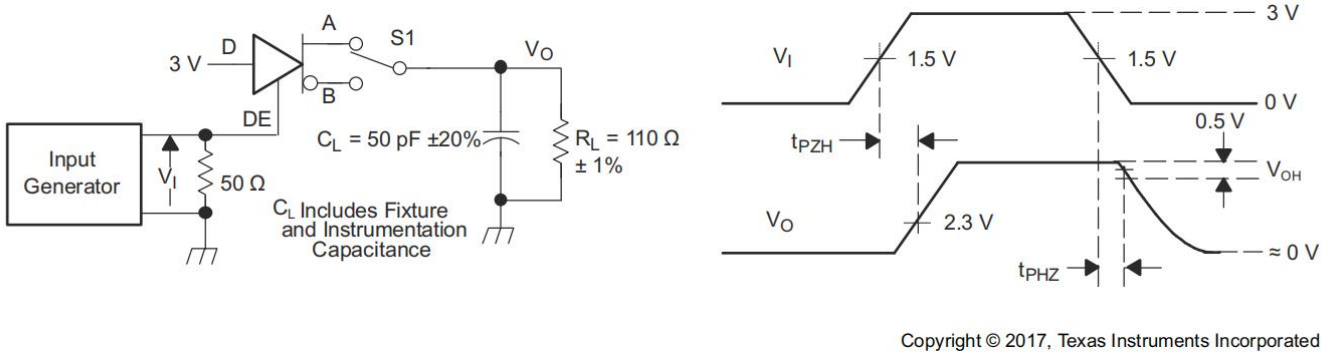
图 8-3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage





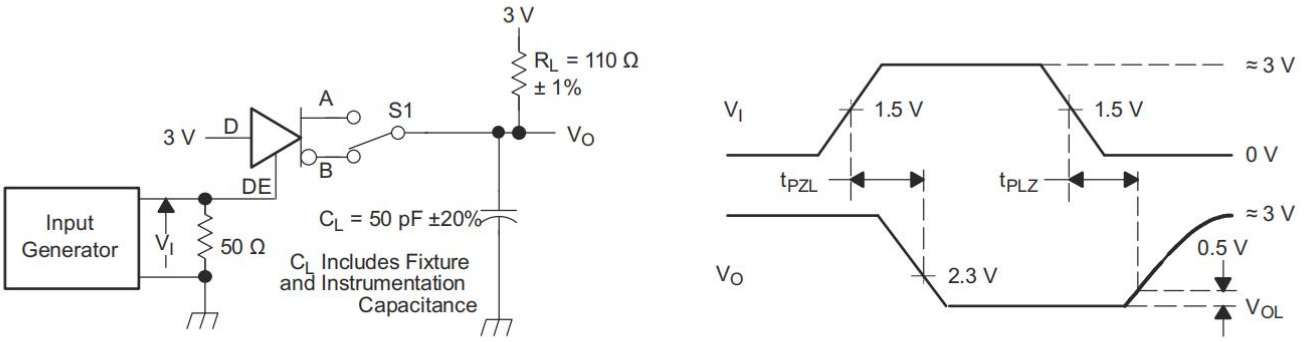
Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 60 ns, t_f < 6 ns Z_O = 50 Ω

图 8-4. Driver Switching Test Circuit and Voltage Waveforms



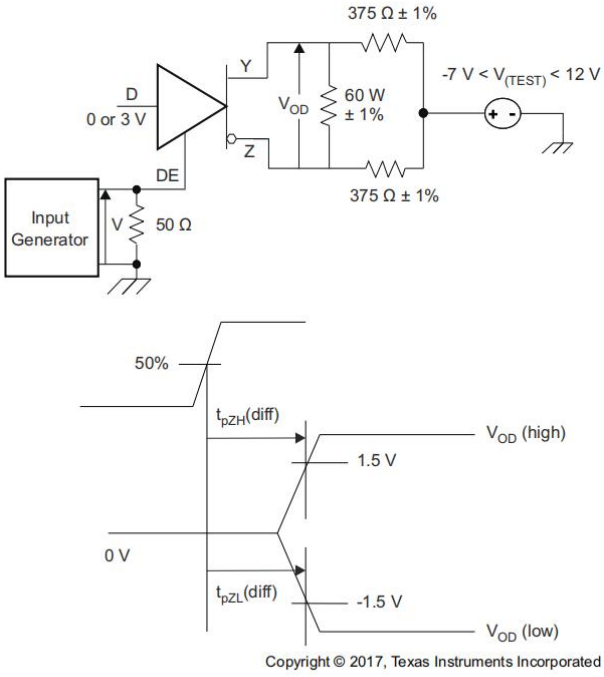
Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 60 ns, t_f < 6 ns Z_O = 50 Ω

图 8-5. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 60 ns, t_f < 6 ns Z_O = 50 Ω

图 8-6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms



The time $t_{PZL(x)}$ is the measure from DE to V_{OD}(x). V_{OD} is valid when it is greater than 1.5 V.

图 8-7. Driver Enable Time from DE to V_{OD}

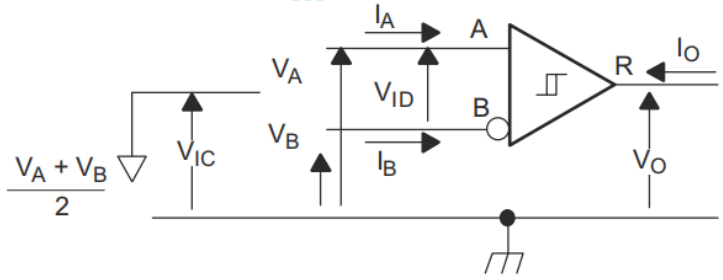
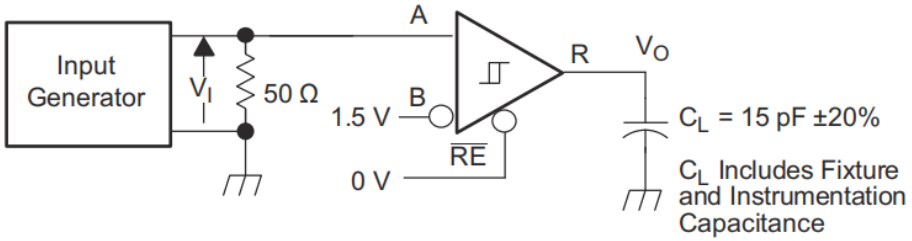


图 8-8. Receiver Voltage and Current Definitions



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

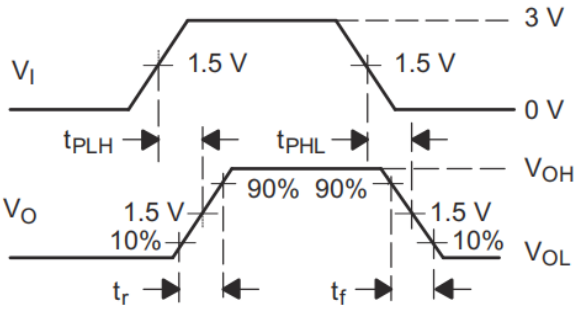


图 8-9. Receiver Switching Test Circuit and Voltage Waveforms

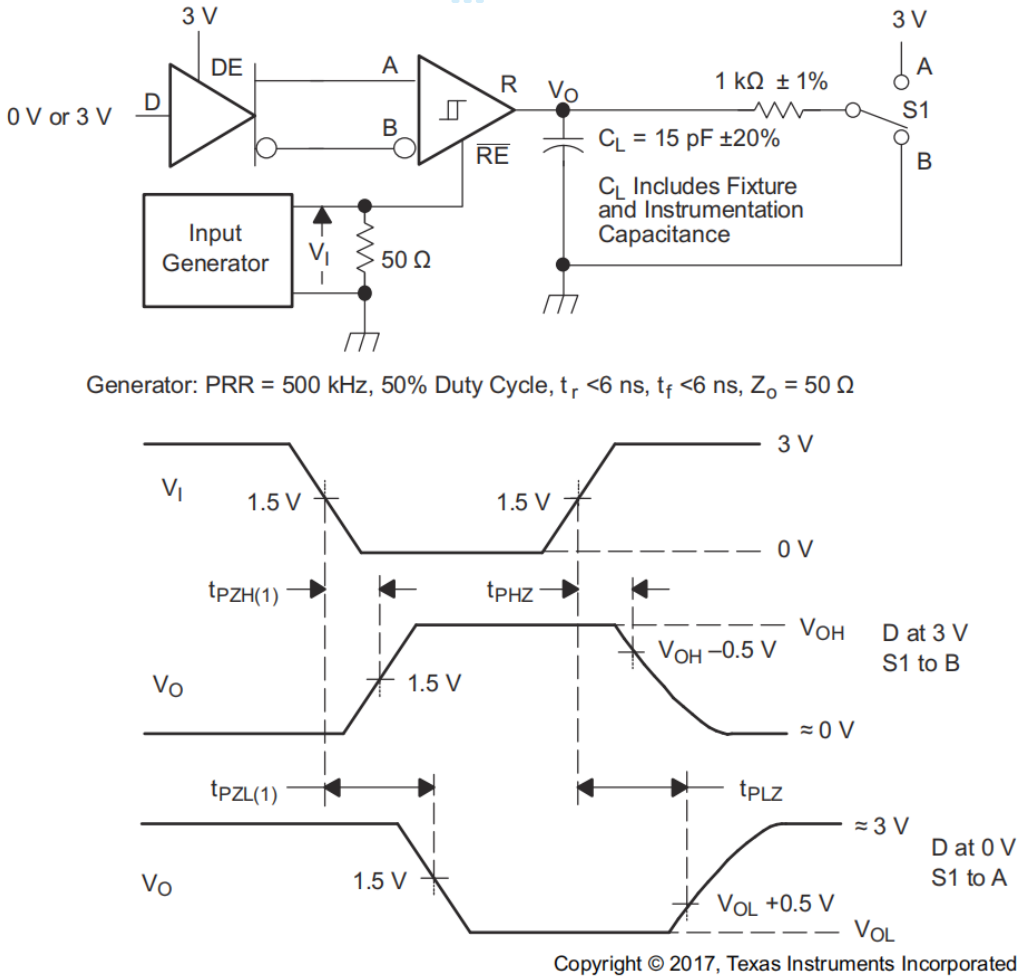


图 8-10. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled

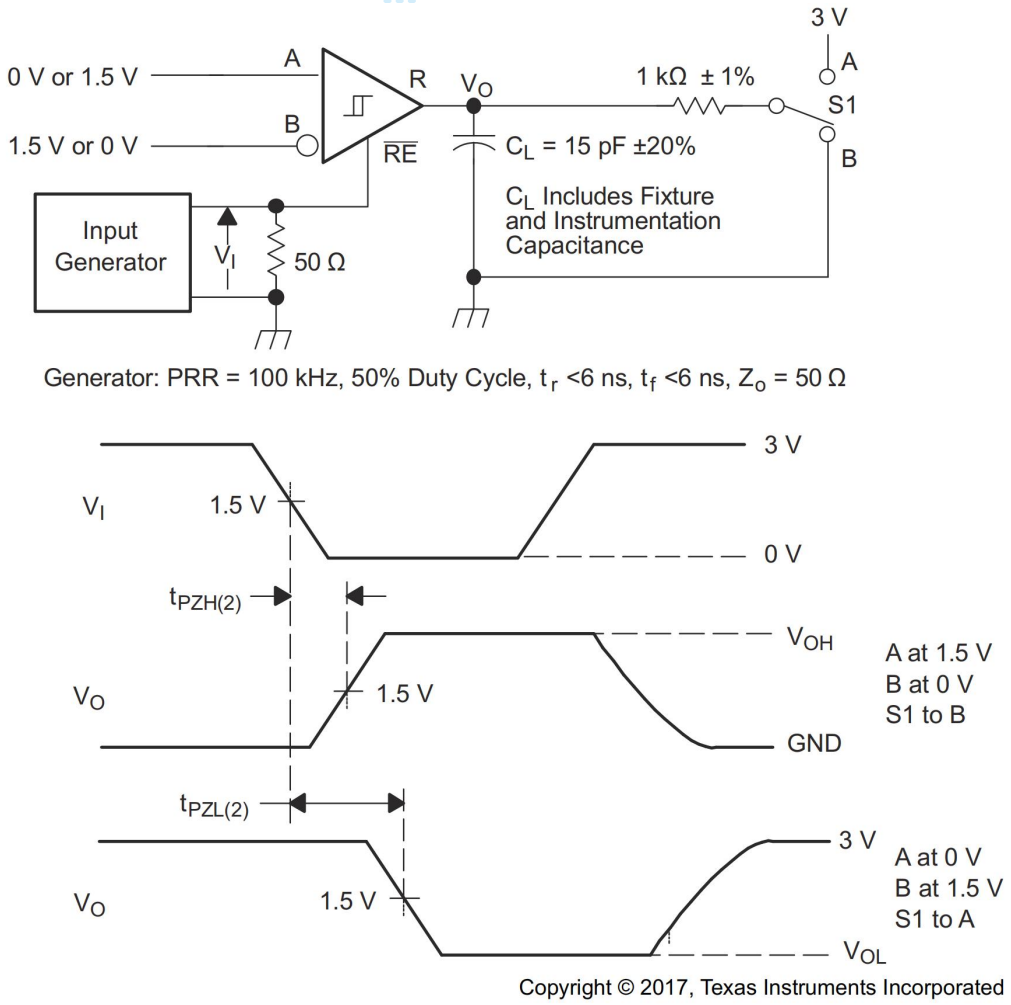
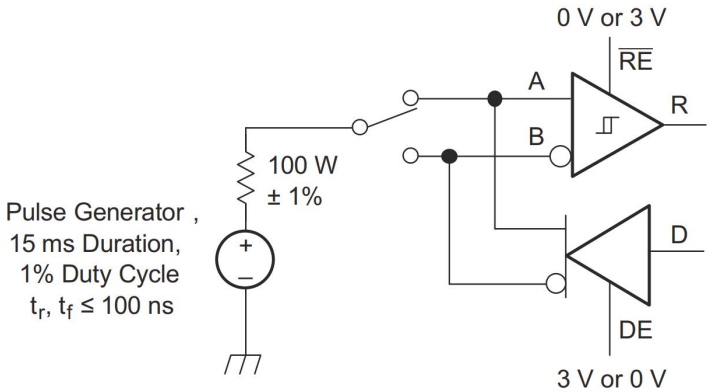
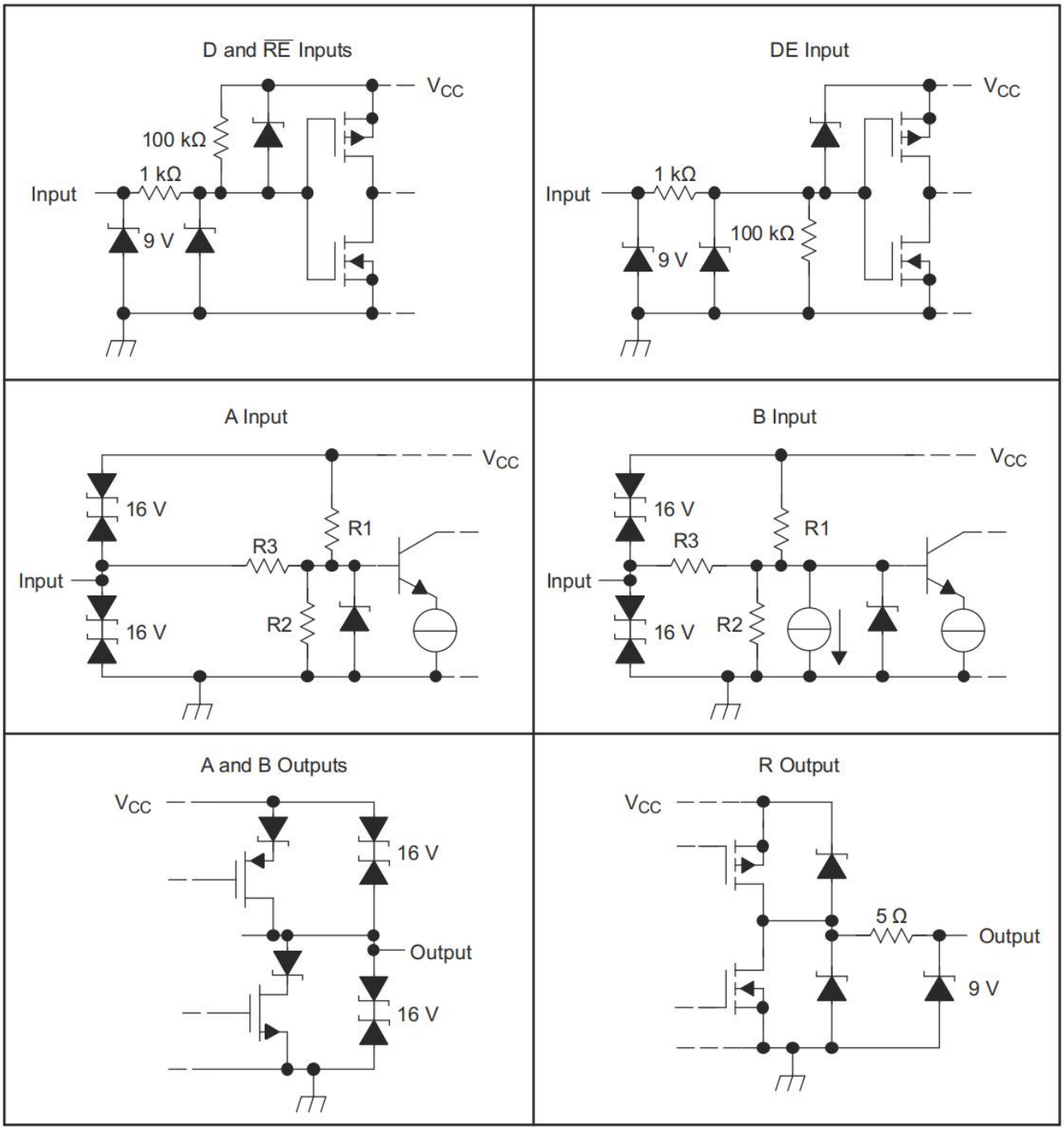


图 8-11. Receiver Enable Time From Standby (Driver Disabled)



NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

图 8-12. Test Circuit, Transient Over Voltage Test



	R1/R2	R3
SN65HVD10	9 kW	45 kW
SN65HVD11	36 kW	180 kW
SN65HVD12	36 kW	180 kW

图 8-13. Equivalent Input and Output Schematic Diagrams

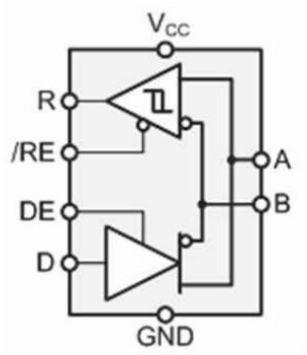
9 Detailed Description

9.1 Overview

The SN65HVD10, SN65HVD11, and SN65HVD12 are 3.3 V, half-duplex, and RS-485 transceivers that are available in 3 speed grades suitable for data transmission up to 32 Mbps, 10 Mbps, and 1 Mbps.

These devices have both active-high driver enables and active-low receiver enables. A standby current of less than
5 µA can be achieved by disabling both driver and receiver.

9.2 Functional Block Diagram



9.3 Feature Description

Internal ESD protection circuits protect the transceiver bus terminals against ±16-kV Human Body Model (HBM) electrostatic discharges and ±4-kV electrical fast transients (EFT) according to IEC61000-4-4.

The SN65HVD1x half-duplex family provides internal biasing of the receiver input thresholds for open-circuit, bus-idle, or short-circuit fail-safe conditions, as well as a typical receiver hysteresis of 35 mV.

9.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition, the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground; therefore, when left open, the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC}; therefore, when left open while the driver is enabled, output A turns high and B turns low.

表 **9-1. Driver Functions**(1)

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus High by default

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R,

turns high. When V_{ID} is negative and lower than the negative input threshold, V_{IT-}, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and V_{IT-}, the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go fail-safe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or when the bus is not actively driven (idle bus).

表 **9-2. Receiver Functions**(1)

DIFFERENTIAL INPUT $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R	FUNCTION
$V_{ID} > V_{IT+}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

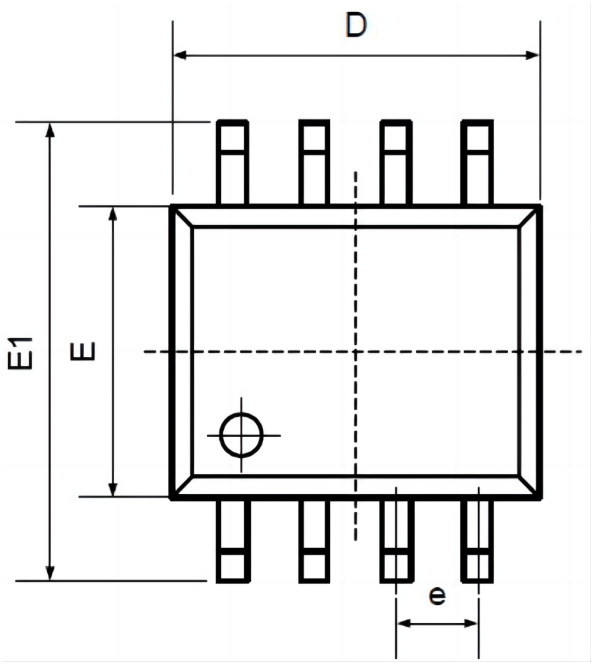
9.4.1 Low-Power Standby Mode

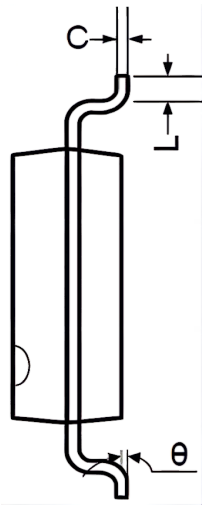
When both the driver and receiver are disabled (DE low and $\overline{RE}$ high) the device is in standby mode. If the enable inputs are in this state for less than 60 ns, the device does not enter standby mode. This guards against inadvertently entering standby mode during driver or receiver enabling. Only when the enable inputs are held in this state for 300 ns or more, the device is assured to be in standby mode. In this low-power standby mode, most internal circuitry is powered down, and the supply current is typically less than 1 µA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.

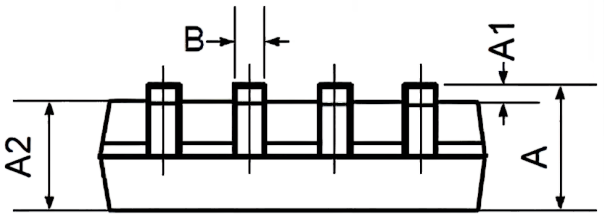
Order information

Order Number	Package	Package Quantity	Marking On The park
SN65HVD10DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD10DR
SN65HVD10P-TUDI	DIP8	Tube,50,A box of 2000	SN65HVD10P
SN65HVD10QDR-TUDI	SOP8	Tape,Reel,2500	SN65HVD10QDR
SN65HVD11DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD11DR
SN65HVD11P-TUDI	DIP8	Tube,50,A box of 2000	SN65HVD11P
SN65HVD11QDR-TUDI	SOP8	Tape,Reel,2500	SN65HVD11QDR
SN65HVD12DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD12DR
SN65HVD12P-TUDI	DIP8	Tube,50,A box of 2000	SN65HVD12P
SN65HVD12QDR-TUDI	SOP8	Tape,Reel,2500	SN65HVD12QDR
SN75HVD10DR-TUDI	SOP8	Tape,Reel,2500	SN75HVD10DR
SN75HVD10P-TUDI	DIP8	Tube,50,A box of 2000	SN75HVD10P
SN75HVD11DR-TUDI	SOP8	Tape,Reel,2500	SN75HVD11DR
SN75HVD11P-TUDI	DIP8	Tube,50,A box of 2000	SN75HVD11P
SN75HVD12DR-TUDI	SOP8	Tape,Reel,2500	SN75HVD12DR
SN75HVD12P-TUDI	DIP8	Tube,50,A box of 2000	SN75HVD12P

Package SOP8

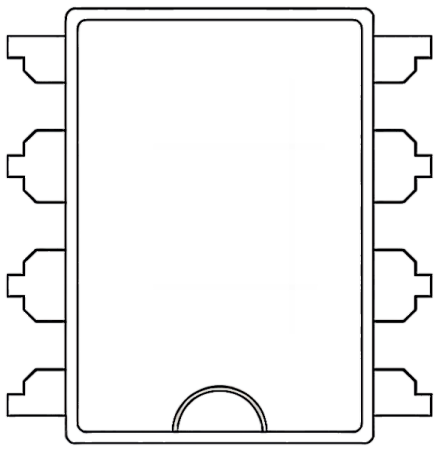


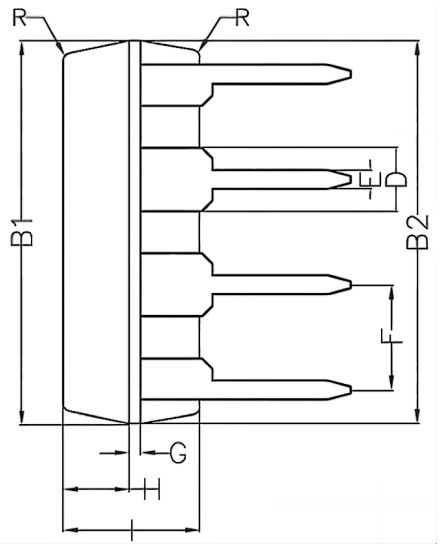


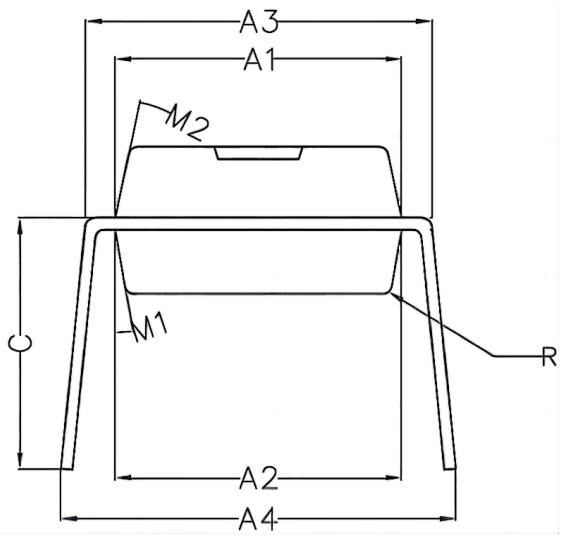


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package DIP8







Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

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