XPC54620

4.5-V to 17-V Input, 6A, Synchronous, Step-Down Converter

FEATURES

- Integrated 17 mΩ and 12 mΩ MOSFETs
- Split Power Rail: 1.6 V to 17 V on PVIN
- 200-kHz to 1.6-MHz Switching Frequency
- Synchronizes to External Clock
- 0.8 V ±1% Voltage Reference Overtemperature
- Low 7µA Shutdown Quiescent Current
- Monotonic Start-Up into Prebiased Outputs
- –40°C to 125°C Operating Junction Temperature Range
- Adjustable Slow Start and Power Sequencing
- Power Good Output Monitor for Undervoltage and Overvoltage
- Adjustable Input Undervoltage Lockout

APPLICATIONS

- High Density Distributed Power Systems
- High Performance Point of Load Regulation
- Broadband, Networking and Optical Communications Infrastructure

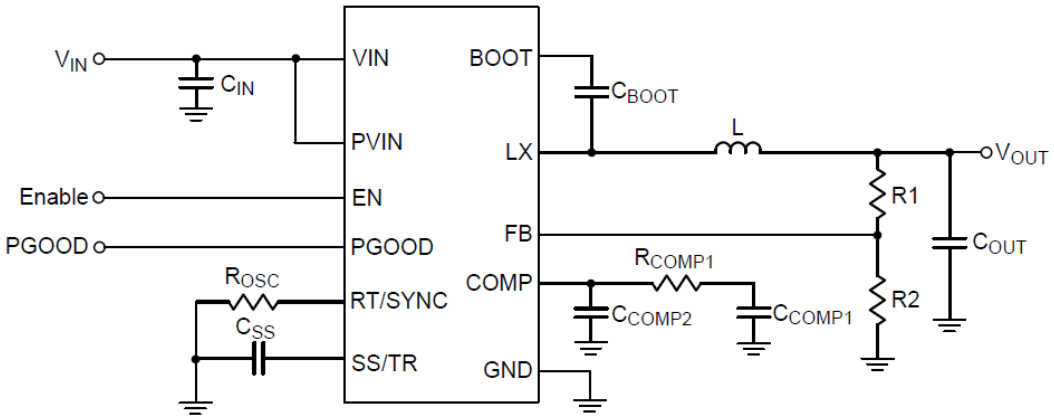
DESCRIPTION

The XPC54620 in thermally enhanced 3.50 mm × 3.50 mm QFN package is a full featured 17-V, 6-A, synchronous, step-down converter which is optimized for small designs through high efficiency and integrating the high-side and low-side MOSFETs. Further space savings are achieved through current mode control, which reduces component count, and by selecting a high switching frequency, reducing the footprint of the inductor.

The output voltage start-up ramp is controlled by the SS/TR pin which allows operation as either a stand-alone power supply or in tracking situations. Power sequencing is also possible by correctly configuring the enable and the open-drain power good pins.

Cycle-by-cycle current limiting on the high-side FET protects the device in overload situations and is enhanced by a low-side sourcing current limit which prevents current runaway. There is also a low-side sinking current limit that turns off the low-side MOSFET to prevent excessive reverse current. Thermal shutdown disables the part when die temperature exceeds thermal shutdown temperature.

TYPICAL APPLICATION



REVISION HISTORY

Release	Rev	Changes	Date
Released	0.9	First release	1/31/2024

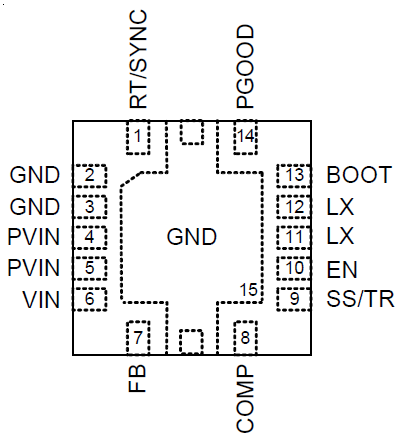
ORDERING INFORMATION

Part Number	Output Current (A)	VOUT (V)	Top Marking	MPQ
XPC54620	6	Adjustable	54620	3,000

MPQ = Minimum Packaging Quantity.
For production orders greater than MPQ, the order must be a multiple of MPQ per package size above.

PIN CONFIGURATION AND DESCRIPTION

Top View



Pin Configuration

Pin	Name	Description
1	RT/SYNC	Automatically selects between RT mode and SYNC mode. An external timing resistor adjusts the switching frequency of the device; in SYNC mode, the device synchronizes to an external clock.
2,3	GND	Return for control circuitry and low-side power MOSFET.
4,5	PVIN	Power input. Supplies the power switches of the power converter.
6	VIN	Supplies the control circuitry of the power converter.
7	FB	Inverting input of the error amplifier. FB senses the switch output through an external resistor divider network.
8	COMP	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation to this pin.
9	SS/TR	Slow-start and tracking. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing.
10	EN	Enable pin. Float to enable. Adjust the input undervoltage lockout with two resistors.
11,12	LX	Switch node.
13	BOOT	A bootstrap cap is required between BOOT and LX. The voltage on this cap carries the gate drive voltage for the high-side MOSFET.
14	PGOOD	Power Good fault pin. Asserts low if output voltage is low because of thermal shutdown, dropout, over- voltage, EN shutdown, or during slow start.
15	Thermal Pad	Thermal pad of the package and signal ground and it must be soldered down for proper operation.

ABSOLUTE MAXIMUM RATINGS(1)

Parameter	Min	Max	Units
VIN	-0.3	20	V
PVIN	-0.3	20	V
EN	-0.3	6	V
BOOT	-0.3	27	V
FB	-0.3	6	V
COMP	-0.3	6	V
PGOOD	-0.3	6	V
SS/TR	-0.3	6	V
RT/SYNC	-0.3	6	V
BOOT to LX	-0.3	7	V
LX	-1	20.3	V
LX (t <= 10ns)	-5	26.3	V
PVIN to LX	-1	20.3	V
PVIN to LX (t <= 10ns)	-5	26.3	V
Junction Temperature	-40	150	°C
Storage Temperature	-65	150	°C
Electrostatic Discharge (HBM)	-2000	+2000	V
Electrostatic Discharge (CDM)	-2000	+2000	V

(1) Operation of the device outside of these parameters may cause permanent damage.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Units
Input voltage	VIN	4.5	17	V
Power stage input voltage	PVIN	1.6	17	V
Output current		0	6	A
Operating junction temperature	T_J	-40	+125	°C

Thermal Information

Junction to ambient thermal resistance is a function of board layout and ambient air flow condition. This data is based on four-layer XPC54620 EVB in still air box in accordance with JEDEC standard JESD51 on natural convection.

Parameter	Symbol	Typ	Units
Junction-to-ambient thermal resistance	θ_{JA}	15.5	°C/W
Junction-to-case thermal resistance	θ_{JC}	10.5	°C/W

ELECTRICAL SPECIFICATIONS

T_J = -40˚C to 125˚C, V_{IN} = 4.5V to 17V, PVIN = 1.6V to 17V (unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage (VIN and PVIN Pins)						
PVIN operating input voltage	PVIN		1.6		17	V
VIN operating input voltage	VIN		4.5		17	V
VIN internal UVLO threshold	V_{UVLO}	VIN rising		4.3	4.5	V
VIN internal UVLO hysteresis	ΔV_{UVLO}			70		mV
VIN shutdown current	Isd	V_{EN} = 0V		7	10	μA
VIN quiescent current	Iq	V_{FB} = 810mV		600	900	μA
Enable And UVLO (EN Pin)						
EN threshold	V_{IH}	Rising		1.21	1.26	V
	V_{IL}	Falling	1.05	1.15		V
Input current	IEN_1.1	V_{EN} = 1.1V		1.6		μA
Hysteresis current	IEN_1.3	V_{EN} = 1.3V		3.7		μA
Voltage Reference						
Voltage reference	V_{REF}	0A ≤ ILoad ≤ 6A	0.792	0.8	0.808	V
Timing Resistor and External Clock (RT/SYNC Pin)						
Switching frequency	f_{OSC}	R_{OSC} = 240 kOhm	160	200	240	kHz
		R_{OSC} = 100 kOhm	400	480	560	kHz
		R_{OSC} = 29 kOhm	1440	1600	1760	kHz
Minimum pulse width	MIN_WIDTH			50		ns
RT/SYNC high threshold	RT_H	High Level			2	V
RT/SYNC low threshold	RT_L	Low Level	0.8			V
SYNC falling edge to LX rising edge delay	DELAY	Measure at 500kHz with R_{OSC} resistor in series		66		ns
Switching frequency range	FOSC_SYNC	Including Sync mode and RT Mode set point	200		1600	kHz
MOSFET						
High Side ON-Resistance	Rhs_on	V_{BOOT} - V_{LX} = 5V		17	30	mΩ
Low Side ON-Resistance	Rls_on	VIN = 12V		12	25	mΩ
LX (LX Pin)						
Minimum on-time	Ton_min	Measured at 90% to 90% of V_{LX}, I_{LX} = 2A, 25°C		110		ns
Minimum off-time	Toff_min	V_{BOOT} - V_{LX} = 3V		0		ns
BOOT (BOOT Pin)						
BOOT- LX UVLO				2.6	3	V
Slow Start and Tracking (SS/TR Pin)						
SS charge current	Iss			2.7		μA

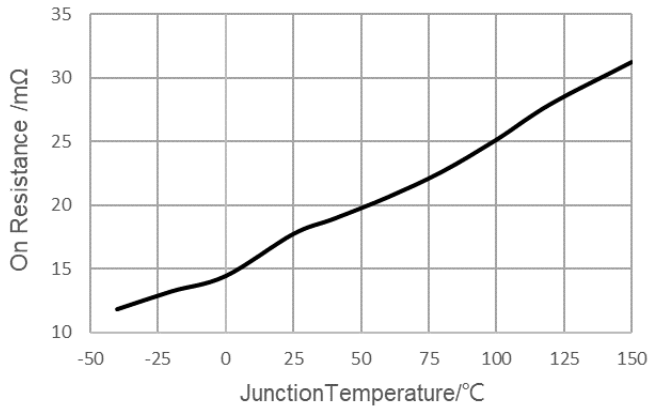
T_J = -40˚C to 125˚C, V_{IN} = 4.5V to 17V, PVIN = 1.6V to 17V (unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
SS/TR to feedback matching	offset	$V_{SS/TR}$ = 0.4V		5	20	mV
Current Limit						
High-Side Switch Current Limit	Ihcs		8	13		A
Low-Side Switch Sourcing Current Limit	Ilcs1		7	10		A
Low-Side Switch Sinking Current Limit	Ilcs2			3.5		A
Error Amplifier						
Error Amplifier Transconductance	gm	-2μA < I_{COMP} < 2μA, V_{COMP} = 1V		1300		uMhos
Error Amplifier DC Gain	gain		1000	3100		V/V
Error Amplifier Source/Sink	Isource/sink			±100		μA
COMP to Iswitch gm				16		A/V
Power Good (PGOOD Pin)						
Power Good Rising Threshold	rise_good	V_{FB} Rising (Good)		94		$\%V_{REF}$
	rsie_fault	V_{FB} Rising (Fault)		109		$\%V_{REF}$
Power Good Falling Threshold	fall_fault	V_{FB} Falling (Fault)		91		$\%V_{REF}$
	fall_good	V_{FB} Falling (Good)		106		$\%V_{REF}$
Power Good Sink Current Capability	outl	PGOOD signal fault, I_{PGOOD} sinks 2mA			0.3	V
Power Good Leakage Current		PGOOD signal good, V_{PGOOD} = 5.5V		30	100	nA
Minimum VIN for Indicating PGOOD	VIN_min	V_{PGOOD} < 0.5V, I_{PGOOD} sinks 100μA		0.8	1	V
Minimum SS/TR Voltage for Indicating PGOOD	SSOK				1.4	V
Thermal Shutdown						
Thermal Shutdown	Tsd			170		°C
Thermal Shutdown Hysteresis	ΔTsd			10		°C

Note 1. Devices are ESD sensitive. Handling precaution is recommended.
Note 2. The device is not guaranteed to function outside its operating conditions.

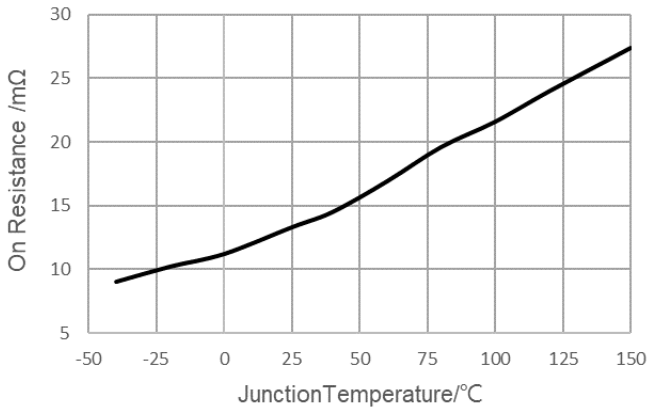
TYPICAL CHARACTERISTICS

High-Side Rds(on) vs Temperature



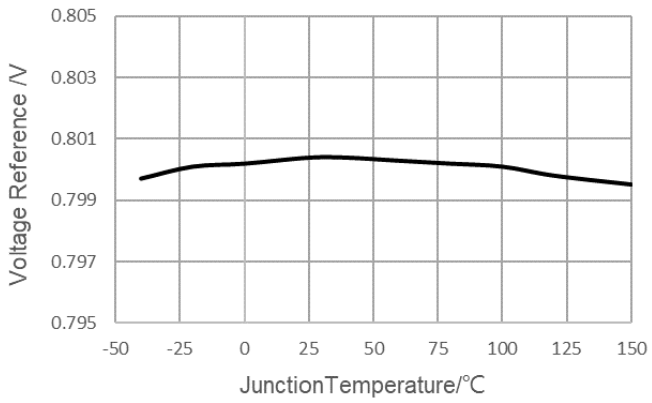
VBOOT - VLX = 5V

Low-Side Rds(on) vs Temperature

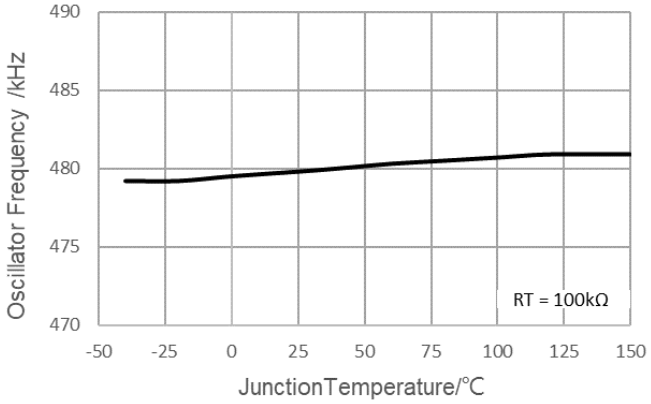


VIN = 12V

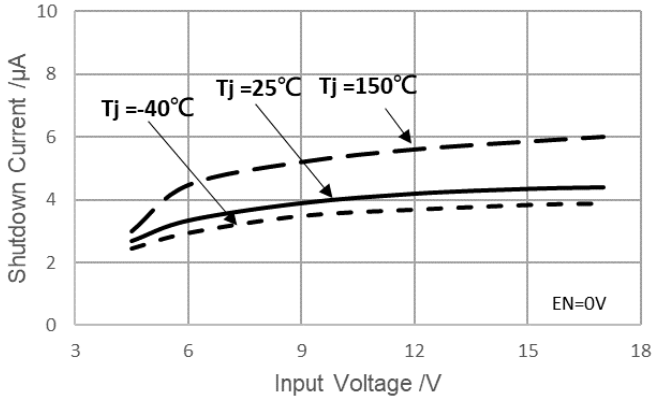
Voltage Reference vs Temperature



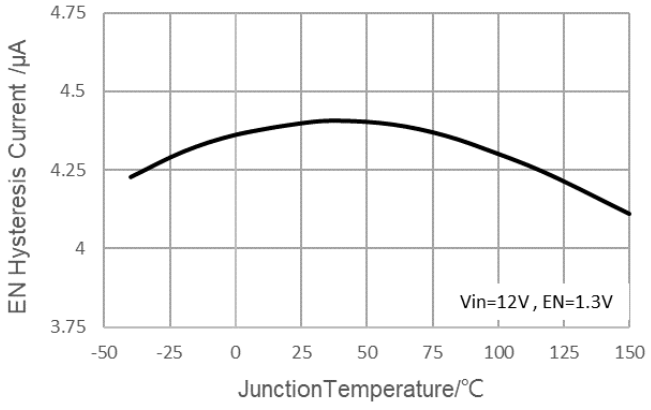
Oscillator Frequency vs Temperature



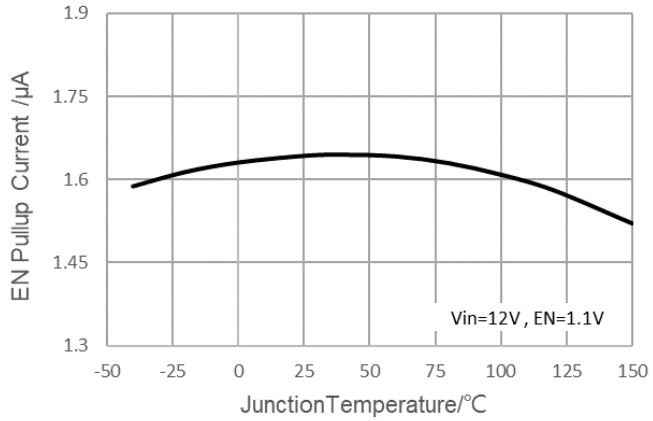
Shutdown Current vs Input Voltage



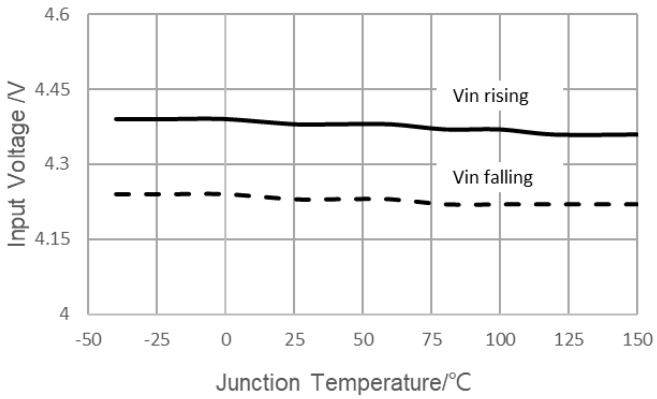
EN Hysteresis Current vs Temperature



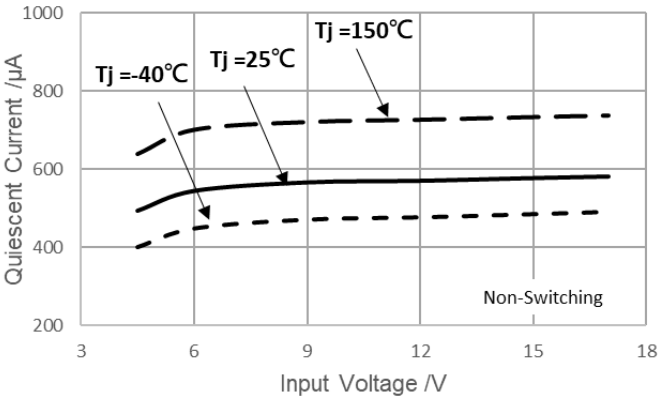
EN Pullup Current vs Temperature



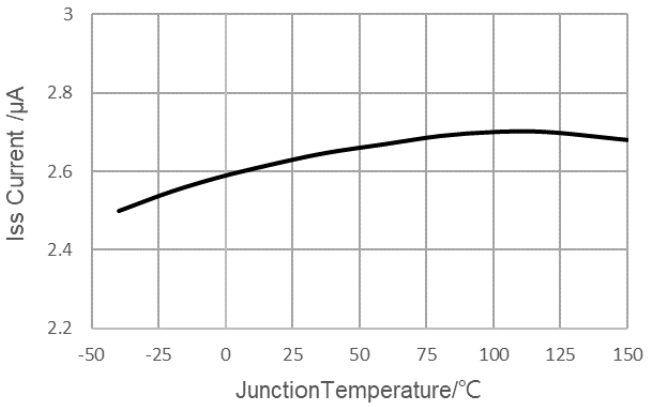
VIN UVLO Threshold vs Temperature



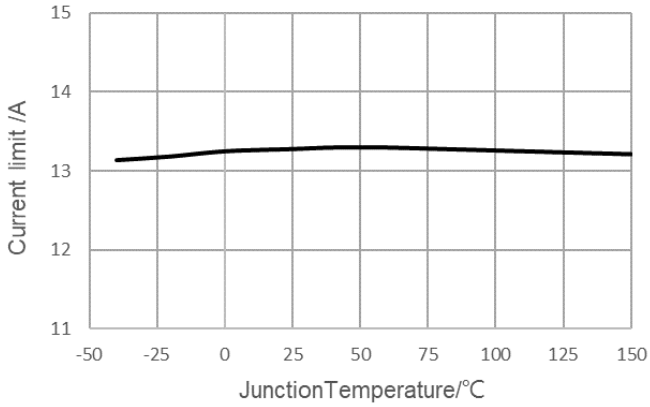
Quiescent Current vs Input Voltage



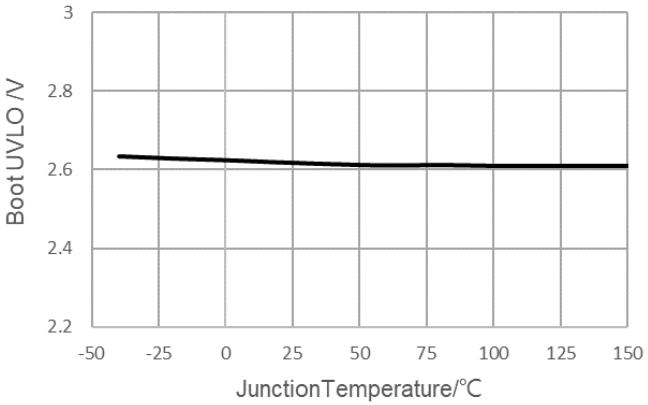
Internal Charge Current vs Temperature

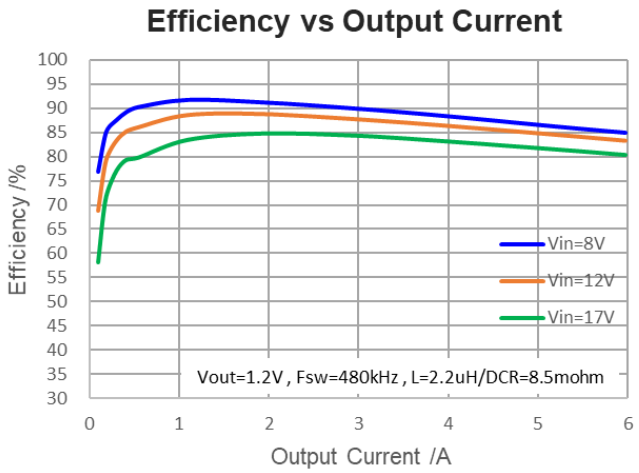


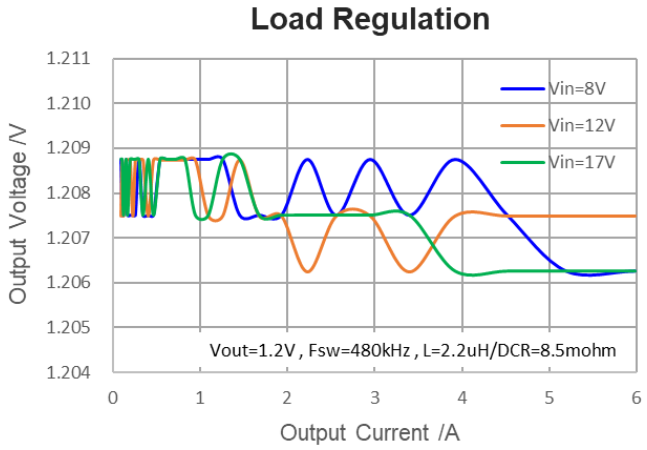
Current limit vs Temperature

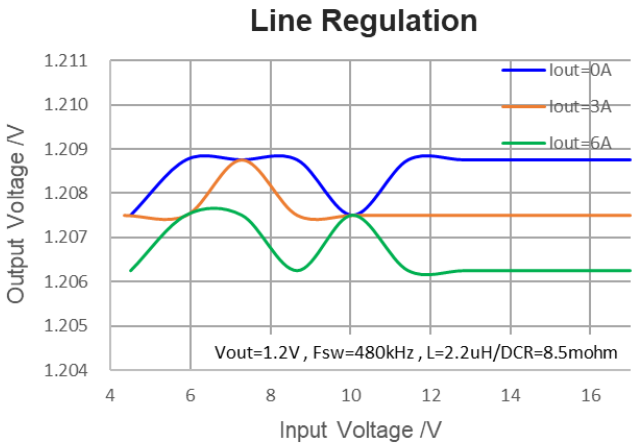


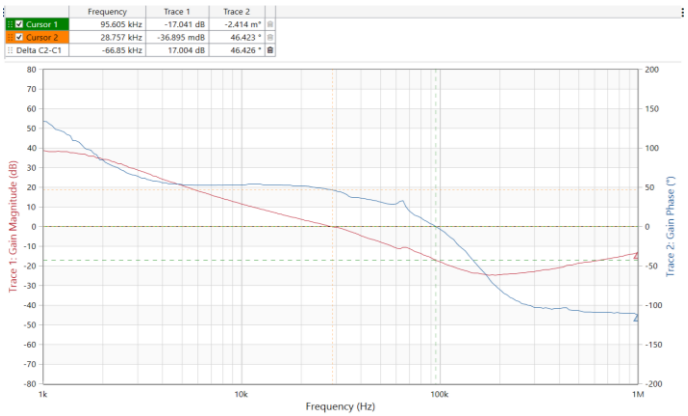
Boot UVLO vs Temperature











Closed loop response

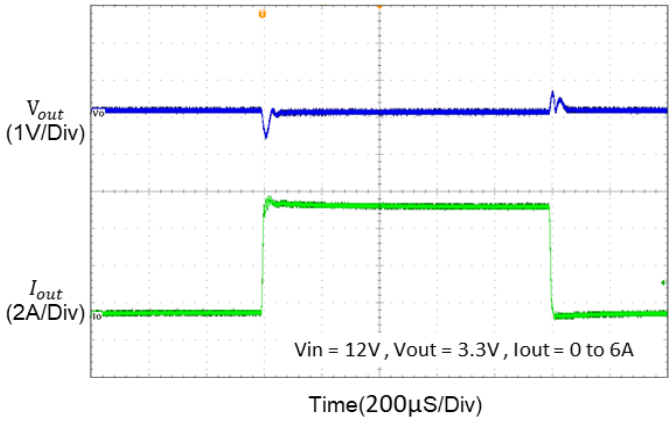
V_{OUT}=1.2V, I_{OUT}=6A, f_{SW}=490kHz

C_{IN}=4 x 4.7uF, C_{OUT}=3 x 47uF, L_{OUT}=2.2uH

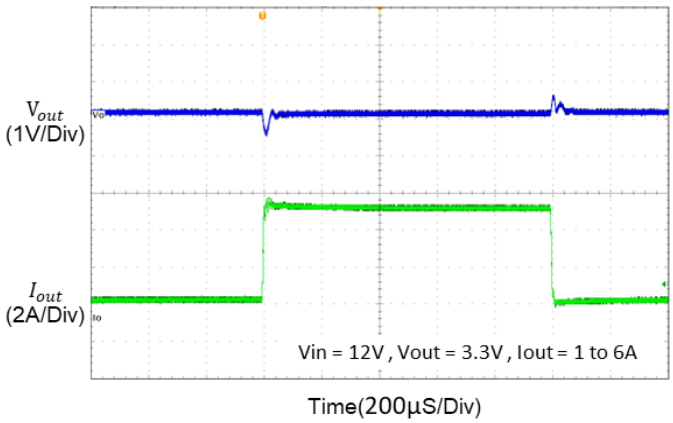
TYPICAL CHARACTERISTICS

Test conditions unless otherwise noted: VIN = PVIN = 12V, V_{OUT} = 3.3V, L_{OUT} = 3.3uH, C_{OUT} = 2 x 100uF.

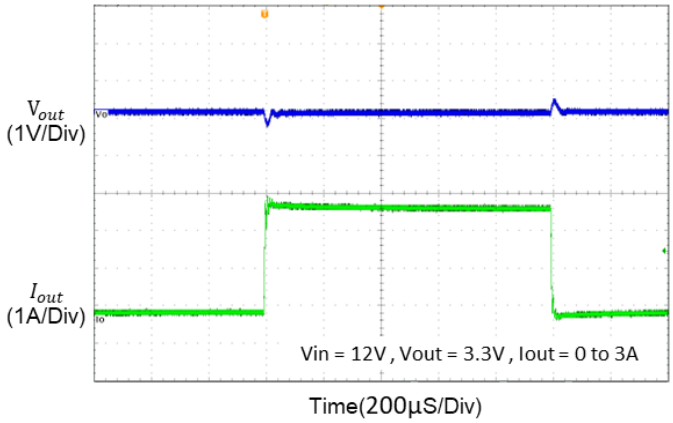
Load Transient Response



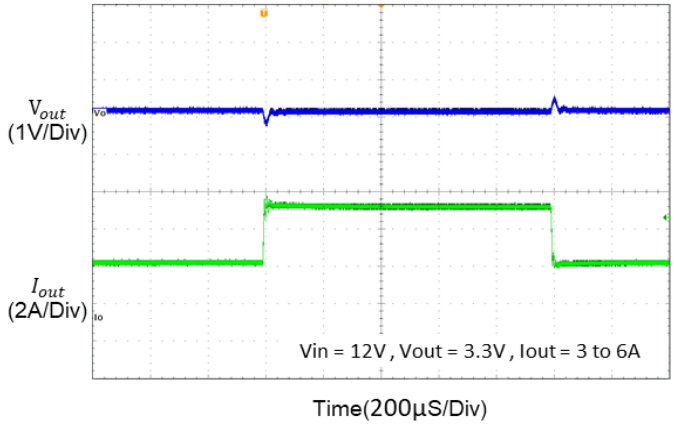
Load Transient Response



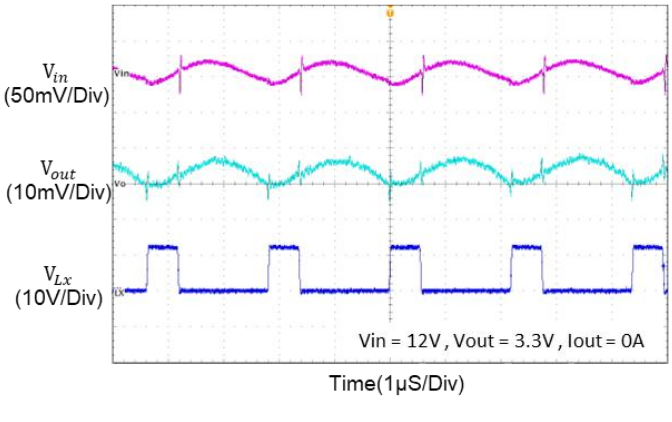
Load Transient Response



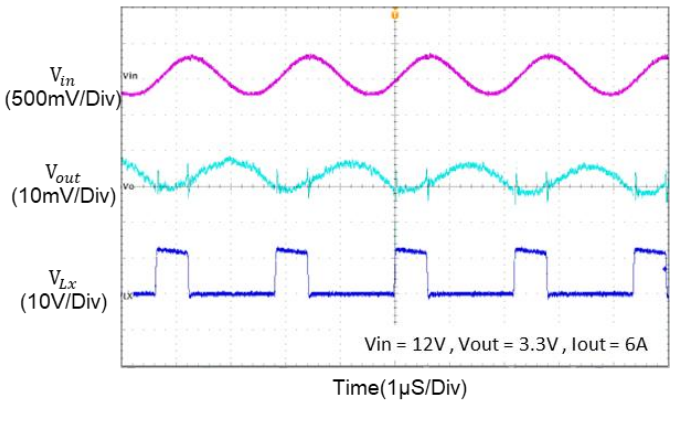
Load Transient Response



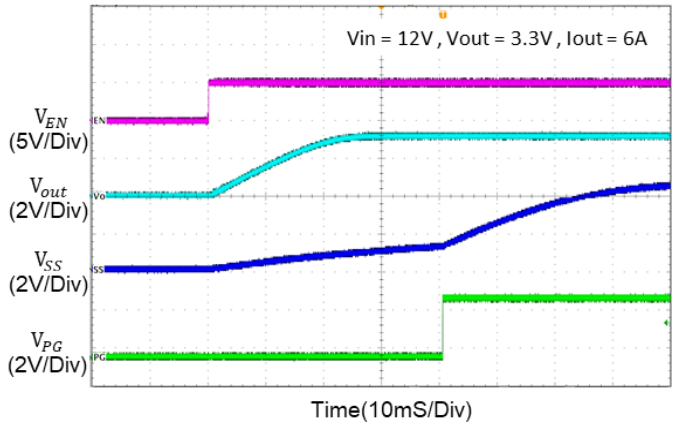
Voltage Ripple



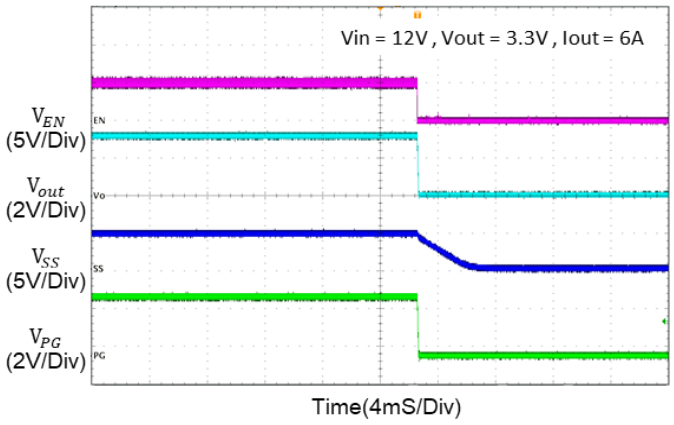
Voltage Ripple



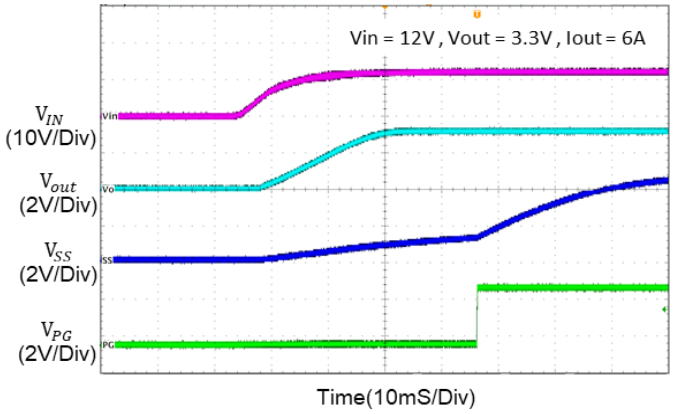
Power On from EN



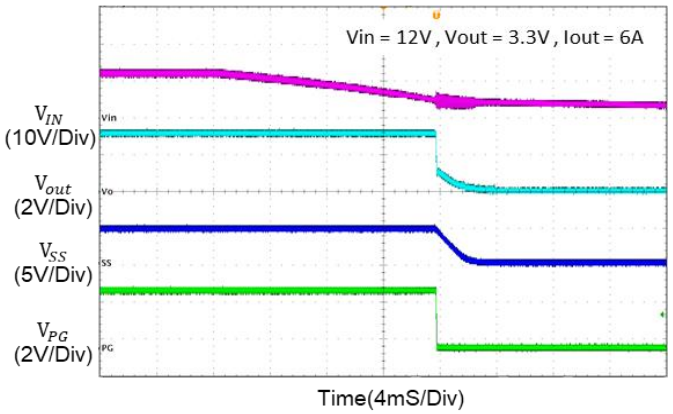
Power Off from EN



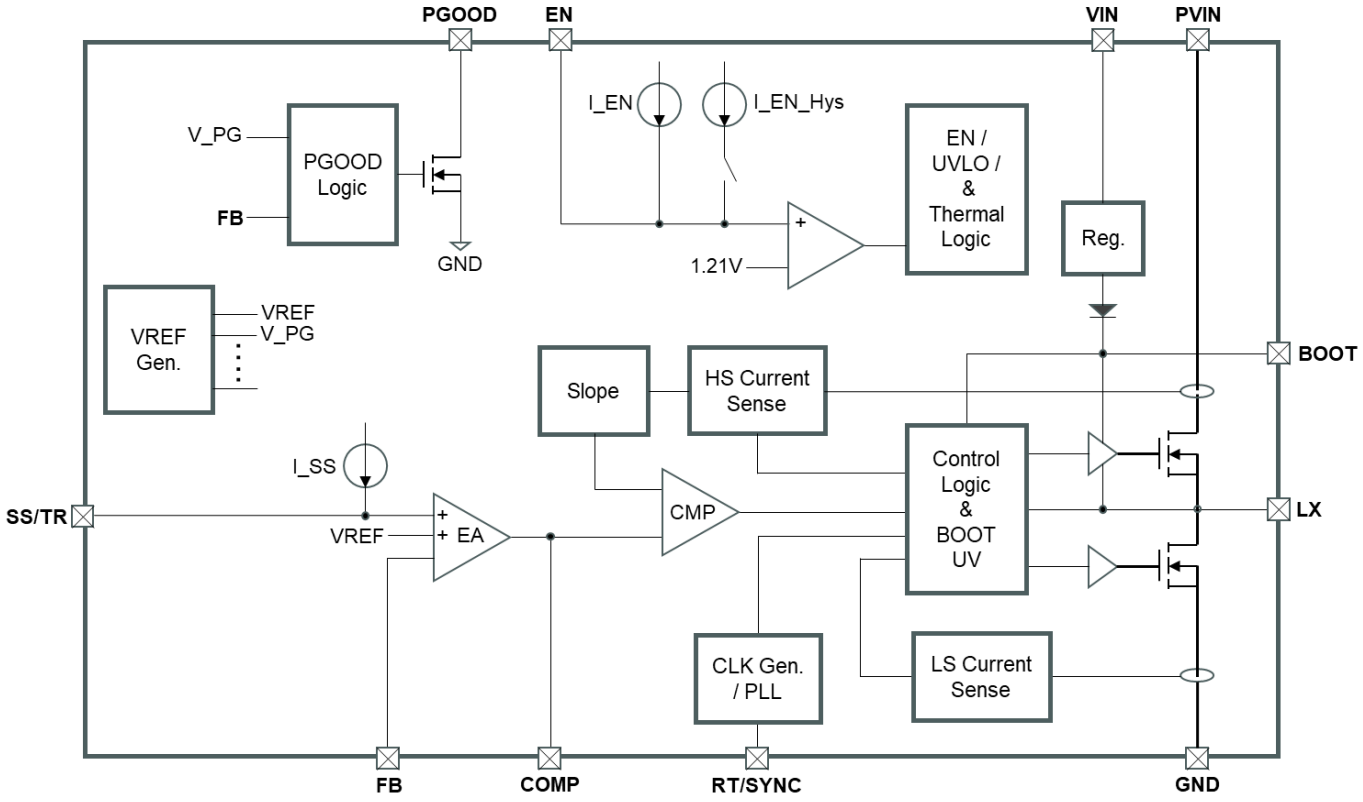
Power On from VIN



Power Off from VIN



FUNCTIONAL BLOCK DIAGRAM



FEATURE DESCRIPTION

Overview

The XPC54620 is a 17-V, 6-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients, the device implements a constant frequency peak current mode control that also simplifies external frequency compensation. The wide switching frequency of 200 kHz to 1600 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor-to-ground on the RT/SYNC pin. The device also can synchronize its switching cycle to the falling edge of an external system clock.

The device has been designed for safe monotonic start-up into prebiased loads. The default start-up is when VIN is typically 4.3V. The EN pin has an internal pullup current source that can be used to adjust the input voltage undervoltage lockout (UVLO) with two external resistors. In addition, the EN pin can be floating for the device to operate with the internal pullup current. The total operating current for the device is approximately 600μA when not switching and under no load. When the device is disabled, the supply current is typically less than 7μA.

The integrated MOSFETs allow for high efficiency power supply designs with continuous output currents up to 6 amperes. The MOSFETs have been sized to optimize efficiency for lower duty cycle applications.

The device reduces the external component count by integrating the boot recharge circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BOOT and LX pins. The boot capacitor voltage is monitored by a BOOT to LX UVLO circuit allowing LX pin to be pulled low to recharge the boot capacitor. The device can operate at 100% duty cycle as long as the boot capacitor voltage is higher than the preset BOOT-LX UVLO threshold which is typically 2.6 V. The output voltage can be stepped down to as low as the 0.8-V voltage reference (V_{REF}).

The device has a power good comparator (PGOOD) with hysteresis which monitors the output voltage through the FB pin. The PGOOD pin is an open-drain MOSFET which is pulled low when the FB pin voltage is less than 91% or greater than 109% of the reference voltage Vref and asserts high when the FB pin voltage is 94% to 106% of the V_{REF}.

The SS/TR (slow start/tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor or resistor divider should be coupled to the pin for slow start or critical power supply sequencing requirements.

The device is protected from output overvoltage, overload, and thermal fault conditions. The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage circuit power good comparator. When the overvoltage comparator is activated, the high-side MOSFET is turned off and prevented from turning on until the FB pin voltage is lower than 106% of the V_{REF}. The device implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections which help control the inductor current and avoid current runaway. The device also shuts down if the junction temperature is higher than thermal shutdown trip point. The device is restarted under control of the slow-start circuit automatically when the junction temperature drops 10°C typically below the thermal shutdown trip point.

Fixed Frequency PWM Control

The device uses an adjustable fixed frequency, peak current mode control. The output voltage is compared through external resistors on the FB pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn-on of the high-side power switch. The error amplifier output is converted into a current reference which compares to the high-side power switch current. When the power switch current reaches current reference generated by the COMP voltage level the high-side power switch is turned off and the low-side power switch is turned on.

Continuous Current Mode Operation (CCM)

As a synchronous buck converter, the device normally works in CCM (Continuous Conduction Mode) under all load conditions.

VIN and Power VIN Pins (VIN and PVIN)

The device allows for a variety of applications by using the VIN and PVIN pins together or separately. The VIN pin voltage supplies the internal control circuits of the device. The PVIN pin voltage provides the input voltage to the power converter system. If tied together, the input voltage for VIN and PVIN can range from 4.5 V to 17 V. If using the VIN separately from PVIN, the VIN pin must be between 4.5 V and 17 V, and the PVIN pin can range from as low as 1.6 V to 17 V. A voltage divider connected to the EN pin can adjust the either input voltage UVLO appropriately. Adjusting the input voltage UVLO on the PVIN pin helps to provide consistent power up behavior.

Voltage Reference

The voltage reference system produces a precise ±1% voltage reference over temperature by scaling the output of a temperature stable bandgap circuit.

Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output (V_{OUT}) to the FB pin. It is recommended to use 1% tolerance or better divider resistors, referring to the typical application schematic.

$$VOUT = Vref \left(1 + \frac{R1}{R2}\right)$$

Safe Start-Up into Pre-biased Outputs

The device has been designed to prevent the low-side MOSFET from discharging a prebiased output. During monotonic prebiased start-up, the low-side MOSFET is not allowed to sink current until the SS/TR pin voltage is higher than 1.4 V.

Error Amplifier

The device uses a transconductance error amplifier. The error amplifier compares the FB pin voltage to the lower of the SS/TR pin voltage or the internal 0.8-V voltage reference. The transconductance of the error amplifier is 1300 µA/V during normal operation. The frequency compensation network is connected between the COMP pin and ground.

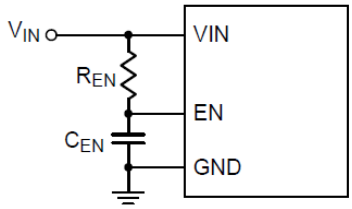
Slope Compensation

The device adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations. The available peak inductor current remains constant over the full duty cycle range.

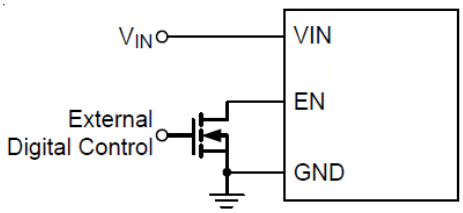
Enable and Adjusting Undervoltage Lockout

The EN pin is a device enable input. Pulling the EN pin to logic low that is typically less than the set threshold voltage 1.15V, the device shuts down and enters to low quiescent current state about 7μA. The regulator starts switching again once the EN pin voltage exceeds the threshold voltage 1.21V. In additional, the EN pin is implemented with an internal pull-up current source which allows to enable the device when the EN pin is floating.

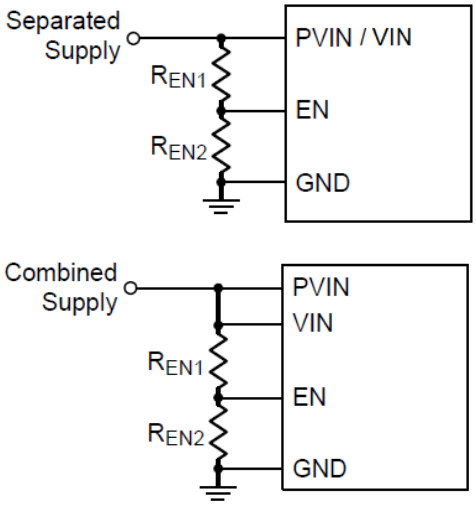
For general external timing control, the EN pin can be externally pulled high by adding a capacitor and a resistor from the VIN pin as following shown.



An external MOSFET can be added to implement digital control from the EN pin to ground, as following shown. In this case, there is no need to connect a pull-up resistor between the VIN and EN pins since the EN pin is pulled up by the internal current source. The device can simply achieve the digital control only through an external MOSFET on EN pin.



The EN pin can also be applied to adjust its Under-Voltage Lockout (UVLO) threshold with two external resistors divider from the both input VIN and PVIN pins used together or separately, and the application structures can refer to following 2 graphs.



Under above application structures, the adjustable UVLO function of EN pin allows to achieve a secondary UVLO on PVIN pin, a higher UVLO on VIN pin or even a common UVLO on both VIN and PVIN pins. For example, the VIN UVLO is 4.3V we knew. If the system needs a higher UVLO, to utilize accurate Enable threshold and 2 resistor combination, we can get an external UVLO level we design as following equations.

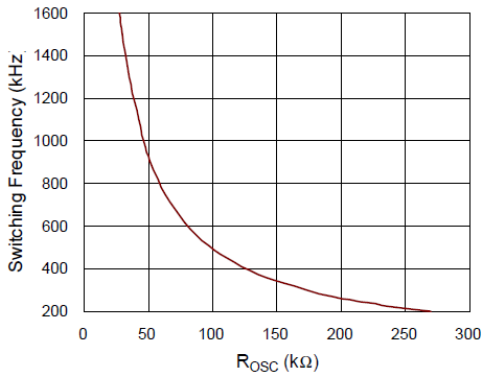
$$Ext\ UVLO\_IH = (VIH - Ien1.0 * Ren) * \left(1 + \frac{Ren1}{Ren2}\right)$$

$$Ext\ UVLO\_IL = (VIL - Ien1.3 * Ren) * \left(1 + \frac{Ren1}{Ren2}\right)$$

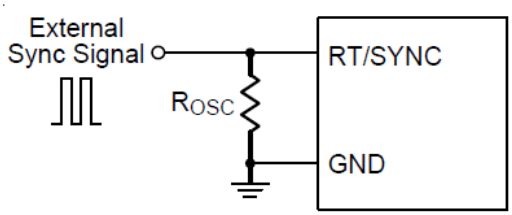
Where Ren = Ren2 // Ren1.

Adjustable Switching Frequency and Synchronization (RT/SYNC)

The RT/SYNC pin can be used to set the switching frequency of the device in two modes. In RT mode, a resistor (RT resistor) is connected between the RT/SYNC pin and GND. The switching frequency of the device is adjustable from 200 kHz to 1600 kHz by placing a maximum of 240kΩ and minimum of 29kΩ, respectively. Following graph is the Switching Frequency vs RT value.



In SYNC mode, an external clock is connected directly to the RT/SYNC pin. The device is synchronized to the external clock frequency with PLL. The SYNC mode overrides the RT mode. The device is able to detect the proper mode automatically and switch from the RT mode to SYNC mode. The range of sync duty cycle must be from 20% to 80%, and the amplitude of sync signal must be higher than 2V and lower than 0.8V. During the SYNC mode operation, the switching cycle of LX pin is synchronized to the falling edge of the external sync signal. Before the external sync signal is provided to the RT/SYNC pin, the device operates at the original switching frequency set by resistor ROSC. When the sync signal is provided, the SYNC mode overrides the RT mode to force the device synchronizing to external frequency. This IC can easily switch between RT mode and SYNC mode, and the application structure can be configured as graph.



Slow Start (SS/TR)

The device uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the reference voltage and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a slow-start time. The device has an internal pullup current source of 2.7μA that charges the external slow-start capacitor. The calculations for the slow-start time (Tss, 10% to 90%) and slow-start capacitor (Css) are shown as following equation The voltage reference (Vref) is 0.8 V and the slow-start charge current (Iss) is 2.7 μA.

$$Tss = \frac{Css * Vref}{Iss}$$

When the input UVLO is triggered, the EN pin is pulled below 1.21 V, or a thermal shutdown event occurs, the device stops switching and enters low current operation. At the subsequent power up when the shutdown condition is removed, the device does not start switching until it has discharged its SS/TR pin to ground ensuring proper soft-start behavior.

Power Good (PGOOD)

The PGOOD pin is an open-drain output. When the FB pin is between 94% and 106% of the internal voltage reference the PGOOD pin pulldown is deasserted and the pin floats. XinJi recommends using a pullup resistor between the values of 10kΩ and 100kΩ to a voltage source that is 5.5 V or less. The PGOOD is in a defined state when the VIN input voltage is greater than 1 V but with reduced current sinking capability. The PGOOD achieves full current sinking capability when the VIN input voltage is above 4.5 V.

The PGOOD pin is pulled low when FB is lower than 91% or greater than 109% of the nominal internal reference voltage. Also, if the PGOOD is pulled low and the input UVLO or thermal shutdown are asserted, the EN pin is pulled low or the SS/TR pin is set below 1.4 V.

Output Overvoltage Protection (OVP)

The device incorporates an output overvoltage protection (OVP) circuit to minimize output voltage overshoot. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. When the condition is removed, the regulator output rises and the error amplifier output transitions to the steady-state voltage. In some applications with small output capacitance, the power supply output voltage can respond faster than the error amplifier. This leads to the possibility of an output overshoot. The OVP feature minimizes the overshoot by comparing the FB pin voltage to the OVP threshold. If the FB pin voltage is greater than the OVP threshold the high-side MOSFET is turned off preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

High-Side MOSFET overcurrent Protection

The device implements current mode control which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference the high-side switch is turned off.

Low-Side MOSFET overcurrent Protection

While the low-side MOSFET is turned on its conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET may also sink current from the load. If the low-side sinking current limit is exceeded the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario both MOSFETs are off until the start of the next cycle.

Over-Temperature Protection

An Over-Temperature Protection (OTP) is contained in the device. The protection is triggered to force the device shutdown for protecting itself when the junction temperature exceeds 170°C typically. Once the junction temperature drops below the hysteresis 10°C typically, the device is re-enabled and automatically reinstates the power up sequence.

APPLICATION INFORMATION

Output Inductor Selection

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 30% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where △IL is the peak-to-peak inductor ripple current.

Input Capacitor Selection

The input capacitor is used to supply the AC input current to the step-down converter and maintain the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{C_{IN}} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

Thus, the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_{IN} = \frac{I_{OUT}}{f_{SW} \times \Delta V_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The input capacitor can be electrolytic, tantalum or ceramic. To minimize the potential noise, a small X5R or X7R ceramic capacitor, i.e., 0.1uF, should be placed as close to the IC as possible when using electrolytic capacitors.

Two 10μF and one 4.7μF low ESR ceramic capacitors are recommended for bypassing the PVIN pin and VIN pin respectively in typical applications.

Output Capacitor Selection

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right)$$

where R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, while lower ESR capacitors get lower output ripple voltage.

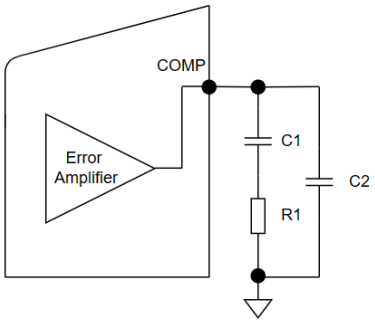
The output capacitors also affect the system stability and transient response, and a 94uF ceramic capacitor (47uF×2) is recommended for typical application.

Bootstrap Capacitor Selection

A 0.1-μF ceramic capacitor must be connected between the BOOT-LX pin for proper operation. We recommend using a ceramic capacitor with X5R or better grade dielectric. The capacitor must have a 10-V or higher voltage rating.

Compensation Network Design

In order to ensure stable operation while maximizing the dynamic performance, the appropriate loop compensation is important. Generally, follow the steps below to calculate the compensation components:



1. Set up the crossover frequency, f_C. In general, one-twentieth to one-sixth of the switching frequency is recommended to be the crossover frequency.
2. R1 can be determined by:

$$R_1 = \frac{2\pi \times f_C \times C_{\mathrm{OUT}}}{g_M \times g_{\mathrm{CS}}} \times \frac{V_{OUT}}{V_{REF}}$$

Where g_M=1300uA/V, g_{CS}=16A/V.

3. A compensation zero can be placed at or before the dominant pole of buck which is provided by output capacitor and maximum output loading (R_{LOAD}). Calculate C1:

$$C_1 = \frac{C_{\mathrm{OUT}} \times R_{\mathrm{LOAD}}}{R_1}$$

4. The compensation pole is set to the frequency at the ESR zero or 1/2 of the operating frequency. Output capacitor and its ESR provide a zero, and optional C2 can be used to cancel this zero. Calculate C2:

$$C_2 = \frac{C_{\mathrm{OUT}} \times R_{\mathrm{ESR}}}{R_1}$$

If 1/2 of the operating frequency is lower than the ESR zero, the compensation pole is set at 1/2 of the operating frequency. Calculate C2:

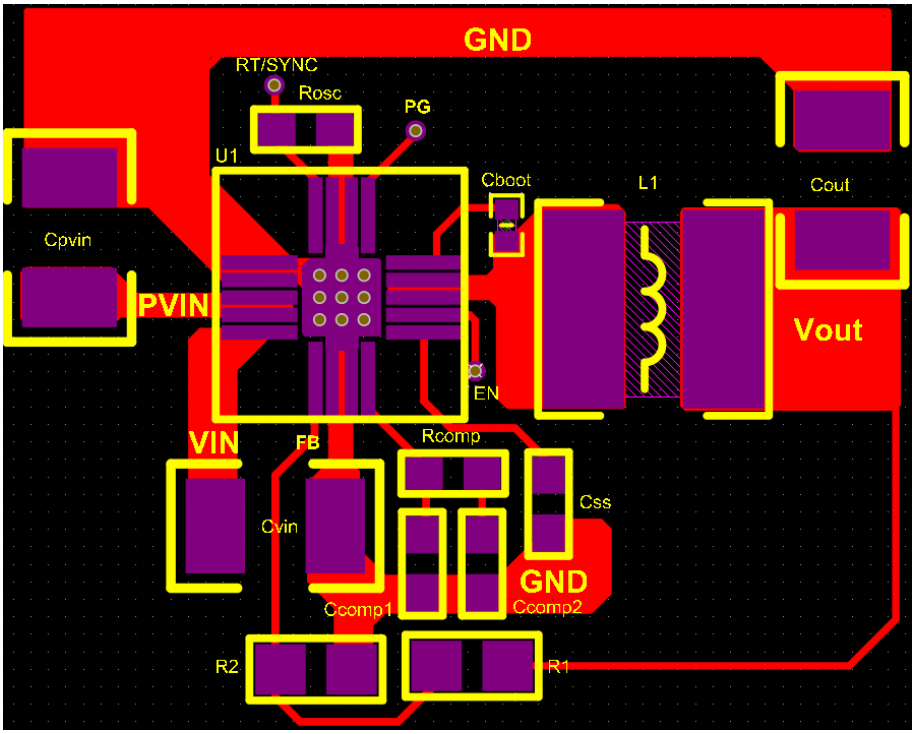
$$C_2 = \frac{1}{2\pi \times \frac{f_{SW}}{2} \times R_1}$$

5. Generally, C2 is an optional component used to enhance noise immunity.

Layout Guidelines

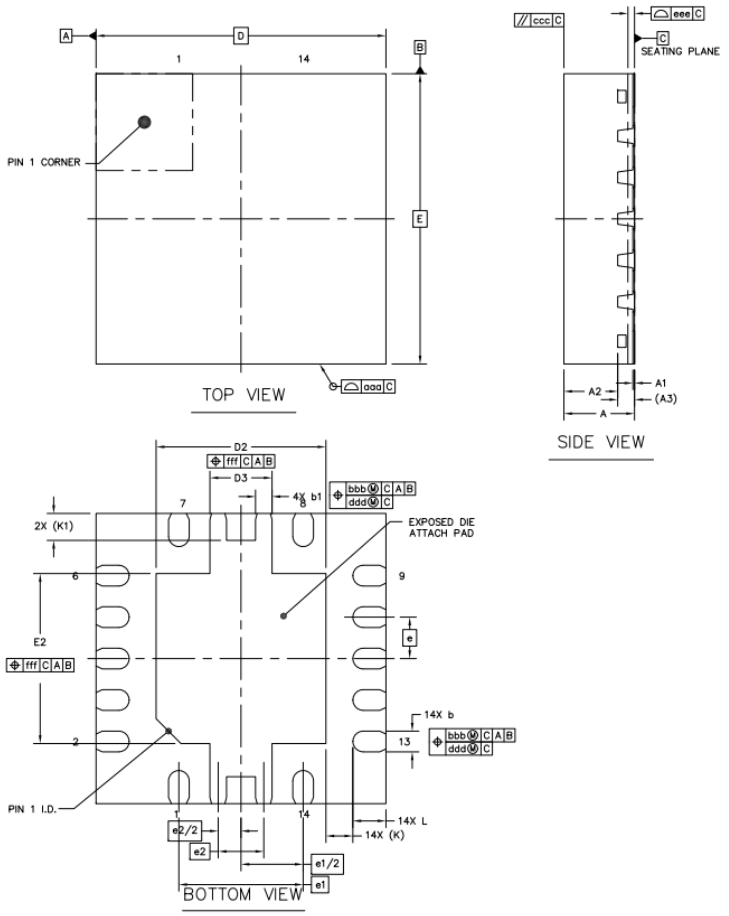
Layout is extremely important for power supply designs, please follow the guidelines as below for optimal performance of the device.

- Keep the traces of the main current paths as short and wide as possible.
- Place the input capacitors as close as possible to the VIN and PVIN pins. Low ESR ceramic bypass capacitors with X5R or X7R dielectric are strongly recommended.
- LX node is with high frequency voltage swing and should be kept at minimized PCB area. Place output inductor close to LX node while keep analog components away from the LX node to prevent noise pickup.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the device.
- Connect all analog grounds to a common node and then connect the common node to the power ground behind the output capacitors.
- Tie GND pin directly to the power pad under the IC.
- Please refer to figure as below for optimal PCB layout example.



PHYSICAL DIMENSIONS

Table: Chip Dimensions

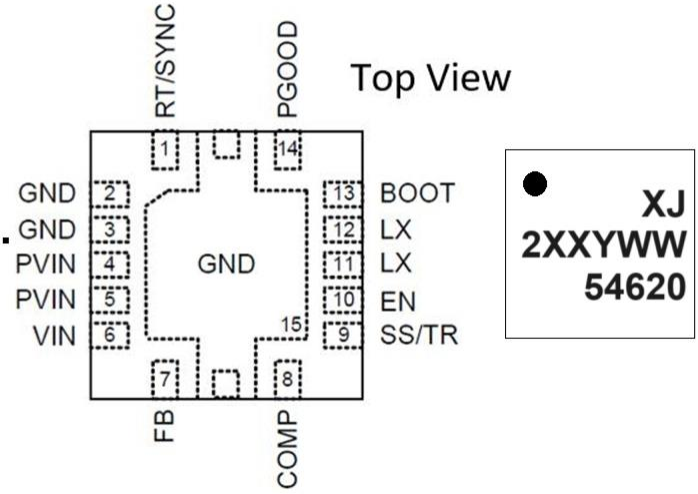


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
		b1	0.15	0.2	0.25
BODY SIZE	X	D		3.5 BSC	
	Y	E		3.5 BSC	
LEAD PITCH		e		0.5 BSC	
		e1		1.5 BSC	
		e2		0.55 BSC	
EP SIZE	X	D2	1.95	2.05	2.15
	Y	E2	1.95	2.05	2.15
	X	D3	0.65	0.75	0.85
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.325 REF	
EXPOSED PAD EDGE TO PACKAGE EDGE		K1		0.325 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

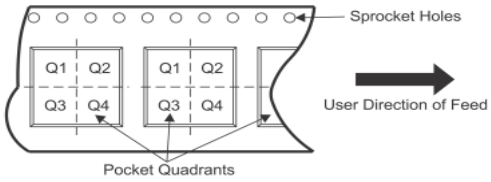
NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;
4.FINISH: Cu/EP · Sn8~20s

MARKING AND REEL INFORMATION

Format:



Pin 1 located in Q1 direction in T&R



Remark:

Font: Arial

Logo of XINJI should be required and placed on assigned Logo position as upside illustration.

Trace-ability Code:

1. Manufacturing Location Code + Assembly lot#+Year Code+WK code Line 1

a) 1st digit: Assembly location code: JCET: 2
b) 2nd & 3rd digit: Assembly lot number
c) 4th digit: Year code:

Year Code 2020-2051

Year	Code
2020	0
2021	1
2022	2
2023	3
2024	4
2025	5
2026	7
2027	C

Year	Code
2028	D
2029	E
2030	F
2031	H
2032	I
2033	J
2034	K
2035	L

Year	Code
2036	N
2037	P
2038	R
2039	S
2040	T
2041	U
2042	V
2043	X

Year	Code
2044	Y
2045	Z
2046	b
2047	c
2048	d
2049	h
2050	i
2051	j

d)5th & 6th digit: Week code, 01 means the 1st Work Week base on XinJi's calendar.

2. Line2: Product Name Code:

Product Name	P/N Code	Remark
XPC54620	54620	