



ZL30771, ZL30772, ZL30773

IEEE 1588 & Synchronous Ethernet Packet Clock Network Synchronizers

Product Brief

October 2017

Features

- **One, Two or Three DPLL Channels**
 - Packet and/or physical-layer frequency, phase and time synchronization
 - Physical-layer compliance with ITU-T G.8262, G.813, G.812, Telcordia GR-1244, GR-253
 - Packet-timing compliance with ITU-T G.8261, G.8263, G.8273.2, G.8273.4
 - Enables 5G wireless applications with sub-100ns time/phase alignment requirements
 - Programmable bandwidth, 0.1mHz to 470Hz
 - Hitless reference switching and mode switching
 - High-resolution holdover averaging
 - Programmable phase slope limit for transients, down to 1 ns/s
 - Per-DPLL phase adjustment, 1ps resolution
- **Input Clocks**
 - Accepts up to 10 differential or CMOS inputs
 - Any input frequency from 0.5Hz to 900MHz
 - Per-input activity and frequency monitoring
 - Automatic or manual reference switching
 - Fast lock to 1 PPS input, <30 seconds
 - Any input can be a 1PPS SYNC input for REF+SYNC frequency/phase/time locking
 - Any input can be a clock with embedded 1PPS
 - Per-input phase adjustment, 1ps resolution
- **Output Clock Frequency Generation**
 - Any output frequency from <0.5Hz to 1045MHz (180MHz max for Synth0)
 - High-resolution fractional frequency conversion with 0ppm error
 - Synthesizers 1 & 2 have integer and fractional dividers to make a total of 5 frequency families
 - Output jitter from Synths 1 & 2 is <0.3ps RMS
 - Output jitter from fractional dividers is typically < 1ps RMS, many frequencies <0.5ps RMS
 - Each HPOUTP/N pair can be LVDS, LVPECL, HCSL, 2xCMOS, HSTL or programmable diff.
 - Four output banks each with VDDO pin; CMOS output voltages from 1.5V to 3.3V
 - Per-synthesizer phase adjust, 1ps resolution

Ordering Information

ZL30771LFG7	1-Channel	80-lead LGA	Trays
ZL30772LFG7	2-Channel	80-lead LGA	Trays
ZL30773LFG7	3-Channel	80-lead LGA	Trays

Matte Tin

Package size: 11 x 11 mm

-40°C to +85°C

- Per-output programmable duty cycle
- Precise output alignment circuitry and per-output phase adjustment
- Per-output enable/disable and glitchless start/stop (stop high or low)
- **Local Oscillator**
 - Operates from a single TCXO or OCXO: 23.75-25MHz, 47.5-50MHz, 114.285-125MHz
 - Very-low-jitter applications can connect a TCXO or OCXO as the stability reference and a low-jitter XO as the jitter reference
- **General Features**
 - Automatic self-configuration at power-up from internal Flash memory
 - Input-to-output alignment <2ns
 - Internal compensation (1ppt) for local oscillator frequency error in DPLLs and input monitors
 - Numerically controlled oscillator behavior in each DPLL and each fractional output divider
 - Programmable Time of Day counters
 - Easy-to-configure design requires no external VCXO or loop filter components
 - 7 GPIO pins with many possible behaviors
 - SPI or I²C processor Interface
 - 1.8V and 3.3V core VDD voltages
 - Power: 1.3W for 2 inputs, 1 synth, 6 LVDS out
 - Easy-to-use evaluation/programming software
 - Factory programmable power-up configuration

Applications

- Central system timing ICs for SyncE and/or IEEE 1588, SONET/SDH, OTN, wireless base station and other carrier-grade systems
- G.8262/813 EEC/SEC, Telcordia Stratum 2-4

1. Block Diagram

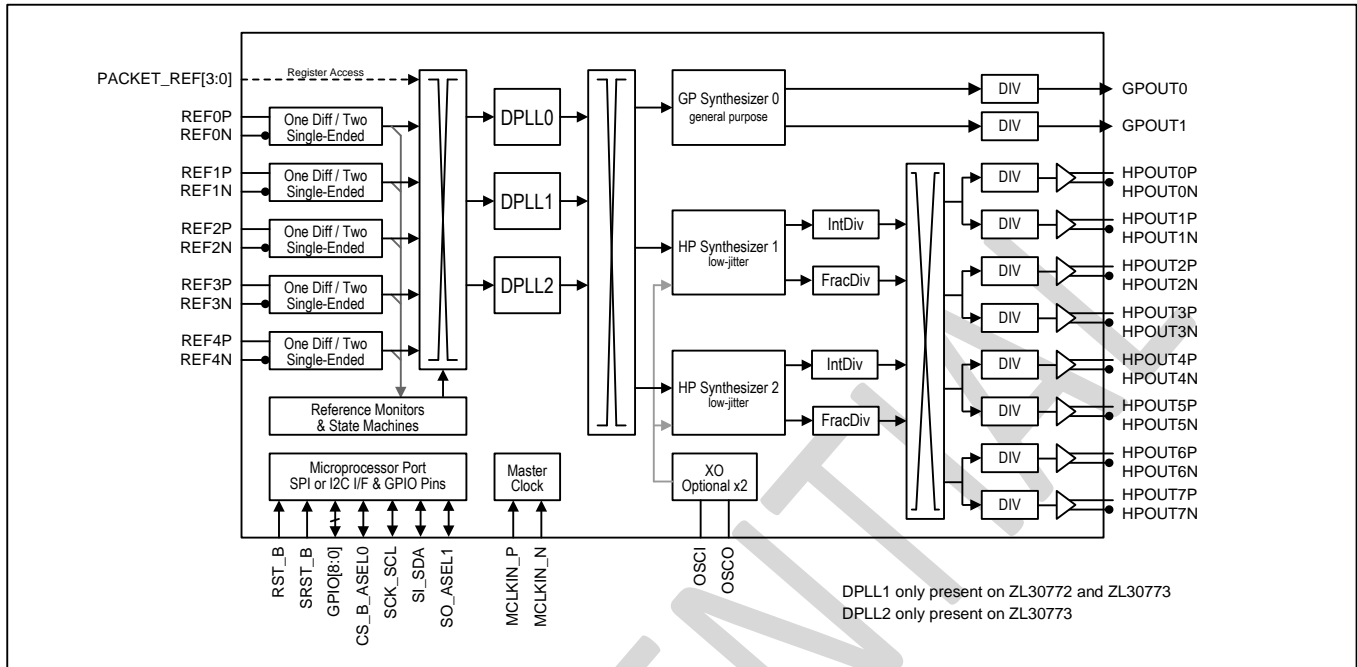


Figure 1 - Functional Block Diagram

2. Application Example

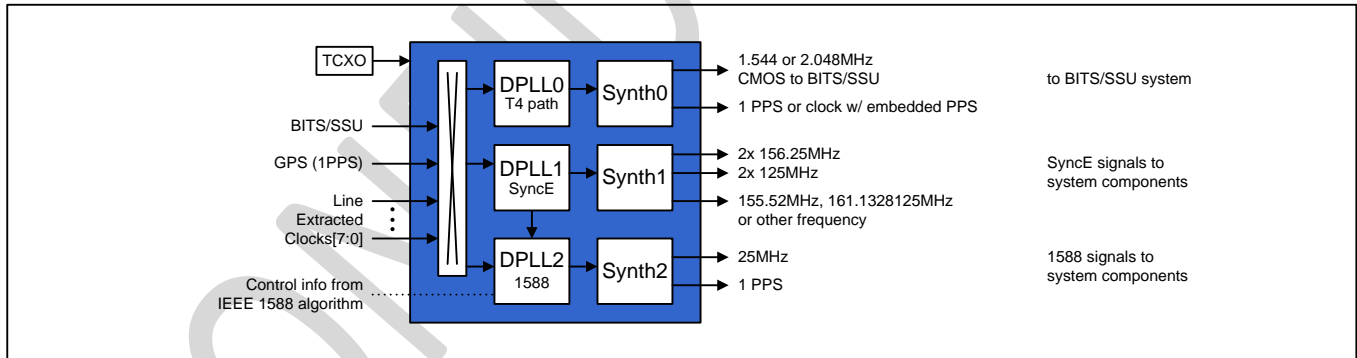


Figure 2 - Synchronous Ethernet and IEEE 1588 Central Timing Application

3. Detailed Features

3.1 Input Block Features

- Ten input reference pins; each can accept a CMOS signal or the POS side of a differential pair; or two can be paired to accept both sides of a differential pair
- Any input can be a SYNC signal for REF+SYNC frequency/phase/time locking
- Any input can be a clock signal with embedded PPS signal (duty cycle distortion indicates PPS location)
- Input clocks can be any frequency from 0.5Hz up to 900MHz (180MHz max for CMOS inputs)
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN, wireless
- Inputs constantly monitored by programmable frequency and single-cycle monitors
- Single-cycle monitor can quickly disqualify a reference when measured period is incorrect
- Frequency measurement (ppb or Hz) and monitoring (coarse, fine, and frequency-step monitors)
- Optional input clock invalidation on GPIO assertion to react to LOS signals from PHYs
- Input-to-input phase measurement, 1ps resolution
- Input-to-DPLL phase measurement, 1ps resolution
- Per-input phase adjustment, 1ps resolution

3.2 DPLL Features

- One, two or three full-featured DPLLs
- Very high-resolution DPLL architecture
- State machine automatically transitions among freerun, tracking and holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 0.1mHz to 470Hz
- Less than 0.1dB gain peaking
- Fast frequency/phase/time lock capability for PPS and clock+PPS input references
- Programmable phase-slope limiting (PSL)
- Programmable frequency rate-of-change limiting (FCL)
- Programmable tracking range (i.e. hold-in range)
- Truly hitless reference switching and mode switching
 - Physical-to-physical reference switching
 - Physical-to-packet reference switching
 - Packet-to-physical reference switching
 - Packet-to-packet reference switching
- Per-DPLL phase adjustment, 1ps resolution
- High-resolution frequency and phase measurement
- Fast detection of input clock failure and transition to holdover mode
- High-resolution holdover frequency averaging, better than 0.01ppb when using <10mHz filter
- Time-of-Day registers: 48-bit seconds, 32-bit nanoseconds, writeable on input PPS edge

3.3 Synthesizer Features

- Any-to-any frequency conversion with 0ppm error
- Two low-jitter synthesizers (Synth1, Synth2) with very high-resolution fractional scaling (i.e. non-integer multiplication)
- Two output dividers per low-jitter synthesizer: one integer (4 to 15 plus half divides 4.5 to 7.5) and one 40-bit fractional
- One general-purpose synthesizer (Synth0)
- A total of five output frequency families
- Easy-to-configure, completely encapsulated design requires no external VCXO or loop filter components

3.4 Low-Jitter Output Clock Features

- Up to 16 single-ended outputs (up to 8 differential outputs) from Synth1 and Synth2
- Each output can be one differential output or two CMOS outputs
- Output clocks can be any frequency from 0.5Hz to 1045MHz (250MHz max for CMOS and HSTL)

- Output jitter from Synth1 and Synth2 integer dividers is <0.3ps RMS
- Output jitter from fractional dividers is <1ps RMS, many frequencies <0.5ps RMS
- In CMOS mode, the HPOUTxN frequency can be an integer divisor of the HPOUTxP frequency (Example 1: HPOUT3P 125MHz, HPOUT3N 25MHz. Example 2: HPOUT2P 25MHz, HPOUT2N 1Hz)
- Outputs directly interface (DC coupled) with LVDS, LVPECL, HSTL, HCSL and CMOS components
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN
- Can produce clock frequencies for microprocessors, ASICs, FPGAs and other components
- Can produce PCIe clocks
- Sophisticated output-to-output phase alignment
- Per-synthesizer phase adjustment, 1ps resolution
- Per-output phase adjustment
- Per-output duty cycle / pulse width configuration
- Per-output enable/disable
- Per-output glitchless start/stop (stop high or low)

3.5 General-Purpose Output Clock Features

- Two CMOS outputs from Synth0
- Any frequency from 0.5Hz to 180MHz
- Output jitter is typically 20-30ps
- Useful for applications where the component or system receiving the signal has low bandwidth such as a central timing IC
- Can output a clock signal with embedded PPS (ePPS) (duty cycle distortion indicates PPS location)

3.6 Local Oscillator

- Operates from a single low-cost XO (jitter reference for the device). Acceptable frequencies: 23.75MHz to 25MHz, 47.5MHz to 50MHz, 114.285MHz to 125MHz. Best jitter: ≥ 48 MHz.
- Very-low-jitter applications can connect a TCXO or OCXO (any frequency, any output jitter) as the stability reference and a low-cost low-jitter XO as the jitter reference
- This ability to have separate jitter and stability references greatly reduces the cost of the TCXO or OCXO (no jitter requirement, no high-frequency-requirement) and allows reuse of already-qualified TCXO and OCXO components
- Supports redundant TCXOs connected to two REF pins

3.7 General Features

- Automatic self-configuration at power-up from internal Flash memory
- Input-to-output alignment <200ps with external feedback
- Fast REF+SYNC locking for frequency and 1PPS phase alignment with lower-cost oscillator
- Generates output SYNC signals: 1PPS (IEEE 1588), 2kHz or 8kHz (SONET/SDH) or other frequency
- Internal compensation for local oscillator frequency error in DPLLs and input monitors, 1ppt resolution
- Numerically controlled oscillator (NCO) behavior allows system software to steer DPLL frequency or fractional output divider frequency with resolution better than 0.005ppt
- Spread-spectrum modulation available in each fractional output divider (PCIe compliant)
- Seven general-purpose I/O pins each with many possible status and control options
- SPI or I²C serial microprocessor interface

3.8 Evaluation Software

- Simple, intuitive Windows-based graphical user interface
- Supports all device features and register fields
- Makes lab evaluation of the device quick and easy
- Generates configuration scripts to be stored in internal Flash memory
- Generates full or partial configuration scripts to be run on a system processor
- Works with or without an evaluation board

3.9 Packet Time Synchronization

The Time Synchronization Algorithm is suitable for use in a wide variety of markets and applications, including the following IEEE 1588-2008 Profiles:

- Annex J.3 Delay Request-Response Default Profile
- Annex J.4 Peer-to-peer Default Profile
- ITU-T G.8265.1 Telecom Profile for Frequency Synchronization
- ITU-T G.8275.1 Telecom Profile for Phase with Full Timing Support Networks
- ITU-T G.8275.2 Telecom Profile for Phase with Partial Timing Support Networks
- CableLabs CM-SP-RDTI Remote DTI Profile
- SMPTE ST-2059-2 Professional Broadcast Environment Profile
- IEEE C37.238 Standard Profile for Use of IEEE 1588 Precision Time Protocol in Power System Applications.
- IEC 61850-9-3 Power Utility Automation Profile
- IEEE802.1as AVB-TSN gPTP
- IEEE 1588-2017 Annex J.5 High Accuracy Profile (based on White Rabbit)
- IETF TICTOC Enterprise Profile

3.9.1 Application Targets

The Time Synchronization Algorithm is suitable for many end application targets:

- Frequency accuracy performance for GSM, WCDMA-FDD, LTE-FDD femtocell, small cell (residential, urban, rural, enterprise), picocell and macrocell applications, with target performance less than ± 15 ppb.
- Frequency performance for ITU-T G.823 and G.824 synchronization interface, as well as G.8261 PNT EEC, PNT PEC and CES interface specifications.
- Phase Synchronization performance for WCDMA-TDD, Mobile WiMAX, TD-SCDMA, CDMA2000, LTE-TDD and LTE-A femtocell, small cell (residential, urban, rural, enterprise), picocell and macrocell applications with target performance less than ± 1 μ s phase alignment.
- Time Synchronization for TAI, UTC-traceability and GNSS/GPS replacement.

3.9.2 Packet Networks

The Time Synchronization Algorithm is suitable for high performance over a variety of packet networks:

- ITU-T G.8261 Appendix VI
- ITU-T G.8261.1 network limit compliant
- ITU-T G.8271.1 network limit compliant
- ITU-T G.8271.2 (draft) network limit compliant
- Native Ethernet (switched) & IP (routed) networks
- xDSL
- Microwave
- Fully aware, partially aware and unaware timing supported networks
- Networks including intermediate Boundary Clocks and Transparent Clocks
- Networks with and without SyncE or frequency physical layer support

3.9.3 Clock Specifications

The Time Synchronization Algorithm is suitable to address a variety of standardized clock specifications, including:

- ITU-T G.8263 PEC-S
- ITU-T G.8273.2 T-BC full on-path without SyncE
- ITU-T G.8273.2 T-BC full on-path with SyncE
- ITU-T G.8273.2 T-TSC full on-path without SyncE
- ITU-T G.8273.2 T-TSC full on-path with SyncE
- ITU-T G.8273.4 T-BC-P (draft)
- ITU-T G.8273.4 T-TSC-A (draft)
- ITU-T G.8273.4 T-TSC-P (draft)

3.9.4 Monitoring and Redundancy

The Time Synchronization Algorithm includes monitoring and redundancy for high availability synchronization, including:

- Synchronization to the best available Server
- Client monitoring of secondary Server references
- Monitoring includes full time synchronization reporting of secondary Server
- Supports a programmable number of secondary Server connections
- Hitless reference switching between multiple Servers
- Holdover when Server packet connectivity is lost
- TIE clear option to build out, or clear, phase offsets between Server references

3.9.5 General

The Time Synchronization Algorithm includes many advanced features to aid in high-accuracy and high-stability applications, including:

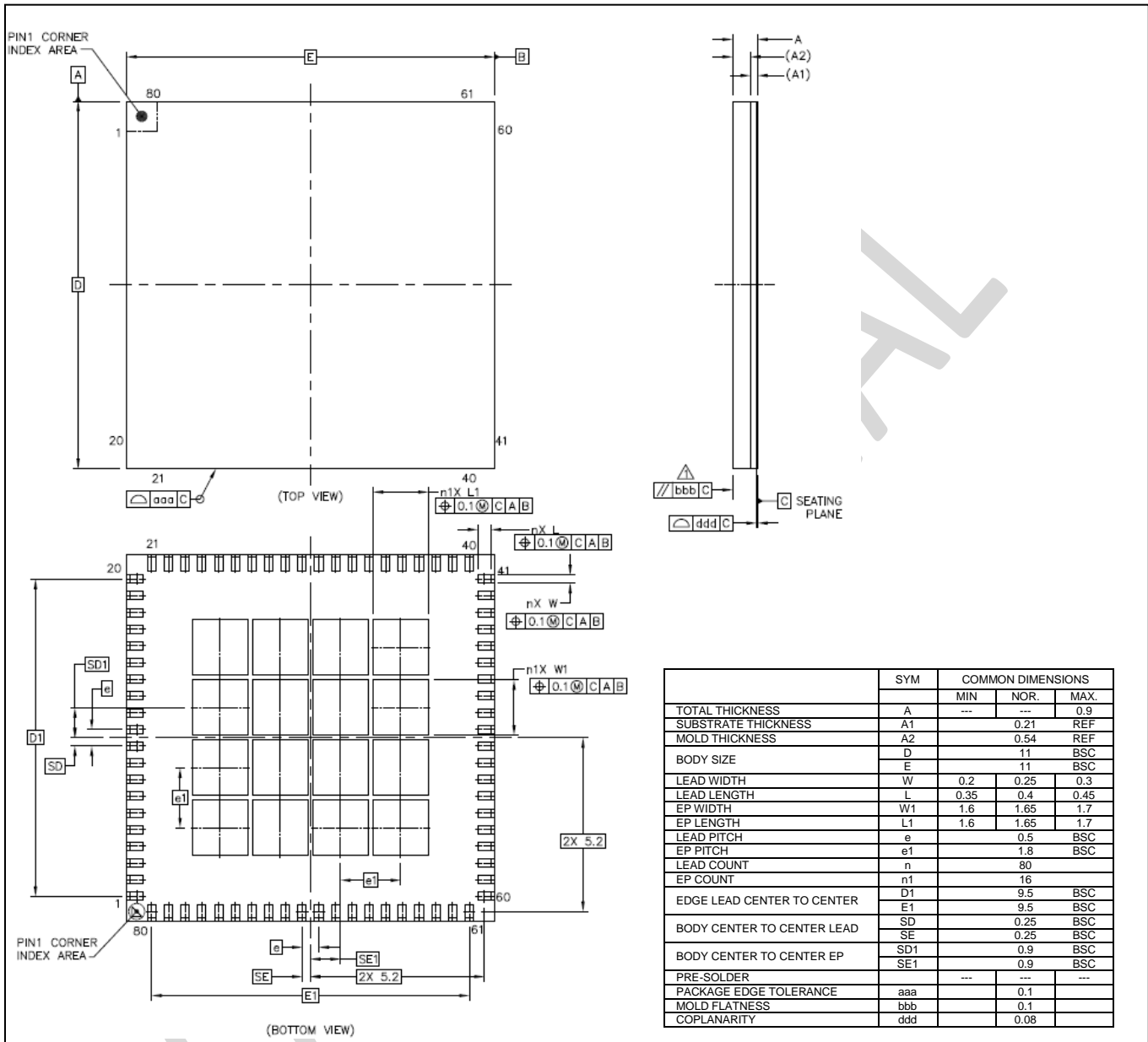
- Full PLL state machine (Freerun, Holdover, Frequency Lock Acquiring, Frequency Lock Acquired, Phase Lock Acquired), with programmable thresholds for state transitions
- Programmable, non-linear packet selection with PDV suppression
- Programmable bandwidth configurability from sub-mHz to hundreds of MHz.
- Programmable packet rates from 1 packet/second to over 128 packets/second
- Programmable phase slope limiting, down to 1 ns/s
- Programmable frequency change limiting, down to 1 ppb/s
- Warm start to initialize or seed the Time Synchronization Algorithm from a stored or last-known-good frequency offset to improve convergence
- Programmable thresholds for management of phase errors - when to adjust with frequency offsets and when to adjust with phase jumps
- User ability to manually add frequency offsets due to temperature or ageing (especially during holdover state)

3.9.6 Reporting

The Time Synchronization Algorithm includes user reporting to aid in performance debugging, including:

- Set of user notifications about packet network events, such as packet loss, small transient phase jumps, large transient phase jumps, outliers, network path re-routes
- Set of metrics related to the synchronization, such as frequency stability and phase stability
- Independent reporting of the forward path and reverse path lock status
- Oscillator stability analysis for excessive ageing or temperature variation
- Server tracking impairments such as pull-in range exceeded

4. Package Outline Drawing





Microsemi Corporate Headquarters
One Enterprise
Aliso Viejo, CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

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