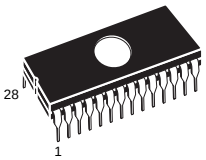
M27C256B

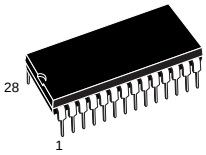
256 Kbit (32Kb × 8) UV EPROM and OTP EPROM

Feature summary

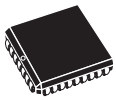
- 5V ± 10% supply voltage in Read operation
- Access time: 45ns
- Low power consumption:
  - Active Current 30mA at 5MHz
  - Standby Current 100µA
- Programming voltage: 12.75V ± 0.25V
- Programming time: 100µs/Word
- Electronic signature
  - Manufacturer Code: 20h
  - Device Code: 8Dh
- ECOPACK® packages available



FDIP28W (F)



PDIP28 (B)



PLCC32 (C)

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1 Summary description

The M27C256B is a 256 Kbit EPROM offered in the two ranges UV (ultra violet erase) and OTP (one time programmable). It is ideally suited for microprocessor systems and is organized as 32,768 by 8 bits.

The FDIP28W (window ceramic frit-seal package) has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C256B is offered in PDIP28 and PLCC32 packages.

In order to meet environmental requirements, ST offers the M27C256B in ECOPACK® packages.

ECOPACK packages are Lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*.

Figure 1. Logic diagram

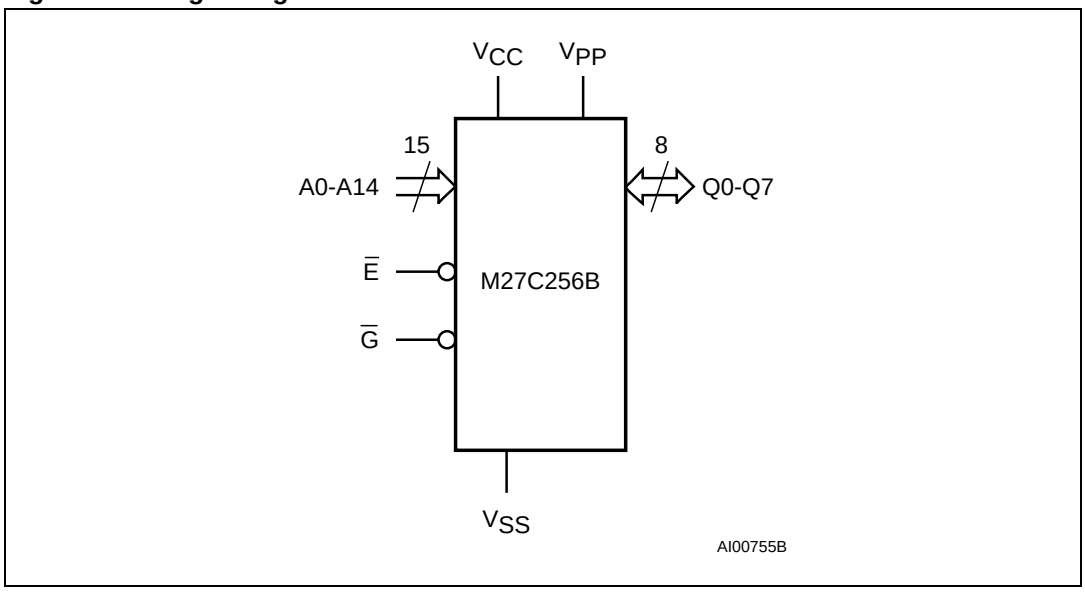


Table 1. Signal names

A0-A14	Address Inputs
Q0-Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally
DU	Don't Use

Figure 2. DIP connections

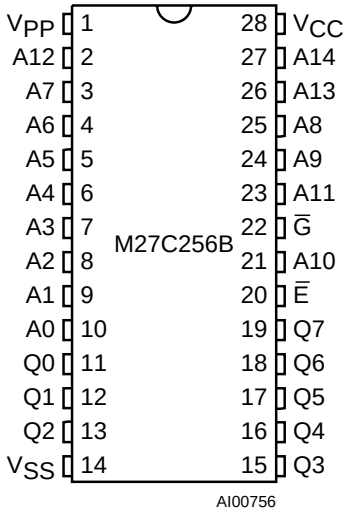
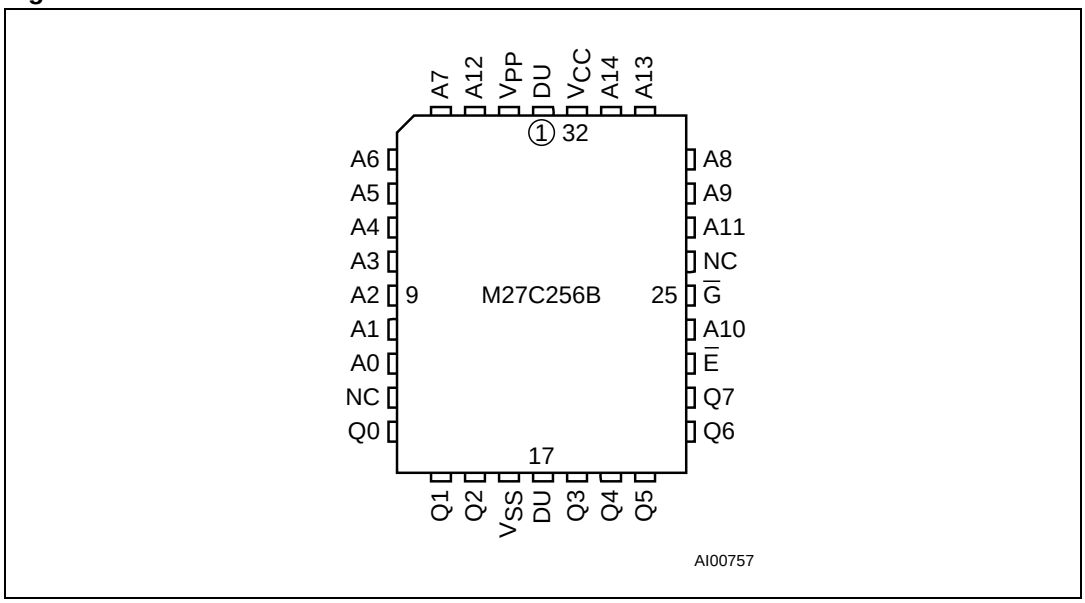


Figure 3. LCC connections



2 Device operation

The operating modes of the M27C256B are listed in the Operating Modes. A single power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

2.1 Read mode

The M27C256B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

2.2 Standby mode

The M27C256B has a standby mode which reduces the supply current from 30mA to 100µA. The M27C256B is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

2.3 Two-line output control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

- the lowest possible memory power dissipation,
- complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

2.4 System considerations

The power switching characteristics of Advance CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of this transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

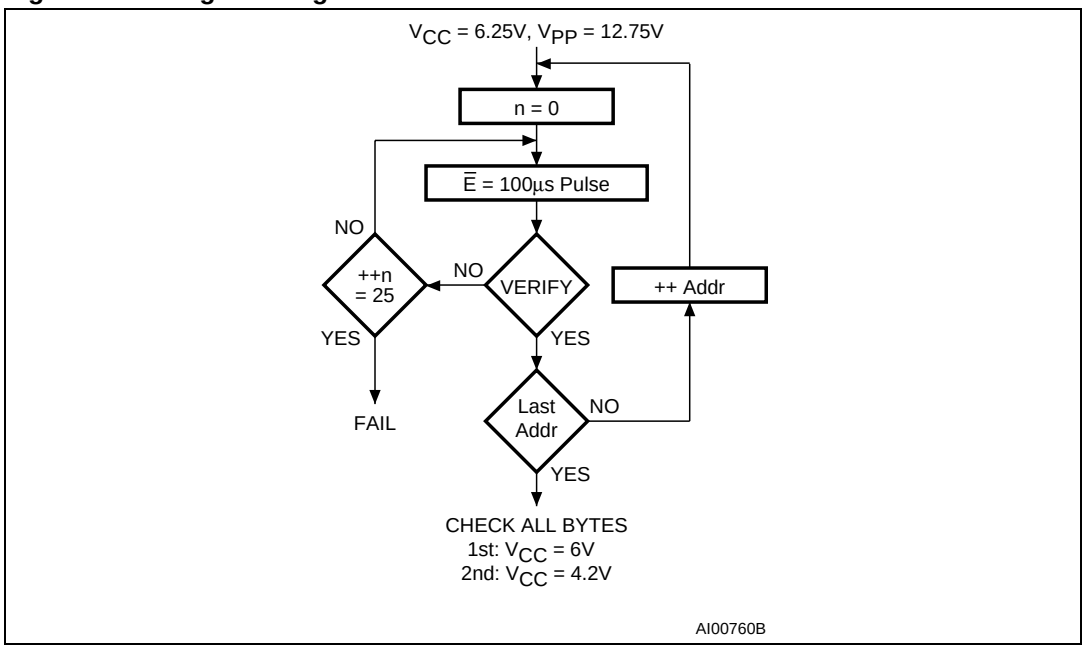
2.5 Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C256B are in the "1" state. Data is introduced by selectively programming "0"s into the desired bit locations. Although only "0"s will be programmed, both "1"s and "0"s can be present in the data word. The only way to change a '0' to a '1' is by die exposure to ultraviolet light (UV EPROM). The M27C256B is in the programming mode when V_{PP} input is at 12.75V, $\overline{G}$ is at V_{IH} and $\overline{E}$ is pulsed to V_{IL}. The data to be programmed is applied to 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25 V.

2.6 PRESTO II programming algorithm

PRESTO II Programming Algorithm allows to program the whole array with a guaranteed margin, in a typical time of 3.5 seconds. Programming with PRESTO II involves the application of a sequence of 100µs program pulses to each byte until a correct verify occurs (see *Figure 4.*). During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Figure 4. Programming flowchart



2.7 Program inhibit

Programming of multiple M27C256Bs in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C256B may be common. A TTL low level pulse applied to a M27C256B's $\overline{E}$ input, with V_{PP} at 12.75V, will program that M27C256B. A high level $\overline{E}$ input inhibits the other M27C256Bs from being programmed.

2.8 Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}, $\overline{E}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

2.9 Electronic signature

The Electronic Signature (ES) mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The ES mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C256B. To activate the ES mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C256B, with $V_{CC} = V_{PP} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the STMicroelectronics M27C256B, these two identifier bytes are given in *Table 3* and can be read-out on outputs Q7 to Q0.

2.10 Erasure operation (applies for UV EPROM)

The erasure characteristics of the M27C256B is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C256B in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C256B is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C256B window to prevent unintentional erasure. The recommended erasure procedure for the M27C256B is exposure to short wave ultraviolet light which has wavelength 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C256B should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

Table 2. Operating modes(1)

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q7-Q0
Read	V_{IL}	V_{IL}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

1. X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V.

Table 3. Electronic signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	0	0	1	1	0	1	8Dh

3 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature(1)	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}(2)	Input or Output Voltage (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9}(2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

1. Depends on range.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

4 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 5. AC measurement conditions

	High Speed	Standard
Input Rise and Fall Times	≤10ns	≤20ns
Input Pulse Voltages	0 to 3V	0.4V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 5. AC testing input output waveform

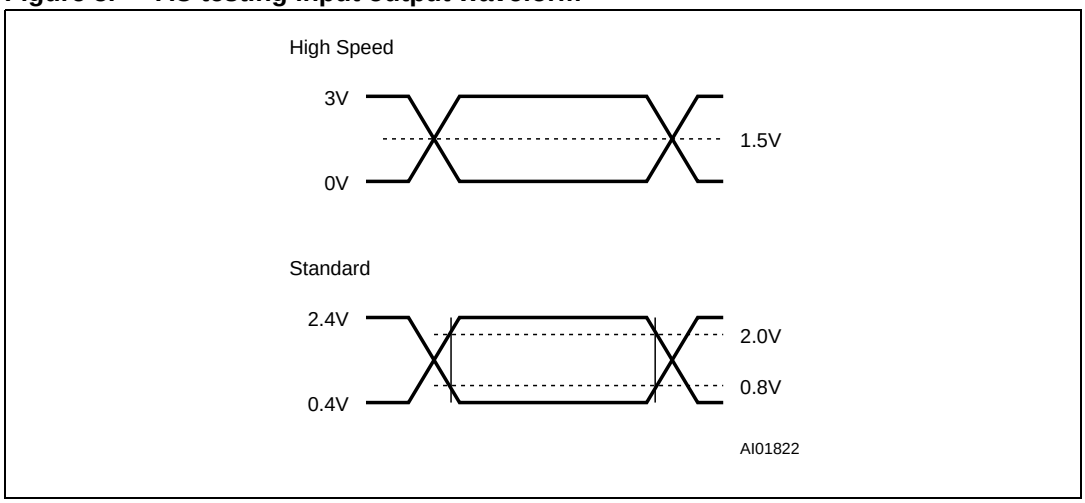


Figure 6. AC testing load circuit

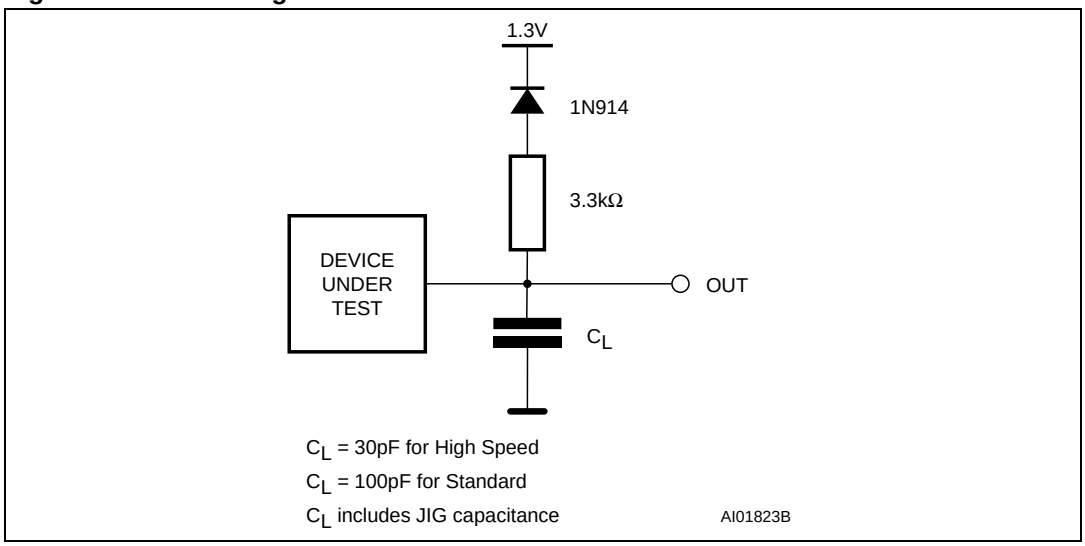


Table 6. Capacitance(1) (2)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

1. Sampled only, not 100% tested.
2. (T_A = 25 °C, f = 1 MHz)

Table 7. Read mode DC characteristics(1) (2)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤V_{IN} ≤V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤V_{OUT} ≤V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		100	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}(3)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	3.6		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

1. T_A = 0 to 70°C, –40 to 85°C, –40 to 105°C or –40 to 125°C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC}.
2. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
3. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 8. Programming mode DC characteristics(1) (2)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \leq V_{IN} \leq V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	3.6		V
V_{ID}	A9 Voltage		11.5	12.5	V

1. T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V.
2. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Figure 7. Read mode AC waveforms

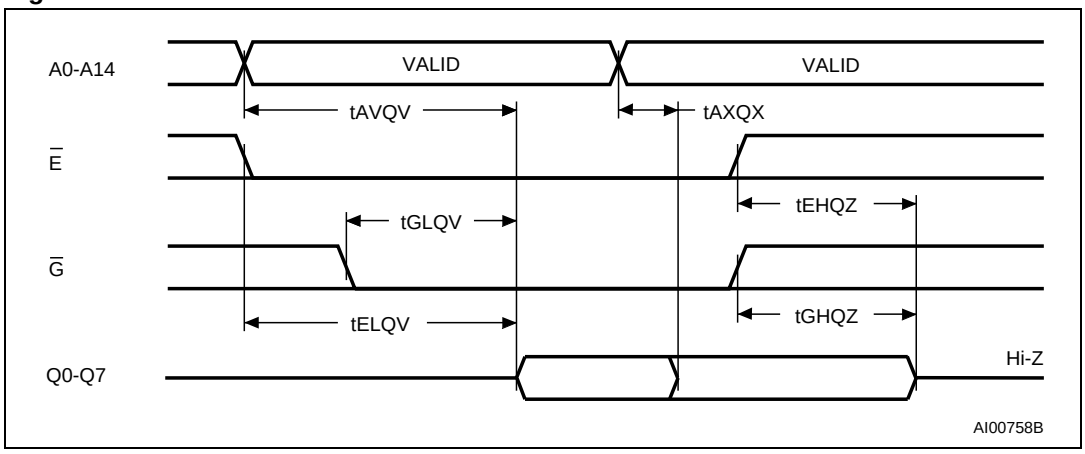


Table 9. Read mode AC characteristics(1) (2)

Symbol	Alt	Parameter	Test Condition	M27C256B								Unit
				-45(3)		-60		-70		-80		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		45		60		70		80	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		45		60		70		80	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		25		30		35		40	ns
t_{EHQZ}(4)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	25	0	30	0	30	0	30	ns
t_{GHQZ}(4)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	25	0	30	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		0		ns

1. T_A = 0 to 70°C, –40 to 85°C, –40 to 105°C or –40 to 125°C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC}
2. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
3. Speed obtained with High Speed AC measurement conditions.
4. Sampled only, not 100% tested.

Table 10. Read mode AC characteristics 2(1) (2)

Symbol	Alt	Parameter	Test Condition	M27C256B								Unit
				-90		-10		-12		-15/-20/-25		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		90		100		120		150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		90		100		120		150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		40		50		60		65	ns
t_{EHQZ}(3)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	30	0	40	0	50	ns
t_{GHQZ}(3)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	30	0	40	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		0		ns

1. T_A = 0 to 70°C, –40 to 85°C, –40 to 105°C or –40 to 125°C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC}
2. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
3. Sampled only, not 100% tested.

Figure 8. Programming and Verify modes AC waveforms

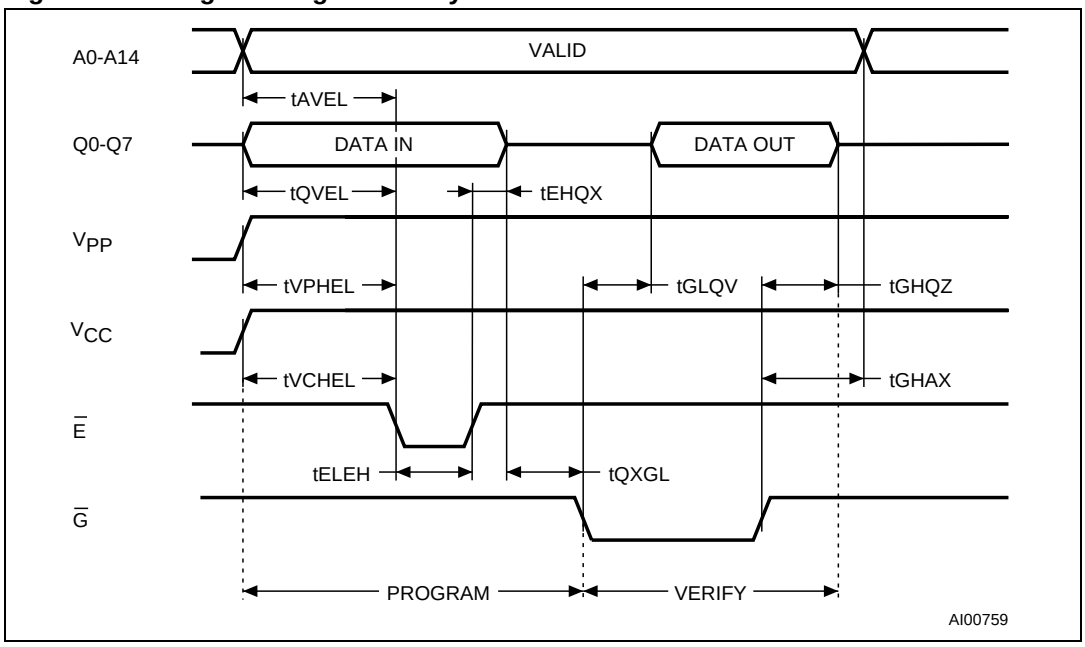


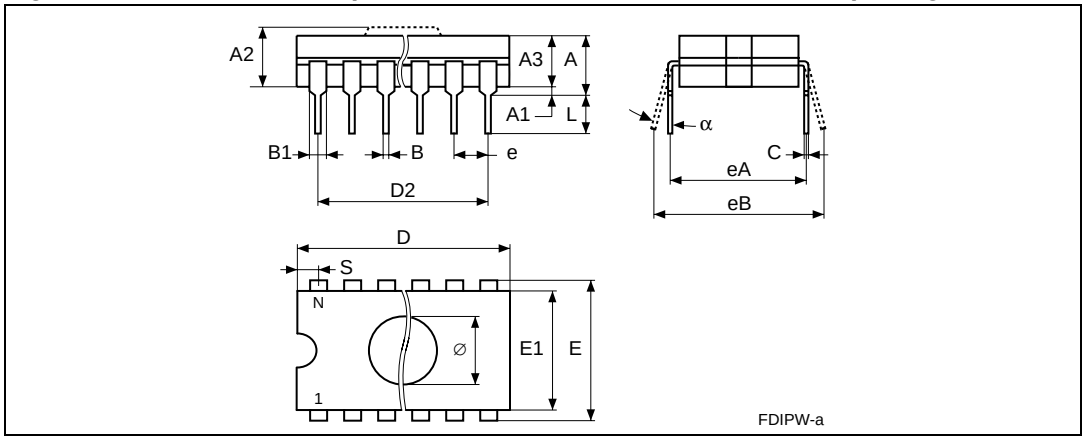
Table 11. Programming mode AC characteristics(1) (2)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ}	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

1. T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V.
2. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

5 Package mechanical

Figure 9. FDIP28WB - 28 pin Ceramic Frit-seal DIP, with window, package outline

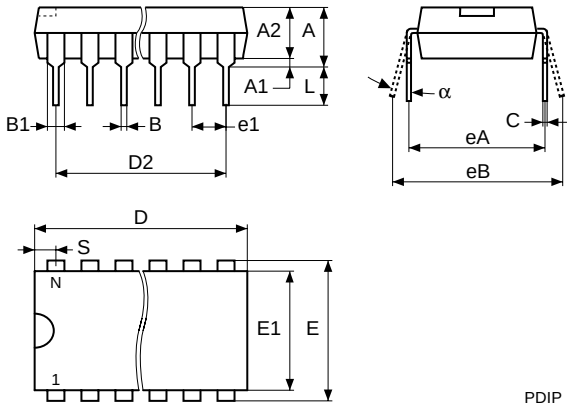


1. Drawing is not to scale.

Table 12. FDIP28WB - 28 pin Ceramic Frit-seal DIP, with window (round 0.280"), package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.72			0.225
A1		0.51	1.40		0.020	0.055
A2		3.91	4.57		0.154	0.180
A3		3.89	4.50		0.153	0.177
B		0.41	0.56		0.016	0.022
B1	1.45	–	–	0.057	–	–
C		0.23	0.30		0.009	0.012
D		36.50	37.34		1.437	1.470
D2	33.02	–	–	1.300	–	–
E	15.24	–	–	0.600	–	–
E1		13.06	13.36		0.514	0.526
e	2.54	–	–	0.100	–	–
eA	14.99	–	–	0.590	–	–
eB		16.18	18.03		0.637	0.710
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
∅	7.11	–	–	0.280	–	–
α		4°	11°		4°	11°
N	28			28		

Figure 10. PDIP28 - 28 pin Plastic DIP, 600 mils width, package outline

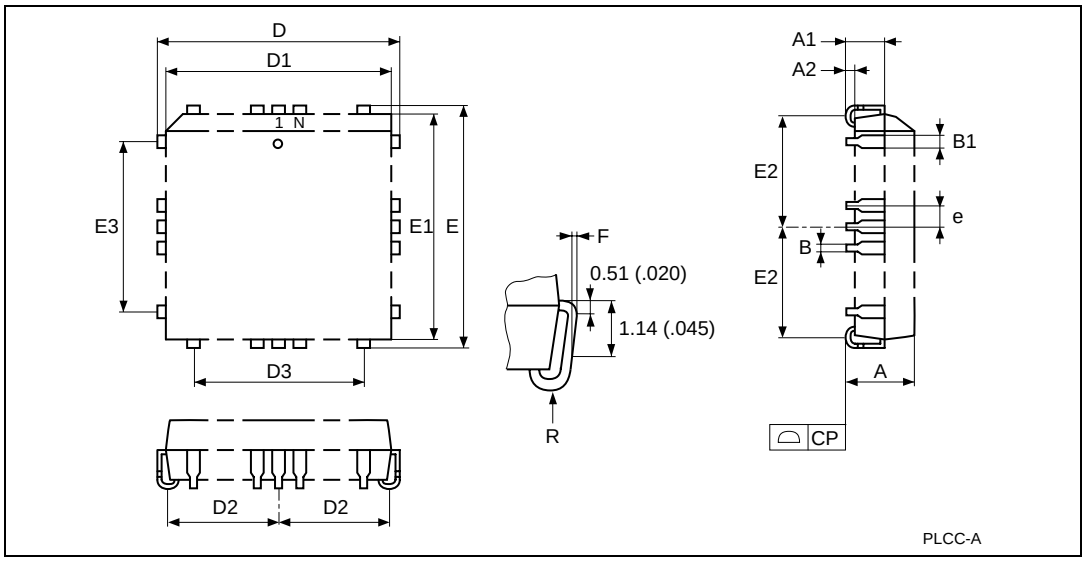


1. Drawing is not to scale.

Table 13. PDIP28 - 28 pin Plastic DIP, 600 mils width, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	4.445			0.1750		
A1	0.630			0.0248		
A2	3.810	3.050	4.570	0.1500	0.1201	0.1799
B	0.450			0.0177		
B1	1.270			0.0500		
C		0.230	0.310		0.0091	0.0122
D	36.830	36.580	37.080	1.4500	1.4402	1.4598
D2	33.020	–	–	1.3000	–	–
E	15.240			0.6000		
E1	13.720	12.700	14.480	0.5402	0.5000	0.5701
e1	2.540	–	–	0.1000	–	–
eA	15.000	14.800	15.200	0.5906	0.5827	0.5984
eB		15.200	16.680		0.5984	0.6567
L	3.300			0.1299		
S		1.78	2.08		0.070	0.082
α		0°	10°		0°	10°
N	28			28		

Figure 11. PLCC32 - 32 pin Rectangular Plastic Leaded Chip Carrier, package outline



1. Drawing is not to scale.

Table 14. PLCC32 - 32 pin Rectangular Plastic Leaded Chip Carrier, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.17	3.56		0.125	0.140
A1		1.53	2.41		0.060	0.095
A2		0.38	–		0.015	–
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
CP			0.10			0.004
D		12.32	12.57		0.485	0.495
D1		11.35	11.51		0.447	0.453
D2		4.78	5.66		0.188	0.223
D3	7.62	–	–	0.300	–	–
E		14.86	15.11		0.585	0.595
E1		13.89	14.05		0.547	0.553
E2		6.05	6.93		0.238	0.273
E3	10.16	–	–	0.400	–	–
e	1.27	–	–	0.050	–	–
F		0.00	0.13		0.000	0.005
R	0.89	–	–	0.035	–	–
N	32			32		

6 Part numbering

Table 15. Ordering information scheme

Example: M27C256B -70 X C 1 TR

Device Type
M27

Supply Voltage
C = 5V

Device Function
256B = 256 Kbit (32Kb x 8)

Speed
-45 (1)= 45 ns
-60 = 60 ns
-70 = 70 ns
-80 = 80 ns
-90 = 90 ns
-10 = 100 ns
-12 = 120 ns
-15 = 150 ns
-20 = 200 ns
-25 = 250 ns

V_{CC} Tolerance
blank = ± 10%
X = ± 5%

Package
F = FDIP28W
B = PDIP28
C = PLCC32

Temperature Range
1 = 0 to 70 °C
3 = –40 to 125 °C
6 = –40 to 85 °C

Options
TR = Tape & Reel Packing

1. High Speed, see AC Characteristics section for further information.

For a list of available options (Speed, Package, etc) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

7 Revision history

Table 16. Document revision history

Date	Version	Revision Details
July 1998	1.0	First Issue
20-Sep-2000	1.1	AN620 Reference removed
29-Nov-2000	1.2	PLCC codification changed (*Table 15.*)
02-Apr-2001	1.3	FDIP28W mechanical dimensions changed (*Table 12.*)
29-Aug-2002	1.4	Package mechanical data clarified for PDIP28 (*Table 13.*), PLCC32 (*Table 14.*, *Figure 11.*) and TSOP28 (*Table 15.*, *Figure 13.*)
18-May-2006	2	Document converted to new template (sections added, information moved). TSOP28 package removed. Packages are ECOPACK® compliant. X option removed from *Table 15: Ordering information scheme*.

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