钛地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65HVD251

Industrial CAN Bus Transceiver

网址 www.sztdbdt.com

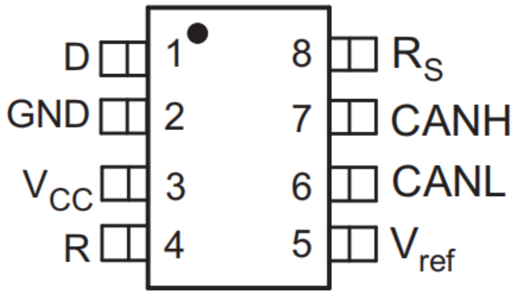
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

●Drop-In Improved Replacement for the PCA82C250 and PCA82C251
●Bus-Fault Protection of±36V
●Meets or Exceeds ISO 11898
●Signaling Rates(1)up to 1 Mbps
●High Input Impedance Allows up to 120 Nodes on a Bus
●Bus Pin ESD Protection Exceeds 14KV HBM
●Unpowered Node Does Not Disturb the Bus
●Low-Current Standby Mode:200-μA Typical
●Thermal Shutdown Protection
●Glitch-Free Power-Up and Power-Down CAN Bu Protection for Hot-Plugging
DeviceNet Vendor ID#806



D Package 8-Pin SOIC
Top View

Applications

●CAN Data Buses
●Industrial Automation
●SAE J1939 Standard Data Bus Interface
●NMEA 2000 Standard Data Bus Interface

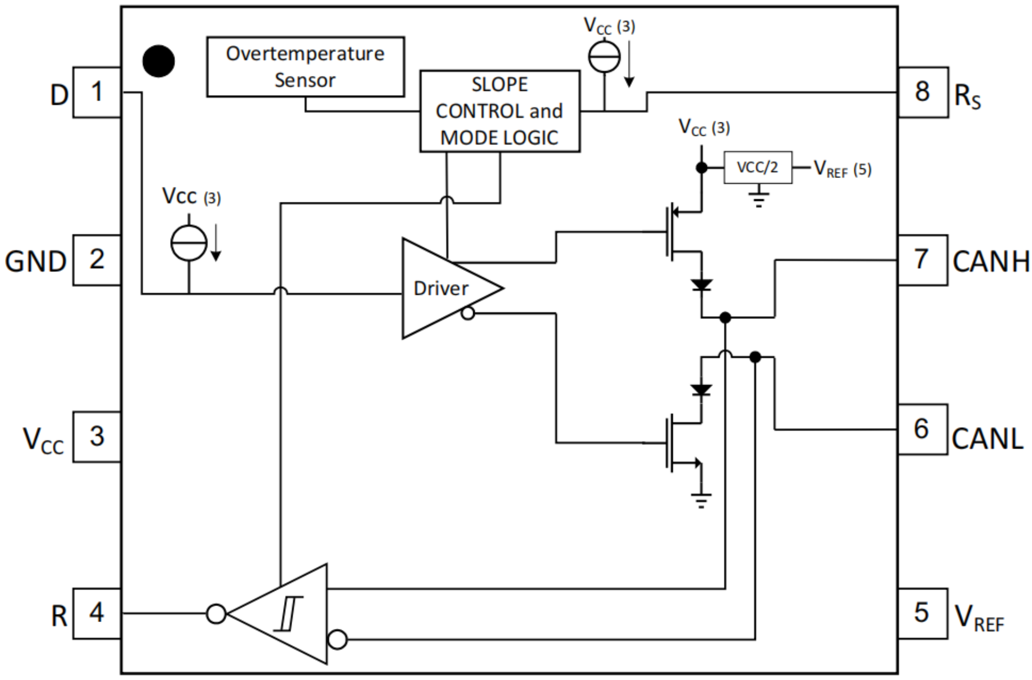
Description

The HVD251 is intended for use in applicationsemploying the Controller Area Network(CAN) serialcommunication physical layer in accordance with theISO 11898 Standard.The HVD251 providesdifferential transmit capability to the bus anddifferential receive capability to a CAN controller atspeeds up to 1 megabits per second(Mbps).
Designed for operation in harsh environments,thedevice features cross-wire,overvoltage and loss ofground protection to ±36 V.Also featured areovertemperature protection as well as -7-V to 12-Vcommon-mode range,and tolerance to transients of±200 V.The transceiver interfaces the single-endedCAN controller with the differential CAN bus found inindustrial,building automation,and automotiveapplications.

Rs,pin 8,selects one of three different modes ofoperation:high-speed,slope control,or low-powermode.The high-speed mode of operation is selectedby connecting pin 8 to ground, allowing thetransmitter output transistors to switch as fast aspossible with no limitation on the rise and fall slope.The rise and fall slope can be adjusted by connectinga resistor to ground at pin 8;the slope is proportionalto the pin's output current.Slope control with anexternal resistor value of 10 kΩ gives about 15-V /μsslew rate;100 kΩ gives about 2-V/μs slew rate.

If a high logic level is applied to the Rs pin 8,thedevice enters a low-current standby mode where thedriver is switched off and the receiver remains active.The local protocol controller returns the device to thenormal mode when it transmits to the bus.

Block Diagram



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CANH	7	I/O	High-level CAN bus line
CANL	6	I/O	Low-level CAN bus line
D	1	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states), also called TXD, driver input
GND	2	GND	Ground connection
R	4	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states), also called RXD, receiver output
R_S	8	I	Mode select pin: strong pulldown to GND = high-speed mode, strong pull up to V_{CC} = low-power mode, 10-kΩ to 100-kΩ pulldown to GND = slope control mode
V_{CC}	3	Supply	Transceiver 5-V supply voltage
V_{REF}	5	O	Reference output voltage

6 Specifications

6.1 Absolute Maximum Ratings[1][2]

			MIN	MAX	UNIT
Supply voltage, V_{CC}			–0.3	7	V
Voltage at any bus pin(CANH or CANL)			–36	36	V
Transient voltage per ISO 7637, pulse 1, 2, 3a, 3b		CANH, CANL	–200	200	V
Input voltage, V_I (D, Rs, or R)			–0.3	V_{CC} + 0.5	V
Receiver output current, I_O			–10	10 mA	mA
Electrical fast transient/burst	IEC 61000-4-4, Classification B	CANH, CANL	–3	3	kV
Continuous total power dissipation			(see *Dissipation Ratings*)		

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground pin.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	All pins	±6000	V
			CANH, CANL and GND	±14000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5		5.5	V
Voltage at any bus terminal (separately or common mode) V_I or V_{IC}		–7[1]		12	V
High-level input voltage, V_{IH}	D input	0.7 V_{CC}			V
Low-level input voltage, V_{IL}	D input			0.3 V_{CC}	V
Differential input voltage, V_{ID}		–6		6	V
Input voltage to Rs, $V_{I(Rs)}$		0		V_{CC}	V
Input voltage at Rs for standby, $V_{I(Rs)}$		0.75 V_{CC}		V_{CC}	V
Rs wave-shaping resistance		0		100	kΩ
High-level output current, I_{OH}	Driver	–50			mA
	Receiver	–4			
Low-level output current, I_{OL}	Driver			50	mA
	Receiver			4	
Operating free-air temperature, T_A	SN65HVD251	–40		125	°C
	SN55HVD251	–55		125	
Junction temperature, T_J				145	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

6.4 Thermal Information

THERMAL METRIC[1]		SN55HVD251	SN65HVD251		UNIT
		DRJ (SON)	D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52	44.6	66.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	73	78.7	48.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Supply Current

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
I_{CC}	Supply current	Standby	Rs at V_{CC}, D at V_{CC}			275	µA
		Dominant	D at 0 V, 60-Ω load, Rs at 0 V			65	mA
		Recessive	D at V_{CC}, no load, Rs at 0 V			14	

(1) All typical values are at 25°C and with a 5-V supply.

6.6 Electrical Characteristics: Driver

over recommended operating conditions (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
$V_{O(D)}$	Bus output voltage (Dominant)	CANH	Figure 10 and Figure 11 , D at 0 V Rs at 0 V, T ≥ –40°C	2.75	3.5	4.5	V
		CANL		0.5		2	
$V_{O(R)}$	Bus output voltage (Recessive)	CANH	Figure 10 and Figure 11 , D at 0.7 V_{CC}, Rs at 0 V	2	2.5	3	
		CANL		2	2.5	3	
$V_{OD(D)}$	Differential output voltage (Dominant)		Figure 10 , D at 0 V, Rs at 0 V	1.5	2	3	V
			Figure 12 , D at 0 V, Rs at 0 V, R_{NODE} = 330 Ω	1.2	2	3.1	V
			Figure 12 , D at 0 V, Rs at 0 V, R_{NODE} = 165 Ω, V_{CC} ≥ 4.75 V	1.2	2	3.1	V
$V_{OD(R)}$	Differential output voltage (Recessive)		Figure 10 and Figure 11 , D at 0.7 V_{CC}	–120		12	mV
			D at 0.7 V_{CC}, no load, T ≤ 85°C	–0.5		0.05	V

(1) All typical values are at 25°C and with a 5-V supply.

Electrical Characteristics: Driver (continued)

over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage	Figure 18, Rs at 0 V		600		mV
I_{IH}	High-level input current, D Input	D at 0.7 V_{CC}	–40		0	µA
I_{IL}	Low-level input current, D Input	D at 0.3 V_{CC}	–60		0	µA
$I_{OS(SS)}$	Short-circuit steady-state output current	Figure 20, V_{CANH} at –7 V, CANL Open	–200			mA
		Figure 20, V_{CANH} at 12 V, CANL Open			2.5	
		Figure 20, V_{CANL} at -7 V, CANH Open	–2			
		Figure 20, V_{CANL} at 12 V, CANH Open			200	
C_O	Output capacitance	See receiver input capacitance				
I_{OZ}	High-impedance output current	See receiver input current				
$I_{IRs(s)}$	Rs input current for standby	Rs at 0.75 V_{CC}	–10			µA
$I_{IRs(f)}$	Rs input current for full speed operation	Rs at 0 V	–550		0	µA

6.7 Electrical Characteristics: Receiver

over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	Rs at 0 V, (See Table 1)			750	900	mV
V_{IT-}	Negative-going input threshold voltage			500	650		
V_{hys}	Hysteresis voltage (V_{IT+} - V_{IT-})				100		
V_{OH}	High-level output voltage	Figure 15, I_O = –4 mA		0.8 V_{CC}			V
V_{OL}	Low-level output voltage	Figure 15, I_O = 4 mA				0.2 V_{CC}	V
I_I	Bus input current	CANH or CANL at 12 V	Other bus pin at 0 V, Rs at 0 V, D at 0.7 V_{CC}			600	µA
		CANH or CANL at 12 V, V_{CC} at 0 V				715	
		CANH or CANL at -7 V		–460			
		CANH or CANL at -7 V, V_{CC} at 0 V		–340			
C_I	Input capacitance, (CANH or CANL)	Pin-to-ground, V_I = 0.4 sin (4E6πt) + 0.5 V, D at 0.7 V_{CC}			20		pF
C_{ID}	Differential input capacitance	Pin-to-pin, V_I = 0.4 sin (4E6πt) + 0.5 V, D at 0.7 V_{CC}			10		pF
R_{ID}	Differential input resistance	D at 0.7 V_{CC}, Rs at 0 V		40		100	kΩ
R_{IN}	Input resistance, (CANH or CANL)	D at 0.7 V_{CC}, Rs at 0 V		20		50	kΩ
	Receiver noise rejection	See Figure 22					

6.8 VREF-Pin Characteristics

over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Reference output voltage	–5 µA < I_O < 5 µA	0.45 V_{CC}		0.55 V_{CC}	V
		–50 µA < I_O < 50 µA	0.4 V_{CC}		0.6 V_{CC}	

6.9 Power Dissipation Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Device power dissipation	V_{CC} = 5 V, Tj = 27°C, RL = 60 Ω, R_S at 0 V, Input to D a 500-kHz 50% duty cycle square wave		97.7		mW
		V_{CC} = 5.5 V, Tj = 130°C, RL = 60 Ω, R_S at 0 V, Input to D a 500-kHz 50% duty cycle square wave		142		mW
T_{SD}	Thermal shutdown junction temperature			165		°C

6.10 Switching Characteristics: Driver

over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}	Propagation delay time, low-to-high-level output	Figure 13, Rs at 0 V		40	70	ns
		Figure 13, Rs with 10 kΩ to ground		90	125	
		Figure 13, Rs with 100 kΩ to ground		500	800	
t_{pHL}	Propagation delay time, high-to-low-level output	Figure 13, Rs at 0 V		85	125	
		Figure 13, Rs with 10 kΩ to ground		200	260	
		Figure 13, Rs with 100 kΩ to ground		1150	1450	
$t_{sk(p)}$	Pulse skew ($\|t_{pHL} - t_{pLH}\|$)	Figure 13, Rs at 0 V		45	85	
		Figure 13, Rs with 10 kΩ to ground		110	180	
		Figure 13, Rs with 100 kΩ to ground		650	900	
t_r	Differential output signal rise time	Figure 13, Rs at 0 V	35	80	100	
t_f	Differential output signal fall time		35	80	100	
t_r	Differential output signal rise time	Figure 13, Rs with 10 kΩ to ground	100	150	250	
t_f	Differential output signal fall time		100	150	250	
t_r	Differential output signal rise time	Figure 13, Rs with 100 kΩ to ground	600	950	1550	
t_f	Differential output signal fall time		600	950	1550	
t_{en}	Enable time from standby to dominant	Figure 17			0.5	μs

6.11 Switching Characteristics: Device

over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{loop1}	Total loop delay, driver input to receiver output, recessive to dominant	Figure 19, Rs at 0 V		60	100	ns
		Figure 19, Rs with 10 kΩ to ground		100	150	
		Figure 19, Rs with 100 kΩ to ground		440	800	
t_{loop2}	Total loop delay, driver input to receiver output, dominant to recessive	Figure 19, Rs at 0 V		115	150	ns
		Figure 19, Rs with 10 kΩ to ground		235	290	
		Figure 19, Rs with 100 kΩ to ground		1070	1450	
t_{loop2}	Total loop delay, driver input to receiver output, dominant to recessive	Figure 19, Rs at 0 V, V_{CC} from 4.5 V to 5.1 V		105	145	ns

6.12 Switching Characteristics: Receiver

over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}	Propagation delay time, low-to-high-level output	Figure 15		35	50	ns
t_{pHL}	Propagation delay time, high-to-low-level output			35	50	
$t_{sk(p)}$	Pulse skew ($\|t_{pHL} - t_{pLH}\|$)				20	
t_r	Output signal rise time			2	4	
t_f	Output signal fall time			2	4	
$t_{p(sb)}$	Propagation delay time in standby	Figure 21, Rs at V_{CC}			500	

6.13 Dissipation Ratings

PACKAGE	CIRCUIT BOARD MODEL	T_A = 25°C POWER RATING	DERATING FACTOR [1] ABOVE T_A = 25°C	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
SOIC (D)	Low-K[2]	576 mW	4.8 mW/°C	288 mW	96 mW
	High-K[3]	924 mW	7.7 mW/°C	462 mW	154 mW
PDIP (P)	Low-K[2]	888 mW	7.4 mW/°C	444 mW	148 mW
	High-K[3]	1212 mW	10.1 mW/°C	606 mW	202 mW
WSON (DRJ)	Low-K[2]	403 mW	4.03 mW/°C	262 mW	100 mW
	High-K (no Vias)[3]	1081 mW	10.8 mW/°C	703 mW	270 mW
	High-K (with Vias)	2793 mW	27.9 mW/°C	1815 mW	698 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.
(3) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

7 Parameter Measurement Information

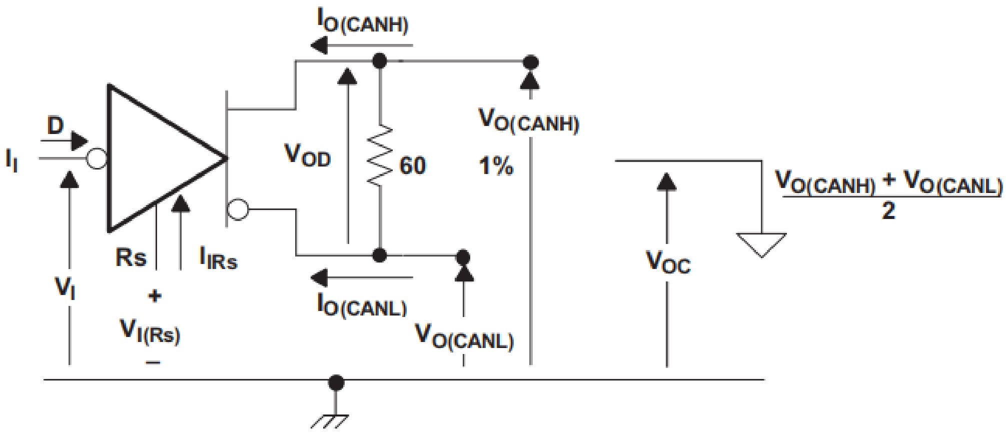


Figure 10. Driver Voltage, Current, and Test Definition

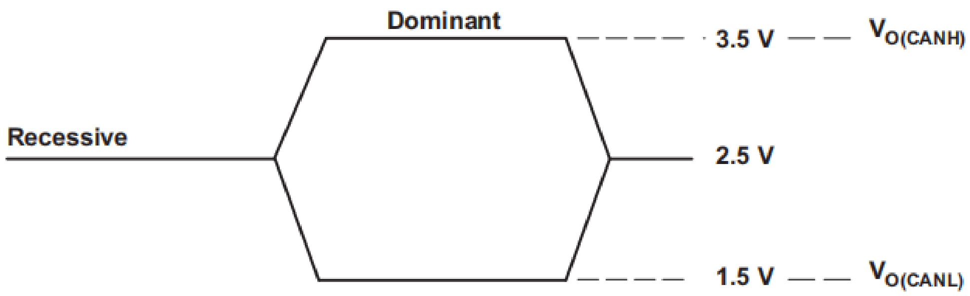


Figure 11. Bus Logic State Voltage Definitions

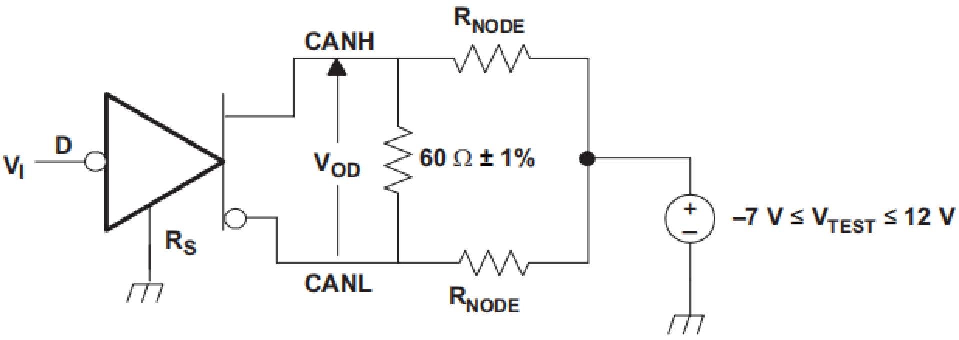


Figure 12. Driver V_{OD}

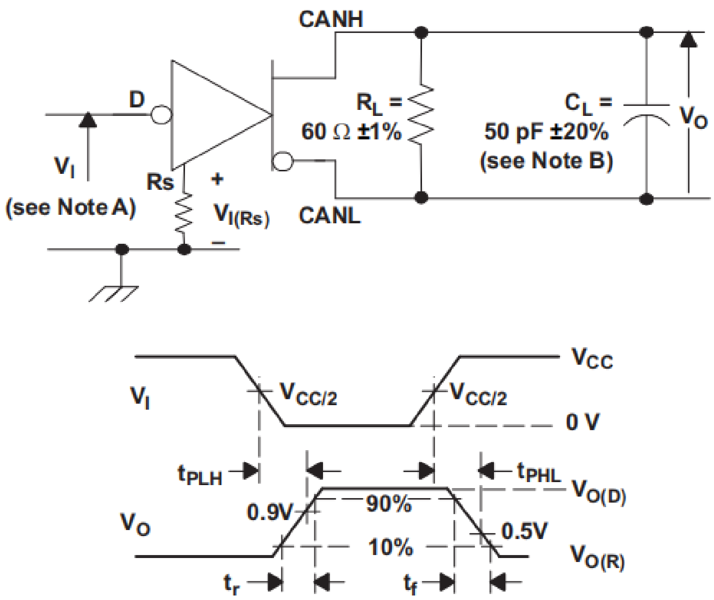


Figure 13. Driver Test Circuit and Voltage Waveforms

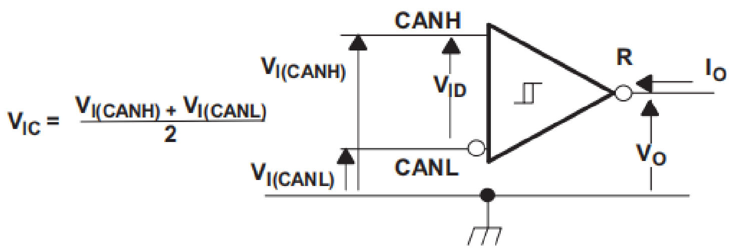
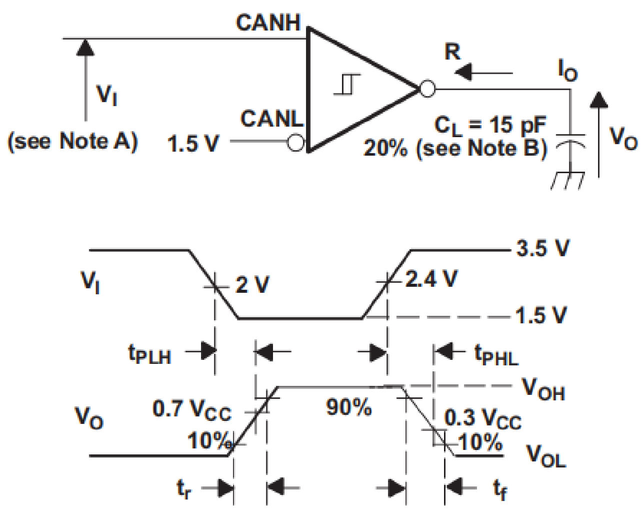


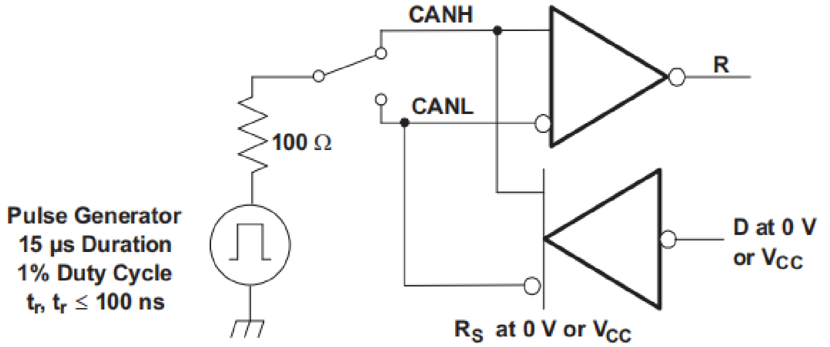
Figure 14. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, $t_r \le$ 6ns, $t_f \le$ 6ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 15. Receiver Test Circuit and Voltage Waveforms



This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 16. Test Circuit, Transient Overvoltage Test

Table 1. Receiver Characteristics Over Common Mode Voltage

INPUT		DIFFERENTIAL INPUT	OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R	
12 V	11.1 V	900 mV	L	V_{OL}
–6.1 V	–7 V	900 mV	L	
–1 V	–7 V	6 V	L	
12 V	6 V	6 V	L	
–6.5 V	–7 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–7 V	–1 V	6 V	H	
6 V	12 V	6 V	H	
open	open	X	H	

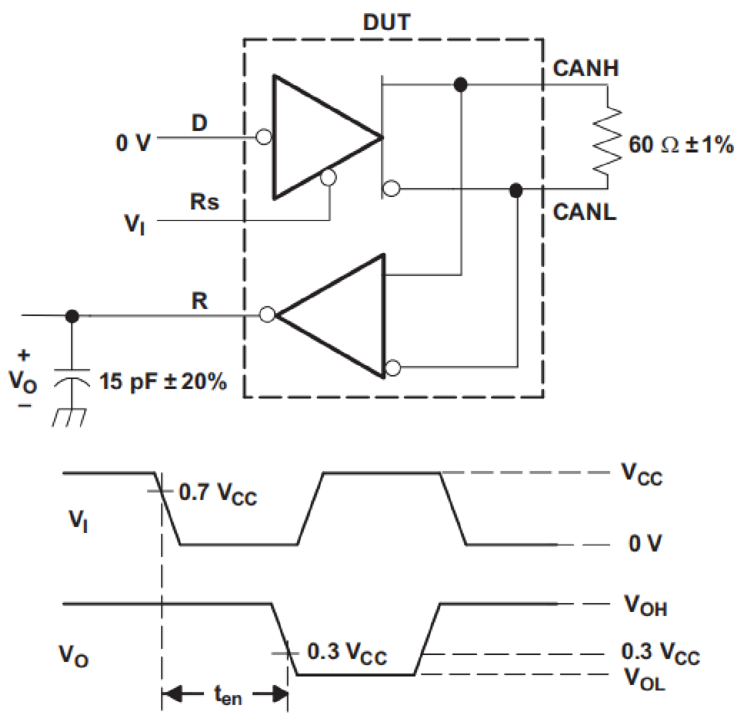
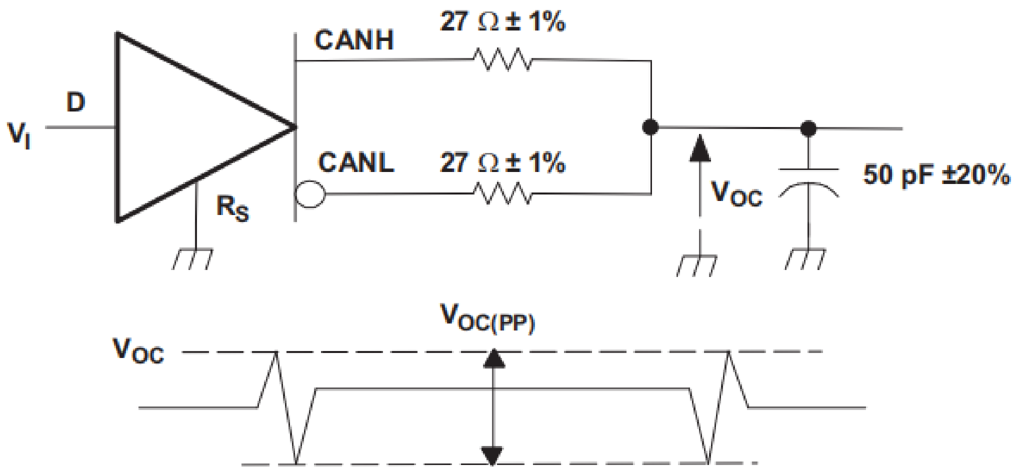


Figure 17. T_{en} Test Circuit and Voltage Waveforms



The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50 Ω.

Figure 18. Peak-to-Peak Common Mode Output Voltage

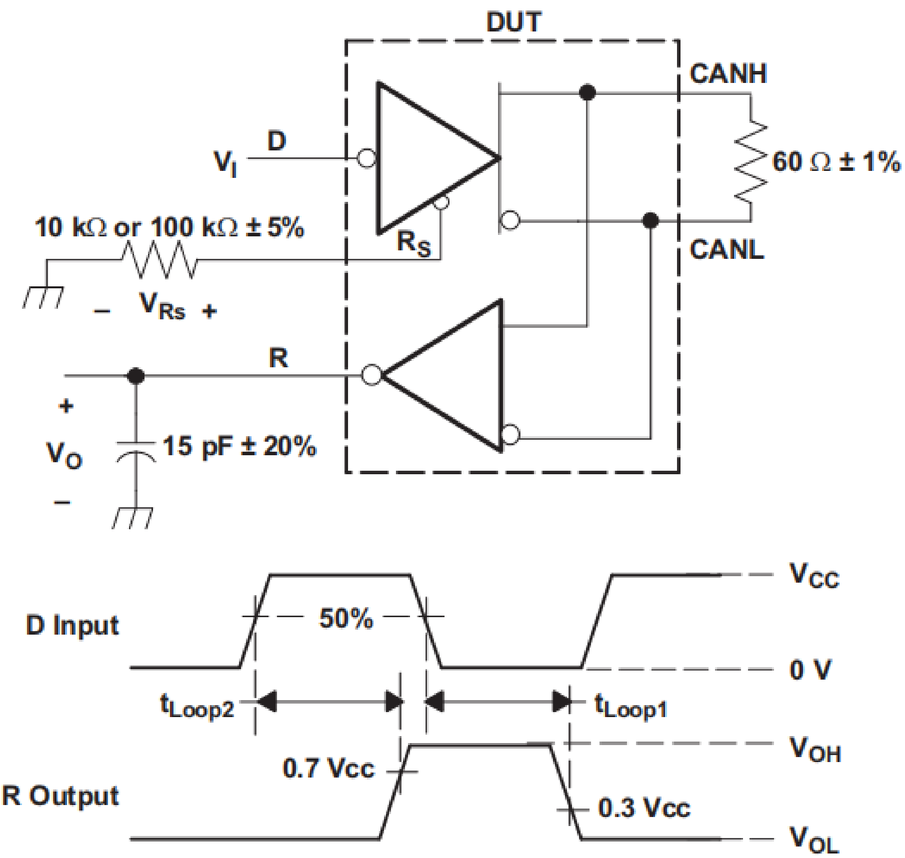


Figure 19. T_{LOOP} Test Circuit and Voltage Waveforms

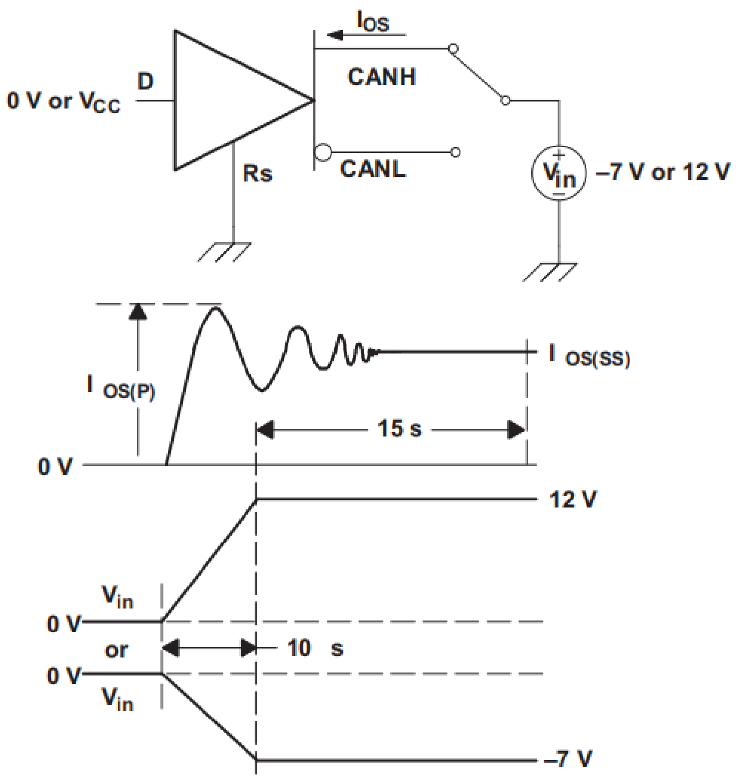
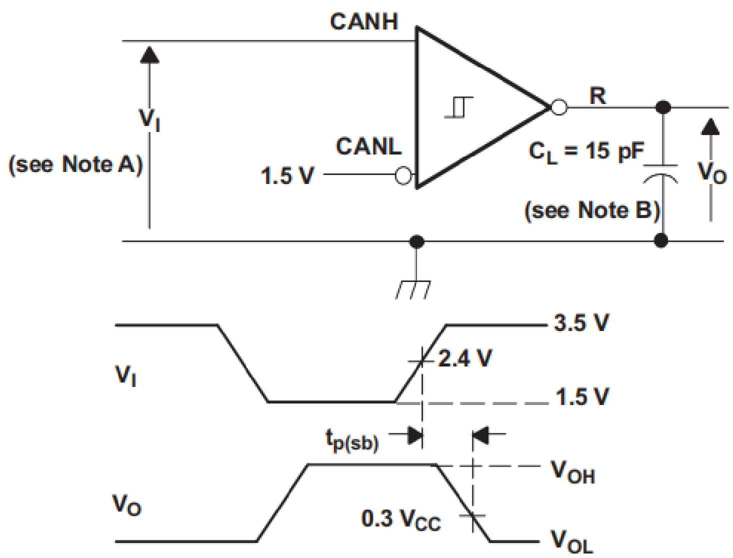


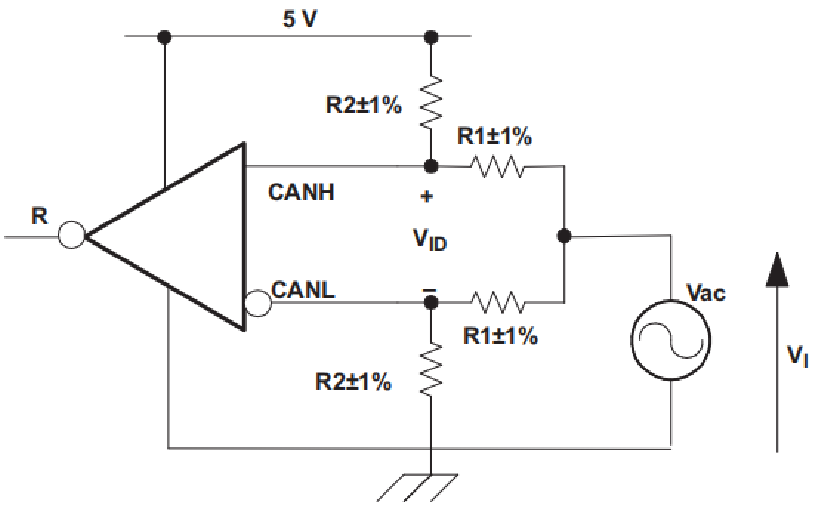
Figure 20. Driver Short-Circuit Test



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50 Ω.

B. CL includes instrumentation and fixture capacitance within ±20%.

Figure 21. Receiver Propagation Delay in Standby Test Circuit and Waveform



V_{ID}	R1	R2
500 mV	50	450
900 mV	50	227

A. All input pulses are supplied by a generator having the following characteristics: f_{IN} < 1.5 MHz, T_A = 25°C, V_{CC} = 5 V.

B. The receiver output should not change state during application of the common-mode input waveform.

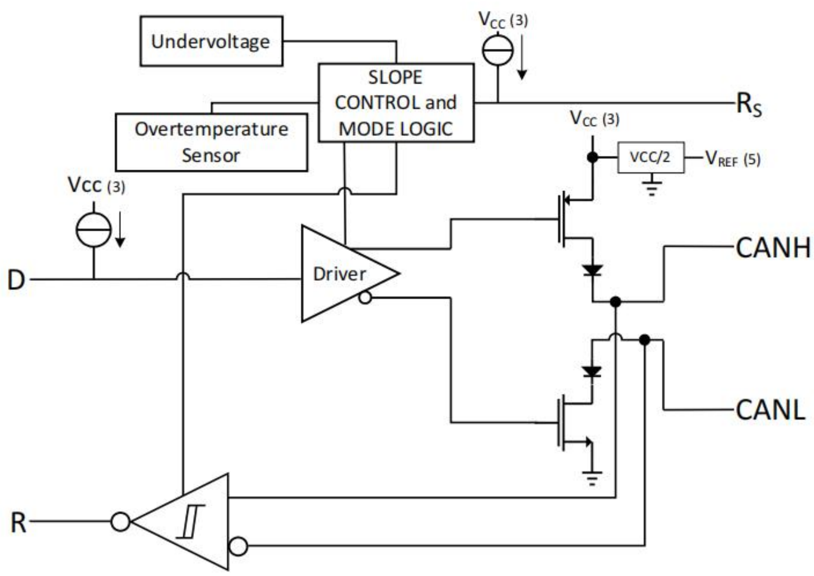
Figure 22. Common-Mode Input Voltage Rejection Test

8 Detailed Description

8.1 Overview

The SNx5HVD251CAN bus transceiver is compatible with the ISO 11898-2 High Speed CAN (Controller Area Network) physical layer standard. It is design to interface between the differential bus lines in controller area network and the CAN protocol controller at data rates up to 1 Mbps.

8.2 Functional Block Diagram



8.3 Feature Description

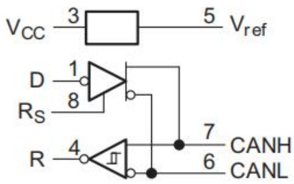


Figure 23. Function Diagram (Positive Logic)

8.3.1 Mode Control

R_S, Pin 8, selects one of three possible modes of operation: high-speed, slope control, or low-power mode.

8.3.2 High-Speed Mode

The high-speed mode of operation can be selected by setting R_S (Pin 8) low. High-speed allows the output to switch as fast as possible with no internal limitations on the output rise and fall slopes. The CAN bus driver and receiver are fully operational and the CAN communication is bi-directional. The driver is translating a digital input on D to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on R.

8.3.3 Slope Control Mode

The rise and fall slope of the SNx5HVD251 driver output can be adjusted by connecting a resistor from Rs (Pin 8) to ground (GND), or to a low-level input voltage as shown in Figure 24. The slope of the driver output signal is proportional to the pin's output current. This slope control is implemented with an external resistor value of 10 kΩ to achieve a ~15-V/μs slew rate, and up to 100 kΩ to achieve a ~2.0-V/μs slew rate. Figure 8 shows a plot of differential output transition time vs slope resistance from which the slew rate can be calculated.

Feature Description (continued)

8.3.4 Low-Power Mode

If a high-level input (>0.75 V_{CC}) is applied to R_S (Pin 8), the circuit enters a low-current, listen only standby mode during which the driver is switched off and the receiver remains active. If using this mode to save system power while waiting for bus traffic, the local controller can monitor the R output pin for a falling edge which indicates that a dominant signal was driven onto the CAN bus. The local controller can then drive the R_S pin low to return to slope control mode or high-speed mode.

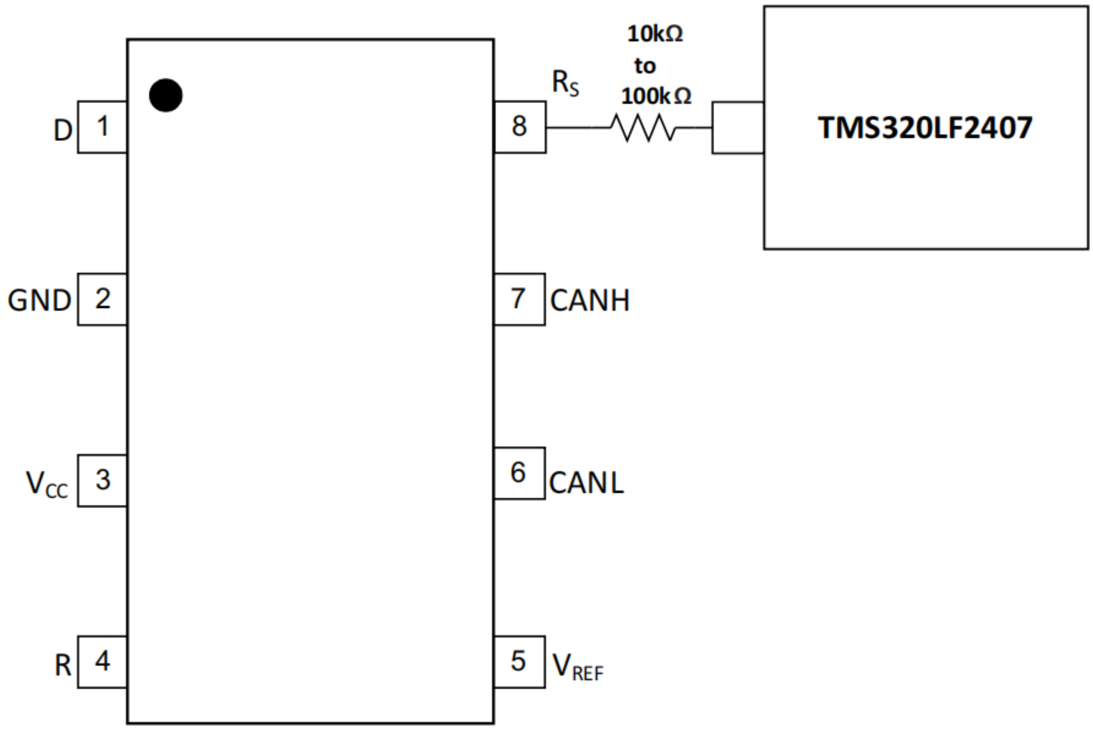


Figure 24. Slope Control

8.3.5 Thermal Shutdown

The SNx5HVD251 has a thermal shutdown feature that turns off the driver outputs when the junction temperature nears 165°C. This shutdown prevents catastrophic failure from bus shorts, but does not protect the circuit from possible damage. The user should strive to maintain recommended operating conditions and not exceed absolute-maximum ratings at all times. If an SNx5HVD251 is subjected to many, or long-duration faults that can put the device into thermal shutdown, it should be replaced.

8.4 Device Functional Modes

Table 2. Driver

INPUTS	Voltage at R_S, V_{Rs}	OUTPUTS		BUS STATE
D		CANH	CANL	
L	V_{Rs} < 1.2 V	H	L	Dominant
H	V_{Rs} < 1.2 V	Z	Z	Recessive
Open	X	Z	Z	Recessive
X	V_{Rs} > 0.75 V_{CC}	Z	Z	Recessive
X	Open	Z	Z	Recessive

Table 3. Receiver

DIFFERENTIAL INPUTS [V_{ID} = V(CANH) - V(CANL)]	OUTPUT R (1)
$V_{ID} \geq 0.9$ V	L
0.5 V < V_{ID} < 0.9 V	?
$V_{ID} \leq 0.5$ V	H
Open	H

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

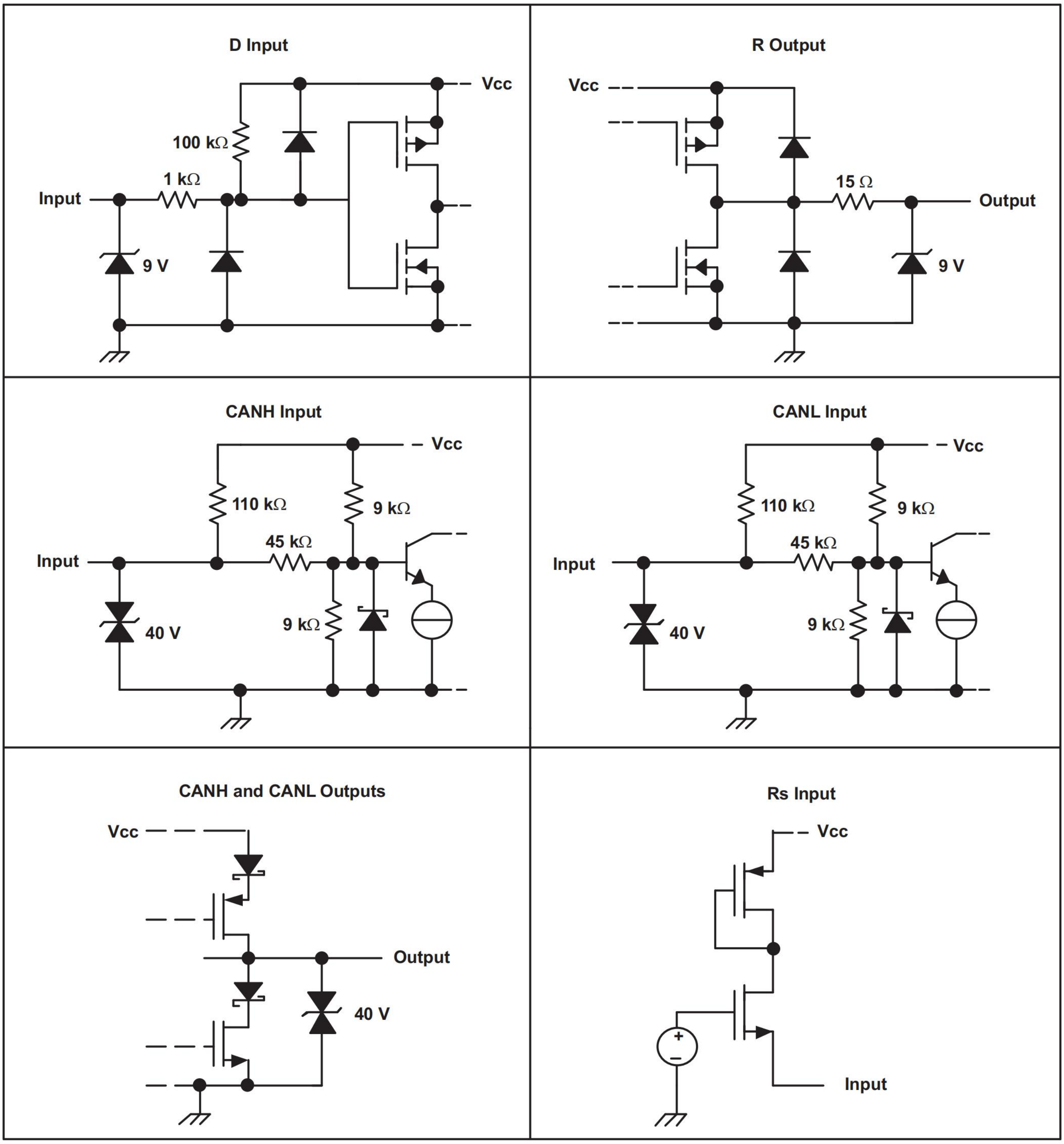
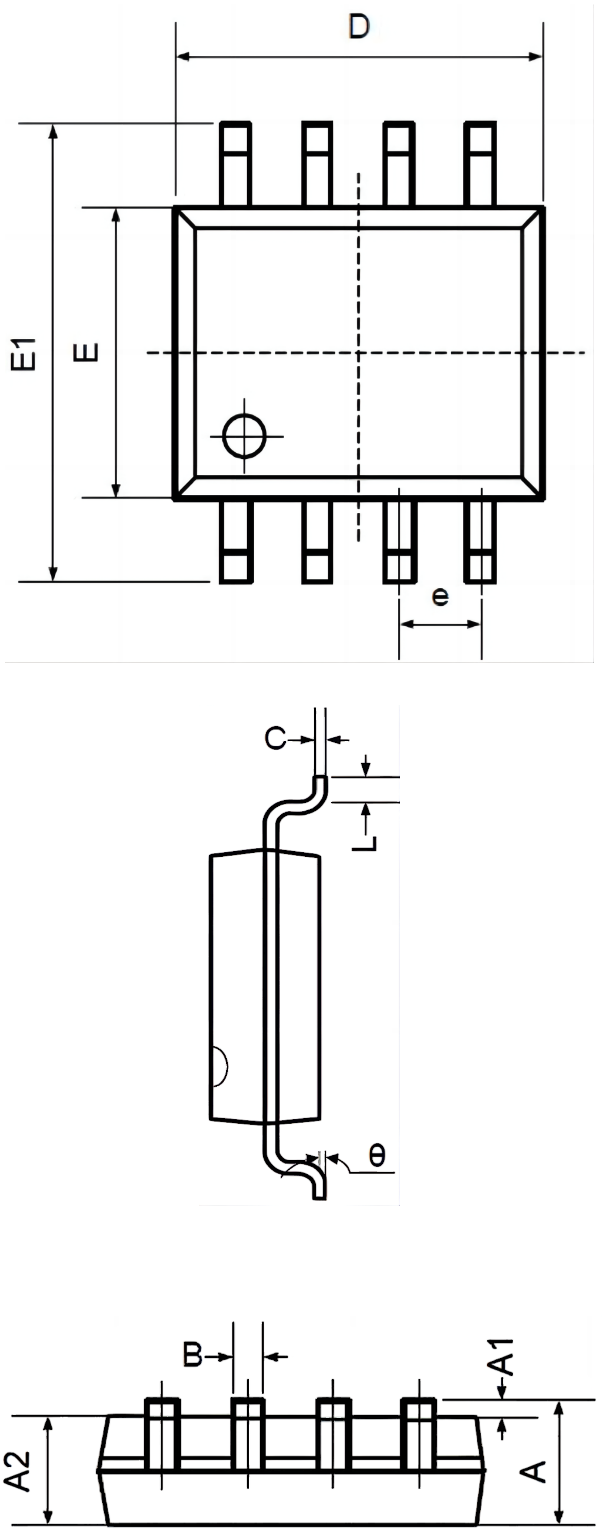


Figure 25. Equivalent Input and Output Schematic Diagrams

Order information

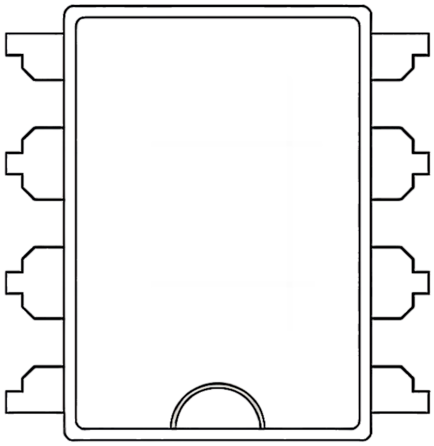
Order Number	Package	Package Quantity	Marking On The park
SN65HVD251DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD251DR
SN65HVD251P-TUDI	DIP8	Tube,50,A box of 2000	SN65HVD251P

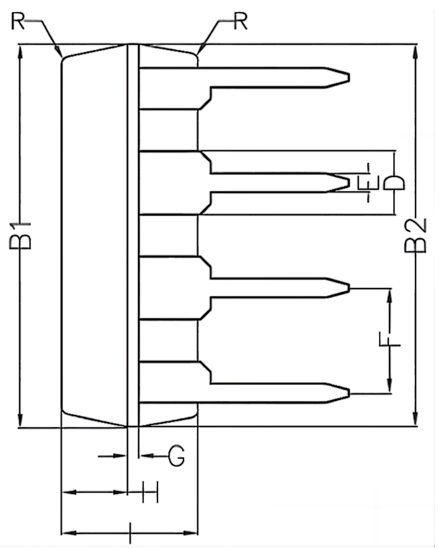
Package SOP8

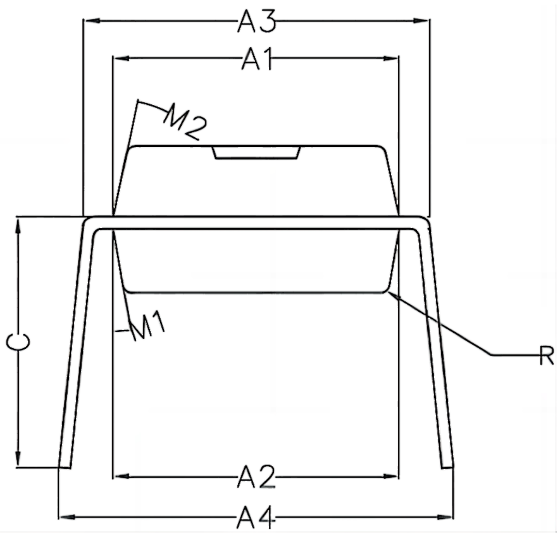


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package DIP8







Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

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