Single Schmitt-Trigger Inverter

Features

- Wide Supply Voltage Range: 1.65 V to 5.5 V
- CMOS Low Power Consumption
- Input Accept Voltage to 5.5 V
- I_{OFF} Supports Partial Power-Down-Mode Operation
- t_{pd} = 3.3 ns at 3.3 V
- High Output Drive: ±24 mA at V_{CC} = 3.0 V
- Operating Temperature Range:
  -40 °C to 125 °C
- SOT353 - 5L

Applications

Industrial Equipment
Desktops or Notebook PCs
Digital Video Cameras (DVC)
Telecom Equipment
Mobile Phones
Personal Navigation Device (GPS)
Portable Media Player
Wireless Equipment

General Description

AWS74LVC1G14 is a single inverter with Schmitt-trigger inputs. The device accepts any supply voltage from 1.65 V to 5.5 V. The function of AWS74LVC1G14 is $Y = \overline{A}$.

The device functions as an independent inverter with Schmitt-trigger inputs, so the device has different input threshold levels for positive going (V_{T+}) and negative going (V_{T-}) signals to provide hysteresis (ΔV_T) which makes the device tolerant to slow or noisy input signals.

The AWS74LVC1G14 is fully specified for partial power-down applications using off output current (I_{OFF}). The outputs for this device enter a high-impedance state when the device is powered down, preventing any damaging backflow current through the device.

Typical Application Circuit

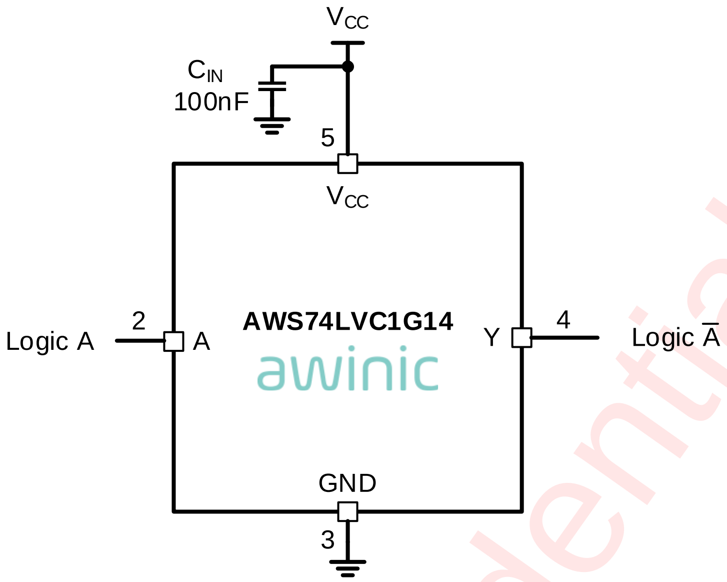
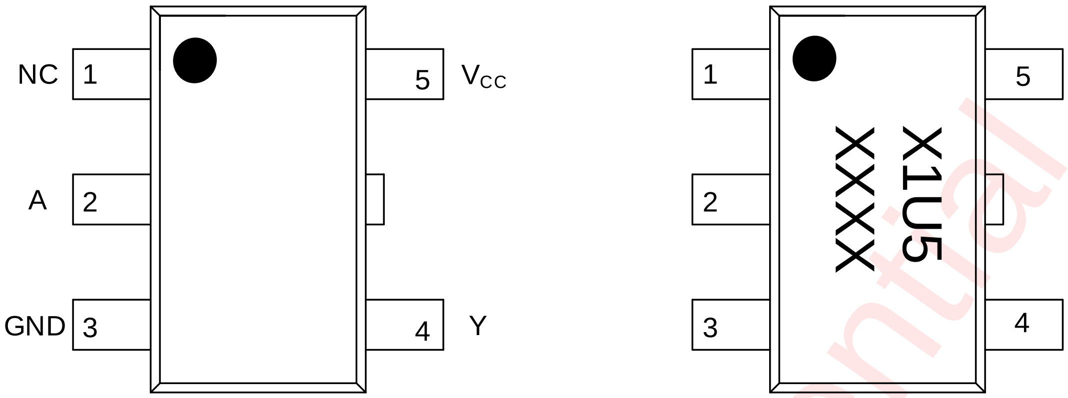


Figure 1 Typical Application

Pin Configuration And Top Mark

AWS74LVC1G14STR
（Top View）

AWS74LVC1G14STR Marking
（Top View）



X1U5 - AWS74LVC1G14STR
XXXX - Production Tracing Code

Figure2 Pin Configuration

Pin Definition

No.	NAME	DESCRIPTION
1	NC	Not connected
2	A	Data input A
3	GND	Ground
4	Y	Data output
5	V_{CC}	Supply voltage

Pin Functions

Input A	Output Y
L	H
H	L

$Y=\overline{A}$

H=High Voltage Level

L=Low Voltage Level

Functional Block Diagram

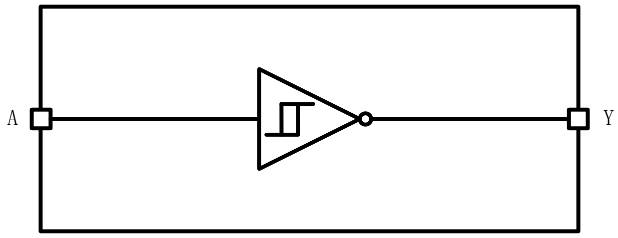


Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWS74LVC1G14STR	-40 °C ~ 125 °C	SOT353 - 5L	X1U5	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage range V_{CC}		-0.5 V to 6.5 V
Input voltage range (NOTE 1)		-0.5 V to 6.5V
Output voltage range (NOTE 1)		-0.5 V to 6.5 V
Input clamp current, I_{IK}	$V_I < 0$	±50 mA
Output clamp current, I_{OK}	$V_O < 0$	±50 mA
Output current, I_O	V_O = 0 V to V_{CC}	50 mA
Maximum operating junction temperature T_{JMAX}		150 °C
Storage temperature T_{STG}		-65 °C to 150 °C
Lead temperature (soldering 10 seconds)		260 °C
ESD		
HBM (All pins, per ESDA/JEDEC JS-001-2023) (NOTE 2)		±6 kV
CDM (All pins, per ESDA/JEDEC JS-002-2022)		±1.5 kV
Latch-Up		
Test condition: JESD78F		+IT：400 mA -IT：-400 mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply voltage		1.65	5.5	V
V_I	Input voltage(NOTE1)		0	5.5	V
V_O	Output voltage	Active mode	0	V_{CC}	V
		Power-Down Mode, V_{CC} = 0 V	0	5.5	V
T_A	Operating free-air temperature T_A		-40	125	°C

NOTE1: All unused data inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Electrical Characteristics

DC Electrical Characteristics

Typical values are measured at V_{CC} = 3.3 V, T_A = 25 °C. Full = -40 °C ~ 125 °C (unless otherwise noted)

PARAMETER		TEST CONDITION	TEMP	MIN	TYP	MAX	UNIT
V_{T+}	Positive going input threshold voltage	V_{CC} = 1.65 V	25 °C		1.04		V
			Full	0.8		1.2	
		V_{CC} = 2.3 V	25 °C		1.36		
			Full	1.1		1.6	
		V_{CC} = 3.0 V	25 °C		1.65		
			Full	1.5		1.9	
		V_{CC} = 4.5 V	25 °C		2.27		
			Full	2.1		2.8	
		V_{CC} = 5.5 V	25 °C		2.68		
			Full	2.5		3.4	
V_{T-}	Negative going input threshold voltage	V_{CC} = 1.65 V	25 °C		0.58		V
			Full	0.4		0.7	
		V_{CC} = 2.3 V	25 °C		0.84		
			Full	0.5		1	
		V_{CC} = 3.0 V	25 °C		1.16		
			Full	0.8		1.3	
		V_{CC} = 4.5 V	25 °C		1.76		
			Full	1.5		2	
		V_{CC} = 5.5 V	25 °C		2.12		
			Full	1.8		2.4	
ΔV_T	Hysteresis (V_{T+}-V_{T-})	V_{CC} = 1.65 V	25 °C		0.46		V
			Full	0.2		0.6	
		V_{CC} = 2.3 V	25 °C		0.52		
			Full	0.2		0.8	
		V_{CC} = 3.0 V	25 °C		0.49		
			Full	0.2		0.9	
		V_{CC} = 4.5 V	25 °C		0.51		
			Full	0.3		1.1	
		V_{CC} = 5.5 V	25 °C		0.56		
			Full	0.4		1.1	
V_{OH}	HIGH-level output voltage	I_O = -100 µA, V_{CC} = 1.65 V to 5.5 V	25 °C		V_{CC} - 0.001		V
			Full	V_{CC} - 0.1			
		I_O = -4 mA, V_{CC} = 1.65 V	25 °C		1.58		
			Full	1.2			
		I_O = -8 mA, V_{CC} = 2.3 V	25 °C		2.2		
			Full	1.9			

PARAMETER		TEST CONDITION	TEMP	MIN	TYP	MAX	UNIT
		I_O = -16mA, V_{CC} = 3.0 V	25 °C		2.85		
			Full	2.4			
		I_O = -24 mA, V_{CC} = 3.0 V	25 °C		2.77		
			Full	2.3			
		I_O = -32 mA, V_{CC} = 4.5 V	25 °C		4.27		
			Full	3.8			
V_{OL}	LOW-level output voltage	I_O = 100 μA, V_{CC} = 1.65 V to 5.5 V	25 °C		0.002		V
			Full			0.1	
		I_O = 4 mA, V_{CC} = 1.65 V	25 °C		0.08		
			Full			0.45	
		I_O = 8 mA, V_{CC} = 2.3 V	25 °C		0.11		
			Full			0.3	
		I_O = 16 mA, V_{CC} = 3.0 V	25 °C		0.20		
			Full			0.4	
		I_O = 24 mA, V_{CC} = 3.0 V	25 °C		0.30		
			Full			0.55	
		I_O = 32 mA, V_{CC} = 4.5 V	25°C		0.35		
			Full			0.55	
I_I	Input leakage current	A input, V_I = 5.5 V or GND, V_{CC} = 0 V to 5.5 V	25 °C			±1	μA
			Full			±5	
I_{OFF}	Power-off leakage current	V_I or V_O = 5.5 V, V_{CC} = 0 V	25 °C		±0.03	±1	μA
			Full			±8	
I_{CC}	Supply current	V_I = 5.5 V or GND, V_{CC} = 1.65 V to 5.5 V, I_O = 0 A	25 °C		0.03	1	μA
			Full			8	
ΔI_{CC}	Additional supply current	One input at V_{CC} - 0.6 V, Other inputs at V_{CC} or GND, V_{CC} = 3 V to 5.5 V	25 °C		15		μA
			Full			500	
C_I	Input Capacitance	V_{CC} = 3.3 V, V_I = V_{CC} or GND	25 °C		4.8		pF

Switching Characteristics

T_A = 25 °C for typical values, Full = -40 °C ~ 125 °C (unless otherwise noted)

PARAMETERS		TEST CONDITION	TEMP	MIN[1]	TYP[2]	MAX[1]	UNIT
t_{pd}[3]	Propagation delay	V_{CC} = 1.8 V ± 0.15 V, C_L = 30 pF, R_L = 1 kΩ	25 °C		4.7		ns
			Full	1.0		14	
		V_{CC} =2.5 V ± 0.2 V, C_L = 30 pF, R_L = 500 Ω	25 °C		3.6		
			Full	0.5		9.0	
		V_{CC} = 2.7 V, C_L = 50 pF, R_L = 500 Ω	25 °C		3.6		
			Full	0.5		9.0	
		V_{CC} = 3.3 V ± 0.3 V, C_L = 50 pF, R_L = 500 Ω	25 °C		3.3		
			Full	0.5		7.0	
		V_{CC} = 5 V ± 0.5 V, C_L = 50 pF, R_L = 500 Ω	25 °C		2.9		
			Full	0.5		6.0	
C_{pd}[4]	Power dissipation capacitance	V_{CC} = 1.8 V, f = 10 MHz	25 °C		15		pF
		V_{CC} = 2.5 V, f = 10 MHz	25 °C		17		
		V_{CC} = 3.3 V, f = 10 MHz	25 °C		19		
		V_{CC} = 5.0 V, f = 10 MHz	25 °C		26		

NOTES:

1. Specified by design and characterization.
2. Typical value set by testing.
3. t_{pd} is the same as t_{PLH} and t_{PHL}.
4. C_{pd} is used to determine the dynamic power dissipation (Pd in μW).

$Pd = C_{pd} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$

where:

f_i = Input frequency in MHz.

f_o = Output frequency in MHz.

C_L = Output load capacitance in pF.

V_{CC} = Supply voltage in Volts.

N = Number of inputs switching.

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of outputs.

Typical Characteristics

TEST INFORMATION

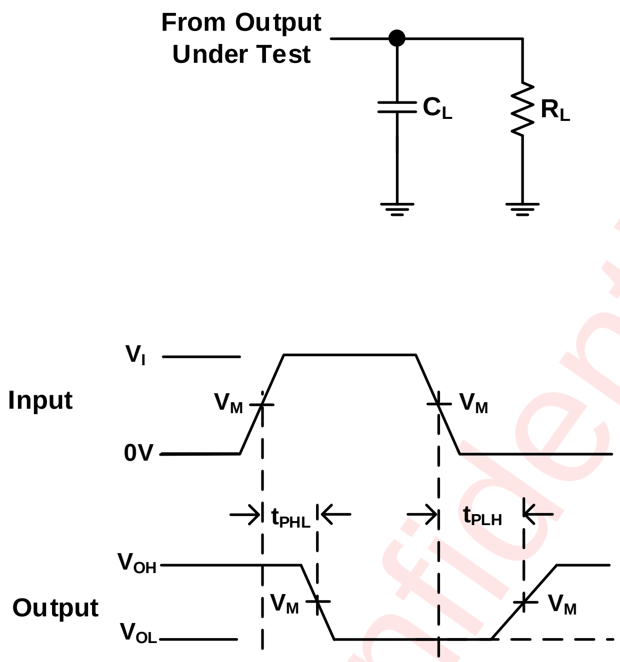


Figure 4 Load Circuit and Propagation Delay Measurement

1. The following table gives the test condition under different supply voltage：

V_{CC}	INPUTS		V_M	C_L	R_L
	V_I	t_r/t_f			
1.8 V ± 0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	30 pF	1 kΩ
2.5 V ± 0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	30 pF	500 Ω
2.7 V	2.7 V	≤ 2.5 ns	1.5 V	50 pF	500 Ω
3.3 V ± 0.3 V	3 V	≤ 2.5 ns	1.5 V	50 pF	500 Ω
5 V ± 0.5 V	V_{CC}	≤ 2.5 ns	$V_{CC}/2$	50 pF	500 Ω

2. Load capacitance including probe and jig capacitance.

3. t_{PHL} and t_{PLH} are measured at V_M.

4. t_{PHL} and t_{PLH} are same as t_{pd}.

Detailed Functional Description

AWS74LVC1G14 is a Schmitt-trigger inverter. The device accepts any supply voltage from 1.65V to 5.5V. The function of AWS74LVC1G14 is $Y = \overline{A}$. The device functions as an independent inverter, but because of Schmitt action, it will have different input threshold levels for a positive-going (V_{T+}) and negative-going signals.

The AWS74LVC1G14 is fully specified for partial power-down applications using off output current (I_{OFF}).The outputs for this device enter a high-impedance state when the device is powered down, preventing any damaging backflow current through the device.

Functional Modes

Input A	Output Y
L	H
H	L

$Y=\overline{A}$

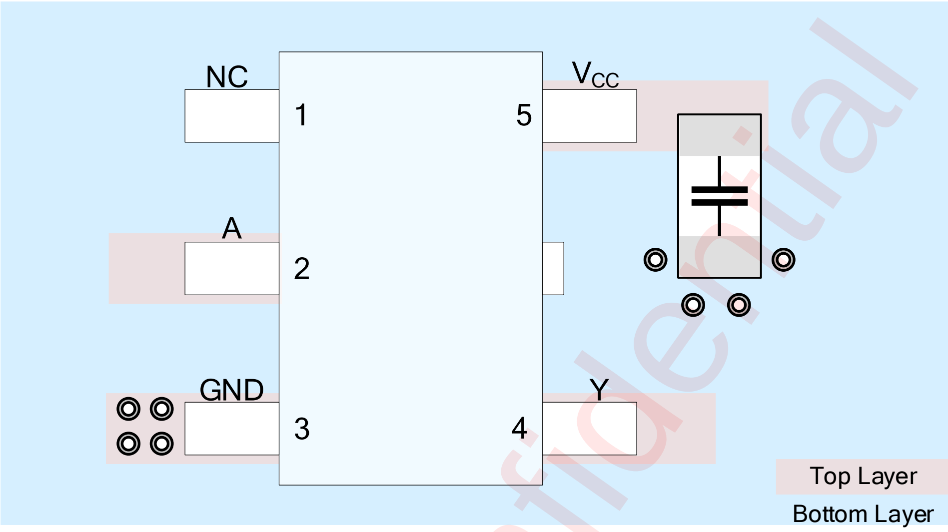
H=High Voltage Level

L=Low Voltage Level

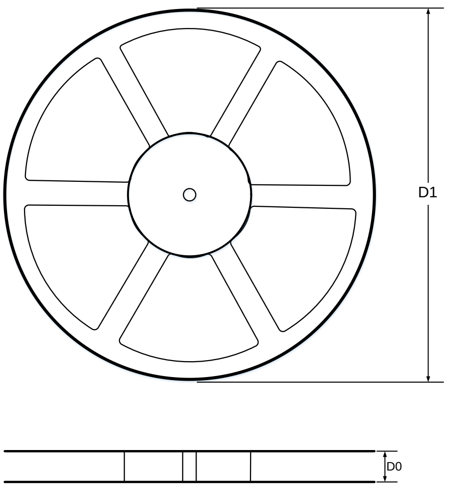
PCB Layout Consideration

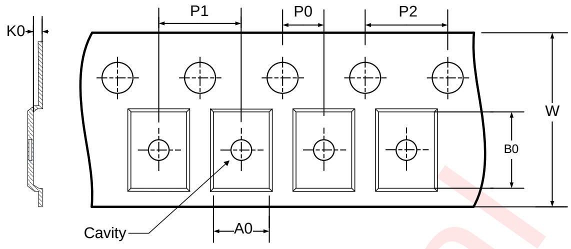
To obtain the optimal performance of AWS74LVC1G14, PCB layout should be considered carefully. Here are some guidelines:

1. We recommend adding a 0.1μF bypass capacitor to prevent power disturbance. The C_{IN} should be placed as close to the V_{CC} pin as possible.



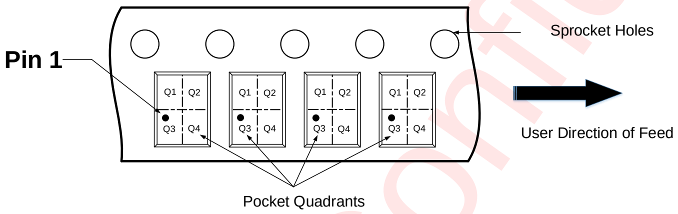
Tape And Reel Information





A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



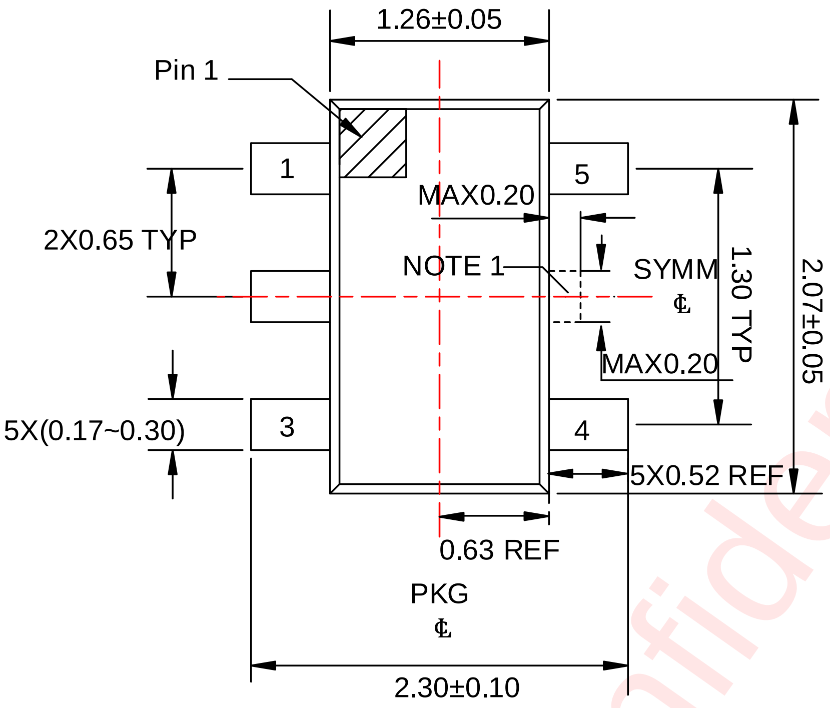
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

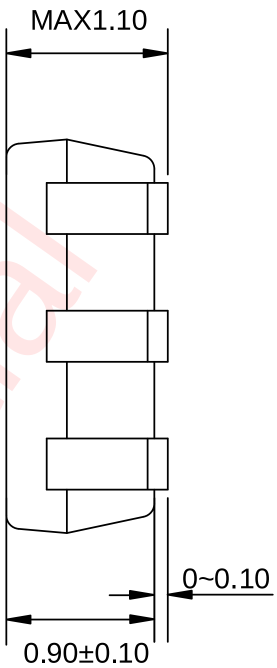
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178.0	8.40	2.40	2.55	1.20	2.00	4.00	4.00	8.00	Q3

All dimensions are nominal

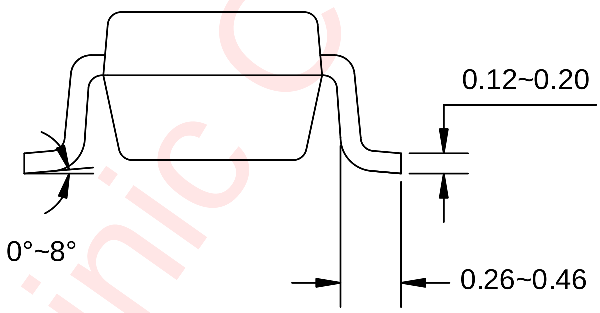
Package Description



Top View



Side View



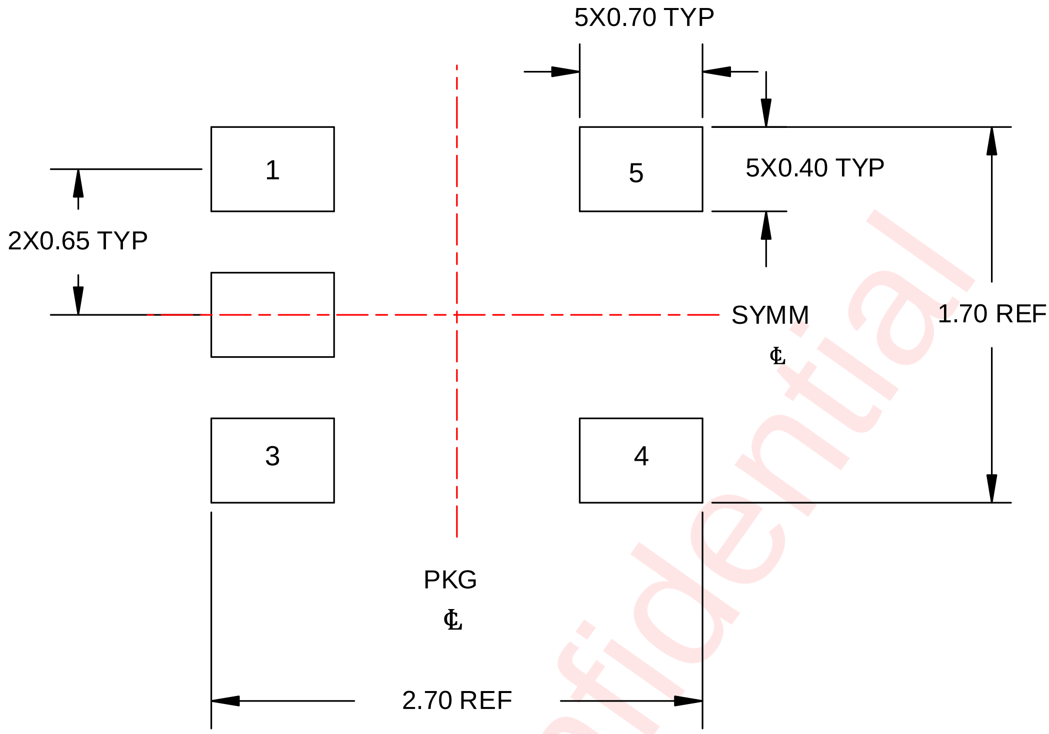
Side View

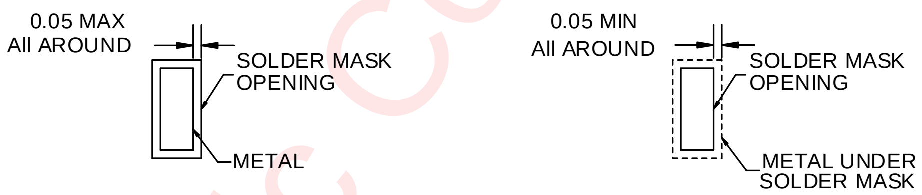
Unit: mm

NOTE:

1.Support pin may differ or may not be present.

Land Pattern Data





NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Mar. 2025	Officially released

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