

# F6922

Dual-Channel Low Noise Amplifier 17.7 – 21.2 GHz

The [F6922](#) is an ultra-low power consumption, dual-channel, low noise amplifier (LNA) RFIC designed for application in Ka-Band SATCOM planar phased array antennas. The exceptional combination of low power consumption, low noise, high gain, and compact size, maximizes the antenna array G/T while minimizing overall system power dissipation. An external bias current provides gain control, standby mode and temperature compensation.

The F6922 includes two independent gain/phase matched LNA channels in a compact 23-pin, 0.5mm pitch BGA package. All inputs and outputs are single-ended and 50Ω matched for ease of integration on to phased array antenna panels.

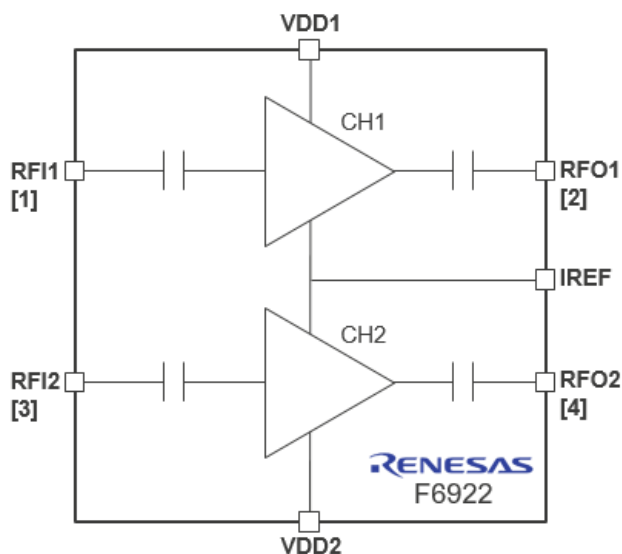


Figure 1. Block Diagram

## Features

- Frequency: 17.7 – 21.2 GHz
- Gain: 19.5dB typ. at 19.5GHz
- Noise figure: 1.8dB
- Output P1dB: -2.3dBm
- Power consumption: 15mW/ch
- Channel isolation: 30dB
- Supply voltage: 0.9 – 1.0V
- Common bias control input
- Compact size for planar integration on  $\lambda/2$  grid
- $2.7 \times 2.7 \times 0.9$  mm, 23-pin BGA
- -40°C to +85°C ambient operating temperature range

*Note:* Performance is typical in the operating band. For more details, see the Specifications and Typical Performance Characteristics sections.

## Applications

- Electronically Steered Phased Array Antennas (ESAs)
- Aerospace, Maritime, and Satcom-on-the-move (SOTM)
- Ka-Band SATCOM Terminals
- Communication, Electronic Warfare (EW), and Radar Systems

## Contents

|                                                     |           |
|-----------------------------------------------------|-----------|
| <b>1. Pin Information .....</b>                     | <b>4</b>  |
| 1.1 Pin Assignments .....                           | 4         |
| 1.2 Pin Descriptions.....                           | 4         |
| <b>2. Specifications.....</b>                       | <b>5</b>  |
| 2.1 Absolute Maximum Ratings.....                   | 5         |
| 2.2 Thermal Information.....                        | 5         |
| 2.3 Recommended Operating Conditions .....          | 5         |
| 2.4 Electrical Specifications .....                 | 6         |
| 2.4.1. DC Electrical Specifications .....           | 6         |
| 2.4.2. RF Electrical Specifications.....            | 6         |
| <b>3. Typical Application Circuit .....</b>         | <b>7</b>  |
| <b>4. Typical Performance Characteristics .....</b> | <b>8</b>  |
| <b>5. Evaluation Board .....</b>                    | <b>10</b> |
| 5.1 Evaluation Board Photos .....                   | 10        |
| 5.2 Evaluation Board Schematic .....                | 11        |
| 5.3 Evaluation Board Operation .....                | 12        |
| 5.3.1. Single Power Supply Operation .....          | 12        |
| 5.3.2. Independent VDD and IREF Bias Control.....   | 12        |
| <b>6. Package Outline Drawings.....</b>             | <b>13</b> |
| <b>7. Marking Diagram.....</b>                      | <b>13</b> |
| <b>8. Ordering Information.....</b>                 | <b>13</b> |
| <b>9. Revision History .....</b>                    | <b>13</b> |

## Figures

|                                                |    |
|------------------------------------------------|----|
| Figure 1. Block Diagram .....                  | 1  |
| Figure 2. Pin Assignments – Top View.....      | 4  |
| Figure 3. Typical Application Circuits .....   | 7  |
| Figure 4. Gain .....                           | 8  |
| Figure 5. Noise Figure .....                   | 8  |
| Figure 6. Input Match.....                     | 8  |
| Figure 7. Output Match.....                    | 8  |
| Figure 8. Input-to-Output Isolation .....      | 8  |
| Figure 9. Ch-to-Ch Isolation.....              | 8  |
| Figure 10. Output 1dB Compression .....        | 9  |
| Figure 11. Output Third Order Intercept .....  | 9  |
| Figure 12. Supply Current, Per Channel .....   | 9  |
| Figure 13. IREF Pin Voltage vs Current .....   | 9  |
| Figure 14. Out of Band Gain.....               | 9  |
| Figure 15. Out of Band Input Compression ..... | 9  |
| Figure 16. Evaluation Board - Top View.....    | 10 |
| Figure 17. Evaluation Board - Bottom View..... | 10 |

|                                             |    |
|---------------------------------------------|----|
| Figure 18. Evaluation Board Schematic ..... | 11 |
|---------------------------------------------|----|

## Tables

|                                      |    |
|--------------------------------------|----|
| Table 1. Bill of Material (BOM)..... | 11 |
|--------------------------------------|----|

## 1. Pin Information

### 1.1 Pin Assignments

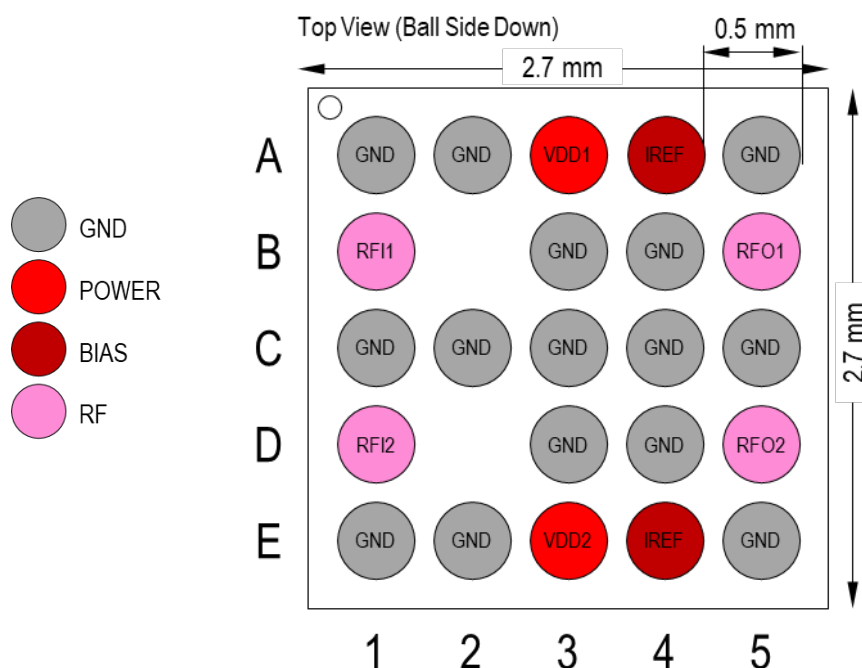


Figure 2. Pin Assignments – Top View

### 1.2 Pin Descriptions

| Pin Number                                                             | Name | Type   | I/O    | Description                                                                                                                                                                              |
|------------------------------------------------------------------------|------|--------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A1, A2, A5,<br>B3, B4,<br>C1, C2, C3, C4, C5,<br>D3, D4,<br>E1, E2, E5 | GND  | Ground | –      | DC and RF ground.                                                                                                                                                                        |
| A3                                                                     | VDD1 | Power  | Input  | Positive supply voltage input for channel 1.                                                                                                                                             |
| E3                                                                     | VDD2 | Power  | Input  | Positive supply voltage input for channel 2.                                                                                                                                             |
| A4, E4                                                                 | IREF | Power  | Input  | Reference bias current input, tied to a common node shared by channels 1 and 2. Connect directly to a current source, voltage source through a resistor, or to the IBx pin of the F61xx. |
| B1                                                                     | RFI1 | Analog | Input  | Channel 1 RF input port.                                                                                                                                                                 |
| D1                                                                     | RFI2 | Analog | Input  | Channel 2 RF input port.                                                                                                                                                                 |
| B5                                                                     | RFO1 | Analog | Output | Channel 1 RF output port.                                                                                                                                                                |
| D5                                                                     | RFO2 | Analog | Output | Channel 2 RF output port.                                                                                                                                                                |

## 2. Specifications

Exposure of the device to parameter values outside of the range listed below may reduce the operating lifetime and adversely and permanently alter the device characteristics. Furthermore, functional operation at or near absolute maximum ratings is not implied.

### 2.1 Absolute Maximum Ratings

| Parameter                  | Symbol        | Conditions                  | Minimum | Maximum | Unit        |
|----------------------------|---------------|-----------------------------|---------|---------|-------------|
| Supply Voltage             | $V_{DD}$      |                             | -0.3    | 1.2     | V           |
| Reference Current          | $I_{REF}$     |                             | 0       | 200     | $\mu A$     |
| Input RF Pin DC Voltage    | $V_{DC\_RFI}$ |                             | -0.3    | 1.0     | V           |
| Output RF Pin DC Voltage   | $V_{DC\_RFO}$ |                             | -0.3    | 1.2     | V           |
| RF Input Power             | $P_{IN}$      | $V_{DD} = 1.0V, VSWR < 2:1$ |         | 0       | dBm         |
| Junction Temperature       | $T_J$         |                             |         | 125     | $^{\circ}C$ |
| ESD – Human Body Model     | $V_{HBM}$     | JS-001-2012                 |         | 1000    | V           |
| ESD – Charged Device Model | $V_{CDM}$     | JESD22-C101                 |         | 250     | V           |

### 2.2 Thermal Information

| Parameter                             | Symbol        | Value       | Unit          |
|---------------------------------------|---------------|-------------|---------------|
| Theta JB. Junction to Board           | $\theta_{JB}$ | 14          | $^{\circ}C/W$ |
| Theta JC. Junction to Case (case top) | $\theta_{JC}$ | 108         | $^{\circ}C/W$ |
| Theta JA. Junction to Ambient         | $\theta_{JA}$ | 47          | $^{\circ}C/W$ |
| Storage Temperature                   | $T_{STOR}$    | -40 to +150 | $^{\circ}C$   |
| Lead Temperature (soldering, 30s)     | $T_{LEAD}$    | 260         | $^{\circ}C$   |

### 2.3 Recommended Operating Conditions

| Parameter                                 | Symbol    | Minimum | Typical | Maximum | Unit        |
|-------------------------------------------|-----------|---------|---------|---------|-------------|
| RF Frequency Range                        | $f_{RF}$  | 17.7    |         | 21.2    | GHz         |
| Power Supply Voltage                      | $V_{DD}$  | 0.9     | 0.95    | 1.0     | V           |
| Reference Bias Current at -40 $^{\circ}C$ | $I_{REF}$ | 43      | 50      | 58      | $\mu A$     |
| Reference Bias Current at +25 $^{\circ}C$ |           | 77      | 90      | 104     | $\mu A$     |
| Reference Bias Current at +85 $^{\circ}C$ |           | 108     | 127     | 146     | $\mu A$     |
| Ambient Temperature                       | $T_A$     | -40     |         | 85      | $^{\circ}C$ |
| RF Pin Load Impedance                     | $Z_{RF}$  |         | 50      |         | $\Omega$    |

## 2.4 Electrical Specifications

Specifications apply when operated at  $T_{AMB} = 25^{\circ}\text{C}$ .

### 2.4.1. DC Electrical Specifications

| Parameter                                 | Symbol         | Conditions                                           | Minimum | Typical | Maximum | Unit          |
|-------------------------------------------|----------------|------------------------------------------------------|---------|---------|---------|---------------|
| Supply Current, Per Channel               | $I_{DD}$       | $V_{DD} = 0.95\text{V}$ , $I_{REF} = 100\mu\text{A}$ |         | 15.5    |         | mA            |
| Supply Current, Idle-state <sup>[1]</sup> | $I_{DD\_IDLE}$ | $I_{REF} = 0\mu\text{A}$                             |         | 1       |         | $\mu\text{A}$ |

1.  $I_{REF}$  pin can be grounded or floating to achieve idle-state.

### 2.4.2. RF Electrical Specifications

Unless stated otherwise, all specifications are for  $V_{DD} = 0.95\text{V}$ ,  $I_{REF} = 100\mu\text{A}$ ,  $T_{AMB} = 25^{\circ}\text{C}$ ,  $Z_S = Z_L = 50\Omega$ ,  $f_{RF} = 17.7 - 21.2\text{GHz}$ .

| Parameter                                    | Symbol          | Condition                                    | Minimum | Typical | Maximum | Unit |
|----------------------------------------------|-----------------|----------------------------------------------|---------|---------|---------|------|
| Gain                                         | G               | $f_{RF} = 19.5\text{ GHz}$                   |         | 19.5    |         | dB   |
| Gain Flatness vs. Frequency                  | $G_{VAR\_FREQ}$ | $f_{RF} = 17.7 - 21.2\text{GHz}$             |         | 1.4     |         | dB   |
|                                              |                 | Within any 250MHz                            |         | 0.1     |         | dB   |
| Noise Figure                                 | NF              |                                              |         | 1.8     |         | dB   |
| Output 1dB Compression Point                 | OP1dB           |                                              |         | -2.3    |         | dBm  |
| Output 3 <sup>rd</sup> Order Intercept Point | OIP3            | Pin = -35 dBm/tone, $\Delta f = 1\text{MHz}$ |         | 10      |         | dBm  |
| Input Return Loss                            | IRL             |                                              |         | 28      |         | dB   |
| Output Return Loss                           | ORL             |                                              |         | 24      |         | dB   |
| Reverse Isolation                            | ISO             |                                              |         | 34      |         | dB   |
| Channel-to-channel Isolation                 | $ISO_{CH-CH}$   | S21-S41                                      | 30      |         |         | dB   |

### 3. Typical Application Circuit

Figure 3 shows two typical application circuits for biasing the F6922.

The top circuit uses a voltage source  $V_{ref}$  to supply the bias reference current  $I_{ref}$  through an external resistor  $R_{ref}$ .  $V_{ref}$  should be set to achieve the recommended  $I_{ref}$  bias currents per the indicated formula. For the typical relationship between  $V_{ref}$  and  $I_{ref}$ , see Figure 13.

The bottom circuit uses the programmable IDAC of the Renesas F61xx beamforming device to provide the reference current directly to the F6922.

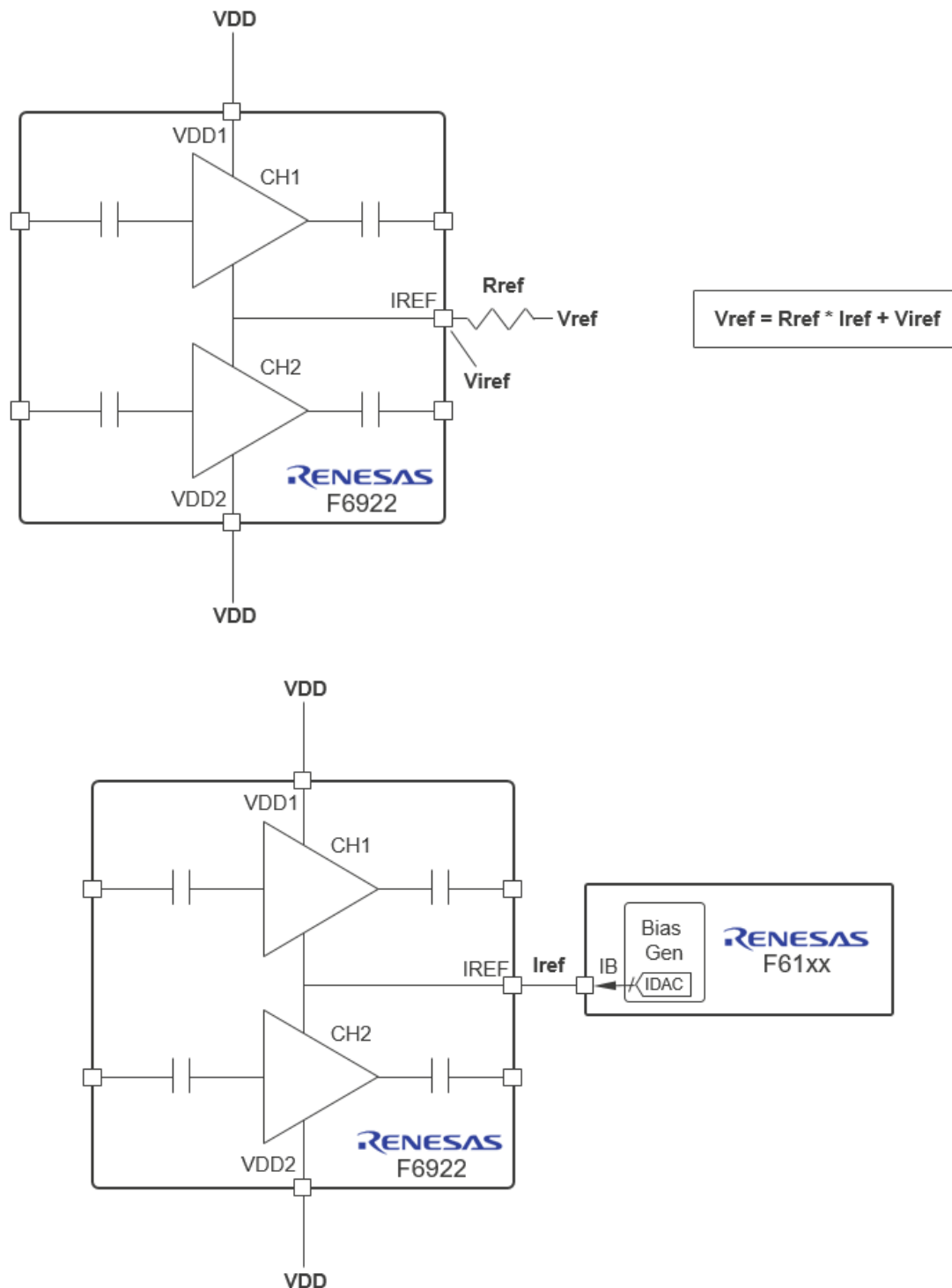


Figure 3. Typical Application Circuits

## 4. Typical Performance Characteristics

Unless stated otherwise,  $Z_S = Z_L = 50\Omega$  on all RF ports,  $V_{DD} = 0.95V$ ,  $T_{AMB} = 25^\circ C$ , Typical Recommended  $I_{REF}$

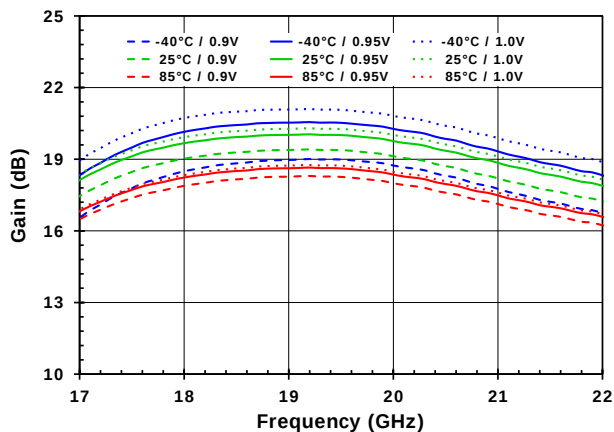


Figure 4. Gain

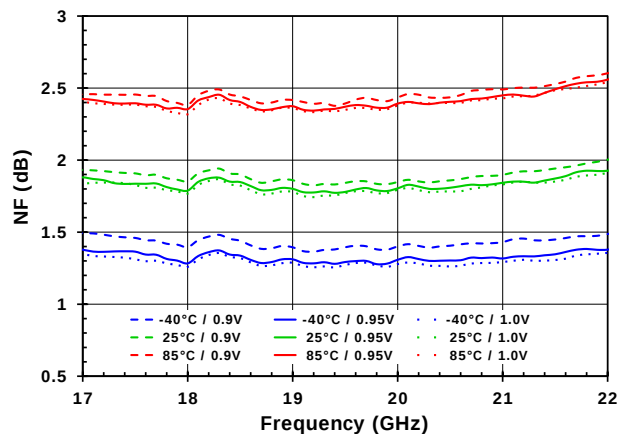


Figure 5. Noise Figure

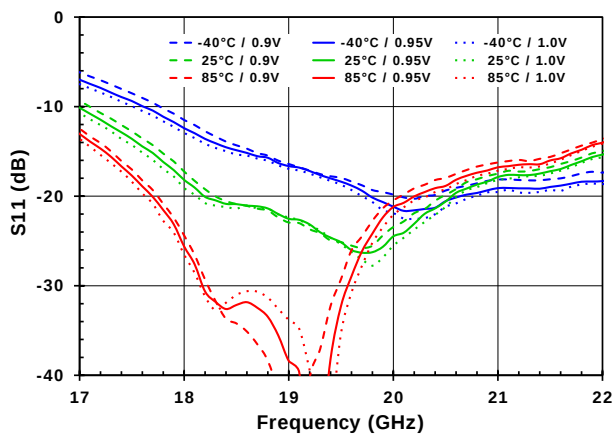


Figure 6. Input Match

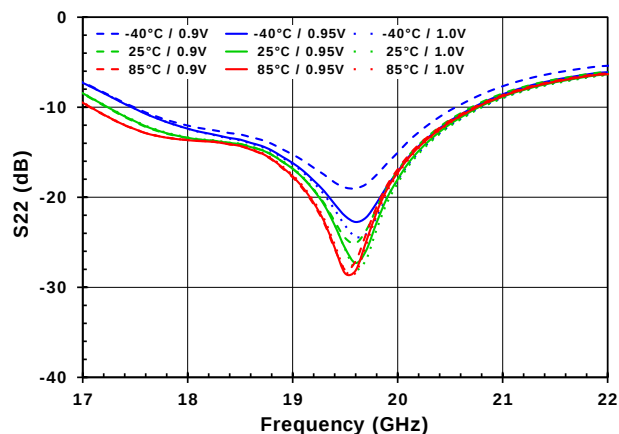


Figure 7. Output Match

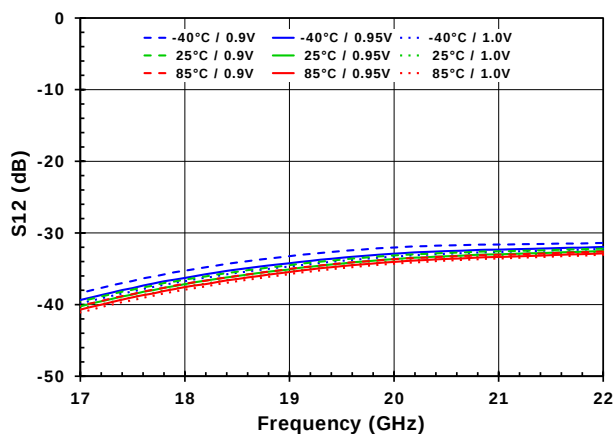


Figure 8. Input-to-Output Isolation

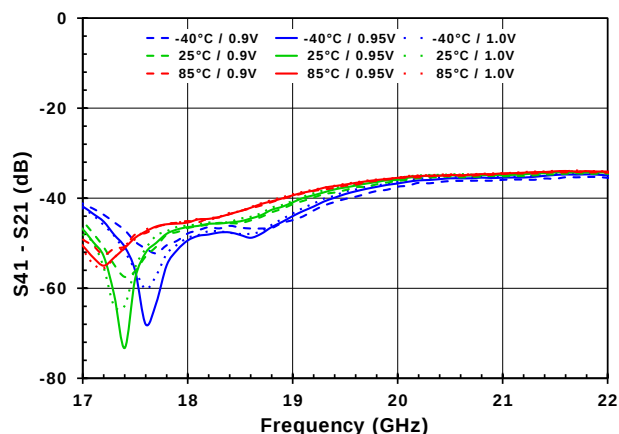


Figure 9. Ch-to-Ch Isolation

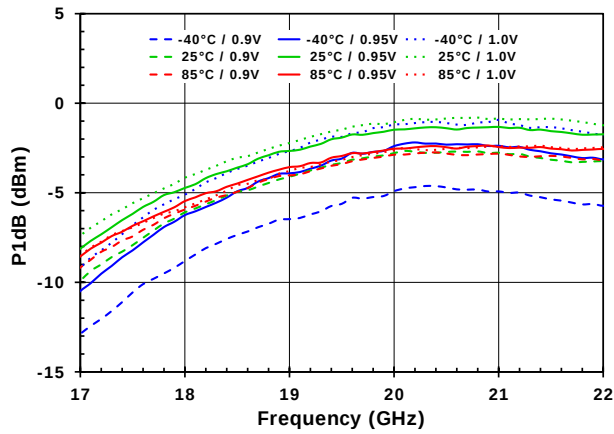


Figure 10. Output 1dB Compression

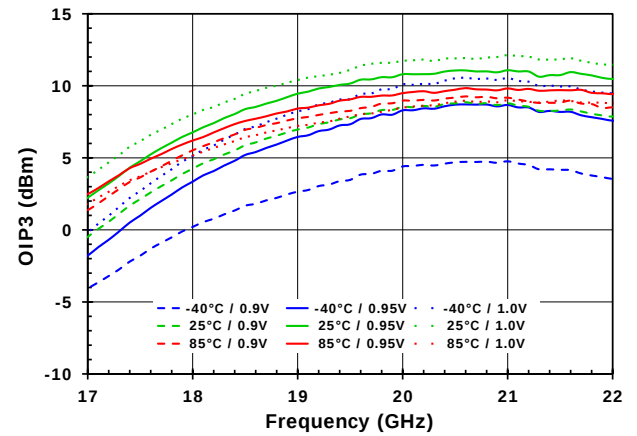


Figure 11. Output Third Order Intercept

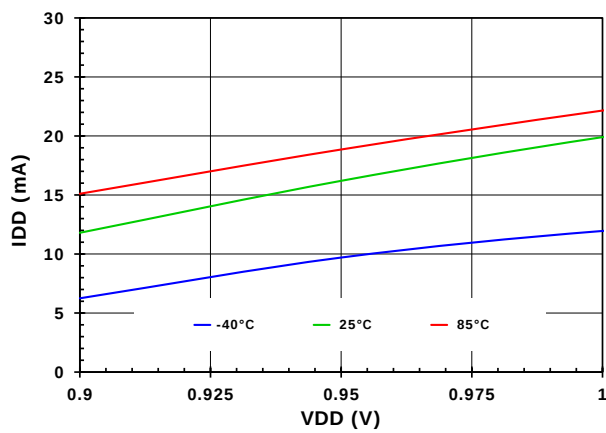


Figure 12. Supply Current, Per Channel

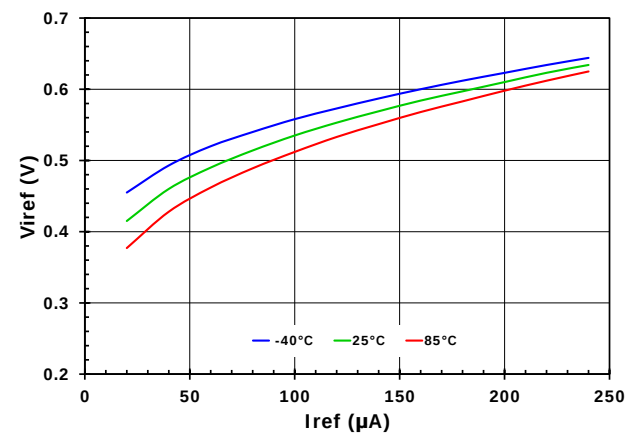


Figure 13. IREF Pin Voltage vs Current

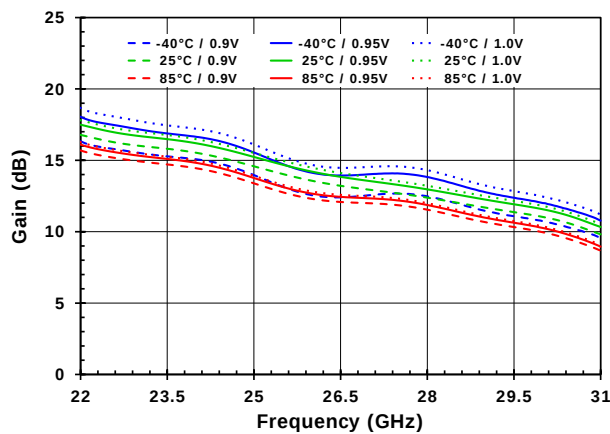


Figure 14. Out of Band Gain

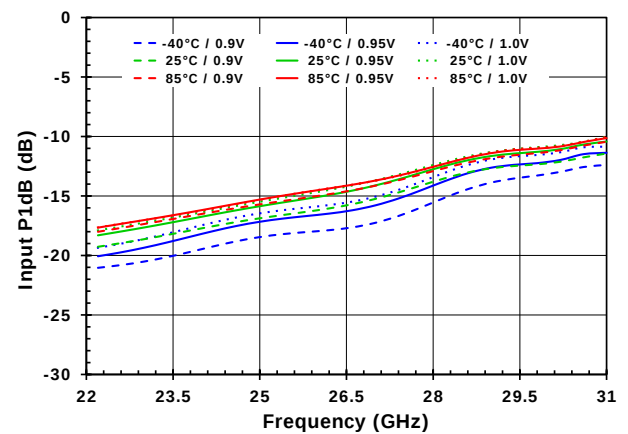


Figure 15. Out of Band Input Compression

## 5. Evaluation Board

For more information about the evaluation board, see the *F69xx Evaluation Board Manual* on the [F6922](#) product page.

### 5.1 Evaluation Board Photos

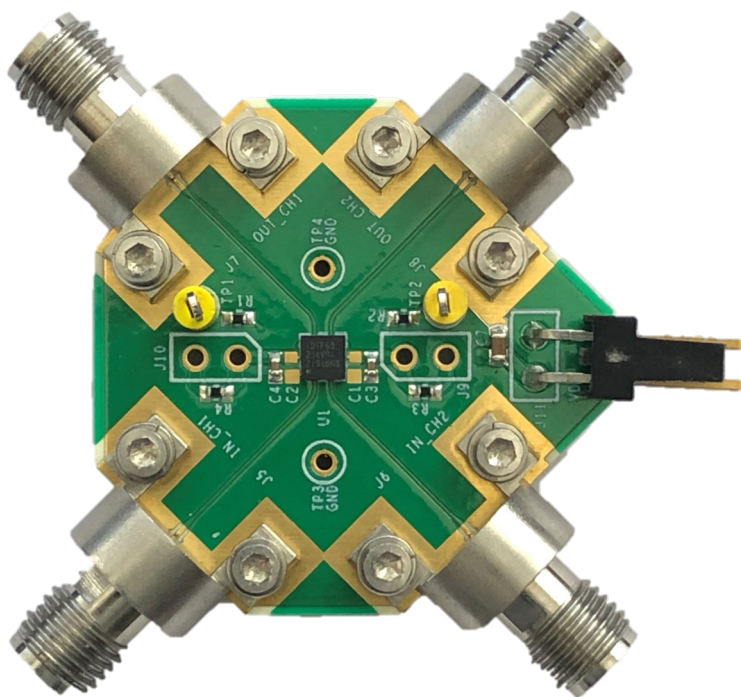


Figure 16. Evaluation Board - Top View

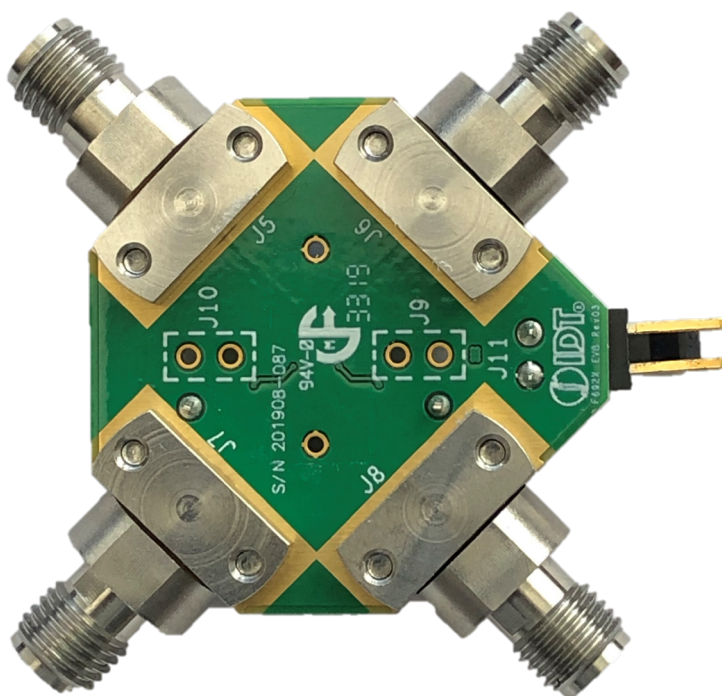


Figure 17. Evaluation Board - Bottom View

## 5.2 Evaluation Board Schematic

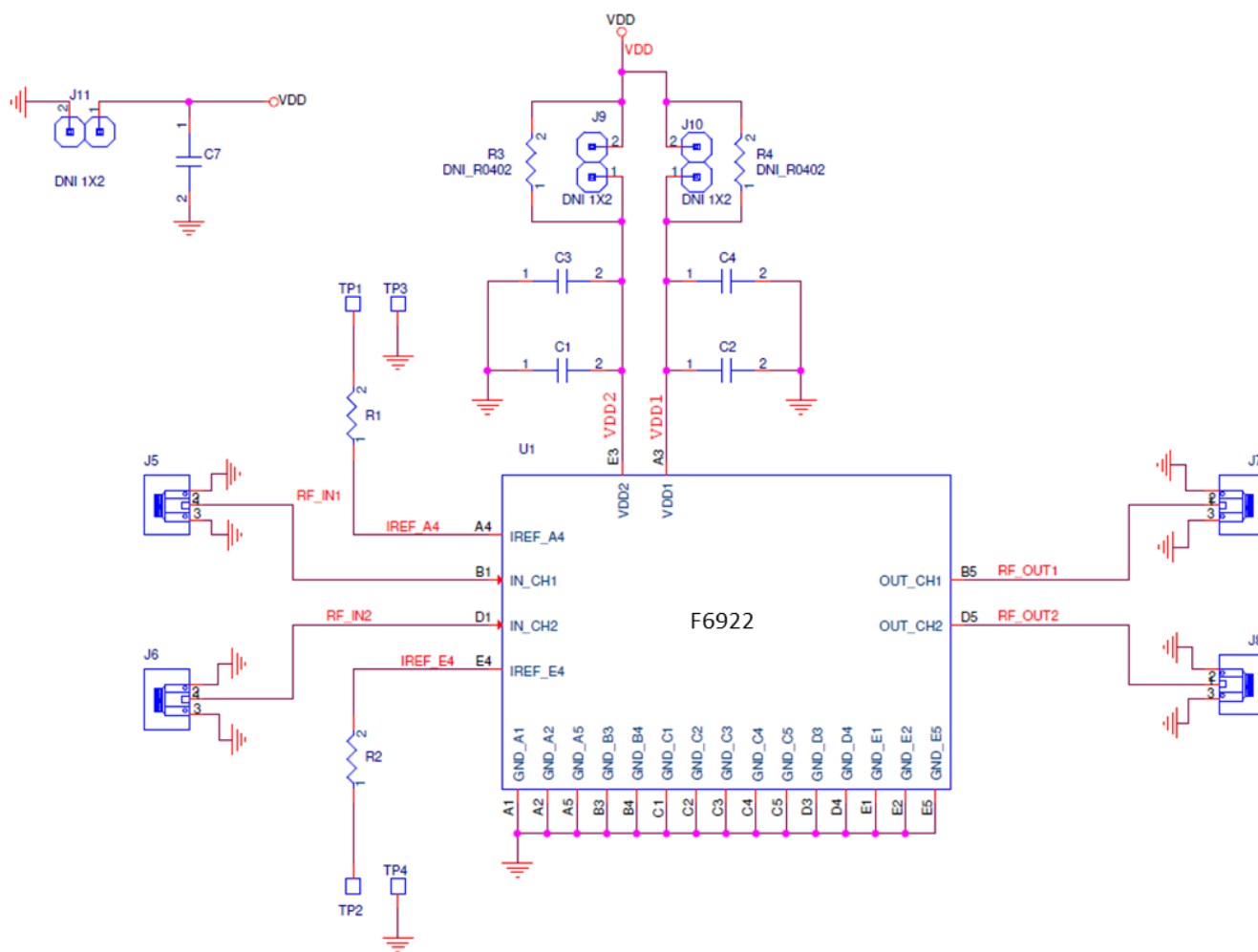


Figure 18. Evaluation Board Schematic

Table 1. Bill of Material (BOM)

| Part Ref. | Qty | Description                                         | Manufacturer Part # | Manufacturer         |
|-----------|-----|-----------------------------------------------------|---------------------|----------------------|
| C1, C2    | 2   | 33pF $\pm 5\%$ , 50V, C0G Ceramic Capacitor (0402)  | GRM1555C1H330J      | MURATA               |
| C3, C4    | 2   | 1uF $\pm 10\%$ , 16V, X6S Ceramic Capacitor (0402)  | GRM155C81C105K      | MURATA               |
| C7        | 1   | 10uF $\pm 20\%$ , 16V, X6S Ceramic Capacitor (0603) | GRM188C81C106M      | MURATA               |
| R1        | 1   | 4.42k $\Omega$ $\pm 1\%$ , 1/16W, Resistor (0402)   |                     |                      |
| R2        | 1   | DNI                                                 |                     |                      |
| R3, R4    | 2   | 0 $\Omega$ Resistors (0402)                         | ERJ-2GE0R00X        | PANASONIC            |
| J5-J8     | 4   | Edge Launch 2.92mm 40GHz                            | ELF-40-002          | SIGNAL MICROWAVE     |
| TP1, TP2  | 2   | Test Point Yellow                                   | 5004                | Keystone Electronics |
| J11       | 1   | CONN HEADER R/A 2POS 2.54MM                         | 1718571002          | MOLEX                |

## 5.3 Evaluation Board Operation

This section provides general information about operating the F6922 evaluation board. For more information about the board, see the *F69xx Evaluation Board Manual* on the [F6922](#) product page.

### 5.3.1. Single Power Supply Operation

Connect the positive and negative outputs of a power supply ( $V_{DD}$ ) to J11. In addition, connect the positive output of the  $V_{DD}$  supply to TP1. While there are two  $I_{REF}$  pins on the F6922 device (which are individually accessible via TP1 and TP2 on the evaluation board), these pins (A4 and E4) are internally connected to the same node on the device, simultaneously controlling the bias of channels 1 and 2. Set the power supply to 0.95V and enable the power supply output. Monitor the  $V_{DD}$  supply output current to confirm the nominal bias point is set correctly (approximately 31mA).

### 5.3.2. Independent VDD and IREF Bias Control

#### 5.3.2.1. Two Voltage Sources

Connect the positive and negative outputs of a power supply ( $V_{DD}$ ) to J11. In addition, connect the positive output of a second supply ( $V_{REF}$ ) to TP1 and the negative output to the negative output of the  $V_{DD}$  supply. Set both power supplies to 0.95V and enable the power supply outputs. Monitor the  $I_{DD}$  of the  $V_{DD}$  supply to confirm the nominal bias point is set correctly (approximately 31mA).

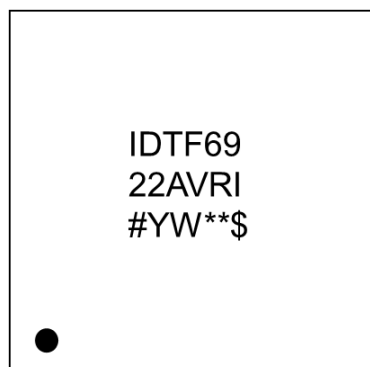
#### 5.3.2.2. Voltage Source and Current Source

Connect the positive and negative outputs of a power supply ( $V_{DD}$ ) to J11. In addition, connect an independent current supply ( $I_{REF}$ ) to TP1 and the ground of the current supply to the negative terminal of the  $V_{DD}$  supply. Set  $V_{DD}$  to 0.95V,  $I_{REF}$  to 100 $\mu$ A, and enable the power supply outputs. Monitor the  $I_{DD}$  of the  $V_{DD}$  supply to confirm the nominal bias point is set correctly (approximately 31mA).

## 6. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

## 7. Marking Diagram



- Lines 1 and 2: Renesas part number
- Line 3:
  - # is the device step.
  - YW is the last digit of the year and workweek code.
  - \*\*\$ is the lot sequential code and mark location code.

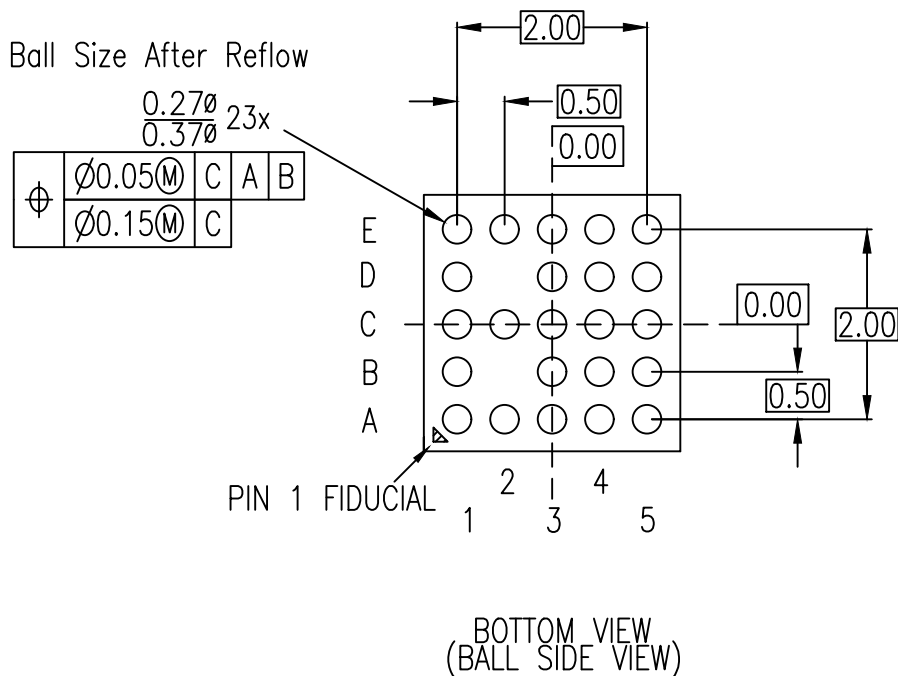
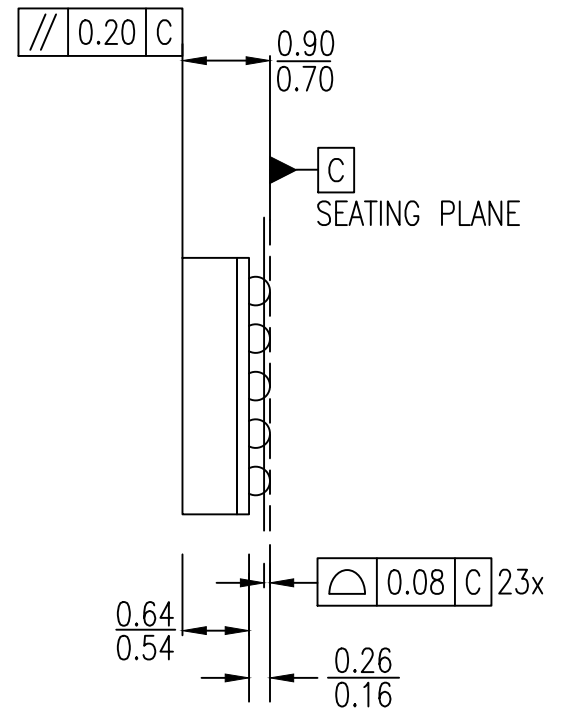
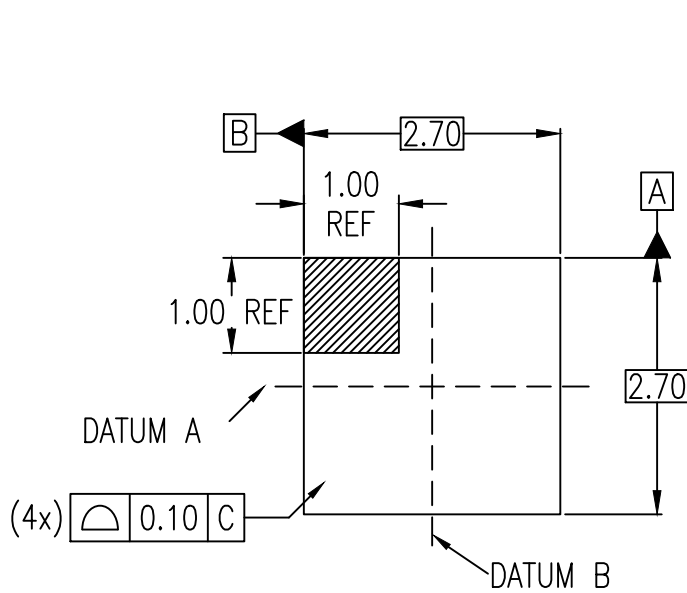
Note: Top view (ball side down)

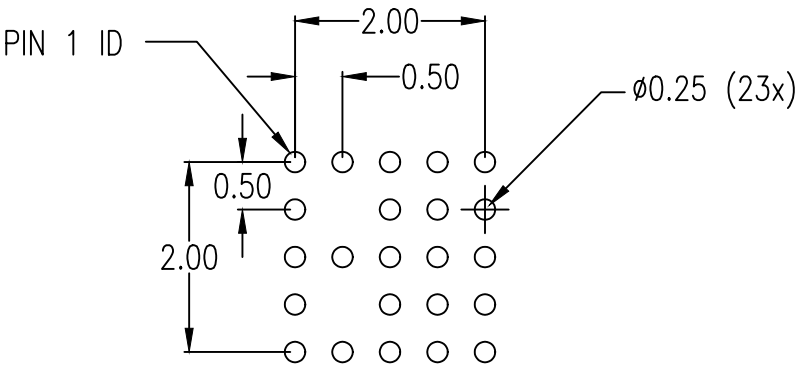
## 8. Ordering Information

| Part Number | Package                                   | MSL Rating | Carrier Type | Temp. Range    |
|-------------|-------------------------------------------|------------|--------------|----------------|
| F6922AVRI   | 2.7 × 2.7 × 0.9 mm <a href="#">23-BGA</a> | 3          | Tray         | -40°C to +85°C |
| F6922AVRI8  | 2.7 × 2.7 × 0.9 mm <a href="#">23-BGA</a> | 3          | Reel         | -40°C to +85°C |
| F6922EVB    | F6922 Evaluation Board                    |            |              |                |

## 9. Revision History

| Revision | Date         | Description      |
|----------|--------------|------------------|
| 1.0      | Jun 25, 2021 | Initial release. |





RECOMMENDED LAND PATTERN DIMENSION  
(TOP VIEW)

- NOTES:
- 1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
  - 2. TOP DOWN VIEW. AS VIEWED ON PCB.
  - 3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| Package Revision History |         |                 |
|--------------------------|---------|-----------------|
| Date Created             | Rev No. | Description     |
| Dec. 6, 2018             | Rev 00  | Initial Release |

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