钍地半导体
Tudi Semiconductor

Product Specification

TUDI- AT93C46D/AT93C46E

Three-Wire Serial EEPROM

网址 www.sztdbdt.com

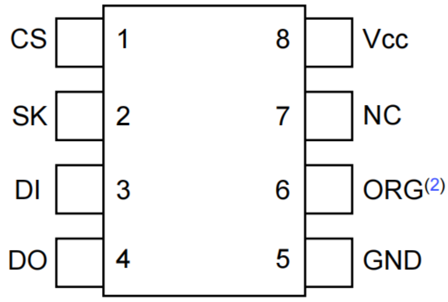
用芯智造 · 卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

8-lead PDIP/SOIC/TSSOP



- Low-Voltage Operation:
  - Vcc = 1.8V to 5.5V
- User-Selectable Internally Organized as 128 x 8 (1K) or 64 x 16 (1K)
- Non-Selectable Internal Organization as 64 x 16 (1K), AT93C46E Only
- Industrial Temperature Range: -40°C to +85°C
- Three-Wire Serial Interface
- 2 MHz Clock Rate (5V)
- Self-Timed Write Cycle within 5 ms Maximum
- High Reliability:
  - Endurance: 1,000,000 write cycles
  - Data retention: 100 years
- Green Package Options (Lead-free/Halide-free/RoHS compliant)
- Die Sale Options: Wafer Form and Tape and Reel

Description

The AT93C46D provides 1,024 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 64 words of 16 bits each (when the ORG pin is connected to Vcc) and 128 words of 8 bits each (when the ORG pin is tied to ground). The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential. The AT93C46D is available in space-saving 8-lead PDIP, 8-lead SOIC, 8-lead TSSOP, 8-pad UDFN and 8-ball VFBGA packages. All packages operate from 1.8V to 5.5V.

The AT93C46E provides 1,024 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 64 words of 16 bits each only. The AT93C46E does not offer the ORG pin so organization is not user-selectable on this device. The device is optimized for use in many industrial and commercial applications where low?power and low-voltage operations are essential. The AT93C46E is also available in space-saving and 8-lead PDIP, 8-lead SOIC and 8-lead TSSOP packages. All packages operate from 1.8V to 5.5V.

The AT93C46D/AT93C46E is enabled through the Chip Select (CS) pin and accessed via a three-wire serial interface consisting of Data Input (DI), Data Output (DO), and Serial Data Clock (SK). Upon receiving a READ instruction at DI, the address is decoded, and the data is clocked out serially on the DO pin. The write cycle is completely self-timed, and no separate erase cycle is required before write. The write cycle is only enabled when the part is in the Erase/ Write Enable state. When CS is brought high following the initiation of a write cycle, the DO pin outputs the Ready/ Busy status of the part.

Pin Descriptions

The descriptions of the pins are listed in Table 2-1.

Table 2-1. Pin Function Table

Name	8-Lead PDIP	8-Lead SOIC	8-Lead TSSOP	8-Pad UDFN(1)	8-Ball VFBGA	Function
CS	1	1	1	1	1	Chip Select
SK	2	2	2	2	2	Serial Data Clock
DI	3	3	3	3	3	Serial Data Input
DO	4	4	4	4	4	Serial Data Output
GND	5	5	5	5	5	Ground
ORG(2)	6	6	6	6	6	Internal Organization
NC	7	7	7	7	7	No Connect
V_{CC}	8	8	8	8	8	Device Power Supply

Note:

1. The exposed pad on this package can be connected to GND or left floating.
2. The Internal Organization (ORG) pin is a No Connect (NC) on the AT93C46E device.

Chip Select (CS)

The Chip Select (CS) pin is used to control device selection. The AT93C46D/AT93C46E is selected when the CS pin is high. When the device is not selected, data will not be accepted via the Serial Data Input (DI) pin, and the Serial Output (DO) pin will remain in a high-impedance state.

Serial Data Clock (SK)

The Serial Data Clock (SK) pin is used to synchronize the communication between a master and the AT93C46D/AT93C46E. Instructions, addresses or data present on the Serial Data Input (DI) pin is latched in on the rising edge of SK, while output on the Serial Data Output (DO) pin is also clocked out on the rising edge of SK.

Serial Data Input (DI)

The Serial Data Input (DI) pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the Serial Data Clock (SK).

Serial Data Output (DO)

The Serial Data Output (DO) pin is used to transfer data out of the AT93C46D/AT93C46E. During a read sequence, data is shifted out on this pin after the rising edge of the Serial Data Clock (SK).

This pin also outputs the Ready/Busy status of the part if CS is brought high after being low for a minimum of t_{CS} and an erase or write operation has been initiated.

Ground (GND)

The ground reference for the power supply. The Ground (GND) pin should be connected to the system ground.

Internal Organization (ORG)

The Internal Organization (ORG) pin is used to select between the x16 or x8 memory organizations of the device. When the ORG pin is tied to V_{CC}, the x16 memory organization is selected. When the ORG pin is tied to GND, the x8 memory organization is selected.

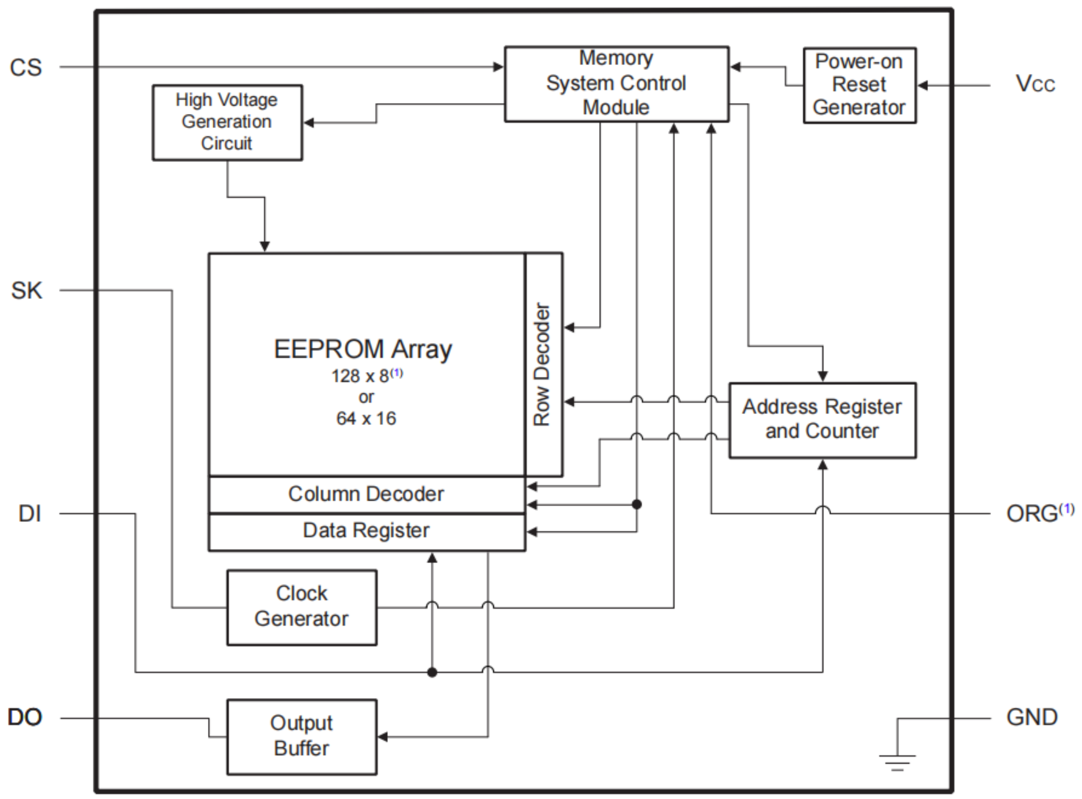
If the ORG pin is left unconnected and the application does not load the input beyond the capability of the internal 1 MΩ pull-up resistor, then the x16 organization is selected.

Note: This pin is a No Connect (NC) on the AT93C46E.

Device Power Supply (V_{CC})

The Device Power Supply (V_{CC}) pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.

Block Diagram



Note:

1. The organization of the AT93C46E is not selectable by the ORG pin and defaults to 64x16. If the x16 organization is the mode of choice and pin 6 (ORG) is left unconnected, Microchip recommends using AT93C46E device.

Electrical Characteristics

Absolute Maximum Ratings

Temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
V_{CC}	6.25V
Voltage on any pin with respect to ground	-1.0V to +7.0V
DC output current	5.0 mA
ESD protection	2 kV

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

Table 4-1. DC and AC Operating Range

AT93C46D/AT93C46E		
Operating Temperature (Case)	Industrial Temperature Range	-40°C to +85°C
V_{CC} Power Supply	Low-Voltage Grade	1.8V to 5.5V

DC Characteristics

Table 4-2. DC Characteristics[1]

Parameter	Symbol	Minimum	Typical	Maximum	Units	Test Conditions
Supply Voltage	V_{CC1}	1.8	—	5.5	V	
Supply Voltage	V_{CC2}	2.7	—	5.5	V	
Supply Voltage	V_{CC3}	4.5	—	5.5	V	
Supply Current	I_{CC1}	—	0.5	2.0	mA	V_{CC} = 5.0V, Read at 1 MHz
Supply Current	I_{CC2}	—	0.5	2.0	mA	V_{CC} = 5.0V, Write at 1 MHz
Standby Current (1.8V Option)	I_{SB1}	—	0.4	1.0	µA	V_{CC} = 1.8V, CS = 0V
Standby Current (2.7V Option)	I_{SB2}	—	6.0	10.0	µA	V_{CC} = 2.7V, CS = 0V
Standby Current (5.0V Option)	I_{SB3}	—	10.0	15.0	µA	V_{CC} = 5.0V, CS = 0V
Input Leakage Current	I_{IL}	—	0.1	1.0	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	—	0.1	1.0	µA	V_{IN} = 0 to V_{CC}

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Parameter	**Symbol**	**Minimum**	**Typical**	**Maximum**	**Units**	**Test Conditions**
Input Low-Voltage	V_{IL1}	-0.6	—	0.8	V	$2.7V \le V_{CC} \le 5.5V$ (Note 2)
Input High-Voltage	V_{IH1}	2.0	—	V_{CC} + 1	V	$2.7V \le V_{CC} \le 5.5V$ (Note 2)
Input Low-Voltage	V_{IL2}	-0.6	—	V_{CC} x 0.3	V	$1.8V \le V_{CC} \le 2.7V$ (Note 2)
Input High-Voltage	V_{IH2}	V_{CC} x 0.7	—	V_{CC} + 1	V	$1.8V \le V_{CC} \le 2.7V$ (Note 2)
Output Low-Voltage	V_{OL1}	—	—	0.4	V	$2.7V \le V_{CC} \le 5.5V$, I_{OL} = 2.1 mA
Output High-Voltage	V_{OH1}	2.4	—	—	V	$2.7V \le V_{CC} \le 5.5V$, I_{OH} = -0.4 mA
Output Low-Voltage	V_{OL2}	—	—	0.2	V	$1.8V \le V_{CC} \le 2.7V$, I_{OL} = 0.15 mA
Output High-Voltage	V_{OH2}	V_{CC} - 0.2	—	—	V	$1.8V \le V_{CC} \le 2.7V$, I_{OH} = -100 µA

Note:

1. Applicable over recommended operating range from: T_A = -40°C to +85°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted).
2. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Table 4-3. AC Characteristics[1]

Parameter	Symbol	Minimum	Typical	Maximum	Units	Test Conditions
Clock Frequency, SK	f_{SK}	0	—	2	MHz	$4.5V \le V_{CC} \le 5.5V$
		0	—	1	MHz	$2.7V \le V_{CC} \le 5.5V$
		0	—	250	kHz	$1.8V \le V_{CC} \le 5.5V$
High Time, SK	t_{SKH}	250	—	—	ns	$2.7V \le V_{CC} \le 5.5V$
		1000	—	—	ns	$1.8V \le V_{CC} \le 5.5V$
Low Time, SK	t_{SKL}	250	—	—	ns	$2.7V \le V_{CC} \le 5.5V$
		1000	—	—	ns	$1.8V \le V_{CC} \le 5.5V$
Minimum CS Low Time	t_{CS}	250	—	—	ns	$2.7V \le V_{CC} \le 5.5V$
		1000	—	—	ns	$1.8V \le V_{CC} \le 5.5V$
CS Setup Time	t_{CSS}	50	—	—	ns	$2.7V \le V_{CC} \le 5.5V$, Relative to SK
		200	—	—	ns	$1.8V \le V_{CC} \le 5.5V$, Relative to SK
DI Setup Time	t_{DIS}	100	—	—	ns	$2.7V \le V_{CC} \le 5.5V$, Relative to SK
		400	—	—	ns	$1.8V \le V_{CC} \le 5.5V$, Relative to SK
CS Hold Time	t_{CSH}	0	—	—	ns	Relative to SK

..........continued

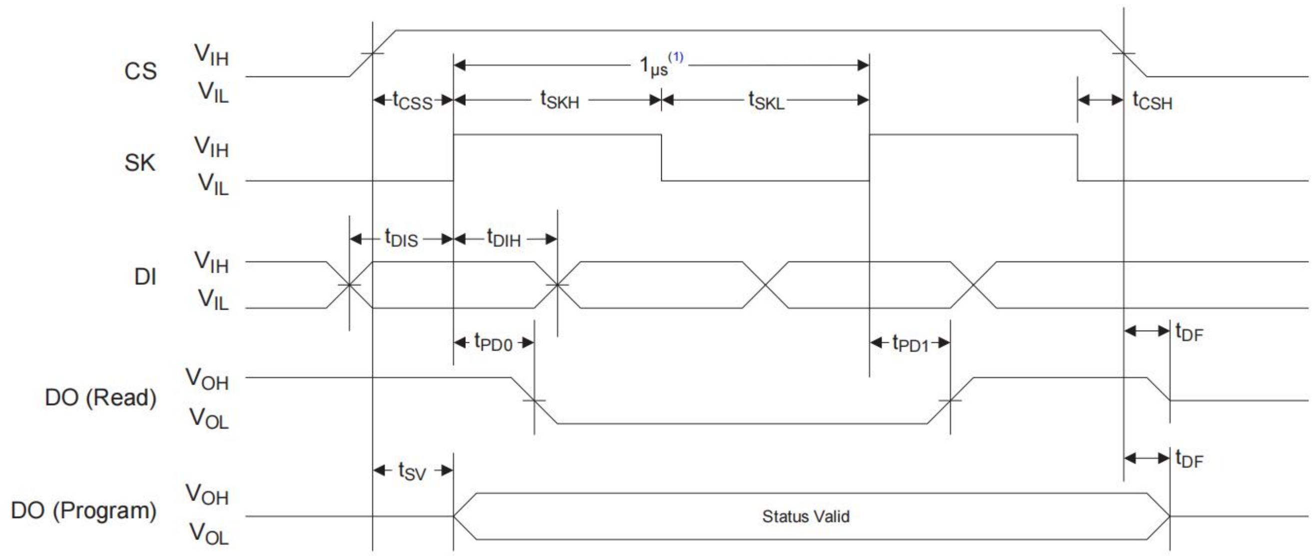
Parameter	Symbol	Minimum	Typical	Maximum	Units	Test Conditions
DI Hold Time	t_{DIH}	100	—	—	ns	$2.7V \le V_{CC} \le 5.5V$, Relative to SK
		400	—	—	ns	$1.8V \le V_{CC} \le 5.5V$, Relative to SK
Output Delay to 1	t_{PD1}	—	—	250	ns	$2.7V \le V_{CC} \le 5.5V$
		—	—	1000	ns	$1.8V \le V_{CC} \le 5.5V$
Output Delay to 0	t_{PD0}	—	—	250	ns	$2.7V \le V_{CC} \le 5.5V$
		—	—	1000	ns	$1.8V \le V_{CC} \le 5.5V$
CS to Status Valid	t_{SV}	—	—	250	ns	$2.7V \le V_{CC} \le 5.5V$
		—	—	1000	ns	$1.8V \le V_{CC} \le 5.5V$
CS to DO in High-Impedance	t_{DF}	—	—	100	ns	$4.5V \le V_{CC} \le 5.5V$, CS = V_{IL}
		—	—	150	ns	$2.7V \le V_{CC} \le 5.5V$, CS = V_{IL}, AT93C46E
		—	—	250	ns	$2.7V \le V_{CC} \le 5.5V$, CS = V_{IL}, AT93C46D
		—	—	400	ns	$1.8V \le V_{CC} \le 5.5V$, CS = V_{IL}
Write Cycle Time	t_{WP}	0.1	3	5	ms	$1.8V \le V_{CC} \le 5.5V$

Note:

1. Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = as specified, C_L = 1 TTL Gate and 100 pF (unless otherwise noted).

Synchronous Data Timing

Figure 4-1. Synchronous Data Timing



Note:

1. This is the minimum SK period.

Electrical Specifications

Power-Up Requirements and Reset Behavior

During a power-up sequence, the V_{CC} supplied to the AT93C46D/AT93C46E should monotonically rise from GND to the minimum V_{CC} level, as specified in Table 4-1, with a slew rate no faster than 0.1 V/µs.

Device Reset

To prevent inadvertent write operations or any other spurious events from occurring during a power-up sequence, the AT93C46D/AT93C46E includes a Power-on Reset (POR) circuit. Upon power-up, the device will not respond to any commands until the V_{CC} level crosses the internal voltage threshold (V_{POR}) that brings the device out of Reset and into Standby mode.

The system designer must ensure the instructions are not sent to the device until the V_{CC} supply has reached a stable value greater than or equal to the minimum V_{CC} level. Additionally, once the V_{CC} is greater than or equal to the minimum V_{CC} level, the bus master must wait at least t_{PUP} before sending the first command to the device. See Table 4-4 for the values associated with these power-up parameters.

Table 4-4. Power-up Conditions[1]

Symbol	Parameter	Min.	Max.	Units
t_{PUP}	Time required after V_{CC} is stable before the device can accept commands	100	—	µs
V_{POR}	Power-on Reset Threshold Voltage	—	1.5	V
t_{POFF}	Minimum time at V_{CC} = 0V between power cycles	500	—	ms

Note:

1. These parameters are characterized but they are not 100% tested in production.

If an event occurs in the system where the V_{CC} level supplied to the AT93C46D/AT93C46E drops below the maximum V_{POR} level specified, it is recommended that a full power cycle sequence be performed by first driving the V_{CC} pin to GND, waiting at least the minimum t_{POFF} time and then performing a new power-up sequence in compliance with the requirements defined in this section.

Pin Capacitance

Table 4-5. Pin Capacitance[1]

Symbol	Test Condition	Max.	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (CS, SK, DI, ORG)	5	pF	V_{IN} = 0V

Note:

1. This parameter is characterized but is not 100% tested in production.

EEPROM Cell Performance Characteristics

Table 4-6. EEPROM Cell Performance Characteristics

Operation	Test Condition	Min.	Max.	Units
Write Endurance[1]	T_A = 25°C, V_{CC} = 5.0V	1,000,000	—	Write Cycles
Data Retention[1]	T_A = 55°C	100	—	Years

Note:

1. Performance is determined through characterization and the qualification process.

Device Commands and Addressing

The AT93C46D/AT93C46E is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the Host processor. A valid instruction starts with a rising edge of CS and consists of a Start bit (SB), followed by the appropriate opcode, and the desired memory address location.

Table 5-1. AT93C46D/AT93C46E Instruction Set

Instruction	SB	Opcode	Address		Data		Comments
			X8[1]	X16[1]	X8	X16	
READ	1	10	A_6-A_0	A_5-A_0			Reads data stored in memory at specified address.
EWEN	1	00	11XXXXX	11XXXX			Write Enable must precede all programming modes.
ERASE	1	11	A_6-A_0	A_5-A_0			Erases memory location A_N-A_0.
WRITE	1	01	A_6-A_0	A_5-A_0	D_7-D_0	D_{15}-D_0	Writes memory location A_N-A_0.
ERAL	1	00	10XXXXX	10XXXX			Erases all memory locations. Valid only at V_{CC3}. See Table 4-2.
WRAL	1	00	01XXXXX	01XXXX	D_7-D_0	D_{15}-D_0	Writes all memory locations. Valid only at V_{CC3}. See Table 4-2.
EWDS	1	00	00XXXXX	00XXXX			Disables all programming instructions.

Note:

1. The 'X' in the address field represent a "don't care" bit, and must be sent to the device.

Table 5-2. Organization Key for Timing Diagrams

I/O	AT93C46D/AT93C46E (1K)	
	x8[1]	x16
A_N	A_6	A_5
D_N	D_7	D_{15}

Note:

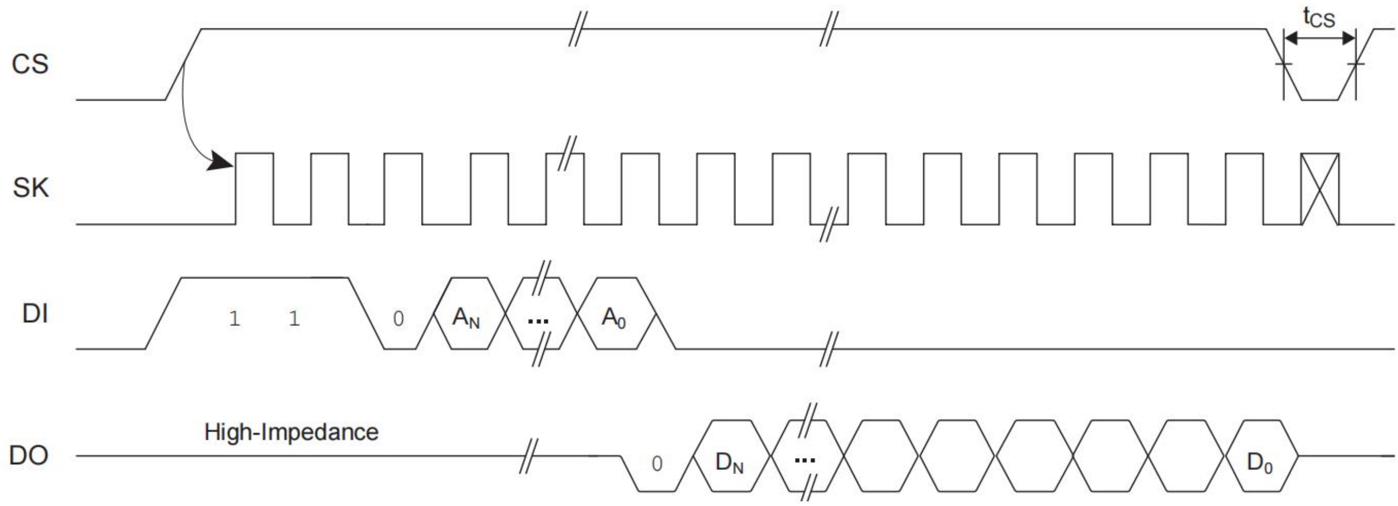
1. The internal organization of the AT93C46E is x16 only.

Read Operation (READ)

The READ instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the DO pin. Output data changes are synchronized with the rising edges of the SK pin.

Note: A dummy bit (logic '0') precedes the 8-bit or 16-bit data output string.

Figure 5-1. READ Timing

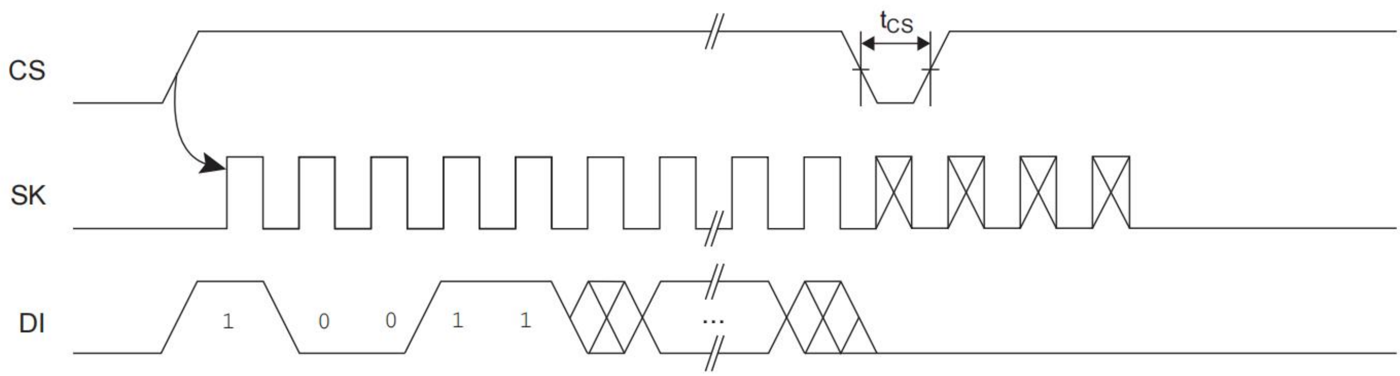


Erase/Write Enable (EWEN)

To ensure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out.

Note: Once in the write enabled state, programming remains enabled until an EWDS instruction is executed, or V_{CC} power is removed from the part.

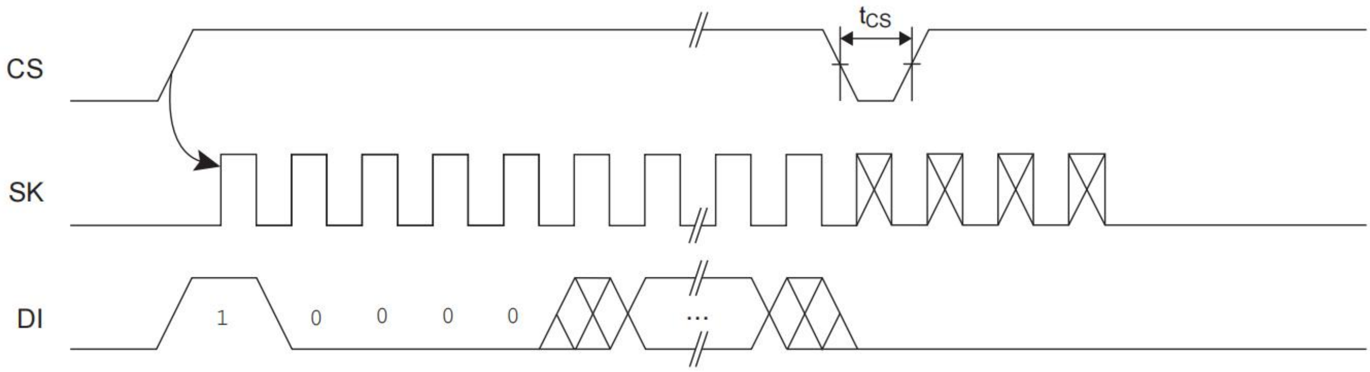
Figure 5-2. EWEN Timing



Erase/Write Disable (EWDS)

To protect against accidental data disturbance, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

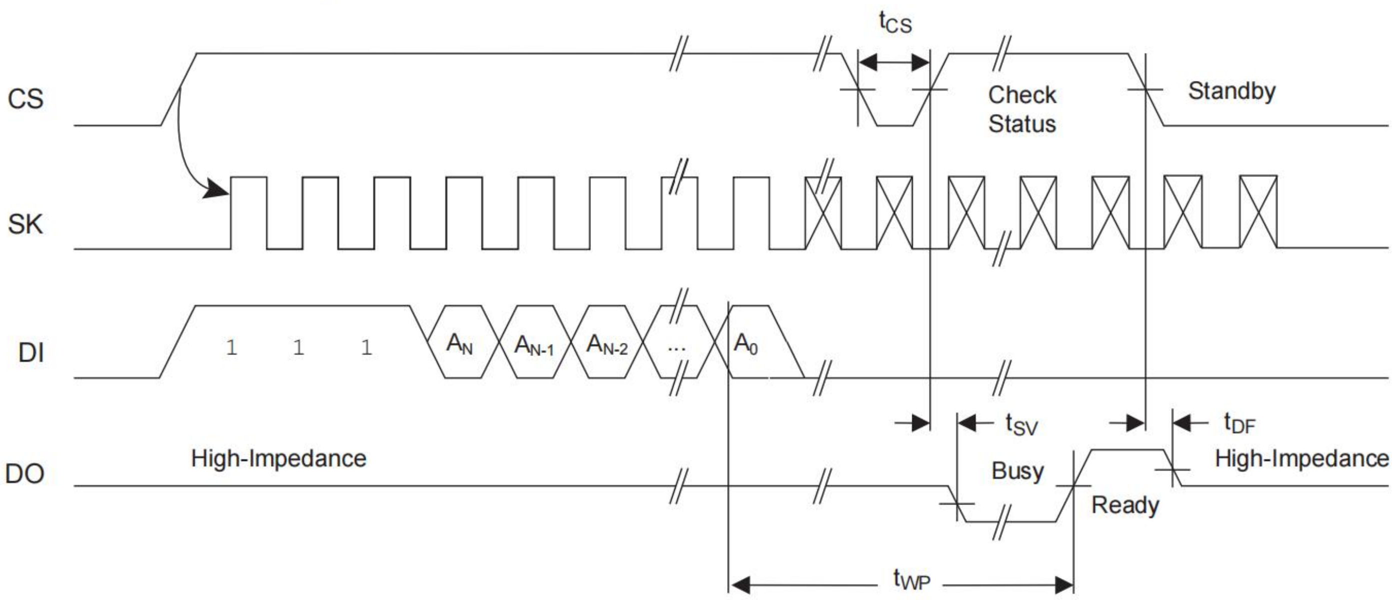
Figure 5-3. EWDS Timing



Erase Operation (ERASE)

The `ERASE` instruction programs all bits in the specified memory location to the logic '1' state. The self-timed erase cycle starts once the `ERASE` instruction and address are decoded. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of t_{CS}. A logic '1' at the DO pin indicates that the selected memory location has been erased, and the part is ready for another instruction.

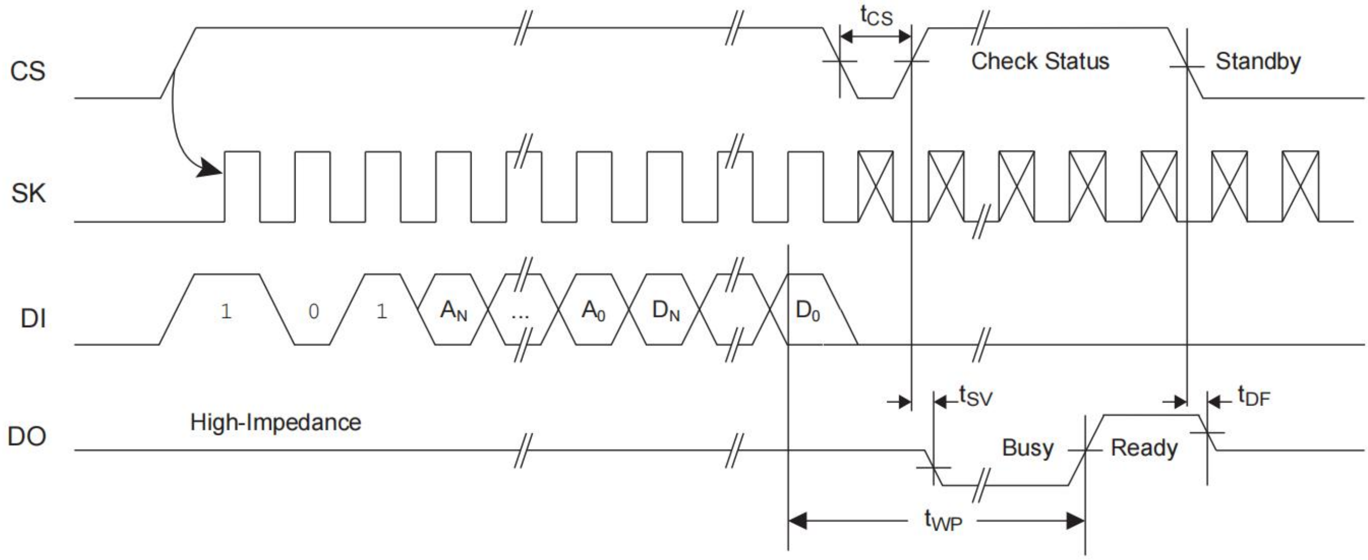
Figure 5-4. ERASE Timing



Write Operation (WRITE)

The `WRITE` instruction contains the 8 bits or 16 bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP}, starts after the last bit of data is received at DI pin. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of t_{CS}. A logic '0' at DO indicates that programming is still in progress. A logic '1' indicates that the memory location at the specified address has been written with the data pattern contained in the instruction, and the part is ready for further instructions. A Ready/Busy status cannot be obtained if CS is brought high after the end of the self-timed programming cycle, t_{WP}.

Figure 5-5. WRITE Timing

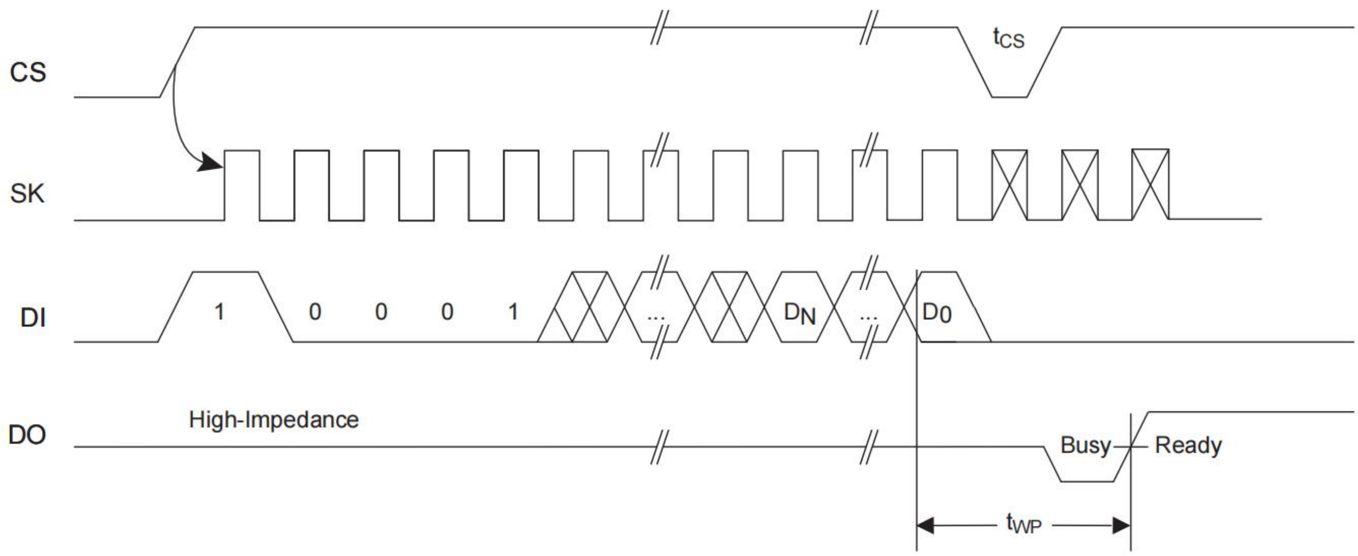


Write All (WRAL)

The Write All (`WRAL`) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of t_{CS}.

Note: The `WRAL` instruction is valid only at V_{CC3} (see Table 4-2).

Figure 5-6. WRAL Timing

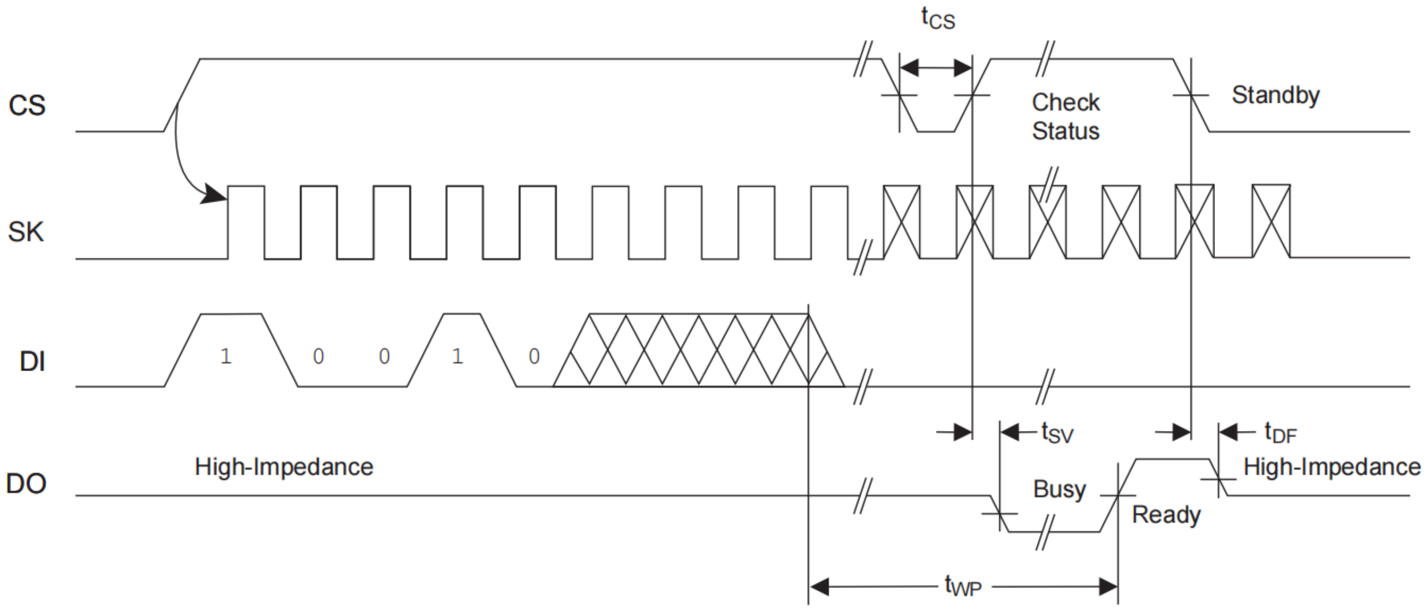


Erase All (ERAL)

The Erase All (`ERAL`) instruction programs every bit in the memory array to the logic '`1`' state and is primarily used for testing purposes. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of t_{CS}.

Note: The `ERAL` instruction is valid only at V_{CC3} (see Table 4-2).

Figure 5-7. ERAL Timing



A T 9 3 C 4 6 D N - S H - B

Product Family
93C = Microwire-compatible Three-Wire Serial EEPROM

Device Density
46 = 1-Kilobit

Device Organization
D = User Selectable
E = 16 x 64 Only

Package Variation (if applicable)
N = SOIC
Y6 = UDFN
U3 = VFBGA

Shipping Carrier Option
B = Bulk
T = Tape and Reel, Standard Quantity Option
E = Tape and Reel, Extended Quantity Option

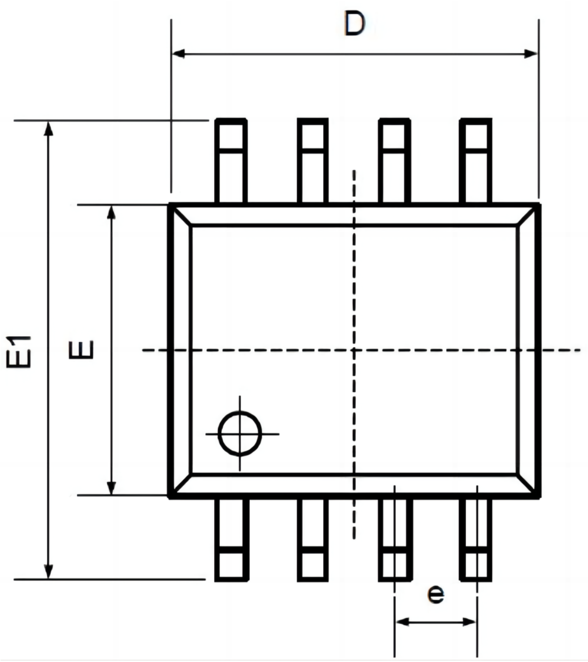
Package Device Grade or Wafer/Die Thickness
H or U = Industrial Temperature Range (-40°C to +85°C)
11 = 11mil Wafer Thickness

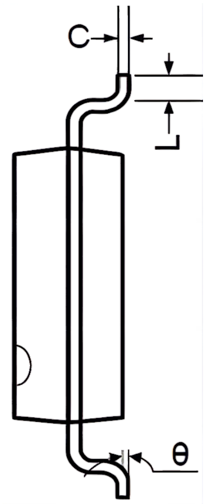
Package Option
S = SOIC
T = TSSOP
Y = 2.0mm x 3.0mm UDFN
P = PDIP
U = VFBGA
WWU= Wafer Unsawn

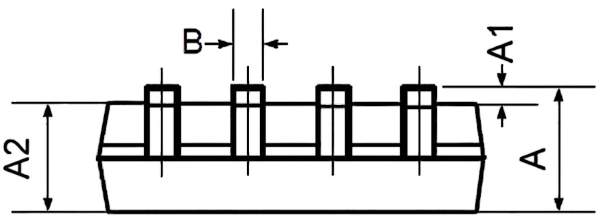
Order information

Order Number	Package	Package Quantity	Marking On The park	Temperature
AT93C46DN-SH-T -TUDI	SOP8	Tape,Reel,2500	AT93C46DN-SH-T	40°C to 85°C
AT93C46EN-SH-T-TUDI	SOP8	Tape,Reel,2500	AT93C46EN-SH-T	

Package SOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Important statement:

●TUDI Semiconductor reserves the right to modify the product manual without prior notice! Before placing an order, customers need to confirm whether the obtained information is the latest version and verify the completeness of the relevant information.

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