4-Channel LDO PMIC For Camera Applications

Features

- VIN1 input voltage range: 0.6V to 2.2V
- DVDD1 output voltage range: 0.6V~1.8V
- DVDD1 dropout voltage: 90mV@1A
- DVDD1 output drive capability: 1.5A(Typ.)
- The output drive capability of DVDD1 can be set by config I²C
- VIN2 input voltage range: 2.3V to 5.5V
- VIN3 input voltage range: 1.8V to 5.5V
- AVDD1/2/3 output voltage range: 1.2V~4.3V
- AVDD1/2/3 dropout voltage: 60mV@300mA
- AVDD1/2/3 output drive capability: 400mA(Typ.)
- The max of AVDD1/2/3 output drive capability can be set to 600mA by config I²C
- AVDD1/2/3 power supply rejection ratio: typical 96dB (I_{OUT}=100mA, Freq=1KHz)
- AVDD1/2/3 noise: typical 9μVrms (I_{OUT}=30mA, BW=10Hz to 100KHz)
- Quiescent current: typical: 90μA
- Shutdown current: typical: 0.9μA
- WLCSP 1.083mmX1.474mmX0.38mm-12B package

Applications

Digital camera

Smart phone

Camera module

General Description

AWP37001CSR is a 4-ch integrated LDO PMIC for camera applications include 1-ch DVDD, 3-ch AVDD, with 1MHz high speed I²C interface, the function setting is flexible such as power sequence, output discharge. The chip can be enabled by I²C.

Due to high load current and lower working voltage of DVDD, AWP37001 used N-MOSFET LDO architecture without charge pump for 1-ch DVDD LDO, for the AVDD, AWP37001 used P-MOSFET LDO architecture. VIN2 serves as the system power supply, providing power to the internal fundamental modules and simultaneously supplying AVDD1 and AVDD2. VIN1 is the power supply for DVDD, while VIN3 is the power supply for AVDD3.

AWP37001 is designed to work with a 2.2μF or more input ceramic capacitor and a 2.2μF or more output ceramic capacitor. The low power dissipation and good dynamic response make AWP37001 very suitable for hand-held communication equipment. Tiny package makes high density mounting of the IC on boards possible.

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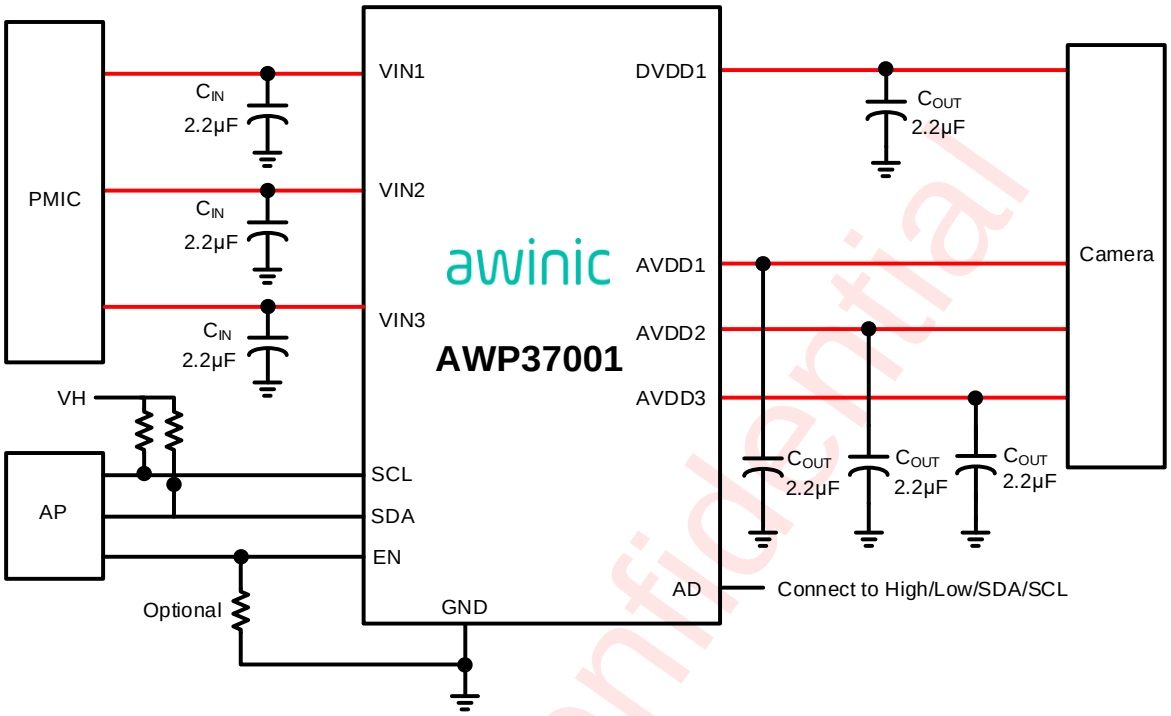
Typical Application Circuit



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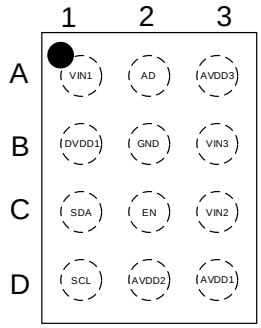
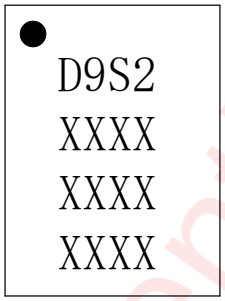
Pin Configuration And Top Mark

AWP37001CSR (Top View)



AWP37001CSR Marking (Top View)



D9S2 – AWP37001CSR
XXXX/XXXX/XXXX – Production Tracing Code

Pin Definition

No.	NAME	DESCRIPTION
A1	VIN1	DVDD1 Power supply input pin，Connecting a 2.2uF or more ceramic capacitor at the input pin
A2	AD	I2C address select, connect to GND,VIN,SCL or SDA for different device address of I2C. Internally pulled down to GND
A3	AVDD3	AVDD3 output channel，Connecting a 2.2uF or more ceramic capacitor at the output pin
B1	DVDD1	DVDD1 output channel，Connecting a 2.2uF or more ceramic capacitor at the output pin
B2	GND	ground pin
B3	VIN3	AVDD3 Power supply input pin，Connecting a 2.2uF or more ceramic capacitor at the input pin
C1	SDA	I2C clock interface
C2	EN	EN pin is used to enable basic circuits necessary for controlling the PMIC. The pin has an internal 10MΩ (typ.) pull-down and should always be connected to a logic high or low.
C3	VIN2	VSYS，AVDD1&AVDD2 Power supply input pin, Connecting a 2.2uF or more ceramic capacitor at the input pin
D1	SCL	I2C data interface
D2	AVDD2	AVDD2 output channel，Connecting a 2.2uF or more ceramic capacitor at the output pin
D3	AVDD1	AVDD1 output channel，Connecting a 2.2uF or more ceramic capacitor at the output pin

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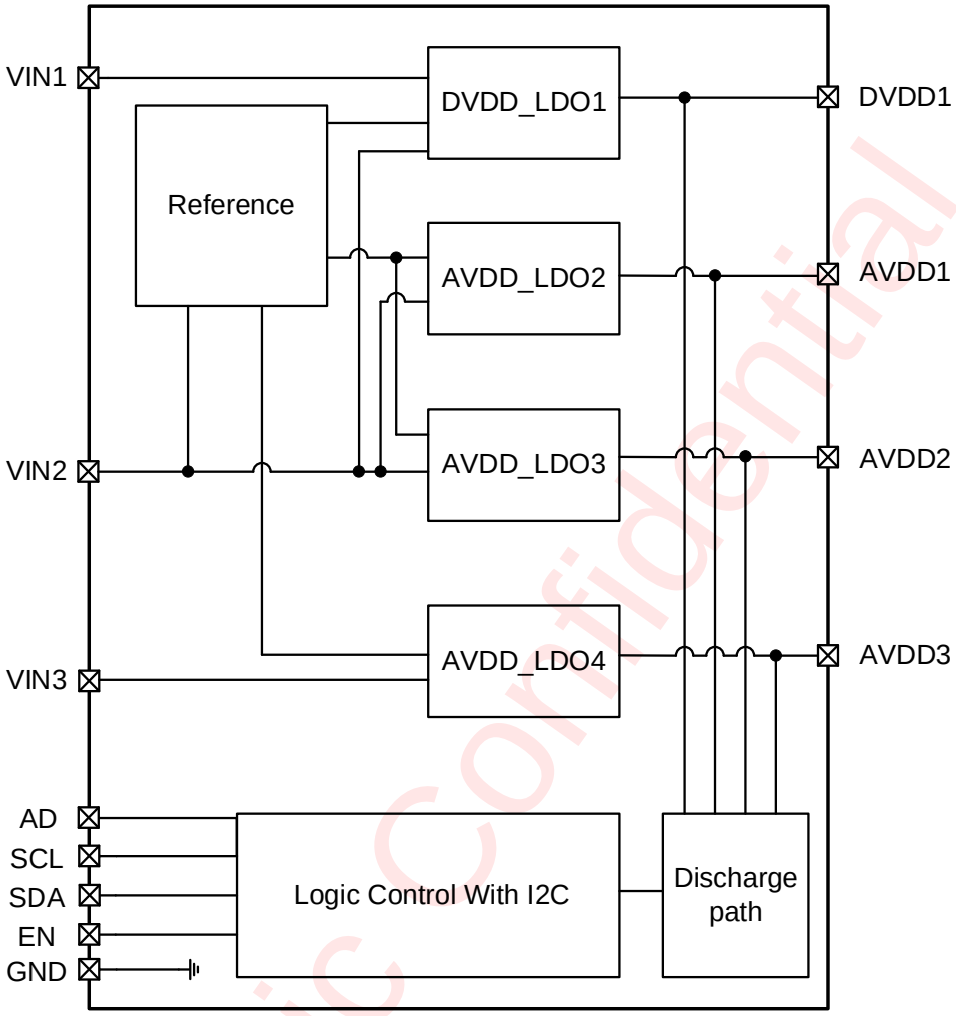
Functional Block Diagram



Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWP37001CSR	-40℃ ~ 85℃	WLCSP 1.083mmX 1.474mmX 0.38mm-12B	D9S2	MSL1	ROHS+HF	4500 units/ Tape and Reel

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Recommended Operating Conditions

Symbol	Parameter	Min	Typ.	Max	Unit
V_{IN1}	Input voltage	0.6		2.2	V
V_{IN2}	Input voltage	2.3		5.5	V
V_{IN3}	Input voltage	1.8		5.5	V
T_J	Operating free-air temperature range	-40	25	85	°C

Absolute Maximum Ratings(NOTE1)

PARAMETERS	RANGE
Input voltage range VIN1、VIN2 and VIN3	-0.3V to 6.5V
Output voltage range	-0.3V to 6.5V
Maximum operating junction temperature T_{JMAX}	150°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

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Electrical Characteristics

V_{IN1}=1.35V, V_{IN2}=3.3V, V_{IN3}=3.3V, V_{EN}>0.84V, I_{OUT}=1mA, C_{IN}=2.2μF, C_{OUT_AVDD}=2.2μF, C_{OUT_DVDD}=2.2μF, T_A=25°C(unless otherwise noted)

PARAMETER		TEST CONDITION			MIN	TYP	MAX	UNIT
Whole device								
I_{SD}	Shutdown Current	V_{EN}<0.36V				0.9	1.8	μA
I_Q	Quiescent Current	I_{OUT}=0mA, V_{EN}>0.84V and all channels disabled by I2C				26	37	μA
		I_{OUT}=0mA, V_{EN}>0.84V and all channels enabled by I2C				90	140	μA
V_{ENH}	EN Input Voltage "H"	-40°C≤T_A≤85°C			0.84			V
V_{ENL}	EN Input Voltage "L"	-40°C≤T_A≤85°C					0.36	V
R_{EN}	EN Pull Down Resistance	V_{EN}=0V to 5.5V				10		MΩ
R_{DISC}	Auto Discharge Resistance	DVDD1						
		REG0x04[3]=0				400		Ω
		REG0x04[3]=1				100		Ω
		AVDD1	AVDD2	AVDD3				
		REG0x04 [0]=0	REG0x04 [1]=0	REG0x04 [2]=0		400		Ω
		REG0x04 [0]=1	REG0x04 [1]=1	REG0x04 [2]=1		150		Ω
T_{SDH}	Thermal Shutdown Threshold	Temperature Rising				150		°C
T_{SDL}	Thermal Shutdown Reset Threshold	Temperature Falling				120		°C
V_{UVLO}	Under Voltage Lock-out	VIN2 Falling			1.85	1.9	1.95	V
V_{UVLO_HYS}	UVLO Hysteresis	VIN2 Rising				0.1		V

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PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
DVDD1							
V_{IN1_RANGE}	Input Supply Range			0.6		2.2	V
V_{OUT_ACC}	Output Voltage Accuracy			-2.0		2.0	%
V_{OUT_RANGE}	Output Voltage Range			0.6		1.8	V
$V_{OUT\_DEFAULT}$	Default Output Voltage				1.2		V
$LOAD_{Reg}$	Load Regulation	1mA≤I_{OUT}≤1000mA			4		mV
$LINE_{Reg\_DVDD1}$	Line Regulation of V_{IN1}	V_{IN2}=3.3V, 1.25V≤V_{IN1} ≤2.2V, $V_{OUT(SET)}$=1.2V, I_{OUT}=1mA			0.1		mV
	Line Regulation of V_{IN2}	V_{IN1}=1.35V, 3V≤V_{IN2} ≤4V, $V_{OUT(SET)}$=1.2V, I_{OUT}=1mA			0.5		mV
$V_{dropout}$(1)	Dropout Voltage of V_{IN1}	I_{OUT}=1A, $V_{OUT(SET)}$=1.2V V_{IN2}=3.3V			90		mV
		I_{OUT}=1A, $V_{OUT(SET)}$=1.2V V_{IN2}=4.4V			76		
	Dropout Voltage of V_{IN2}	I_{OUT}=1A, $V_{OUT(SET)}$=1.2V V_{IN1}=V_{IN2}			1270		mV
PSRR	Power Supply Ripple Rejection of V_{IN1}	I_{OUT}=100mA, V_{IN1}=1.3V+0.05V_{PP}, V_{IN2}=3.2V, $V_{OUT(SET)}$=1.1V	f=1kHz		69		dB
			f=10kHz		59		
			f=100kHz		41		
			f=1MHz		26		
	Power Supply Ripple Rejection of V_{IN2}	I_{OUT}=100mA, V_{IN2}=3.2V+0.2V_{PP}, V_{IN1}=1.3V, $V_{OUT(SET)}$=1.1V	f=1kHz		72		dB
			f=10kHz		69		
			f=100kHz		49		
			f=1MHz		35		
V_N	Output Voltage Noise	I_{OUT}=30mA, $V_{OUT(SET)}$=0.6V, BW=10Hz to 100kHz			41		μVrms
I_{CL}	Output Current Limit	DVDD1					
		REG0X01[1:0]=00		1000	1440		mA
		REG0X01[1:0]=01		1200	1580		mA
		REG0X01[1:0]=10		1300	1720		mA
		REG0X01[1:0]=11 (default)		1500	1860		mA
I_{SC}	Short Current Limit	V_{OUT}<10%*$V_{OUT(SET)}$			260		mA

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PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
VTC	Output Voltage Temperature Coefficient	-40°C≤T_A≤85°C		±50		ppm/°C

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PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
AVDD1、AVDD2 and AVDD3							
V_{IN2_RANGE}	Input Supply Range			2.3		5.5	V
V_{IN3_RANGE}	Input Supply Range			1.8		5.5	V
V_{OUT_ACC}	Output Voltage Accuracy			-2.0		2.0	%
V_{OUT_RANGE}	Output Voltage Range			1.2		4.3	V
$V_{OUT\_DEFAULT}$	Default Output Voltage				2.8		V
$LOAD_{Reg}$	Load Regulation	1mA≤I_{OUT}≤400mA, $V_{OUT(SET)}$=2.8V V_{IN1}=1.35V, V_{IN2}=3.3V, V_{IN3}=3.3V			2		mV
$LINE_{Reg\_AVDD1/2}$	Line Regulation of V_{IN2}	3≤V_{IN2}≤4V, $V_{OUT(SET)}$=2.8V, I_{OUT}=1mA			0.1		mV
$LINE_{Reg\_AVDD3}$	Line Regulation of V_{IN2}	3V≤V_{IN2}≤4V, V_{IN3}=3.3V $V_{OUT(SET)}$=2.8V, I_{OUT}=1mA			0.1		mV
	Line Regulation of V_{IN3}	3V≤V_{IN3}≤4V, V_{IN2}=3.3V $V_{OUT(SET)}$=2.8V, I_{OUT}=1mA			0.1		mV
$V_{dropout}$	Dropout Voltage(1)	I_{OUT}=300mA, $V_{OUT(SET)}$=2.8V			60		mV
PSRR	AVDD1/2 Power Supply Ripple Rejection of V_{IN2}	I_{OUT}=100mA, V_{IN2}=3.8V+0.2V_{PP}, $V_{OUT(SET)}$=2.8V	f=1kHz		96		dB
			f=10kHz		91		
			f=100kHz		72		
			f=1MHz		51		
		I_{OUT}=100mA, V_{IN2}=3.3V+0.2V_{PP}, $V_{OUT(SET)}$=2.8V	f=1kHz		92		dB
			f=10kHz		89		
			f=100kHz		68		
			f=1MHz		48		
		I_{OUT}=100mA, V_{IN2}=3V+0.05V_{PP}, $V_{OUT(SET)}$=2.8V	f=1kHz		81		dB
			f=10kHz		73		
			f=100kHz		53		
			f=1MHz		35		
PSRR	AVDD3 Power Supply Ripple Rejection of V_{IN3}	I_{OUT}=100mA, V_{IN2}=3.3V, V_{IN3}=3.8V+0.2V_{PP}, $V_{OUT(SET)}$=2.8V	f=1kHz		94		dB
			f=10kHz		95		
			f=100kHz		74		
			f=1MHz		51		

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PARAMETER		TEST CONDITION			MIN	TYP	MAX	UNIT
		I_{OUT}=100mA, V_{IN2}=3.3V, V_{IN3}=3.3V+0.2V_{PP}, $V_{OUT(SET)}$=2.8V		f=1kHz		91		dB
				f=10kHz		89		
				f=100kHz		71		
				f=1MHz		48		
		I_{OUT}=100mA, V_{IN2}=3.3V, V_{IN3}=3V+0.05V_{PP}, $V_{OUT(SET)}$=2.8V		f=1kHz		80		dB
				f=10kHz		72		
				f=100kHz		53		
				f=1MHz		35		
V_N	Output Voltage Noise	I_{OUT}=30mA, $V_{OUT(SET)}$=2.8V, BW=10Hz to 100kHz				9		μVrms
I_{CL}	Output Current Limit	AVDD1	AVDD2	AVDD3				
		REG0X02 [1:0]=00	REG0X02 [3:2]=00	REG0X02 [5:4]=0	300	480		mA
		REG0X02 [1:0]=01 (default)	REG0X02 [3:2]=01 (default)	REG0X02 [5:4]=01 (default)	400	580		mA
		REG0X02 [1:0]=10	REG0X02 [3:2]=10	REG0X02 [5:4]=10	500	680		mA
		REG0X02 [1:0]=11	REG0X02 [3:2]=11	REG0X02 [5:4]=11	600	780		mA
I_{SC}	Short Current Limit	V_{OUT}<10%*$V_{OUT(SET)}$				240		mA
VTC	Output Voltage Temperature Coefficient	-40°C≤T_A≤85°C				±50		ppm/°C

(1) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 98% of its nominal value.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
IIC Logic						
V_{IH}	Input Voltage “H”	-40°C≤T_A≤85°C	0.84			V
V_{IL}	Input Voltage “L”	-40°C≤T_A≤85°C			0.36	V

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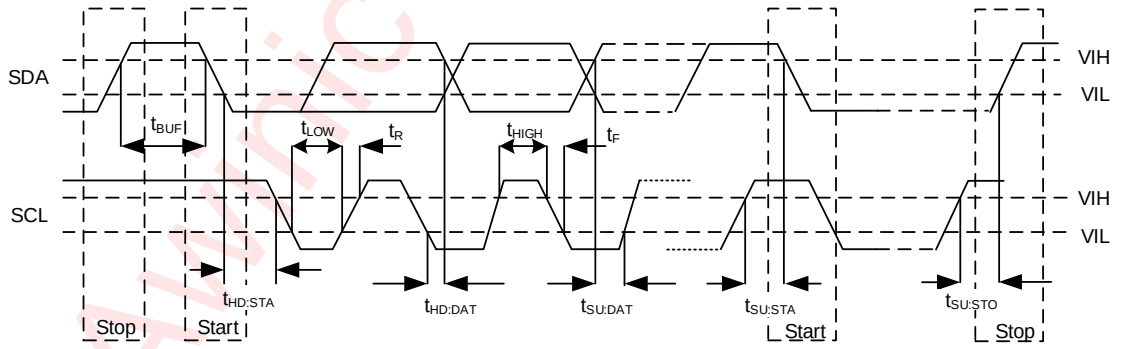
I²C Interface Timing

PARAMETER		FAST MODE			FAST MODE PLUS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
F_{SCL}	Interface clock frequency	-		400	-		1000	kHz
$T_{HD:STA}$	(Repeat-start) Start condition hold time	0.6		-	0.26		-	μs
T_{LOW}	Low level width of SCL	1.3		-	0.5		-	μs
T_{HIGH}	High level width of SCL	0.6		-	0.26		-	μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time	0.6		-	0.26		-	μs
$T_{HD:DAT}$	Data hold time	0		-	0		-	μs
$T_{SU:DAT}$	Data setup time	0.1		-	0.05		-	μs
T_R	Rising time of SDA and SCL	-		0.3	-		0.12	μs
T_F	Falling time of SDA and SCL	-		0.3	-		0.12	μs
$T_{SU:STO}$	Stop condition setup time	0.6		-	0.26		-	μs
T_{BUF}	Time between start and stop condition	1.3		-	0.5		-	μs



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Detailed Functional Description

Work Mode

AWP37001 has 4 LDO regulators. there are three AVDDs and one DVDD. It has 3 power input pins: VIN1~VIN3, 4 output pins: OUT1~OUT4. Power up/down of each regulator can be controlled by the following two ways.

A. Chip Enable Control

B. Automatic power up/down sequence control.

CHIP ENABLE CONTROL

The LDOs can be enabled and disabled independently with the LDOx_EN bits in the register (ENCR, Address 0x0F). To enable the LDOs, the external EN pin should be high, and set the LDOx_EN bits to '1'.

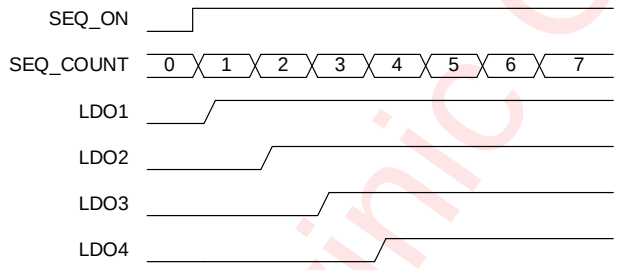
AUTOMATIC POWER UP/DOWN SEQUENCE CONTROL

AWP37001 has 7 SLOTs to which each regulator can be assigned.

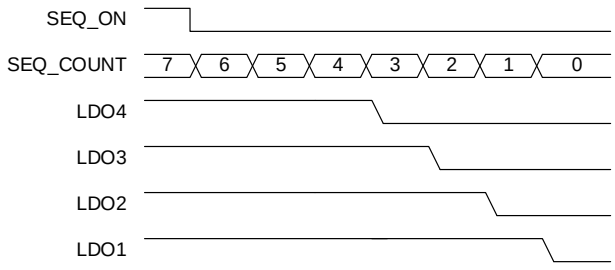
SLOT1	SLOT2	SLOT3	SLOT4	SLOT5	SLOT6	SLOT7

They are started by SEQ_ON signal. When SEQ_ON is high. Internal counter SEQ_COUNT[2:0] starts increment from 0 (3'b000) to 7 (3'b111). When SEQ_ON is low, SEQ_COUNT[2:0] decrements from 7 (3'b111) to 0 (3'b000). Regulators assigned to one of SLOTs starts power-up or power-down when SEQ_COUNT[2:0] matches the SLOT number.

Internal logic signal SEQ_ON is asserted by I2C, writing 2'b00 to SEQ_CTRL will set SEQ_ON to '0', while writing 2'b01 to SEQ_CTRL will set SEQ_ON to '1'.



Example of Power-up in the case of DVDDx & AVDDx are assigned to SLOT1 ~ SLOT4 respectively.



Example of Shut-down in the case of DVDDx & AVDDx are assigned to SLOT1 ~ SLOT4 respectively.

Time Sequence of Chip Enable Control

VIN2 serves as the system power supply, providing power to the internal fundamental modules and simultaneously supplying AVDD1 and AVDD2. VIN1 is the power supply for DVDD, while VIN3 is the power supply for AVDD3. After VIN2 is powered on, the POR signal is output. The digital section requires a delay of T1 (500μs) to load the efuse state. Once this delay has elapsed, I2C communication can be immediately enabled via the EN pin.

EN pin is the enable signal. After EN pin goes high, a delay of T4 (250μs, the internal fundamental module setup time) is required. Once the T4 delay has elapsed, LDOx can be configured immediately via I2C.

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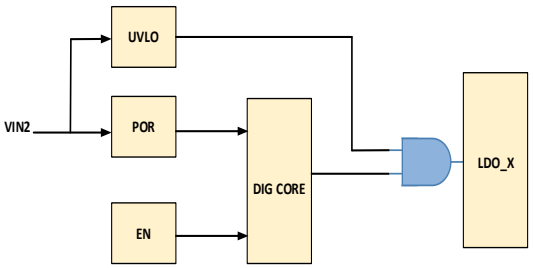
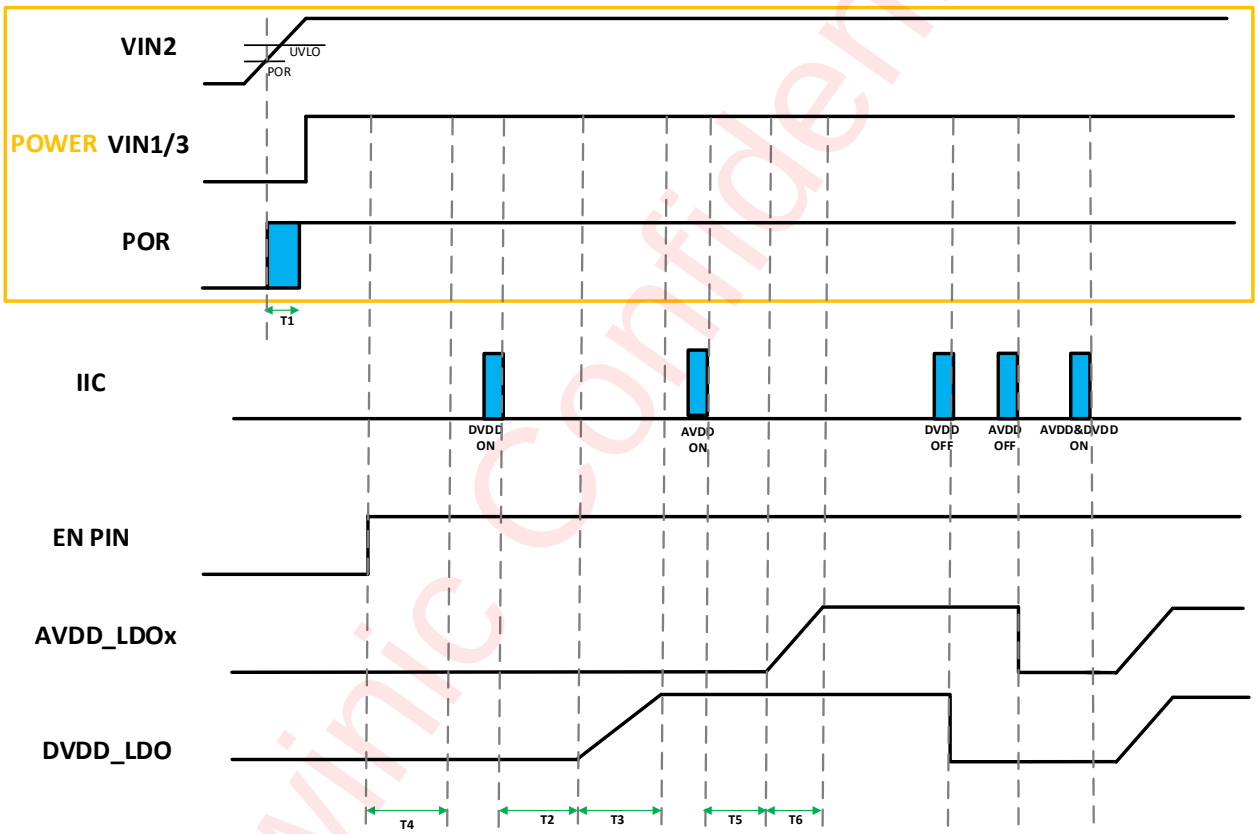


DVDD: The startup time for I2C configuration to DVDD is T2 (90μs), and the time from DVDD startup to completion is T3 (130μs).

AVDD: The startup time for I2C configuration to AVDD is T5 (280μs), and the time from AVDD startup to completion is T6 (300μs).



Output Discharge Setting

Set related bits to select output discharge function for Discharge Resistor (DISCE_MODE, Address 0x03), AWP37001 supports 2 modes for discharge, which controlled by DCE_MODE (bit 7 of DISCE_MODE register). It will force enable each LDO discharge function when DCE_MODE=0.LDOx's discharge function is controlled by bit[0] and [4:6] of DISCE_MODE register when DCE_MODE=1. In addition, bit [0:3] of DISCR register(Address 0x04) can config the value of the discharge resistor.

Output Current Limit

AWP37001 integrates output current limit function, protecting IC from excessive current. When the load is excessively heavy, AWP37001 LDO1 limits the current flowing through the IC to a typical 1860mA (default) current, LDO2/3/4 limits the current flowing through the IC to a typical 580mA (default) current. Once the current-limiting point is reached, the LDO remains in current limit for fixed OCP deglitch timer, then, the LDO

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will shut down, waiting for a hiccup timer to restart again. The restart will continue until faults disappear or new high priority faults(UVLO and OTP) appear, or user powers down this LDO output or the chip. In addition, the chip can also be configured to another mode through a register(Address 0x17), once the current-limiting point is reached, the current limit protection will be triggered and clamp the output current at a predesigned level, and the output will decrease.

UVLO

When the voltage of VIN2 fall below their UVLO falling threshold(1.9V), all LDOs will be shut down, causing a UVLO interrupt. The UVLO status bit will not change until the input voltage rises above its UVLO rising threshold(2.0V), and then one or more LDOs start up immediately.

Short Current Limit

AWP37001 LDO1 integrates a 380mA fold-back current limit function, and LDO2/3/4 integrates a 240mA fold-back current limit function, lowering the system dissipation when output overload or short to Ground.

Thermal shutdown

AWP37001 integrates thermal shutdown function, protect IC from excessively high temperature. When the chip temperature exceeds 150°C, AWP37001 detects it as an over-temperature event, triggering thermal shutdown, which will turn off the main function module, including power MOSFET. This inhibits increase of chip's temperature. IC would keep the protection-state on until the chip's temperature falls below to 120°C. At this moment, the over-temperature protection-state is released, IC resumes to work again. The hysteresis avoids IC's turning off and on frequently around the Thermal Shutdown threshold.

I²C Interface

AWP37001 supports the I²C protocol. The maximum frequency supported by the I²C is 1MHz. The pull-up resistor for the SDA and SCL can be selected from 1kΩ to 10kΩ. Usually, 4.7kΩ is recommended for 400 kHz I²C, 1kΩ is recommended for 1MHz I²C. Additionally, the I²C device supports continuous reading and writing operations.

AWP37001 is compatible with the I³C protocol, but does not support the I³C communication protocol stack.

DEVICE ADDRESS

The I²C device address is 7-bit (A7~A1), followed by the R/W bit A0 (Read=1/Write=0). Set A0 to "0" for writing and "1" for reading.

The I²C device address can be adjusted by AD and registers. There is no priority and respectively control different bits of device address. As shown in the following table:

A7	A6	A5	A4	A3	A2	A1	A0
AD[1]	0	AD[0]	1	IIC_ADDR[1]	IIC_ADDR[0]	1	W/R

Among them, A1,A4 and A6 are fixed bits, which are 1,1 and 0 respectively. A2 and A3 are controlled by register IIC_ADDR(0X0B), while A5 and A7 are determined by the AD pin. The AD pin supports four connection configurations. When AD is tied to VDD, we recommend directly connecting it to VIN2, If connecting to other VIN pins, ensure the AD voltage remains stable and exceeds 0.84V during I²C address verification prior to each communication.

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The I²C address is shown in the following table:

	A7	A6	A5	A4	A3	A2	A1	A0	I²C Address
AD pin	AD[1]	0	AD[0]	1	IIC_ADDR[1]	IIC_ADDR[0]	1	W/R	
AD connect GND	0	0	0	1	0	0	1	W/R	7'h09
AD connect GND	0	0	0	1	0	1	1	W/R	7'h0B (default)
AD connect GND	0	0	0	1	1	0	1	W/R	7'h0D
AD connect GND	0	0	0	1	1	1	1	W/R	7'h0F
AD connect VDD	0	0	1	1	0	0	1	W/R	7'h19
AD connect VDD	0	0	1	1	0	1	1	W/R	7'h1B
AD connect VDD	0	0	1	1	1	0	1	W/R	7'h1D
AD connect VDD	0	0	1	1	1	1	1	W/R	7'h1F
AD connect SCL	1	0	0	1	0	0	1	W/R	7'h49
AD connect SCL	1	0	0	1	0	1	1	W/R	7'h4B
AD connect SCL	1	0	0	1	1	0	1	W/R	7'h4D
AD connect SCL	1	0	0	1	1	1	1	W/R	7'h4F
AD connect SDA	1	0	1	1	0	0	1	W/R	7'h59
AD connect SDA	1	0	1	1	0	1	1	W/R	7'h5B
AD connect SDA	1	0	1	1	1	0	1	W/R	7'h5D
AD connect SDA	1	0	1	1	1	1	1	W/R	7'h5F

I²C START/STOP

I²C START: SDA changes from high level to low level when SCL is high level.

I²C STOP: SDA changes from low level to high level when SCL is high level.

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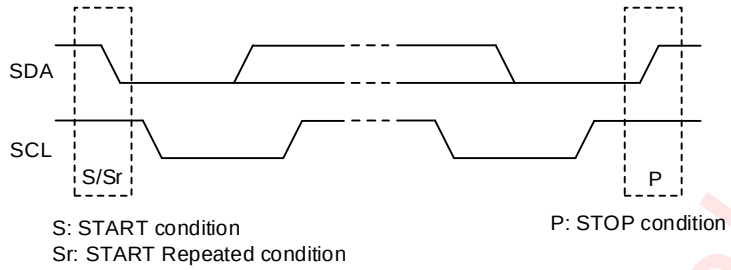
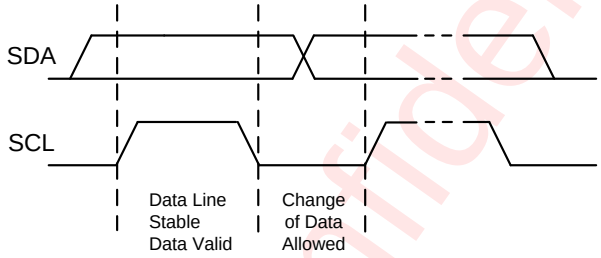


DATA VALIDATION

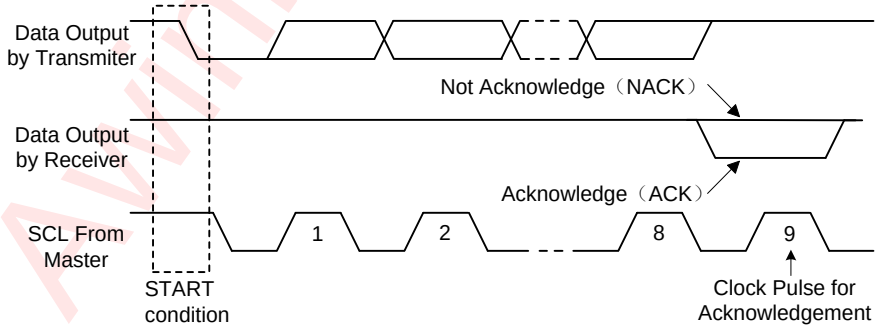
When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.



ACK (ACKNOWLEDGEMENT)

ACK means the successful transition of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is sent and I²C STOP is not sent by master, slave device sends the next data. If ACK is not sent by master, slave device stops to send data and waits for I²C stop.



WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a

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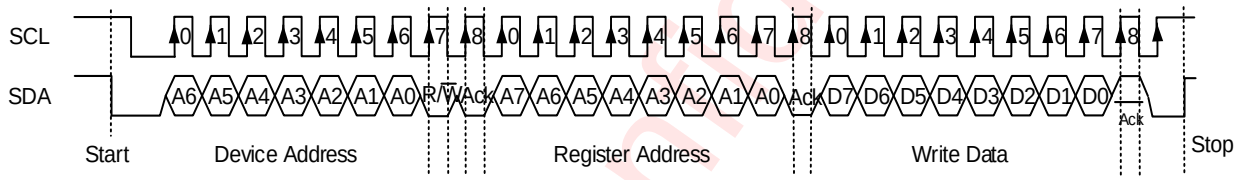
stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The “START” signal is generated by lowering the SDA signal while the SCL signal is high.
b) Master device sends slave address (7-bit) and the data direction bit R/W = 0).
c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends control register address (8-bit).
e) Slave sends acknowledge signal.
f) Master sends data byte to be written to the addressed register.
g) Slave sends acknowledge signal.
h) If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step f and g).
i) Master generates STOP condition to indicate write cycle end.



READ CYCLE

In a read cycle, the following steps should be followed:

a) Master device generates START condition.
b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).
c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends control register address (8-bit).
e) Slave sends acknowledge signal.
f) Master generates STOP condition followed with START condition or REPEAT START condition.
g) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).
h) Slave device sends acknowledge signal if the slave address is correct.
i) Slave sends data byte from addressed register.
j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.
k) If the master device generates STOP condition, the read cycle ends.

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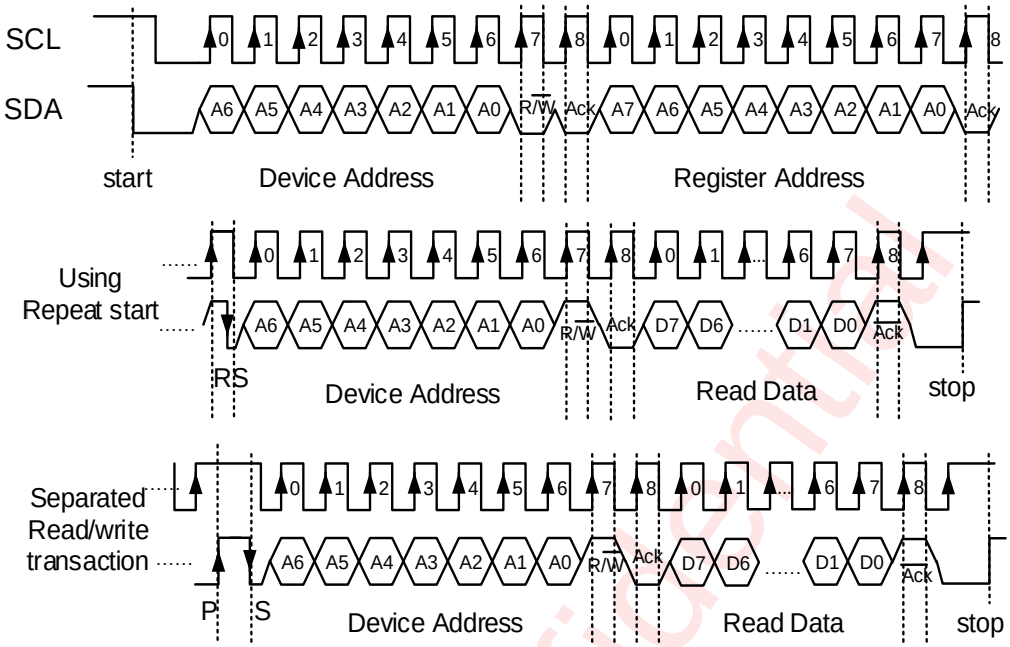

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Register Description

Ad.	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Init
0x00	CHIP_ID	R	CHIP_ID								0x08
0x01	DVDD_CLMTCR	R/W	REV						DVDD1_CLMT		0x03
0x02	AVDD_CLMTCR	R/W	REV		AVDD3_CLMT		AVDD2_CLMT		AVDD1_CLMT		0x15
0x03	DISCE_MODE	R/W	DCE_MODE	AVDD3_DCE	AVDD2_DCE	AVDD1_DCE	REV			DVDD1_DCE	0x00
0x04	DISCR	R/W	REV			AVDD3_DISR	AVDD2_DISR	AVDD1_DISR	REV	DVDD1_DISR	0x00
0x05	DVDD1_VOUT	R/W	DVDD1_VOUT								0x64
0x07	AVDD1_VOUT	R/W	AVDD1_VOUT								0x80
0x08	AVDD2_VOUT	R/W	AVDD2_VOUT								0x80
0x09	AVDD3_VOUT	R/W	AVDD3_VOUT								0x80
0x0B	IIC_ADDR	R/W	REV						IIC_ADDR_SEL		0x01
0x0C	DVDD_SEQ	R/W	REV				DVDD1_SEQ				0x00
0x0D	AVDD_SEQ1	R/W	AVDD2_SEQ				AVDD1_SEQ				0x00
0x0E	AVDD_SEQ2	R/W	REV				AVDD3_SEQ				0x00
0x0F	ENCR	R/W	REV			AVDD3_EN	AVDD2_EN	AVDD1_EN	REV	DVDD1_EN	0x00
0x10	SEQCR	R/W	SEQ_SPEED		SEQ_CTRL		SEQ_ON	SEQ_COUNT			0x00
0x11	FLT_STATUS1	R	OT_SHUTDOWN_ST	OT_WAR_ST	REV			DVDD1_SCP_ST	REV	DVDD1_OCP_ST	0x00
0x12	FLT_STATUS2	R	REV		AVDD3_SCP_ST	AVDD2_SCP_ST	AVDD1_SCP_ST	AVDD3_OCP_ST	AVDD2_OCP_ST	AVDD1_OCP_ST	0x00
0x15	FLT_FLAG1	W/C	OT_SHUTDOWN_FLAG	OT_WAR_FLAG	REV			DVDD1_SCP_FLAG	REV	DVDD1_OCP_FLAG	0x00
0x16	FLT_FLAG2	W/C	REV		AVDD3_SCP_FLAG	AVDD2_SCP_FLAG	AVDD1_SCP_FLAG	AVDD3_OCP_FLAG	AVDD2_OCP_FLAG	AVDD1_OCP_FLAG	0x00
0x17	CTR_MD	R/W	REV							HICCUP_EN	0x01

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Register Detailed Description

CHIP_ID: Chip ID (Address 0x00)

Bit	Symbol	R/W	Description	Init
7:0	CHIP ID	R	Read the chip version 8'h08/8'h0A	0x08

DVDD_CLMTCR: Current Limit Control Register (Address 0x01)

Bit	Symbol	R/W	Description	Init
7:2	REV	R/W	Reserved	0x00
1:0	DVDD1_CLMT	R/W	DVDD1 current limit control: 2'b00: 1000mA 2'b01: 1200mA 2'b10: 1300mA 2'b11: 1500mA	0x03

AVDD_CLMTCR: Current Limit Control Register (Address 0x02)

Bit	Symbol	R/W	Description	Init
7:6	REV	R/W	Reserved	0x00
5:4	AVDD3_CLMT	R/W	AVDD3 current limit control: 2'b00: 300mA 2'b01: 400mA 2'b10: 500mA 2'b11: 600mA	0x01
3:2	AVDD2_CLMT	R/W	AVDD2 current limit control: 2'b00: 300mA 2'b01: 400mA 2'b10: 500mA 2'b11: 600mA	0x01
1:0	AVDD1_CLMT	R/W	AVDD1 current limit control: 2'b00: 300mA 2'b01: 400mA 2'b10: 500mA 2'b11: 600mA	0x01

DISCE_MODE: Discharge Control Register (Address 0x03)

Bit	Symbol	R/W	Description	Init
7	DCE_MODE	R/W	Discharge mode control: 0: Auto mode, all discharge function is enable 1: Manuel mode, all discharge function set by AVDDn_DCE and DVDDn_DCE	0x00
6	AVDD3_DCE	R/W	Discharge function enable control of AVDD3: 0: Disable when DCE_MODE =1 1: Enable when DCE_MODE =1	0x00

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Bit	Symbol	R/W	Description	Init
5	AVDD2_DCE	R/W	Discharge function enable control of AVDD2: 0: Disable when DCE_MODE =1 1: Enable when DCE_MODE =1	0x00
4	AVDD1_DCE	R/W	Discharge function enable control of AVDD1: 0: Disable when DCE_MODE =1 1: Enable when DCE_MODE =1	0x00
3:1	REV	R/W	Reserved	0x00
0	DVDD1_DCE	R/W	Discharge function enable control of DVDD1: 0: Disable when DCE_MODE =1 1: Enable when DCE_MODE =1	0x00

DISCR: Discharge Control Register (Address 0x04)

Bit	Symbol	R/W	Description	Init
7:5	REV	R/W	Reserved	0x00
4	AVDD3_DISR	R/W	DVDD1 discharge resistance select: 0: 400Ω 1: 150Ω	0x00
3	AVDD2_DISR	R/W	AVDD3 discharge resistance select: 0: 400Ω 1: 150Ω	0x00
2	AVDD1_DISR	R/W	AVDD2 discharge resistance select: 0: 400Ω 1: 150Ω	0x00
1	REV	R/W	Reserved	0x00
0	DVDD1_DISR	R/W	AVDD1 discharge resistance select: 0: 400Ω 1: 100Ω	0x00

DVDD1_VOUT: DVDD1 Output Voltage Control Register (Address 0x05)

Bit	Symbol	R/W	Description	Init
7:0	DVDD1_VOUT	R/W	DVDD1 output Voltage set, 0.006V/LSB : 0x00: 0.6v; 0x01:0.606v; 0x02: 0.012v; ... 0xFF: 2.13V;	0x64

AVDD1_VOUT: AVDD1 Output Voltage Control Register (Address 0x07)

Bit	Symbol	R/W	Description	Init
7:0	AVDD1_VOUT	R/W	AVDD1 output Voltage set, 0.0125V/LSB : 0x00: 1.2v; 0x01:1.2125v; 0x02: 1.2250v;	0x80

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Bit	Symbol	R/W	Description	Init
			... 0xFF: 4.3785V;	

AVDD2_VOUT: AVDD2 Output Voltage Control Register (Address 0x08)

Bit	Symbol	R/W	Description	Init
7:0	AVDD2_VOUT	R/W	AVDD2 output Voltage set, 0.0125V/LSB : 0x00: 1.2v; 0x01:1.2125v; 0x02: 1.2250v; ... 0xFF: 4.3785V;	0x80

AVDD3_VOUT: AVDD3 Output Voltage Control Register (Address 0x09)

Bit	Symbol	R/W	Description	Init
7:0	AVDD3_VOUT	R/W	AVDD3 output Voltage set, 0.0125V/LSB : 0x00: 1.2v; 0x01:1.2125v; 0x02: 1.2250v; ... 0xFF: 4.3785V;	0x80

IIC_ADDR: (Address 0x0B)

Bit	Symbol	R/W	Description	Init
7:2	REV	R/W	Reserved	0x00
1:0	IIC_ADDR_SEL	R/W	The IIC address can be adjusted through registers and AD. For specific details, please refer to device address of Detailed Functional Description.	0x01

DVDD_SEQ: DVDD1 Sequence Control Register (Address 0x0C)

Bit	Symbol	R/W	Description	Init
7:4	REV	R/W	Reserved	0x00
3:0	DVDD1_SEQ	R/W	DVDD1 sequence set 4'b0000: disable sequence mode; 4'bx001: set the DVDD1 slot is 1; 4'bx010: set the DVDD1 slot is 2; 4'bx011: set the DVDD1 slot is 3; 4'bx100: set the DVDD1 slot is 4; 4'bx101: set the DVDD1 slot is 5; 4'bx110: set the DVDD1 slot is 6; 4'bx111: set the DVDD1 slot is 7;	0x00

AVDD_SEQ: AVDD Sequence Control Register (Address 0x0D)

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Bit	Symbol	R/W	Description	Init
7:4	AVDD2_SEQ	R/W	AVDD2 sequence set 4'b0000: disable sequence mode; 4'bx001: set the AVDD2 slot is 1; 4'bx010: set the AVDD2 slot is 2; 4'bx011: set the AVDD2 slot is 3; 4'bx100: set the AVDD2 slot is 4; 4'bx101: set the AVDD2 slot is 5; 4'bx110: set the AVDD2 slot is 6; 4'bx111: set the AVDD2 slot is 7;	0x00
3:0	AVDD1_SEQ	R/W	AVDD1 sequence set 4'b0000: disable sequence mode; 4'bx001: set the AVDD1 slot is 1; 4'bx010: set the AVDD1 slot is 2; 4'bx011: set the AVDD1 slot is 3; 4'bx100: set the AVDD1 slot is 4; 4'bx101: set the AVDD1 slot is 5; 4'bx110: set the AVDD1 slot is 6; 4'bx111: set the AVDD1 slot is 7;	0x00

AVDD_SEQ: AVDD Sequence Control Register (Address 0x0E)

Bit	Symbol	R/W	Description	Init
7:4	REV	R/W	Reserved	0x00
3:0	AVDD3_SEQ	R/W	AVDD3 sequence set 4'b0000: disable sequence mode; 4'bx001: set the AVDD3 slot is 1; 4'bx010: set the AVDD3 slot is 2; 4'bx011: set the AVDD3 slot is 3; 4'bx100: set the AVDD3 slot is 4; 4'bx101: set the AVDD3 slot is 5; 4'bx110: set the AVDD3 slot is 6; 4'bx111: set the AVDD3 slot is 7;	0x00

ENCR: Individual Enable Control Register (Address 0x0F)

Bit	Symbol	R/W	Description	Init
7:5	REV	R/W	Reserved	0x00
4	AVDD3_EN	R/W	AVDD3 enable control: 0: disable AVDD3 output when EN pin is High 1: enable AVDD3 output when EN pin is High	0x00
3	AVDD2_EN	R/W	AVDD2 enable control: 0: disable AVDD2 output when EN pin is High 1: enable AVDD2 output when EN pin is High	0x00
2	AVDD1_EN	R/W	AVDD1 enable control: 0: disable AVDD1 output when EN pin is High 1: enable AVDD1 output when EN pin is High	0x00

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1	REV	R/W	Reserved	0x00
0	DVDD1_EN	R/W	DVDD1 enable control: 0: disable DVDD1 output when EN pin is High 1: enable DVDD1 output when EN pin is High	0x00

SEQCR: Sequence Control Register (Address 0x10)

Bit	Symbol	R/W	Description	Init
7:6	SEQ_SPEED	R/W	the seq_count increment period in sequence mode 2'b00: 2000μs 2'b01: 1000μs 2'b10: 500μs 2'b11: 250μs	0x00
5:4	SEQ_CTRL	R/W	sequence control when the AVDD /DVDDD slot isn't 0 2'bx0: power down 2'bx1: power up	0x00
3	SEQ_ON	R/W	the indication of sequence activation 0: power down 1: power up	0x00
2:0	SEQ_COUNT	R/W	the indication of seq_count 3'b000: No LDO active 3'b001: slot 1 active 3'b010: slot 2 active 3'b011: slot 3 active 3'b100: slot 4 active 3'b101: slot 5 active 3'b110: slot 6 active 3'b111: slot 7 active	0x00

FLT_STATUS1: (Address 0x11)

Bit	Symbol	R/W	Description	Init
7	OT_SHUTDOWN_ST	R	system over temperature shutdown status: 0: system temperature not over 155℃; 1: system temperature over 155℃;	0x00
6	OT_WAR_ST	R	system over temperature warning status: 0: system temperature not over 115℃; 1: system temperature over 115℃;	0x00
5:3	REV	R	Reserved	0x00
2	DVDD1_SCP_ST	R	DVDD1 output short circuit protect status: 0: not in scp; 1: in scp;	0x00
1	REV	R	Reserved	0x00
0	DVDD1_OCP_ST	R	DVDD1 output over current protect status: 0: not in ocp; 1: in ocp;	0x00

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FLT_STATUS2: (Address 0x12)

Bit	Symbol	R/W	Description	Init
7:6	REV	R	Reserved	0x00
5	AVDD3_SCP_ST	R	AVDD3 output short circuit protect status: 0: not in scp; 1: in scp;	0x00
4	AVDD2_SCP_ST	R	AVDD2 output short circuit protect status: 0: not in scp; 1: in scp;	0x00
3	AVDD1_SCP_ST	R	AVDD1 output short circuit protect status: 0: not in scp; 1: in scp;	0x00
2	AVDD3_OCP_ST	R	AVDD3 output over current protect status: 0: not in ocp; 1: in ocp;	0x00
1	AVDD2_OCP_ST	R	AVDD2 output over current protect status: 0: not in ocp; 1: in ocp;	0x00
0	AVDD1_OCP_ST	R	AVDD1 output over current protect status: 0: not in ocp; 1: in ocp;	0x00

FLT_FLAG1: (Address 0x15)

Bit	Symbol	R/W	Description	Init
7	OT_SHUTDOWN_FLAG	W/C	system over temperature shutdown flag: 0: no happen; 1: happened;	0x00
6	OT_WAR_FLAG	W/C	system over temperature warning flag: 0: no happen; 1: happened;	0x00
5:3	REV	W/C	Reserved	0x00
2	DVDD1_SCP_FLAG	W/C	DVDD1 output short circuit protect flag: 0: no happen; 1: happened;	0x00
1	REV	W/C	Reserved	0x00
0	DVDD1_OCP_FLAG	W/C	DVDD1 output over current protect flag: 0: no happen; 1: happened;	0x00

FLT_FLAG2: (Address 0x16)

Bit	Symbol	R/W	Description	Init
7:6	REV	W/C	Reserved	0x00
5	AVDD3_SCP_FLAG	W/C	AVDD3 output short circuit protect flag: 0: no happen; 1: happened;	0x00

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Bit	Symbol	R/W	Description	Init
4	AVDD2_SCP_FLAG	W/C	AVDD2 output short circuit protect flag: 0: no happen; 1: happened;	0x00
3	AVDD1_SCP_FLAG	W/C	AVDD1 output short circuit protect flag: 0: no happen; 1: happened;	0x00
2	AVDD3_OCP_FLAG	W/C	AVDD3 output over current protect flag: 0: no happen; 1: happened;	0x00
1	AVDD2_OCP_FLAG	W/C	AVDD2 output over current protect flag: 0: no happen; 1: happened;	0x00
0	AVDD1_OCP_FLAG	W/C	AVDD1 output over current protect flag: 0: no happen; 1: happened;	0x00

CTR_MD: (Address 0x17)

Bit	Symbol	R/W	Description	Init
7:1	REV	R/W	Reserved	0x00
0	HICCUP_EN	R/W	HICCUP mode enable: 0: disable hiccup mode: if det ocp, LDO output current is clamped, output voltage drops. 1: enable hiccup mode: detect ocp_st, and deglitch 1ms; if det ocp, trigger LDO ocp flag=1, ldo off 20ms, then enable LDO and detect again.	0x01

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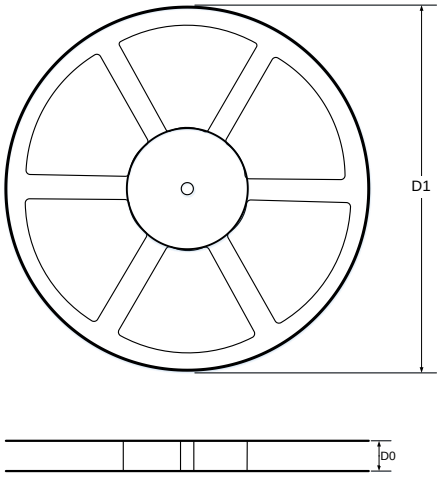
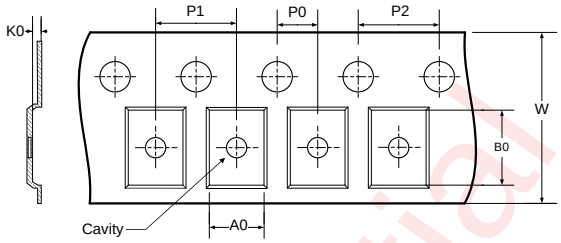
Tape And Reel Information

REEL DIMENSIONS

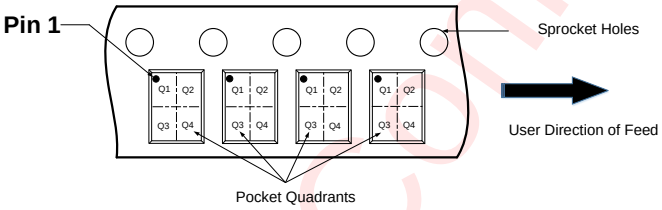


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TBD	TBD	TBD	TBD	TBD	2.00	4.00	4.00	8.00	Q1

All dimensions are nominal

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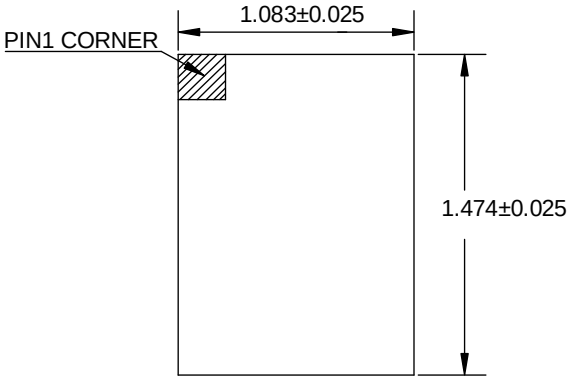
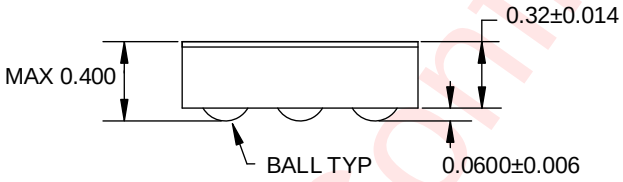
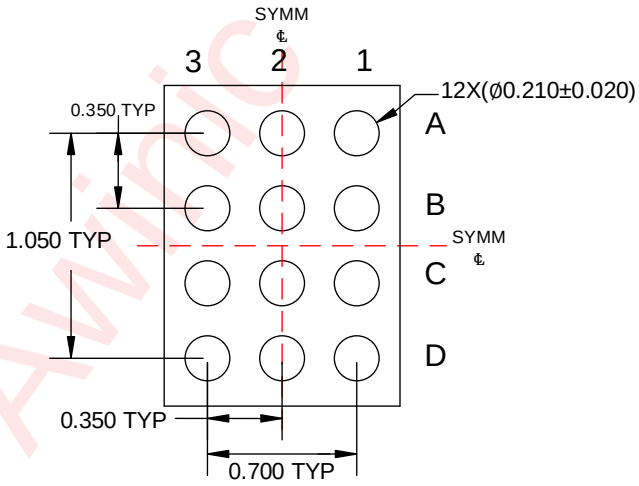
Package Description



Top View



Side View



Bottom View Unit: mm

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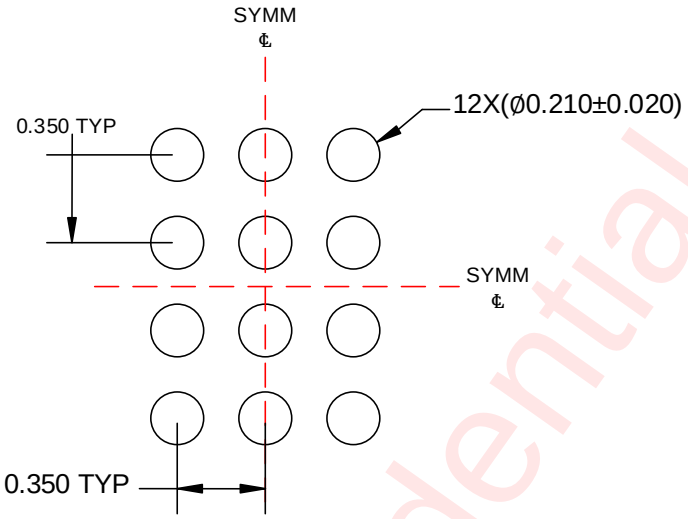
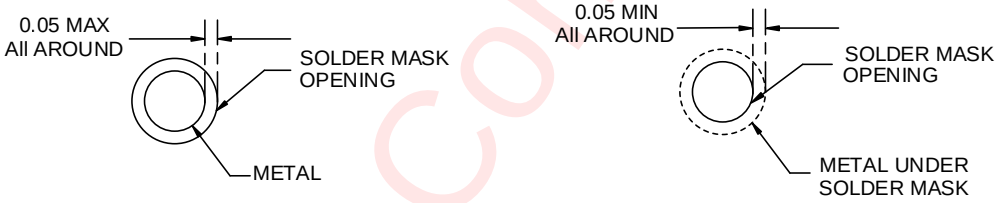
Land Pattern Data





NON-SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit: mm

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Revision History

Version	Date	Change record
V1.0	Mar. 2025	Officially released
V1.1	Jun. 2025	Update Detailed Functional Description
V1.2	Jul. 2025	Add Minimum and Maximum of UVLO,VIH and VIL; Update dropout voltage of DVDD; Update table of I2C address.
V1.3	Aug. 2025	Update Electrical Characteristics

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