USB Type-C Configuration Channel Logic and Port Control

FEATURES

- USB Type-C Cable and Connector Specification Release 1.2 compatible
- Enable control: Active Low (ENB Pin)
- PIN or I²C control
- Mode configuration
  - Host Only – SRC (DFP)
  - Device Only – SNK (UFP)
  - Dual Role Port – DRP
- The DRP mode supports Try.SNK or Try.SRC
- Support different current model controls and identifications (USB Default, 1.5A and 3.0A)
- Configuration Channel (CC)
  - Attachment of USB Port Detection
  - Cable Orientation Detection
  - Role Detection
- Dead Battery Support (SNK mode support when no power applied)
- Accurate internal CC termination resistance and current source with high precision
- Low current consumption
- DC 28V tolerance on VBUS, CC1 and CC2,
- Power supply range: 2.7V~5.5V
- QFN 1.6mm × 1.6mm-12L package

APPLICATIONS

- Smart Phones
- Power Adapters
- Tablets
- Laptops

GENERAL DESCRIPTION

The AW35616 is a Type-C Configuration Channel (CC) Flippable Adapter chip with low power and high efficiency. The AW35616 supports channel identification of USB Type-C and auto detection of different power roles based on chip settings. This chip is compatible with USB Type-C Cable and Connector Specification Release 1.2 for varies of applications.

The AW35616 supports PIN mode and I²C mode through CTRL pin settings. SDA (INOUT1), SCL (INOUT2), INTB (OUT3) and ID pins are used to distinguish necessary functions in different control modes. The ROLE pin controls the Source (SRC) / Sink (SNK) / Dual Role Power (DRP) mode in PIN mode. The global enable signal comes from ENB pin with internal pull-up resistor for more feasibility.

The AW35616 can determine a connection or disconnection in different power modes. The CC logic block monitors the CC1 and CC2 pins voltage to determine whether a USB port has been attached. The CC logic detects the Type-C current mode (USB Default, 1.5 A or 3.0 A) in SNK mode. VBUS detection is implemented to determine a successful attachment in SNK and DRP modes.

The AW35616 operates over a wide supply range with low power consumption. The device is available in QFN 1.6mm × 1.6mm-12L package.

TYPICAL APPLICATION CIRCUIT

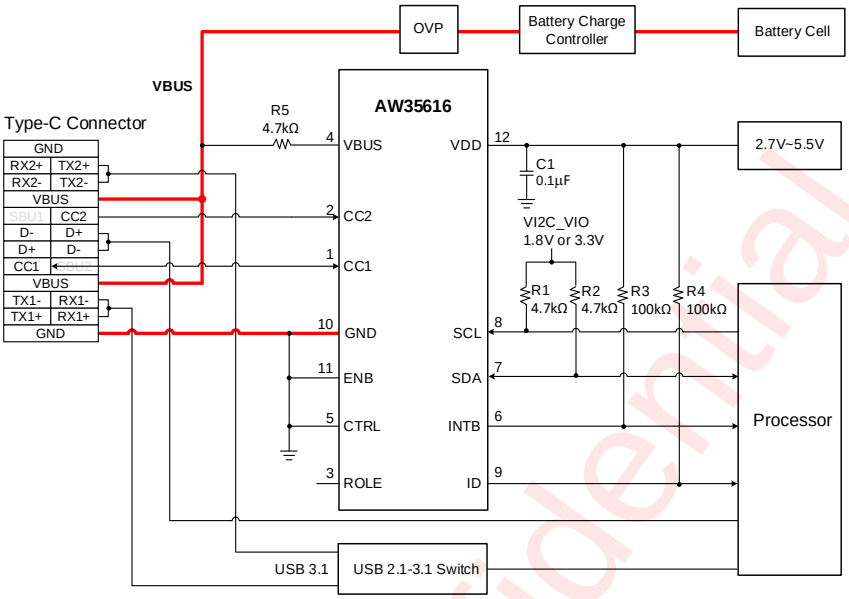


Figure 1 Typical Application Circuit of AW35616

PIN CONFIGURATION AND TOP MARK

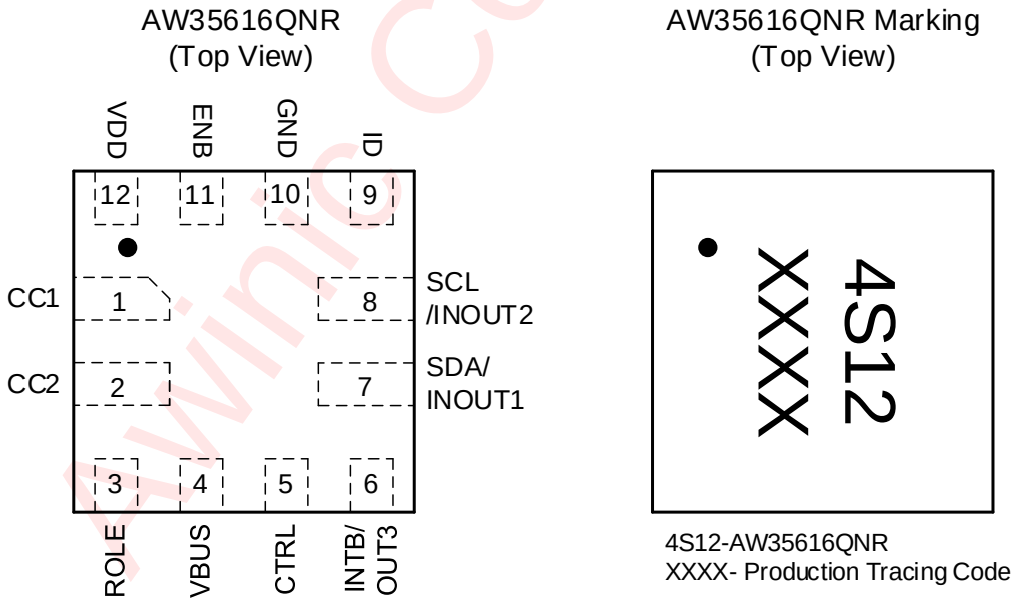


Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
1	CC1	Type-C Configuration Channel 1 with high DC tolerance, and start from SNK when power on.
2	CC2	Type-C Configuration Channel 2 with high DC tolerance, and start from SNK when power on.
3	ROLE	Tri-state input control signal for Type-C working mode selection in PIN mode. Floating: DRP; VDD: SRC; GND: SNK;
4	VBUS	VBUS detection and high voltage protection: DC 28V.
5	CTRL	Tri-state input control signal for PIN or I²C mode selection. Floating: PIN mode VDD: I²C mode with slave address 7'h68; GND: I²C mode with slave address 7'h60;
6	INTB/OUT3	Open drain output signal. INTB: Interruption output signal for I²C mode; OUT3: Audio Acc. connection indication in PIN mode; INTB/OUT3 output Low active.
7	SDA/INOUT1	in-output signal. I²C data in I²C mode; INOUT1 and INOUT2 combined to identify the charging current mode when a SRC is connected in PIN mode.
8	SCL/INOUT2	I²C clock input in I²C mode; INOUT1 and INOUT2 combined to identify the charging current mode when a SRC is connected in PIN mode. INOUT2 and INOUT1 in PIN mode indication: 2'b11: USB Default; 2'b10: 5V@1.5A; 2'b00: 5V@3.0 A; 2'b01: No connection;
9	ID	Open drain output signal for SRC or DRP operating as SRC. Output Low when detects CC channel is connected as SRC or DRP operating as SRC.
10	GND	Ground
11	ENB	Global enable signal. H: Power saving; L: Active;
12	VDD	Power, 2.7~5.5 V

FUNCTIONAL BLOCK DIAGRAM

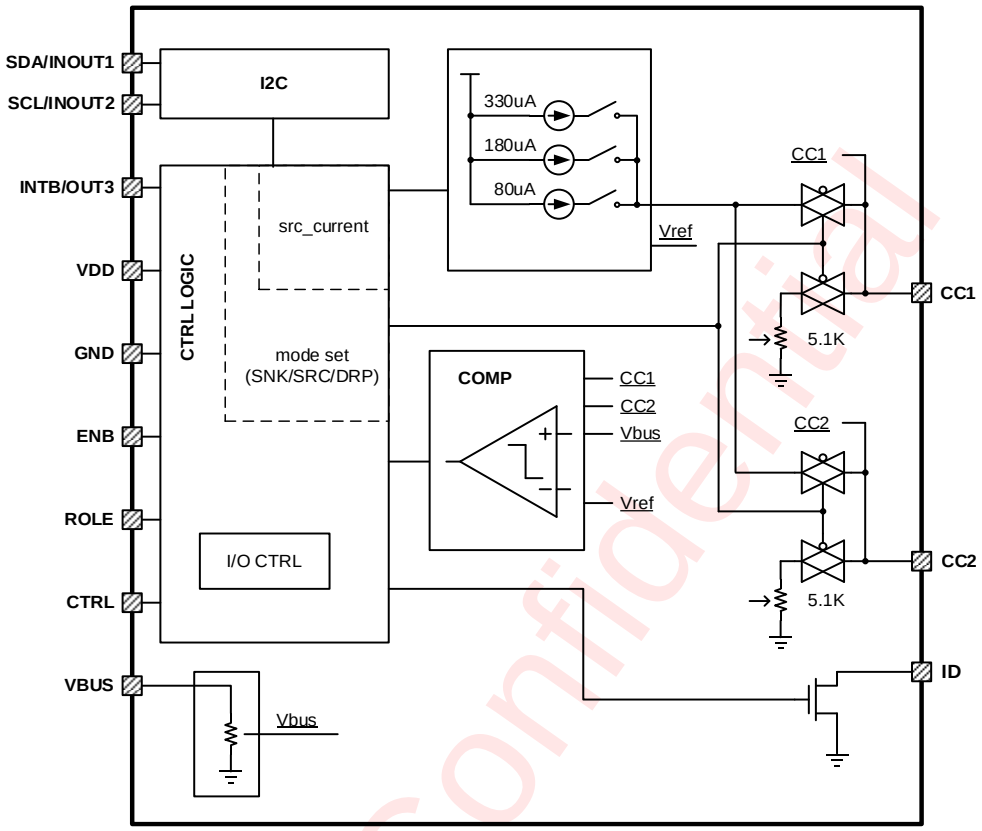


Figure 3 Functional Block Diagram

TYPICAL APPLICATION CIRCUIT

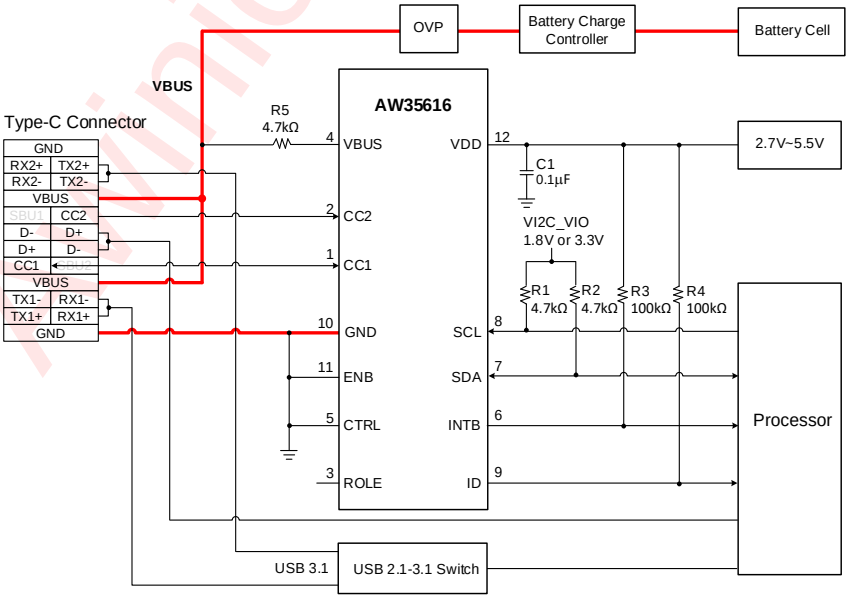


Figure 4 Functional Block Diagram

Notice for typical application circuits:

1: SCL/SDA/INTB is Open Drain output, so a 1K~10K pull-up resistance is needed for each pin.
2: Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground. So low-ESR, 0.1uF ceramic bypass capacitors are necessary between VDD and ground, placed close to the device, not far away from input trace.
3: The R5 is better for surge.
4. The traces of VBUS and GND should be designed wide enough for max charging current.

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW35616QNR	-40°C ~ 85°C	QFN 1.6mm × 1.6mm-12L	4S12	MSL1	RoHS+HF	4500 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS		RANGE
Supply voltage range	VDD	-0.3V to 6V
	VBUS	-0.3V to 28V
I/O voltage range	CC1, CC2	-0.3V to 28V
	SCL, SDA	-0.3V to 6V
	INTB	-0.3V to 6V
	ENB	-0.3V to 6V
Operating free-air temperature range		-40°C to 85°C
Maximum operating junction temperature T_{JMAX}		150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD(Including CDM HBM)		
HBM: ESDA/JEDEC JS-001(NOTE2)	VBUS, CC1, CC2	±4000V
	SCL, SDA, ENB, CTRL, ROLE, ID, INTB, VDD	±2000V
CDM: ESDA/JEDEC JS-002(NOTE3)		±1500V
Latch-Up		
Test condition: JESD78E		±200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: All pins. Test Condition: ESDA/JEDEC JS 001 2017.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS 002 2018.

RECOMMEND OPERATING CONDITIONS

PARAMETERS		MIN	TYP	MAX	UNIT
Supply voltage range	VDD	2.7	3.3	5.5	V
	VBUS	4.0	5.0	21.0	V
Operating temperature T_A		−40	−	85	°C

ELECTRICAL CHARACTERISTICS

V_{DD}=3.6V, T_A=25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{DD}	Power supply	-	2.7	-	5.5	V
V_{EN_L}	ENB pin Low voltage level	V_{DD}=3.6V	-	-	0.4	V
V_{EN_H}	ENB pin High voltage level	V_{DD}=3.6V	1.15	-	-	V
V_{ID_L}/V_{INTB_L}	ID/INTB pin Low voltage level open drain output	V_{DD}=3.6V I_{SNK}=-2mA	-	-	0.4	V
V_{IO3_th}	Tri-state input threshold	V_{DD}=3.6V	0.4	-	0.9×V_{DD}	V
$I_{DD\_disable}$	Power saving current	ENB=H	-	-	1	μA
I_{DD_active}	Active current	ENB=L In Unattached.SRC	-	60	90	μA
		ENB=L In Attached.SRC Deafult current mode	-	140	180	μA
		ENB=L In Unattached.SNK	-	60	90	uA
		ENB=L In Attached.SNK	-	60	90	μA
I_{DD_WAKE}	Wake mode current	ENB=L wkmd = 1'b11	-	35	65	μA
V_{IHI2C}	Logic threshold voltage	SCL/OUT2,SDA/OUT1	1.32	-	-	V
V_{ILI2C}		SCL/OUT2,SDA/OUT1	-	-	0.51	V
I_H	Current source	3.0A mode setting	304	330	356	μA
I_M		1.5A mode setting	166	180	194	μA
I_D		Default mode setting	64	80	96	μA
R_d	SNK pull-down resistor	VDD=3.6V	4.6	5.1	5.6	kΩ
$V_{th\_H\_SNK}$	SNK comparator threshold voltage	3.0A mode setting	1.16	1.23	1.31	V
$V_{th\_M\_SNK}$		1.5A mode setting	0.61	0.66	0.70	V
$V_{th\_D\_SNK}$		Default mode setting	0.15	0.2	0.25	V
$V_{th\_H\_SRC}$	SRC comparator threshold voltage	3.0A mode setting	2.45	2.6	2.74	V
$V_{th\_M\_SRC}$		1.5A mode setting	1.50	1.6	1.65	V
$V_{th\_D\_SRC}$		Default mode setting	1.50	1.6	1.65	V
V_{th_VBUS}	VBUS detection threshold voltage	V_{DD}=3.6V	2.8	3.3	3.8	V

DETAILED FUNCTIONAL DESCRIPTION

GENERAL DESCRIPTION

The AW35616 is a Type-C Configuration Channel Flippable Adapter chip with low power and high efficiency. The AW35616 supports channel identification of USB Type-C connector and auto detection of different power roles based on chip settings. It has high voltage protection circuits on CC1/CC2/VBUS pins. The VBUS, CC1 and CC2 support DC up to 28V. This chip is compatible with USB Type-C Cable and Connector Specification Release 1.2 for varies of applications.

LOGIC CONTROL BLOCK

The logic control block detects CC connection status using voltage level comparisons of CC pins for different connection topologies and settings. Comparison results showing CC signals voltage range are sent to logic control block for state machine and then the connection status of related working mode will be identified. When connection status changes. the logic control block will update outputs of pins and registers. Figure 5 shows the boundaries of SRC and SNK status.

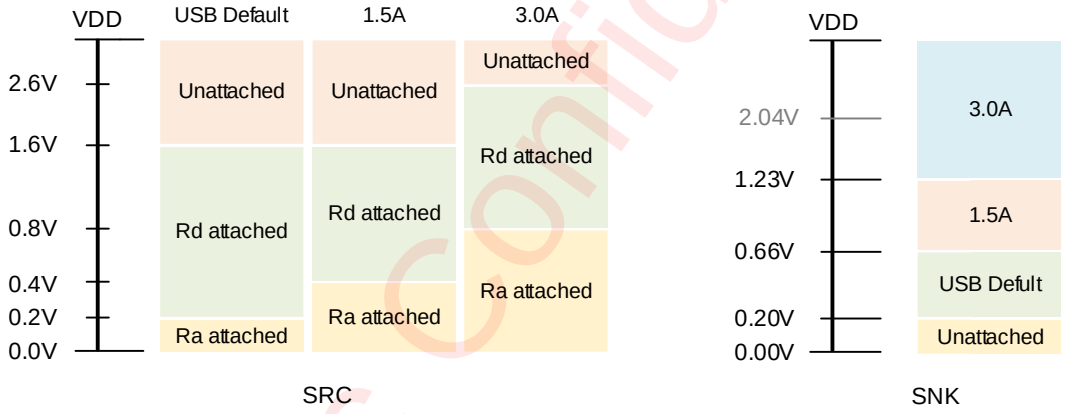


Figure 5 Threshold of Comparison and Status Relationship

In SNK mode, the AW35616 can detect a SRC connection, and can distinguish the terminate SRC current as threshold of SNK comparators (0.2V, 0.66V and 1.23V). The relationship between SNK comparators and detected results are shown in Figure 5. In SRC mode, the AW35616 supports three current level broadcasting in SRC mode, which is compatible with traditional current supply(USB Default, 1.5A and 3.0A). The AW35616 uses different comparators to detect attach status and distinguish Rd and Ra in different SRC modes. The relationship between SRC comparators and detected results are shown in Figure 5. In addition, the AW35616 supports the accessory mode which can distinguish the Audio/Debug attach. The AW35616 supports Try.SNK or Try.SRC function in DRP mode.

WORK MODE FEATURE

According to CC connection status and detection results, the chip can work as SRC (Host), SNK (Device) or DRP mode.

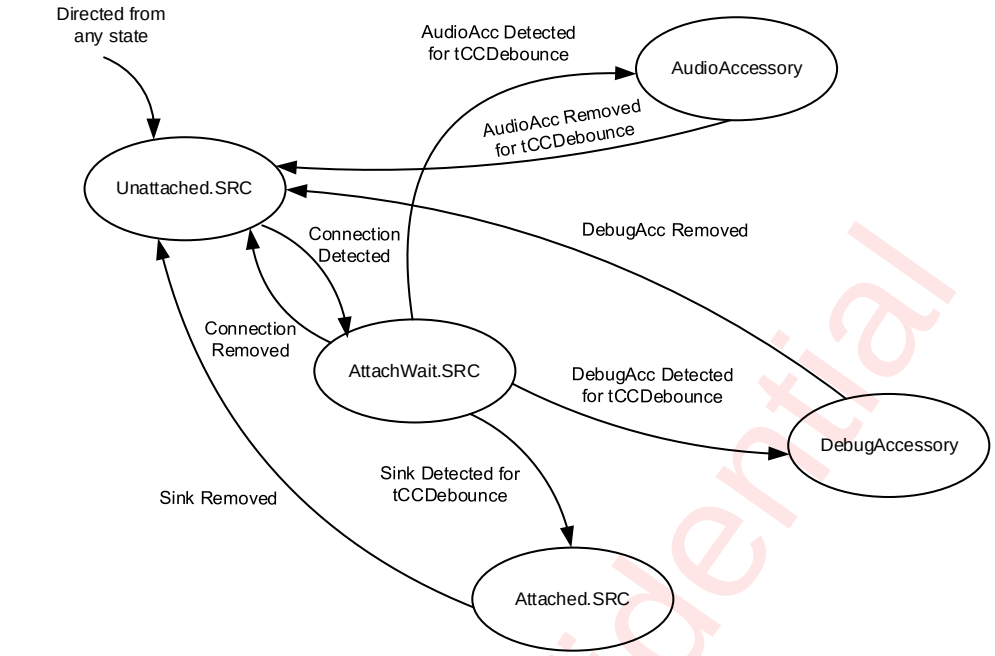


Figure 6 SRC State Diagram

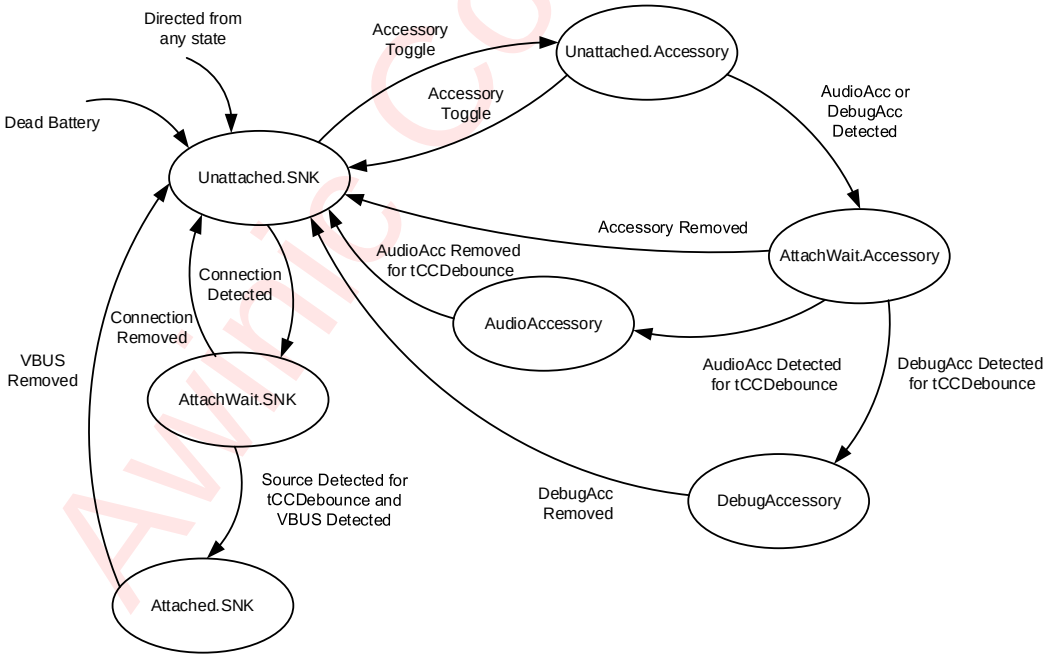


Figure 7 SNK with Accessory Support State Diagram

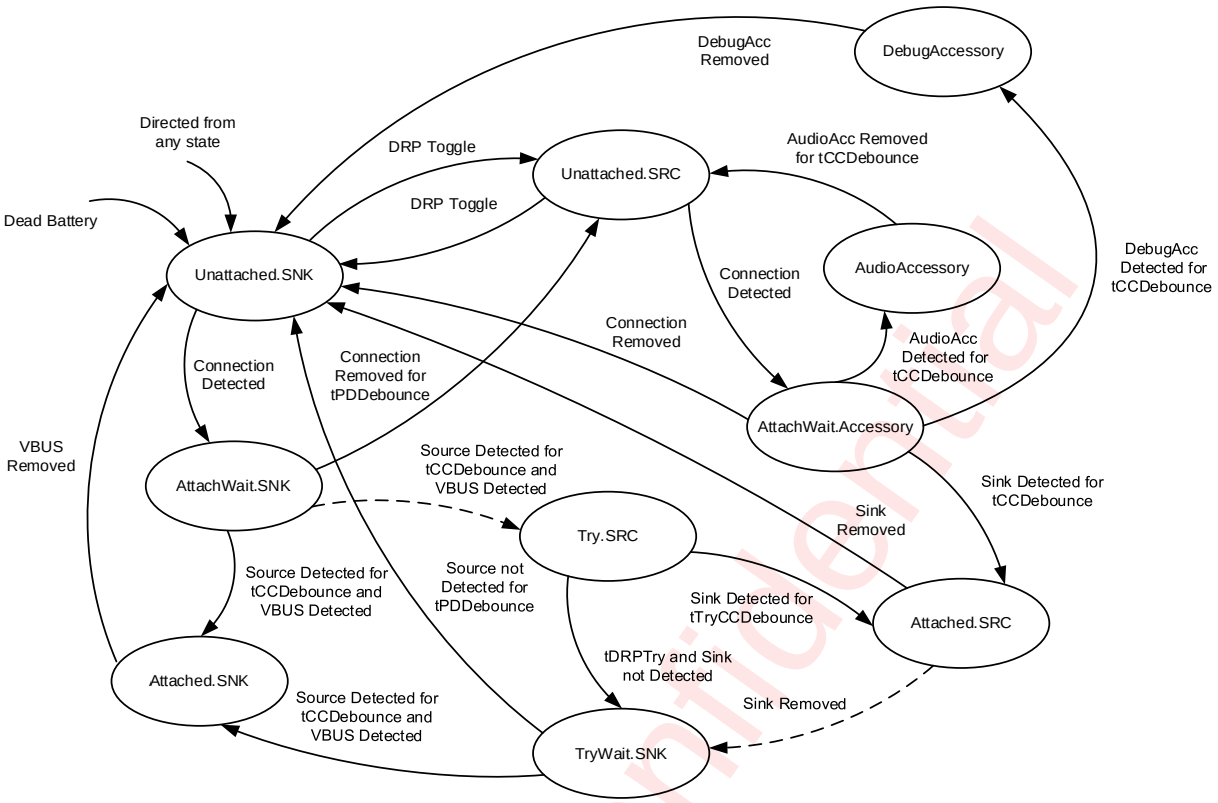


Figure 8 DRP with Accessory and Try.SRC Support State Diagram

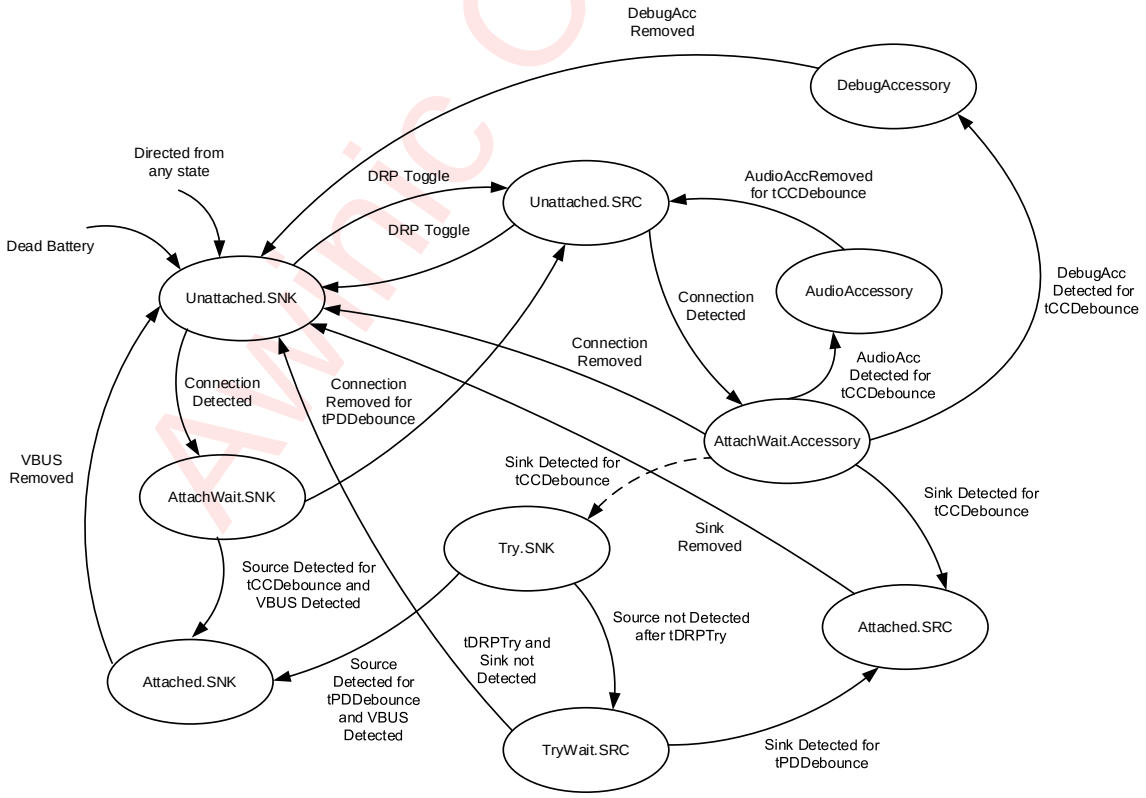


Figure 9 DRP with Accessory and Try.SNK Support State Diagram

DEAD BATTERY

The AW35616 supports the dead battery mode. When VDD is no power, the AW35616 enables Rd resistances on CC so that it can be distinguished and charging by connected SRC. Furthermore, the AW35616 can be distinguished by any source current level SRC in dead battery mode. The AW35616 will auto exit dead battery mode when VDD powered up.

GENERAL I²C OPERATION

The AW35616 supports the I²C protocol. The frequency supported by the I²C is 400 kHz. The pull-up resistor for the SDA and SCL can be selected from 1 to 10kΩ. Usually, 4.7kΩ is recommended for 400 kHz I²C. The voltage allowed for the I²C interface is 1.8 or 3.3V.

DEVICE ADDRESS

The I²C device address is 7-bit (A7~A1), followed by the bit R/W (A0). Set A0 to “0” for writing and “1” for reading. In addition, the CTRL pin is not floating (connected to VDD or GND). Two setting values would result in different I²C device address as show below table.

Addr	Pin Setting	A7	A6	A5	A4	A3	A2	A1	A0
Addr1	VDD	1	1	0	1	0	0	0	R/W
Addr2	GND	1	1	0	0	0	0	0	R/W

when the CTRL pin connects VDD, the I²C slave address is 7’h68;

when the CTRL pin connects GND, the I²C slave address is 7’h60;

I²C START/STOP

All transactions begin with a START and are terminated by a STOP sent by master to slave. A high-to-low transition on the SDA input/output while the SCL input is high defines a START condition. A low-to-high transition on the SDA input/output while the SCL input is high defines a STOP condition.

In particular, the bus stays busy when a repeated START (Sr) is generated instead of a STOP signal corresponding to the latest START (S). Sr and S are usually regarded as equivalent.

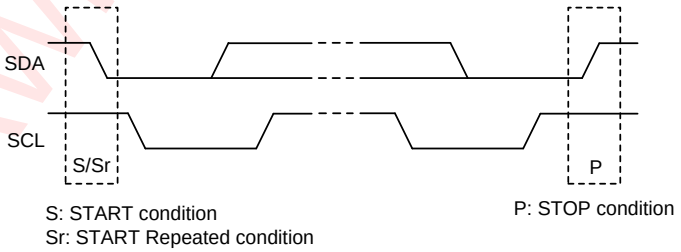


Figure 10 I²C START/STOP Condition Timing

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level. Each SCL pulse corresponds to one bit data transaction.

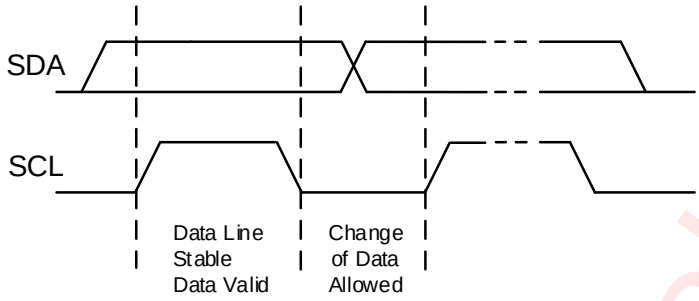


Figure 11 Data Validation Diagram

ACK (ACKNOWLEDGEMENT)

ACK means the successful transaction of I²C bus data. During writing cycle, after master sends 8-bit data, SDA must be released by master and SDA is pulled down to GND by slave chip when slave sends ACK.

During reading cycle, after slave chip sends 8-bit data, slave releases the SDA and waits for ACK from master. If master sends ACK, slave chip sends the next data. If master sends NACK, slave chip stops sending data and waits for I²C stop.

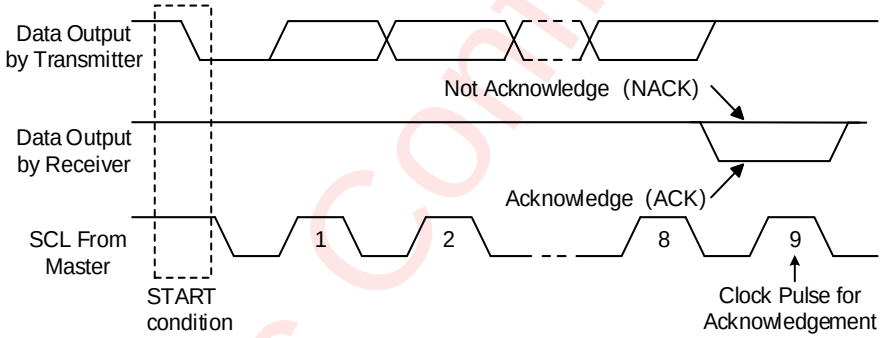


Figure 12 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line aborts the current transaction during the high state of the SCL. New data should be sent to SDA bus during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits and is transferred with the most significant bit first. After each byte, an ACK signal must follow.

In a write process, the following steps should be followed:

a) Master chip generates START condition. The "START" signal is generated by pulling down the SDA signal while the SCL signal is high.

b) Master chip sends slave address (7-bit) and the data direction bit R/W=0.

c) Slave chip sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit).

e) Slave sends acknowledge signal.

f) Master sends data byte to write to the addressed register.
g) Slave sends acknowledge signal.
h) Master generates STOP condition to indicate write cycle ends.

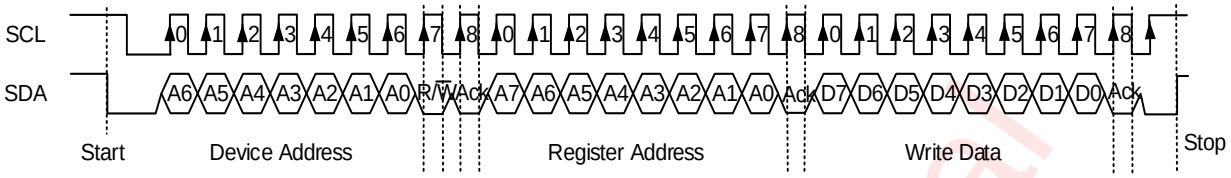


Figure 13 I²C Write Byte Cycle

READ CYCLE

In a read cycle, the following steps should be followed:

a) Master chip generates START condition
b) Master chip sends slave address (7-bit) and the data direction bit (R/W = 0).
c) Slave chip sends acknowledge signal if the slave address is correct.
d) Master sends control register address (8-bit)
e) Slave sends acknowledge signal
f) Master generates STOP condition followed with STOP-START condition or REPEAT START condition
g) Master chip sends slave address (7-bit) and the data direction bit (R/W = 1).
h) Slave chip sends acknowledge signal if the slave address is correct.
i) Slave sends data byte from addressed register.
j) The master chip generates STOP condition, the read cycle ends.

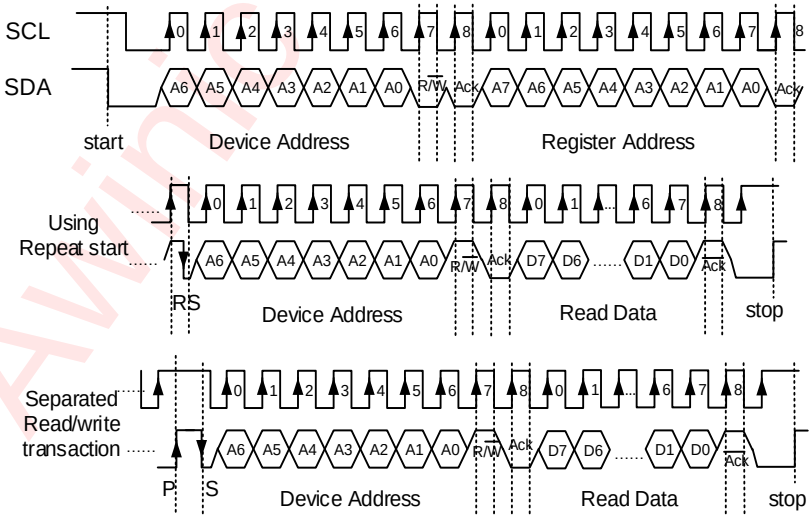


Figure 14 I²C Read Byte Cycle

I²C INTERFACE TIMING

PARAMETER		FAST MODE		FAST MODE PLUS		UNIT
		MIN	MAX	MIN	MAX	
F_{SCL}	Interface clock frequency	-	400	-	1000	kHz
$T_{HD:STA}$	(Repeat-start) START condition hold time	0.6	-	0.26	-	μs
T_{LOW}	Low level width of SCL	1.3	-	0.5	-	μs
T_{HIGH}	High level width of SCL	0.6	-	0.26	-	μs
$T_{SU:STA}$	(Repeat-start) START condition setup time	-	-	0.26	-	μs
$T_{HD:DAT}$	Data hold time	0	-	-	-	μs
$T_{SU:DAT}$	Data setup time	100	-	50	-	ns
T_R	Rising time of SDA and SCL	20	300	-	120	ns
T_F	Falling time of SDA and SCL	20*(VDD/5.5V)	300	20*(VDD/5.5V)	120	ns
$T_{SU:STO}$	STOP condition setup time	0.6	-	0.26	-	μs
T_{BUF}	Time between start and stop condition	1.3	-	0.5	-	μs

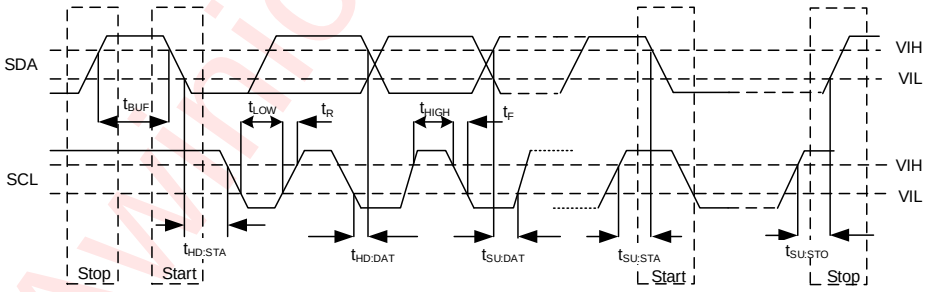


Figure 15 I²C Interface Timing

REGISTER CONFIGURATION

Register List

Name	ADDR	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def
DEV_ID	01h	R	VER_ID					VD_ID			16h
CTR	02h	R/W	ACCDIS	TRY_MD		SRC_CUR_MD		WKMD		INTDIS	24h
INT	03h	R/C						WAKE_FLAG	INTB_FLAG		00h
STATUS	04h	R	VBUSOK	SNK_CUR_MD		PLUG_ST			PLUG_ORI		00h
STATUS1	05h	R							WAKE_ST	ACTIVE_CABLE	00h
RSTN	06h	W/C							TYPEC_RSTN	SFT_RSTN	00h
USB_VID0	07h	R	USB_VID_LSB								4Fh
USB_VID1	08h	R	USB_VID_MSB								34h
CTR2	22h	R/W						TOG_SAVE_MD			00h

ATTENTIONS:

1. Do not use registers that are blank.
2. Values read from undefined register bits are not defined and invalid. Do not write to undefined registers.

Register Detailed Description

DEV_ID (Address: 01h)

Bit	Name	R/W	Description	Default
7:3	VER_ID	R	Chip version ID: 0 0010	0 0010
2:0	VD_ID	R	Chip Vendor ID: 110	110

CTR (Address: 02h)

Bit	Name	R/W	Description	Default
7	ACCDIS	R/W	Accessory disable support: 0: Support 1: Not Support	0
6:5	TRY_MD	R/W	Try SNK/SRC mode set: 01: Try.SNK 10: Try.SRC 00/11: No Try	01
4:3	SRC_CUR_MD	R/W	SRC current mode set: 00/11: USB Default 01: 1.5A 10: 3.0A	00

Bit	Name	R/W	Description	Default
2:1	WKMD	R/W	Power role mode control: 00: SNK 01: SRC 10: DRP 11: Wake mode	10
0	INTDIS	R/W	INTB function: 0: Enable INTB interrupt 1: Disable INTB interrupt	0

INT (Address: 03h)

Bit	Name	R/W	Description	Default
7:3	RESERVED	NA	RESERVED	0 0000
2	WAKE_FLAG	R/C	Wake flag in wake mode: 0: Nothing attached 1: Something attached	0
1:0	INTB_FLAG	R/C	Connect status interrupt: 00: No Interruption 01: Attached 10: Detached	00

STATUS (Address: 04h)

Bit	Name	R/W	Description	Default
7	VBUSOK	R	VBUS detection as SNK 0: VBUS not detected 1: VBUS detected	0
6:5	SNK_CUR_MD	R	Charging current detection as SNK: 00: Standby 01: USB Default 10: 1.5A 11: 3.0A	00

Bit	Name	R/W	Description	Default
4:2	PLUG_ST	R	Plugged port status: 000: Standby 001: SNK 010: SRC 011: Audio Accessory 100: Debug Accessory	000
1:0	PLUG_ORI	R	Plug orientation: 00: Standby 01: CC1 connected 10: CC2 connected 11: Both CC1 and CC2 connected	00

STATUS1 (Address: 05h)

Bit	Name	R/W	Description	Default
7:2	RESERVED	NA	RESERVED	00 0000
1	WAKE_ST	R	Indicate something attach in wake mode: 0: No attached 1: Attached	
0	ACTIVE_CABLE	R	Indicate the CC1 connected Rd/Ra, and the CC2 connected Ra/Rd: 0: No detect Rd Ra connection 1: detected Rd Ra connection	0

RSTN (Address: 06h)

Bit	Name	R/W	Description	Default
7:2	RESERVED	NA	RESERVED	00 0000
1	TYPEC_RSTN	W/C	Reset Type-C function: 0: No use 1: Enable reset, write clear itself	0
0	SFT_RSTN	W/C	Soft-ware reset: 0: No use 1: Enable reset, write clear itself	0

USB_VID0 (Address: 07h)

Bit	Name	R/W	Description	Default
7:0	USB_VID_LSB	R	Low byte of the unique vendor ID authorized by the USB IF: 0x344F	4Fh

USB_VID1 (Address: 08h)

Bit	Name	R/W	Description	Default
7:0	USB_VID_MSB	R	High byte of the unique vendor ID authorized by the USB IF: 0x344F	34h

CRT2 (Address: 22h)

Bit	Name	R/W	Description	Default
7:3	RESERVED	NA	RESERVED	0 0000
2:1	TOG_SAVE_MD	R/W	Disable pull-up and pull-down after a toggle cycle: 00: No disable function 01: 40 ms 10: 80 ms 11: 160 ms	00
0	RESERVED	NA	RESERVED	0

APPLICATION INFORMATION

PIN MODE OR I²C MODE CONTROL

The AW35616 supports PIN mode and I²C mode which controlled by CTRL pin. The following table shows the relationship between control mode and CTRL pin.

CTRL pin	Control mode
Floating	PIN mode
GND	I²C mode, and the slave address is 7'h60;
VDD	I²C mode, and the slave address is 7'h68;

TYPE-C MODE SETTING IN PIN MODE

In PIN mode, the Type-C work mode is controlled by ROLE pin. The AW35616 works as Try.SNK DRP when the ROLE pin is Floating, and works as SNK when ROLE pin is GND, and works as SRC when ROLE pin is VDD. In addition, the AW35616 supports Accessory function in PIN mode. The ROLE pin is not function in I²C mode.

The AW35616 is changed to the control mode, and it need re-enable the ENB pin to active the new mode;

The AW35616 is changed to the Type-C work mode in PIN mode, and it need re-enable the ENB pin to active the new work mode.

INDICATION IN PIN MODE

In PIN mode, the SCL, SDA, ID and INTB are used to indicate the result of Type-C detection. The following table shows the indication of Type-C detection.

Pin	Detection
INTB/OUT3	Audio detection: 1: Nothing attached; 0: Audio attached;
ID	SNK detection: 1: Nothing attached; 0: SNK attached;
SCL/INOUT2, SDA/INOUT1	SRC detection and the current indication: 2'b00: SRC attached, and source current is 5V@3A; 2'b01: Nothing attached; 2'b10: SRC attached, and source current is 5V@1.5A; 2'b11: SRC attached, and source current is USB Defualt;

Notes: The ID pin also indicates the SNK connection in I²C mode.

RECOMMENDED COMPONENTS LIST

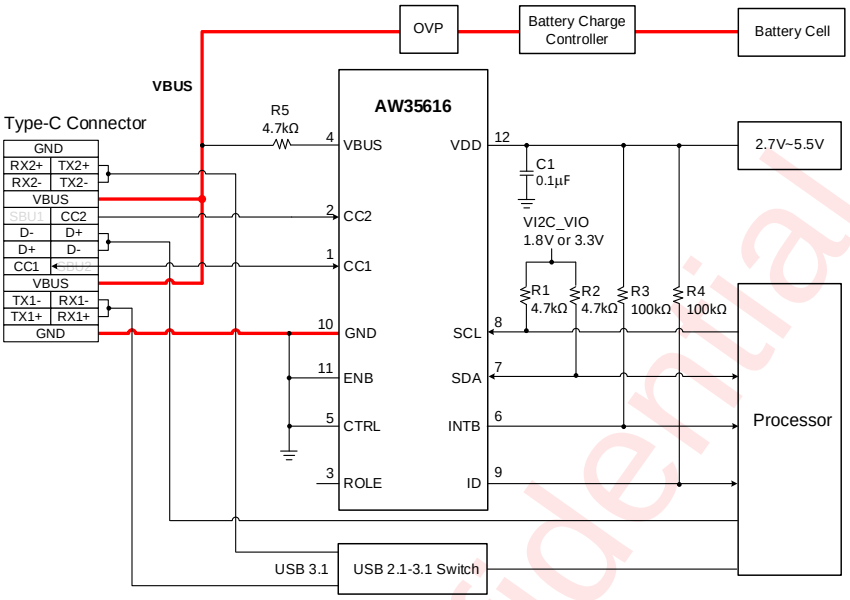
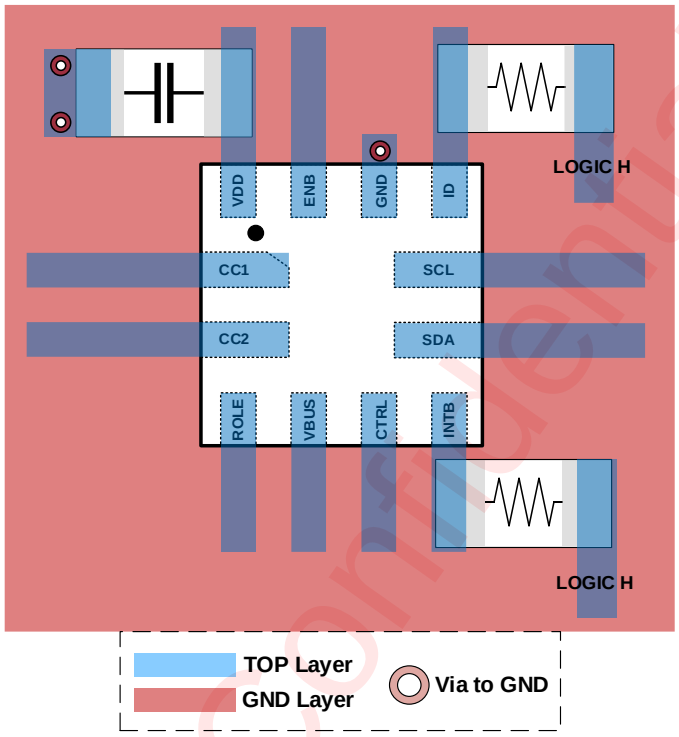


Figure 16 Application Circuit in I²C Control Mode

Symbol	Parameter	Recommended Value			Unit
		Min	Typ	Max	
C1	VDD decoupling capacitance	–	0.1	–	μF
R1	I²C SCL pull-up resistors	–	4.7	–	kΩ
R2	I²C SDA pull-up resistors	–	4.7	–	kΩ
R3	INTB pull-up resistor	-	100	–	kΩ
R4	ID pull-up resistor	-	100	-	kΩ
R5	Resistor for VBUS surge	-	4.7	-	kΩ

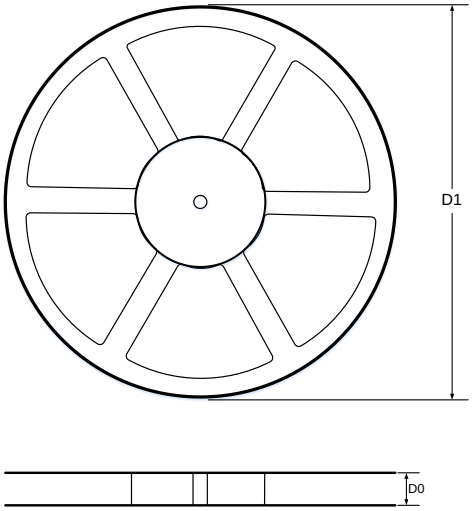
PCB LAYOUT CONSIDERATION

1. A 0.1 μF capacitor should be placed as close as possible to AW35616 VDD pin.
2. Both INTB pin and ID pin need an external $R_{pull-up}$ resistor to VDD.

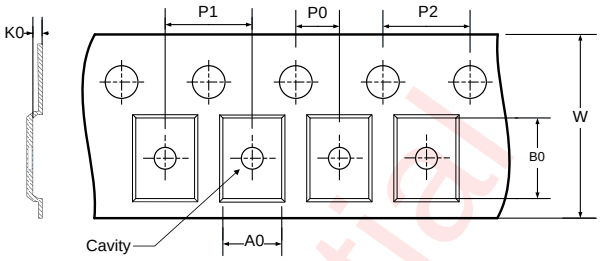


TAPE AND REEL INFORMATION

REEL DIMENSIONS

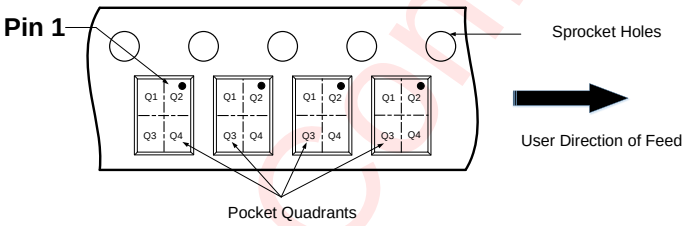


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



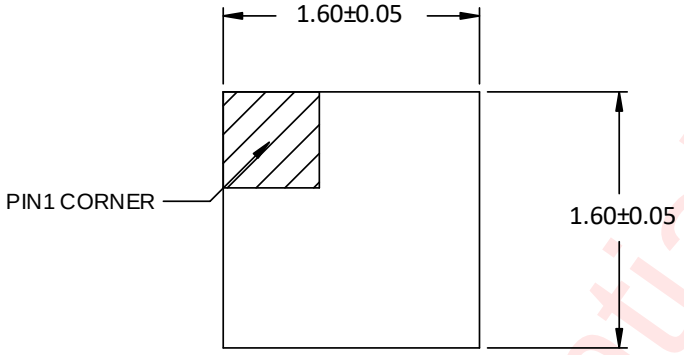
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

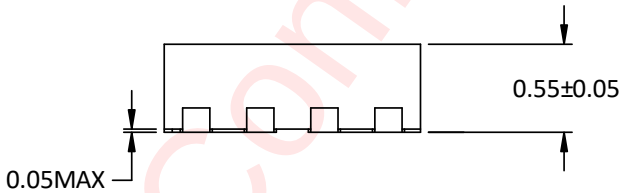
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.81	1.81	0.76	2	4	4	8	Q2

All dimensions are nominal

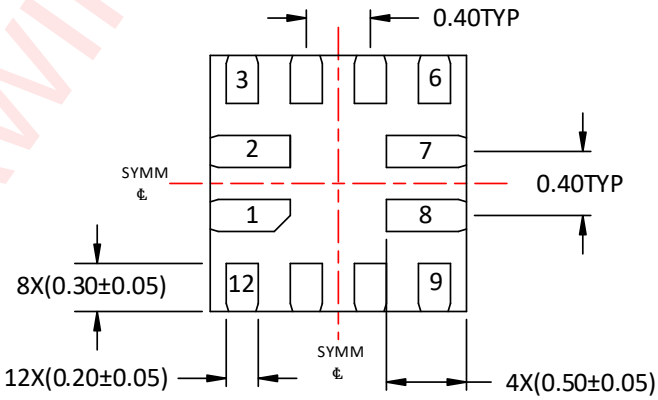
PACKAGE DESCRIPTION



Top View



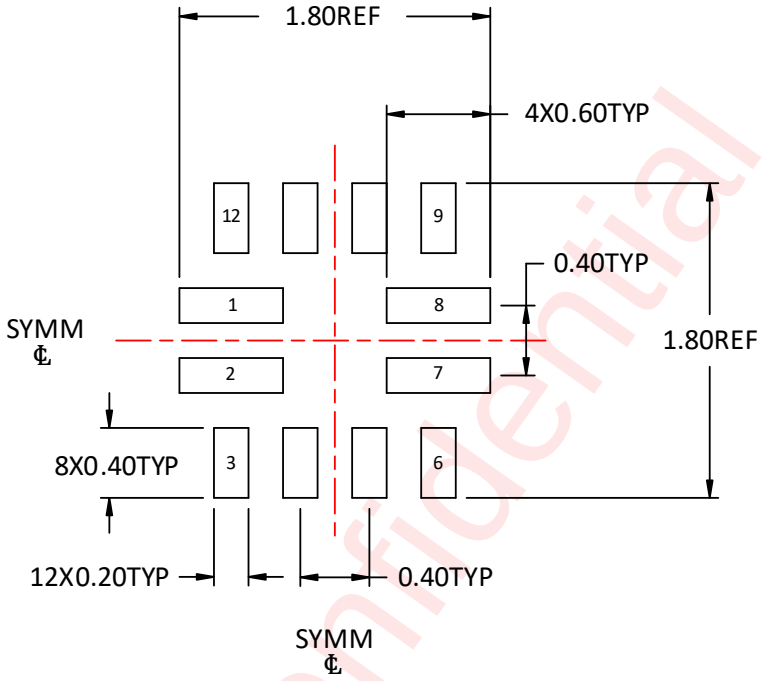
Side View

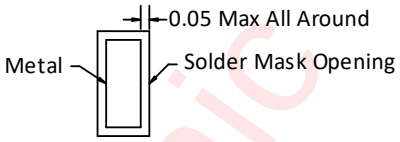


Bottom View

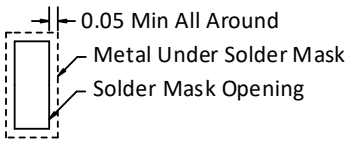
Unit:mm

LAND PATTERN DATA





Non-solder Mask Defined



Solder Mask Defined

Unit: mm

REVISION HISTORY

Version	Date	Change Record
V1.0	Apr. 2022	Officially released
V1.1	Dec. 2022	Update the HBM information -page 6 Update the CC voltage range from 24V to 28V -page 6 Update the description of active cable -page 17 Update the tape and reel information -page 22
V1.2	Jun. 2023	Modified CTR register bit 7 description
V1.3	Jun. 2024	Add Absolute Maximum Ratings of ENB -page 6

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