Low-Power, Microprocessor Supervisory Circuits

Features

- Operating Range: 1.0V to 5.5V
- Precision Supply Voltage Monitor :
  See device comparison
- Low Supply Current: 1.9μA (Typical)
- Guaranteed RESETN Valid at V_{CC} = 1V
- 200ms Reset Time Delay
- Debounced TTL/CMOS-Compatible :
  Manual-Reset Input
- Voltage Monitor for Power-Fail or Low-Battery Warning
- Dual Reset Outputs :
  Active-Low and Active-High
- -40°C to +125°C Operating Temperature Range
- Package :
  SOP-8L

Device comparison

AWS70708Y Z AAA

Package type
SPR:SOP-8

Reset time delay
A:0ms
B:55ms
C:200ms

Reset threshold
L:4.63V
M:4.4V
J:4.0V
T:3.08V
S:2.93V
R:2.63V
Z:2.32V
X:1.63V

Applications

Intelligent Instruments

Security equipment

Critical μP Power Monitoring

General Description

The AWS70708 microprocessor supervisory circuit reduces the complexity and number of components required to monitor power supply and monitor microprocessor activity. It significantly improves system reliability and accuracy compared to separate ICs or discrete components.

The AWS70708 provides power supply monitoring circuitry that generates a reset output during power-up, power-down and brownout conditions. The reset output remains operational with V_{CC} as low as 1V.

In addition, there is a 1.25V threshold detector for power-fail warning, low-battery detection, or monitoring an additional power supply. An active-low manual-reset input (MRB) is also included.

The AWS70708 available in Green SOP-8L package. It operates over an ambient temperature range of -40°C to +125°C.

Typical Application Circuit

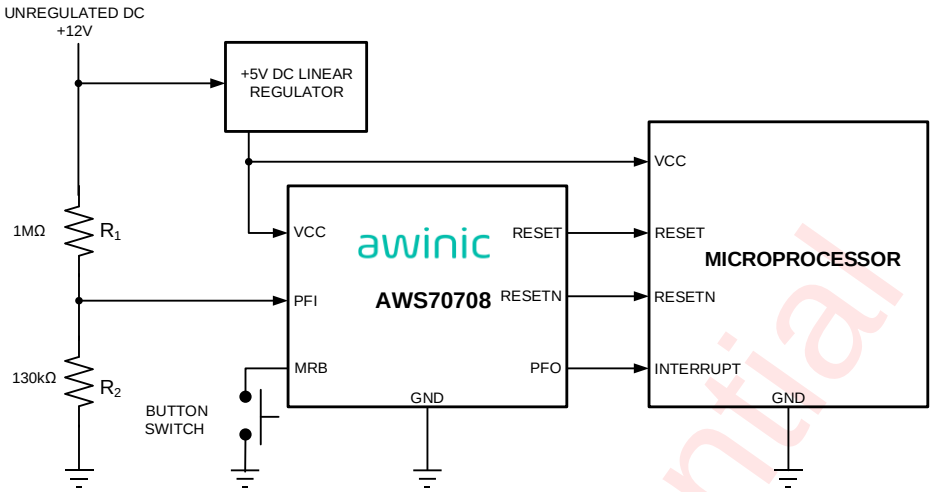
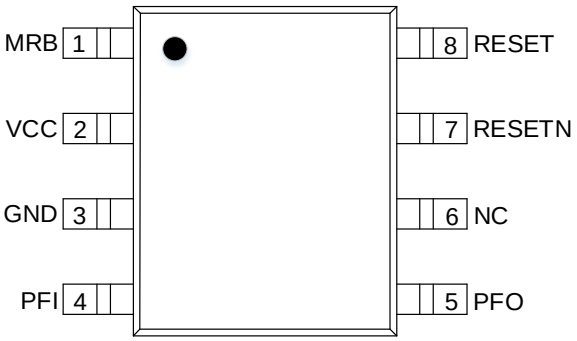


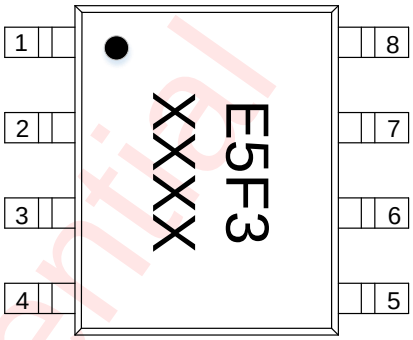
Figure 1 Typical Application Circuit of AWS70708

Pin Configuration And Top Mark

AWS70708MCSPR
（Top View）



AWS70708MCSPR Marking
（Top View）



E5F3 — AWS70708MCSPR
XXXX — Production Tracing Code

Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	MRB	Manual-Reset Input triggers a reset pulse when pulled below 0.8V. This active-low input has an internal 110kΩ pull-up resistance. It can be driven from a TTL or CMOS logic line as well as shorted to ground with a switch.
2	VCC	Power Supply Voltage that is monitored.
3	GND	Ground.
4	PFI	Power-Fail Voltage Monitor Input. When PFI is less than 1.25V, PFO goes low. **Connect PFI to GND or VCC when not used.**
5	PFO	Power-Fail Output goes low and sinks current when PFI is less than 1.25V; otherwise PFO stays high.
6	NC	No Connect.
7	RESETN	Active-Low Reset Output pulses low for 200ms when triggered, and stays low whenever V_{CC} is below the reset threshold. It remains low for 200ms after V_{CC} rises above the reset threshold or MRB goes from low to high.
8	RESET	Active-High Reset Output is the inverse of RESETN. Whenever RESETN is high, RESET is low, and vice versa.

Functional Block Diagram

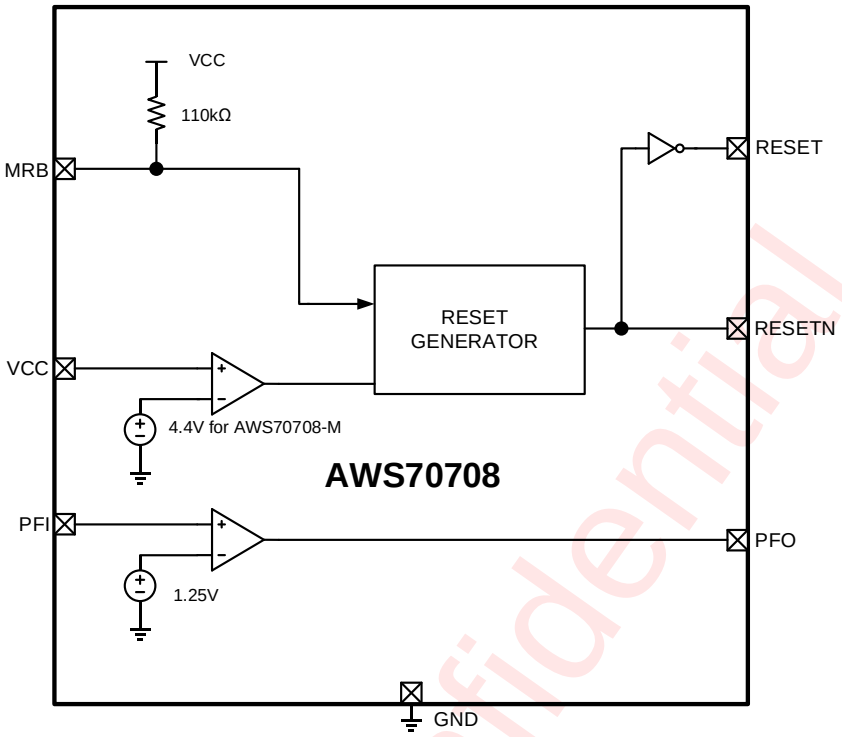


Figure 3 Functional Block

Typical Application Circuits

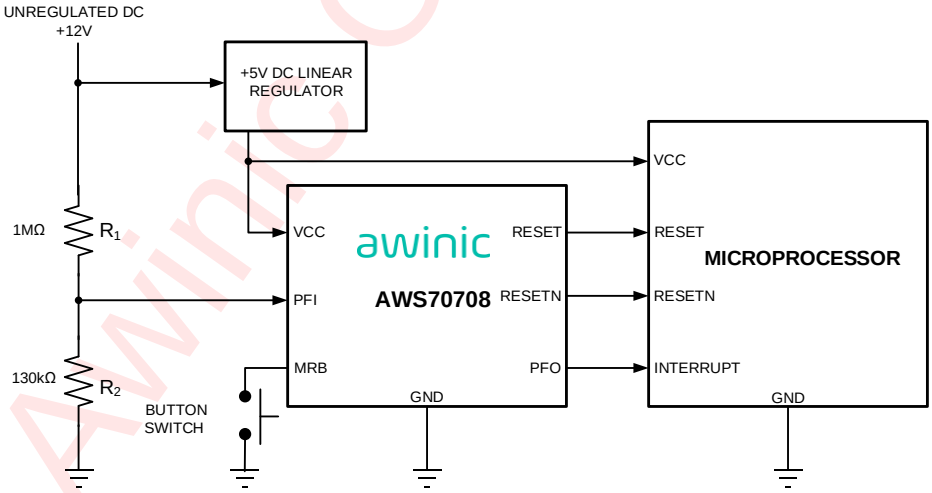


Figure 4 Typical Application Circuit of AWS70708

- ***Notice for typical application circuits:***

1. When the PFI and PFO pins function is not used, **connect PFI to GND or VCC** ,the PFO pins can be floating.
2. If PFI and PFO pin functions are used, it is recommended to use a resistance with a precision of 1% to improve the accuracy of the PFI configuration threshold.
3. If RESET and RESETN use only one of the two pins, the other pin can be floating.
4. If the MRB function is not applicable, the MRB can be floating.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWS70708MCSPR	-40°C～125°C	SOP-8L	E5F3	MSL3	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS	RANGE
Supply voltage range V_{CC}	-0.3V to 6.0V
V_{PFI}, V_{MRB}, V_{PFI}, V_{RESETN}, V_{RESET}, V_{PFO}	-0.3V to 6.0V
Operating free-air temperature range	-40°C to 125°C
Maximum operating junction temperature T_{JMAX}	150°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

ESD Rating and Latch Up

PARAMETERS	VALUE	UNIT
HBM (Human Body Model) (NOTE 2)	±4	kV
CDM(NOTE 3)	±2	kV
Latch-Up(NOTE 4)	+IT：200；-IT：-200	mA

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017

NOTE3: Test method: ESDA/JEDEC JS-002-2018

NOTE4: Test method: JEDEC78E

Electrical Characteristics

V_{CC}=1.0 to 5.5V, T_A=-40°C to +125°C, typical values are at V_{CC}=5V and T_A=25°C.(unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Basic Operation						
Operating Voltage Range (V_{CC})			1.0		5.5	V
Supply Current (I_{SUPPLY})		V_{CC}=5V		1.9		μA
Reset Threshold (V_{TH})						
AWS70708L		T_A = +25°C		4.63		V
AWS70708M		T_A = +25°C		4.4		V
AWS70708J		T_A = +25°C		4		V
AWS70708T		T_A = +25°C		3.08		V
AWS70708S		T_A = +25°C		2.93		V
AWS70708R		T_A = +25°C		2.63		V
AWS70708Z		T_A = +25°C		2.32		V
AWS70708X		T_A = +25°C		1.63		V
Threshold Voltage Accuracy ($\triangle V_{TH}$)		T_A = +25°C		±2.0		%
Reset Threshold Hysteresis		AWS70708T, AWS70708S, AWS70708R, AWS70708Z, AWS70708X		25		mV
		AWS70708J		35		
		AWS70708L, AWS70708M		40		
Timing Requirements						
t_{PD_HL}	Propagation delay from V_{CC} falling below V_{TH} to RESETN	V_{CC} = (V_{TH} +200mV) to (V_{TH} -200mV)		40		μs
t_D	Release time or reset active timeout period			200		ms
t_{MR}	MRB Pulse Width		500			ns
t_{MD}	MRB to RESET Out Delay			100		ns
RESETN/RESET Output Voltage						
RESETN Output Voltage		I_{SOURCE} = 800μA	0.7V_{CC}			V
		I_{SINK} = 3.2mA			0.4	
		V_{CC} = 1V, I_{SINK} = 50μA			0.3	
RESET Output Voltage		I_{SOURCE} = 800μA	0.7V_{CC}			V
		I_{SINK} = 1.2mA			0.4	
MRB Pull-Up Current		MRB = 0V, V_{CC} = 5V		45		μA
MRB Input Threshold		Low			0.3V_{CC}	V
		High	0.7V_{CC}			V
PFI Input Threshold		V_{CC} = 5V		1.25		V
PFI Input Current		V_{PFI} = 5V		0.2		nA
PFO Output Voltage		I_{SOURCE} = 800μA	0.7V_{CC}			V
		I_{SINK} = 3.2mA			0.4	

Typical Characteristics

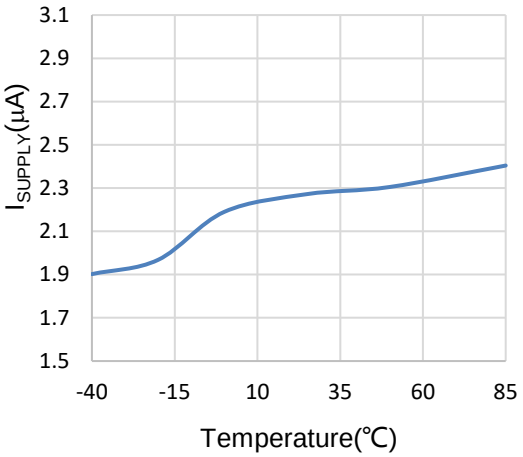


Figure 5 Supply Current vs. Temp.

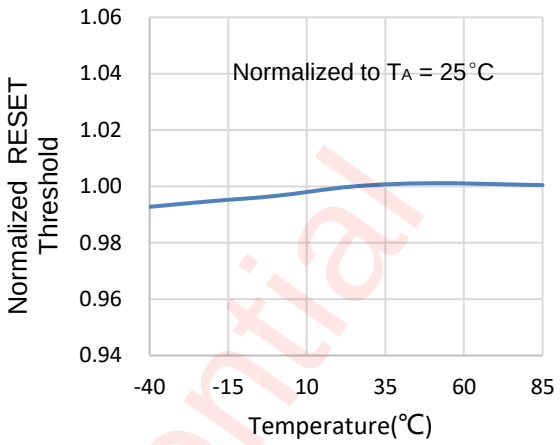


Figure 6 Normalized RESET Threshold vs. Temp.

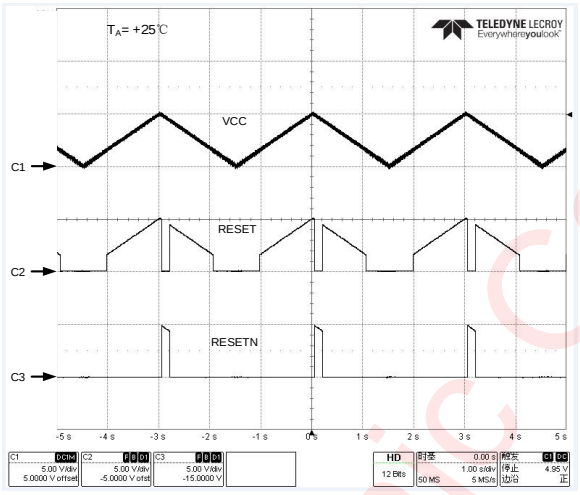


Figure 7 Output Voltage vs. Supply Voltage

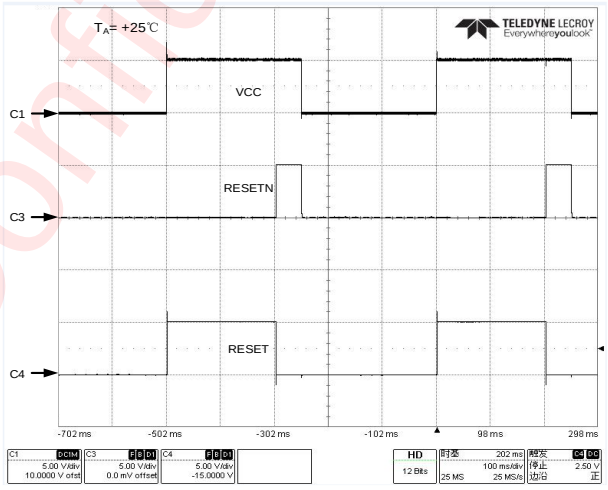


Figure 8 Output Voltage vs. Supply Voltage

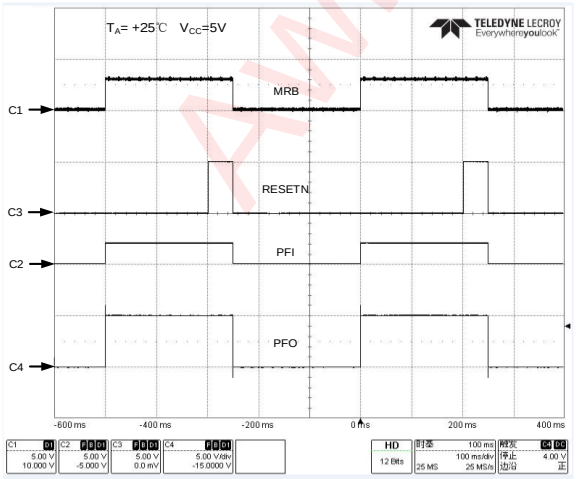


Figure 9 RESETN Output Voltage vs. MRB

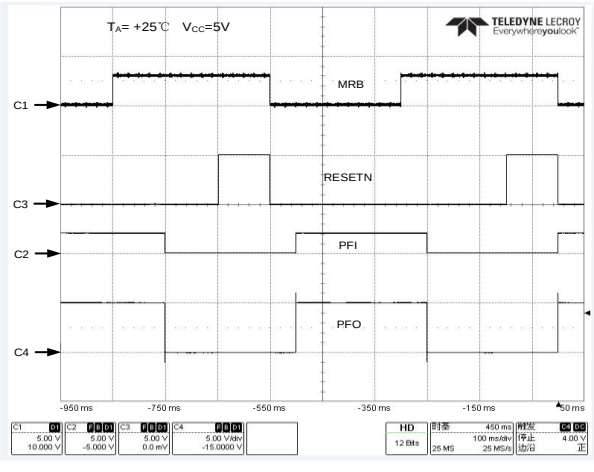


Figure 10 RESETN Output Voltage vs. MRB

Typical Characteristics (Continued)

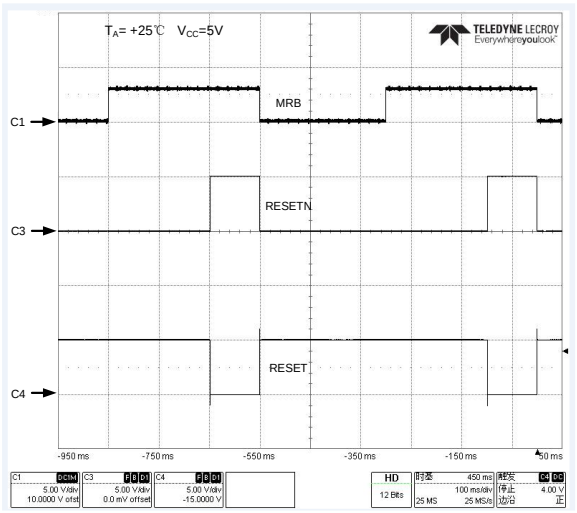


Figure 11 Output Voltage vs. MRB

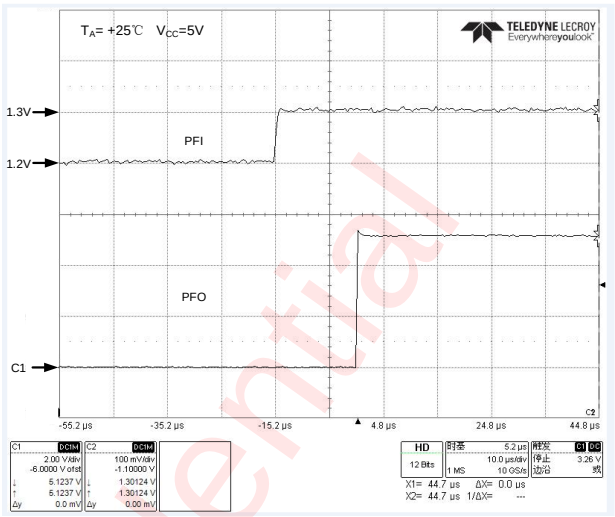


Figure 12 PFO vs. PFI rising

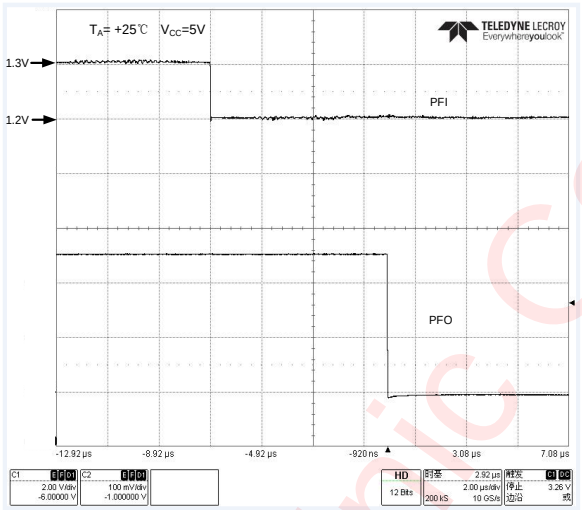


Figure 13 PFO vs. PFI Falling

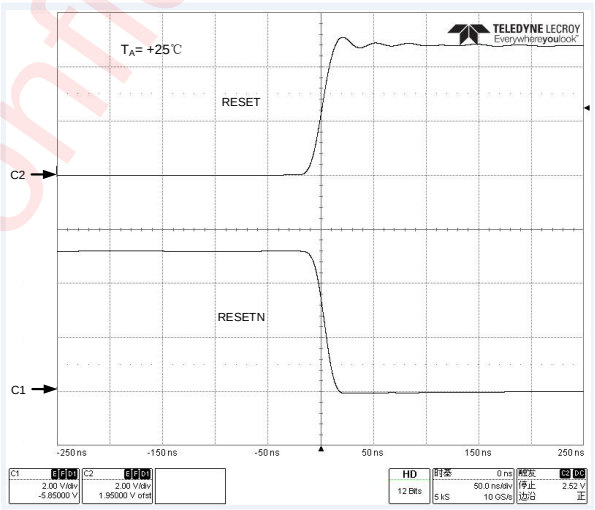


Figure 14 RESETN, RESET Assertion

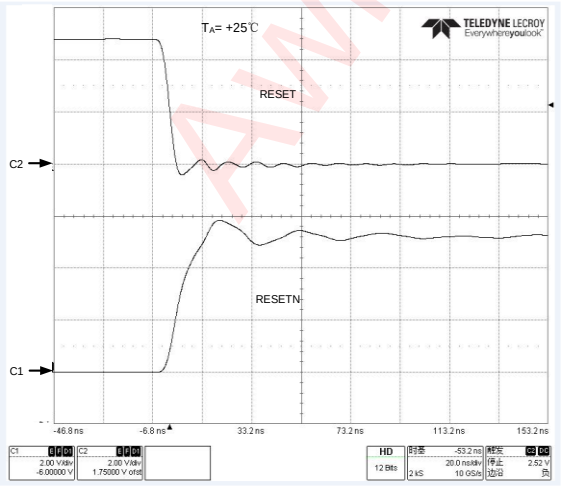


Figure 15 RESETN, RESET De-Assertion

Detailed Functional Description

Reset Output

A microprocessor's (μP's) reset input starts the μP in a known state. Whenever the μP is in an unknown state, it should be held in reset. The AWS70708 assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

On power-up, once V_{CC} reaches 1V, RESETN is a guaranteed logic low of 0.4V or less. As V_{CC} rises, RESETN stays low. When V_{CC} rises above the reset threshold, an internal timer releases RESETN after about 200ms. RESETN pulses low whenever V_{CC} dips below the reset threshold brownout condition. On power-down, once V_{CC} falls below the reset threshold, RESETN stays low and is guaranteed to be 0.4V or less until V_{CC} drops below 1V.

The AWS70708 active-high RESET output is simply the complement of the RESETN output, and is guaranteed to be valid with V_{CC} down to 1.6V.

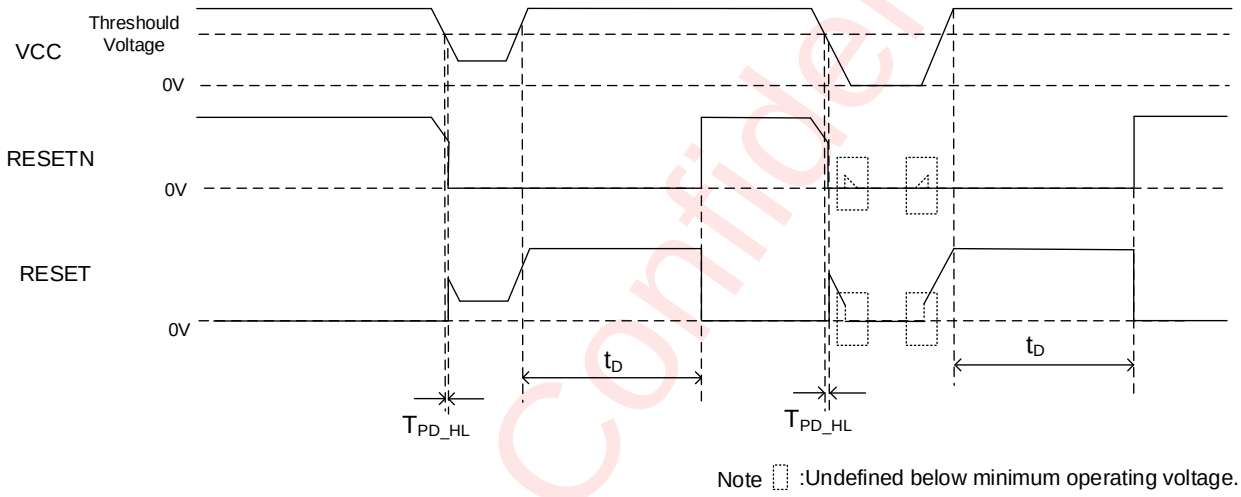


Figure 16 Reset Output Timing Diagram

Power-Fail

The power-fail comparator can be used for various purposes because its output and noninverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.

To build an early-warning circuit for power failure, connect the PFI pin to a voltage divider (see Typical Operating Circuit). Choose the voltage divider ratio so that the voltage at PFI falls below 1.25V just before the +5V regulator drops out. Use PFO to interrupt the μP so it can prepare for an orderly power-down.

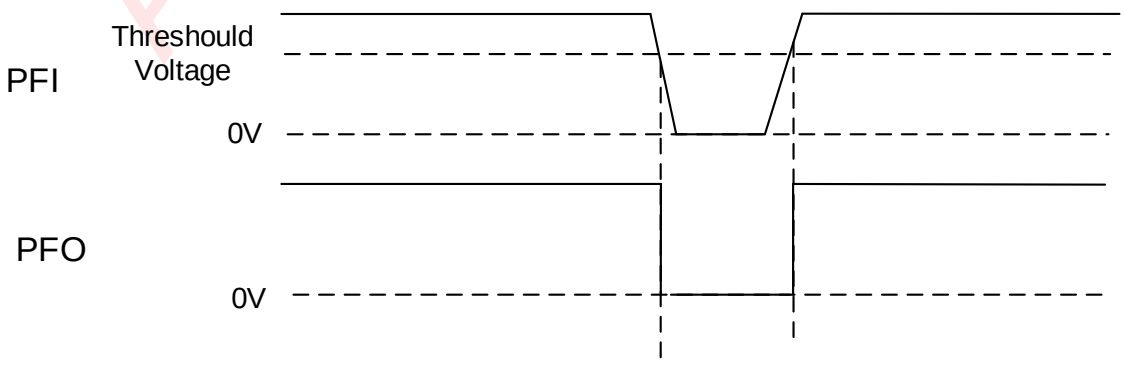


Figure 17 Power-Fail Timing Diagram

Manual-Reset

The manual-reset input (MRB) allows reset to be triggered by a pushbutton switch. MRB is TTL/CMOS-logic compatible, so it can be driven by an external logic line.

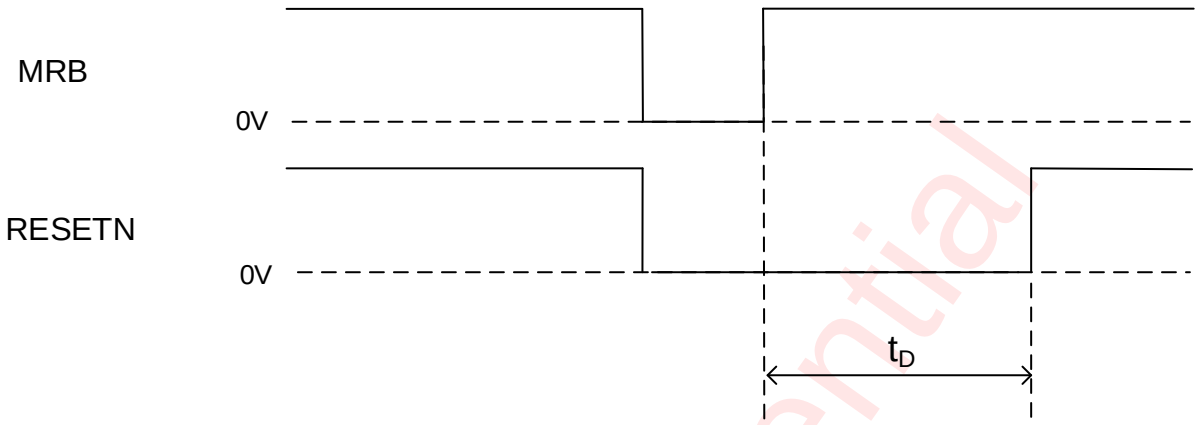


Figure 18 Manual-Reset Timing Diagram

Application Information

Ensuring a Valid RESETN Output Down to V_{CC} = 0V

When V_{CC} falls below 1V, the AWS70708 RESETN output no longer sinks current-it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pull-down resistor is added to the RESETN pin as shown in Figure 19, any stray charge or leakage currents will be drained to ground, holding RESETN low. Resistor value (R1) is not critical. It should be about 100kΩ, large enough not to load RESETN and small enough to pull RESETN to ground.

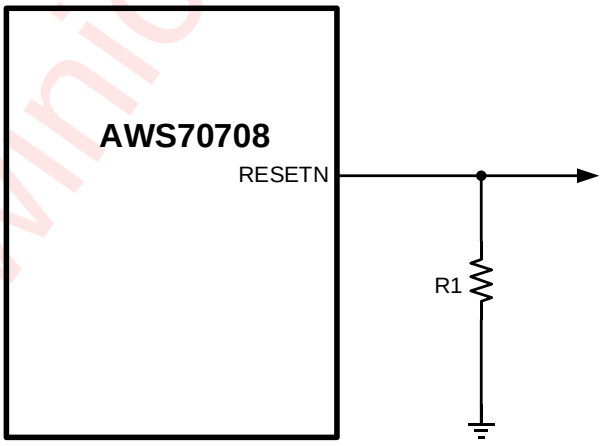


Figure 19 RESETN Valid to Ground Circuit

Monitoring Voltages Other Than the Unregulated DC Input

Monitor voltages other than the unregulated DC by connecting a voltage divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sum of the two resistors in the potential divider network) between PFI and PFO. A capacitor between PFI and GND will reduce the power-fail circuit's sensitivity to high-frequency noise on the line being monitored.

RESETN can be asserted on other voltages in addition to the +5V V_{CC} line. Connect PFO to MRB to initiate a RESETN pulse when PFI drops below 1.25V. Figure 20 shows the AWS70708 configured to assert RESETN when the +5V supply falls below the reset threshold, or when the +12V supply falls below approximately 11V.

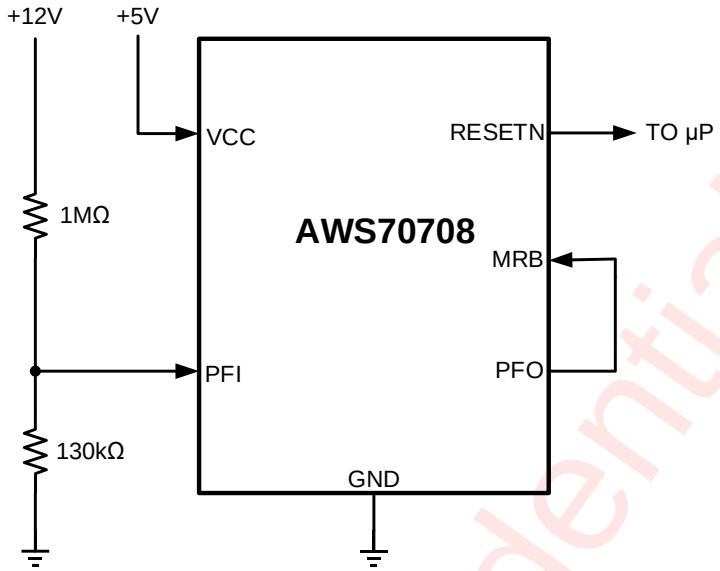
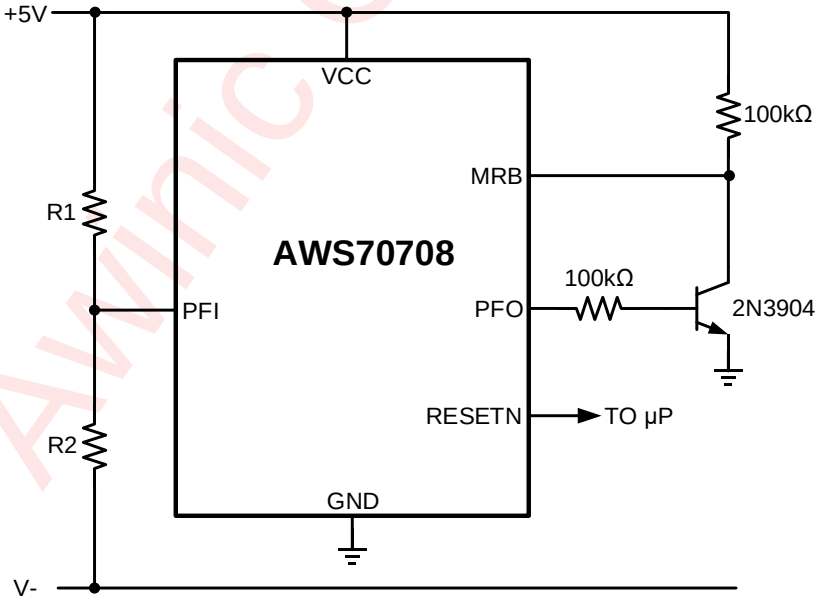


Figure 20 Monitoring Both +5V and +12V

Monitoring a Negative Voltage

The power-fail comparator can also monitor a negative supply rail (Figure 21). When the negative rail is good (a negative voltage of large magnitude), PFO is low, and when the negative rail is degraded (a negative voltage of lesser magnitude), PFO is high. By adding the resistors and transistor as shown, a high PFO triggers reset. As long as PFO remains high, the AWS70708 will keep reset asserted (RESETN = low, RESET = high). Note that this circuit's accuracy depends on the PFI threshold tolerance, the V_{CC} line, and the resistors.



$$\frac{5-1.25}{R1}=\frac{1.25-V\_}{R2} \qquad V\_<0$$

Figure 21 Monitoring a Negative Voltage

PCB Layout Consideration

AWS70708 PCB layout should be considered. Here are some guidelines:

1. If the Power-fail function is used, the R_1 and R_2 resistors are placed close to the chip, route PFI line on PCB as short as possible to reduce parasitic capacitance.
2. A patch or in-line switch can be placed at the pin of the MBR. Pay attention to the height of the device.

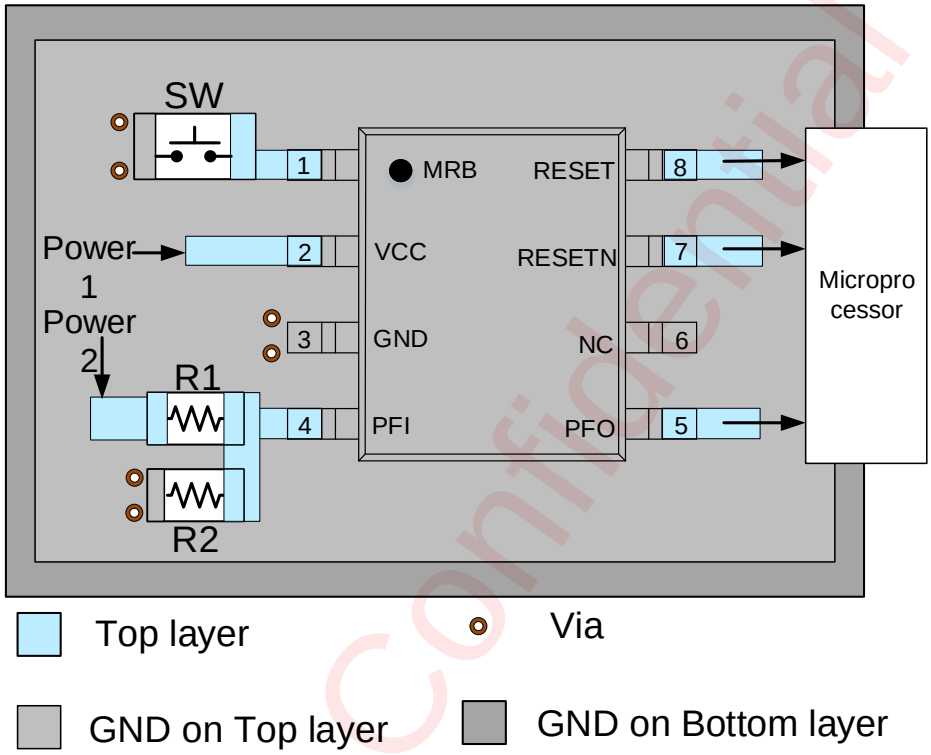
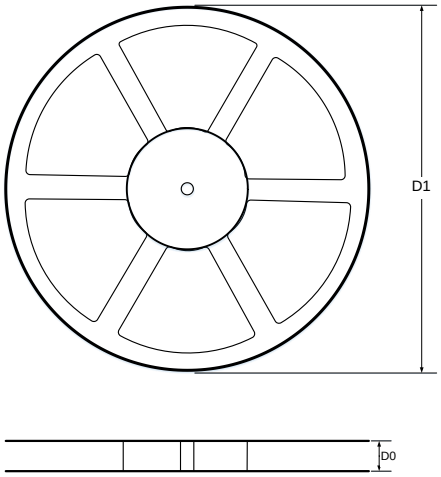


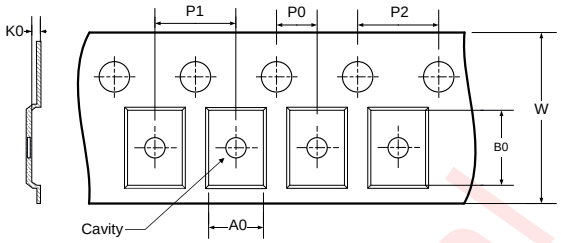
Figure 22 External Components Placements and PCB Layout Example

Tape And Reel Information

REEL DIMENSIONS

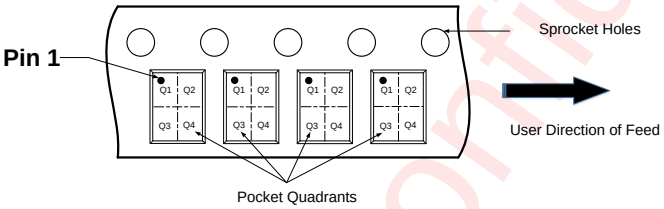


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



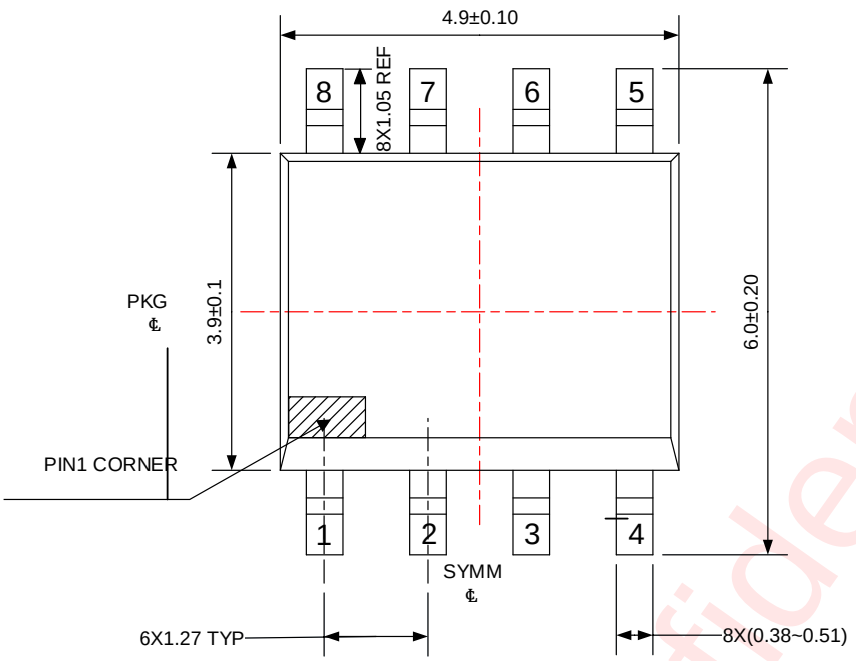
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

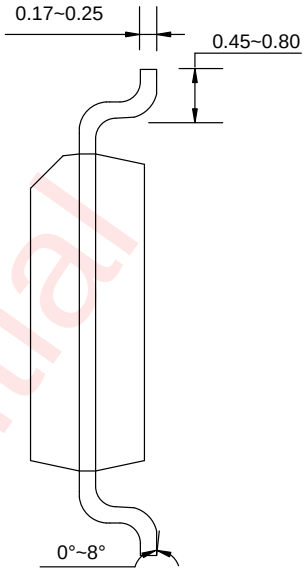
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330.00	12.40	6.40	5.40	2.10	2.00	8.00	4.00	12.00	Q1

All dimensions are nominal

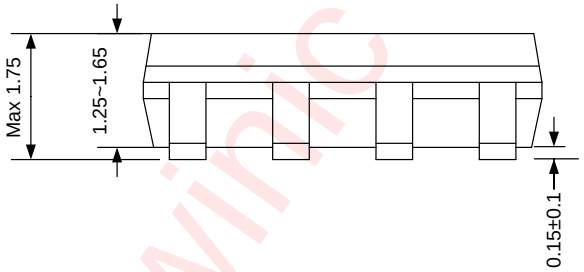
Package Description



Top View



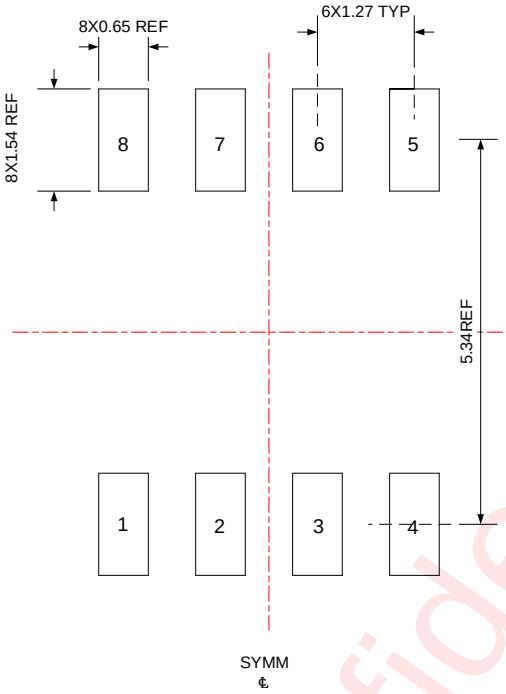
Side View



Side View

Unit：mm

Land Pattern Data



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit：mm

Revision History

Version	Date	Change Record
V1.0	Apr.2023	Officially released
V1.1	Nov.2024	1. Update feature（P1） 2. Update pin configuration and top mark(P3) 3. Update Ordering Information(P6) 4. Update Tape And Reel Information(P15) 5. Update Land Pattern Data(P17)

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