

## 500 mA High Performance Low-Dropout Linear Regulator

### Features

- Input voltage range: 1.4V to 5.5V
- Fixed outputs of 1.1V, 1.2V, 1.8V, 2.5V, 2.8V, 3.0V, 3.3V
- Rated output current: 500mA
- Quiescent current: typical 50 $\mu$ A
- Typical 0.1 $\mu$ A shutdown current
- Typical 530mV dropout voltage ( $I_{OUT}=500\text{mA}$ , 1.8V output)
- Power supply rejection ratio: typical 90dB ( $I_{OUT}=30\text{mA}$ , freq=1kHz, 1.8V output)
- Noise: typical 33 $\mu$ Vrms ( $I_{OUT}=30\text{mA}$ , BW=10Hz to 100kHz, 1.8V output)
- Built-in output short protection: typical 150mA when output short to ground
- DFN 1mmX1mmX0.37mm-4L package and SOT 23-5L package

### General Description

AW37050YXXX is a low dropout voltage regulator featuring low ON resistance, high PSRR, low Noise, good load/line transient response and smooth soft-start.

AW37050YXXX integrates current limit, short circuit protection, thermal shutdown, sufficiently protecting IC from being damaged.

AW37050YXXX is designed to work with a 1 $\mu$ F or more input ceramic capacitor and a 1 $\mu$ F or more output ceramic capacitor. The low power dissipation and good dynamic response make AW37050YXXX very suitable for hand-held communication equipment. Tiny package makes high density mounting of the IC on boards possible.

### Applications

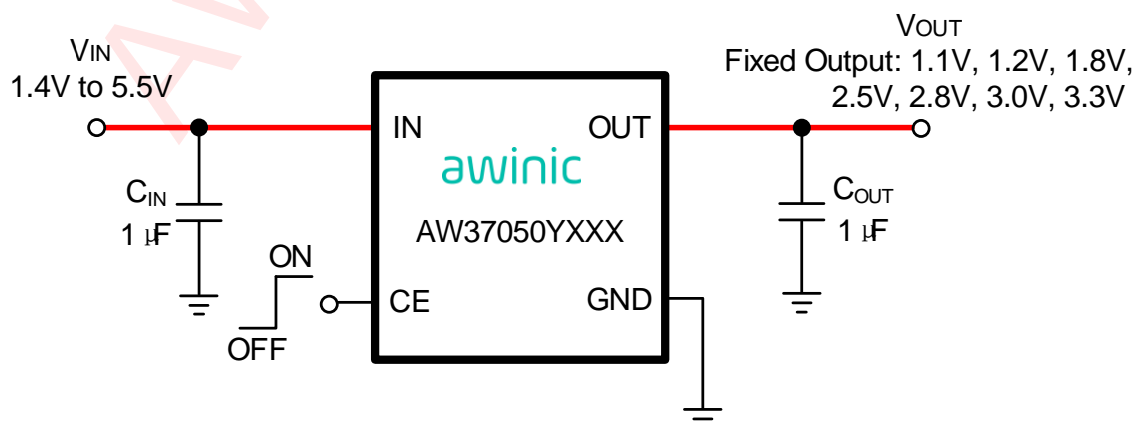
Battery-powered equipment

Smart phone

Digital camera

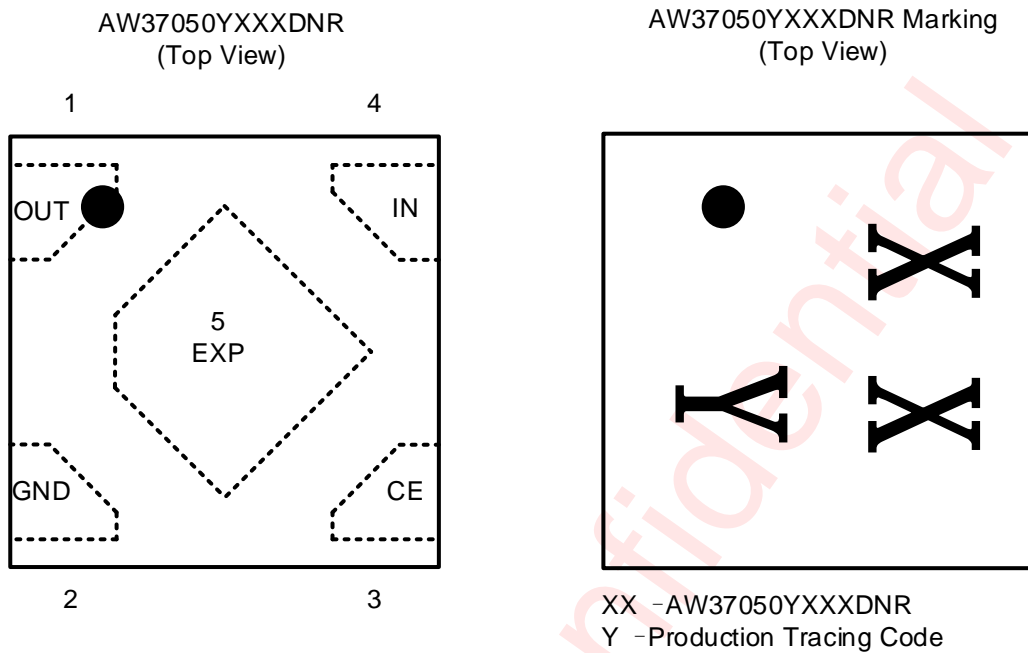
STB

### Typical Application Circuit

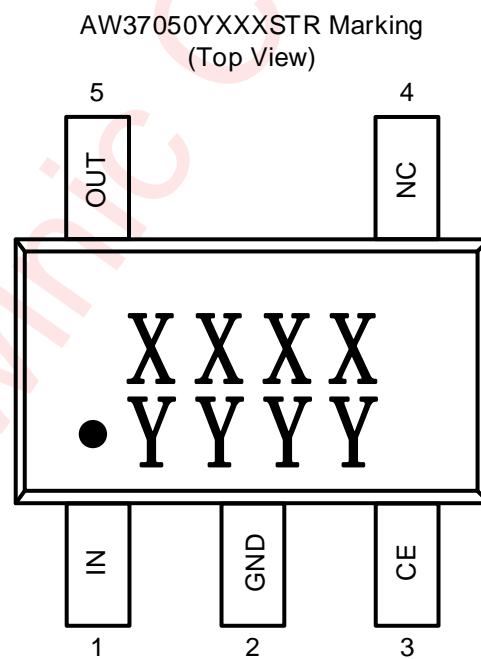


## Pin Configuration And Top Mark

DFN 1mmX1mm-4L



SOT 23-5L



XXXX - AW37050YXXXSTR  
YYYY - Production Tracing Code

## Pin Definition

DFN 1mmX1mm-4L

No.	NAME	DESCRIPTION
1	OUT	Regulated output voltage pin. Put a 1 $\mu$ F or more ceramic capacitor at the output pin.
2	GND	Ground.
3	CE	Chip enable pin. Built-in 140nA pull-down current. (High Active)
4	IN	Input supply pin. Put a 1 $\mu$ F or more bypass capacitor at the power supply.
5	EXP	Expose pad should be tied to ground plane for better power dissipation.

SOT 23-5L

No.	NAME	DESCRIPTION
1	IN	Input supply pin. Put a 1 $\mu$ F or more bypass capacitor at the power supply.
2	GND	Ground.
3	CE	Chip enable pin. Built-in 140nA pull-down current. (High Active)
4	NC	Not connected.
5	OUT	Regulated output voltage pin. Put a 1 $\mu$ F or more ceramic capacitor at the output pin.

## Name Rule

AW37 050 Y XXX ZZZ

### Package

DNR: DFN 1mmX1mmX0.37mm-4L  
STR: SOT 23-5L

### Output Voltage

E.g.  
180: Output Voltage 1.8V

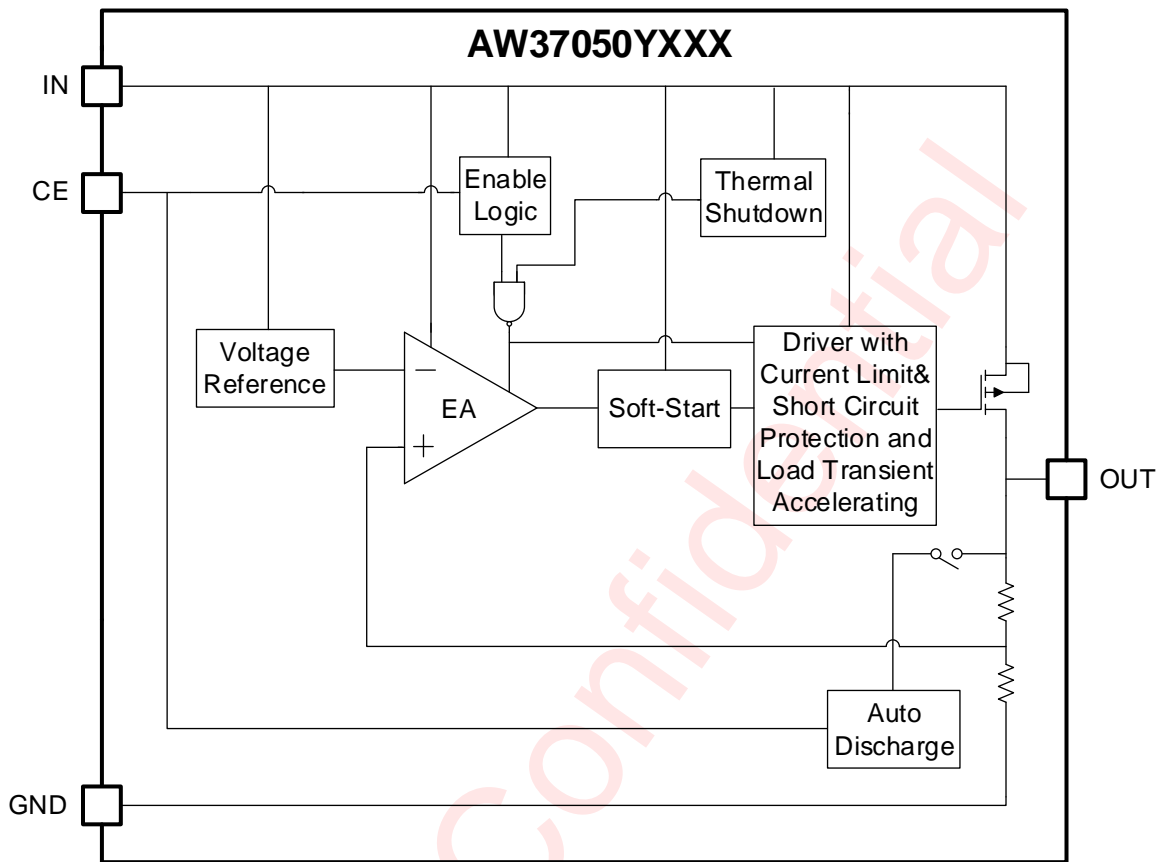
### Auto-discharge Function

D: Available  
B: Not available

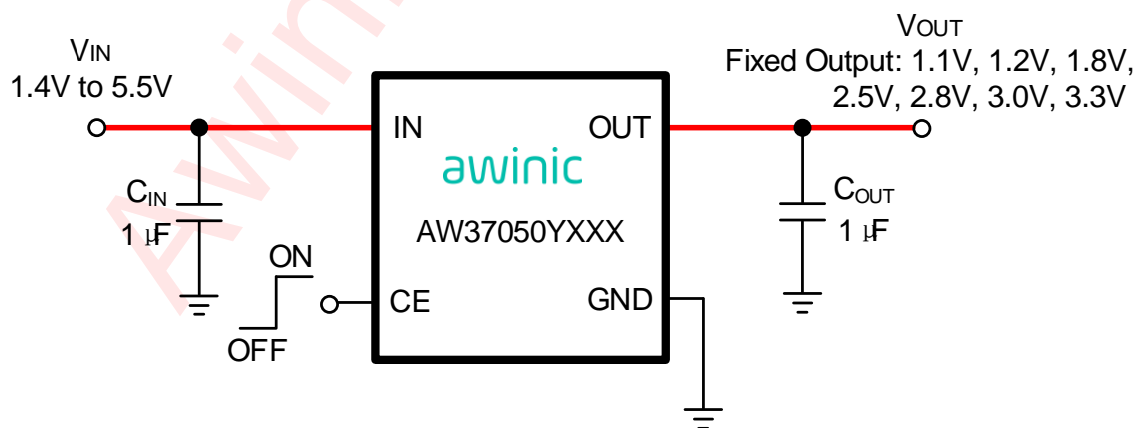
### Rated Current

050: Rated Current 500mA

## Functional Block Diagram



## Typical Application Circuits



AW37050YXXX Application Circuit

### Notice for typical application circuits:

Capacitance of  $C_{IN}$  and  $C_{OUT}$  should be  $1\mu F$  or more.

## Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW37050D110DNR	-40°C~85°C	DFN 1mmX1mm-4L	TR	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37050D120DNR	-40°C~85°C	DFN 1mmX1mm-4L	10	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37050D180DNR	-40°C~85°C	DFN 1mmX1mm-4L	AY	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37050D250DNR	-40°C~85°C	DFN 1mmX1mm-4L	2N	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37050D280DNR	-40°C~85°C	DFN 1mmX1mm-4L	RY	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37050D300DNR	-40°C~85°C	DFN 1mmX1mm-4L	2X	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37050D330DNR	-40°C~85°C	DFN 1mmX1mm-4L	DX	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37050D110STR	-40°C ~ 85°C	SOT 23-5L	Y4N5	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37050D120STR	-40°C ~ 85°C	SOT 23-5L	61GC	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37050D180STR	-40°C ~ 85°C	SOT 23-5L	0KV0	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37050D250STR	-40°C ~ 85°C	SOT 23-5L	D02K	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37050D280STR	-40°C ~ 85°C	SOT 23-5L	YVML	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37050D300STR	-40°C~85°C	SOT 23-5L	SLUE	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37050D330STR	-40°C ~ 85°C	SOT 23-5L	WDTD	MSL3	ROHS+HF	3000 units/ Tape and Reel

**Absolute Maximum Ratings**<sup>(NOTE1)</sup>

PARAMETERS		RANGE
Input voltage range		-0.3V to 6.5V
Enable control voltage range		-0.3V to 6.5V
Output voltage range		-0.3V to VIN+0.3V, max. 6.5V
Maximum operating junction temperature T <sub>J_MAX</sub>		150°C
Recommended operating junction temperature T <sub>J_REC</sub>		-40°C to 125°C
Operating free-air temperature range		-40°C to 85°C
Storage temperature T <sub>STG</sub>		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
Junction-to-ambient thermal resistance R <sub>θJA</sub> <sup>(NOTE2)</sup>	DFN 1mmX1mm-4L	215.4°C/W
	SOT 23-5L	177.4°C/W
Junction-to-case(top) thermal resistance R <sub>θJC(top)</sub> <sup>(NOTE2)</sup>	DFN 1mmX1mm-4L	161.85°C/W
	SOT 23-5L	102.1°C/W
Junction-to-board thermal resistance R <sub>θJB</sub> <sup>(NOTE2)</sup>	DFN 1mmX1mm-4L	156.4°C/W
	SOT 23-5L	42.7°C/W
Junction-to-top characterization parameter ψ <sub>JT</sub> <sup>(NOTE2)</sup>	DFN 1mmX1mm-4L	17.3°C/W
	SOT 23-5L	13.5°C/W
Junction-to-board characterization parameter ψ <sub>JB</sub> <sup>(NOTE2)</sup>	DFN 1mmX1mm-4L	170.4°C/W
	SOT 23-5L	39.4°C/W
Junction-to-case(bottom) thermal resistance R <sub>θJC(bot)</sub> <sup>(NOTE2)</sup>	DFN 1mmX1mm-4L	118°C/W
	SOT 23-5L	31.2°C/W
Maximum power consumption T <sub>A</sub> =25°C, T <sub>J_REC</sub> =125°C	DFN 1mmX1mm-4L	464mW
	SOT 23-5L	564mW
ESD	HBM (Human body model) <sup>(NOTE3)</sup>	±2kV
	CDM(Charged device model) <sup>(NOTE4)</sup>	±1.5kV
Latch-Up <sup>(NOTE5)</sup>		+IT: 200mA - IT: -200mA

**NOTE1:** Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

**NOTE2:** Thermal resistances follow JEDEC 2S2P standards, and is usually highly dependent on PCB layout. Exceptionally, R<sub>θJC(top)</sub> of DFN 1mmX1mm-4L Package follows SEMI standard G43-87.

**NOTE3:** All pins. Test Condition: ESDA/JEDEC JS-001-2017.

**NOTE4:** All pins. Test Condition: ESDA/JEDEC JS-002-2018.

**NOTE5:** Test Condition: JESD78E.

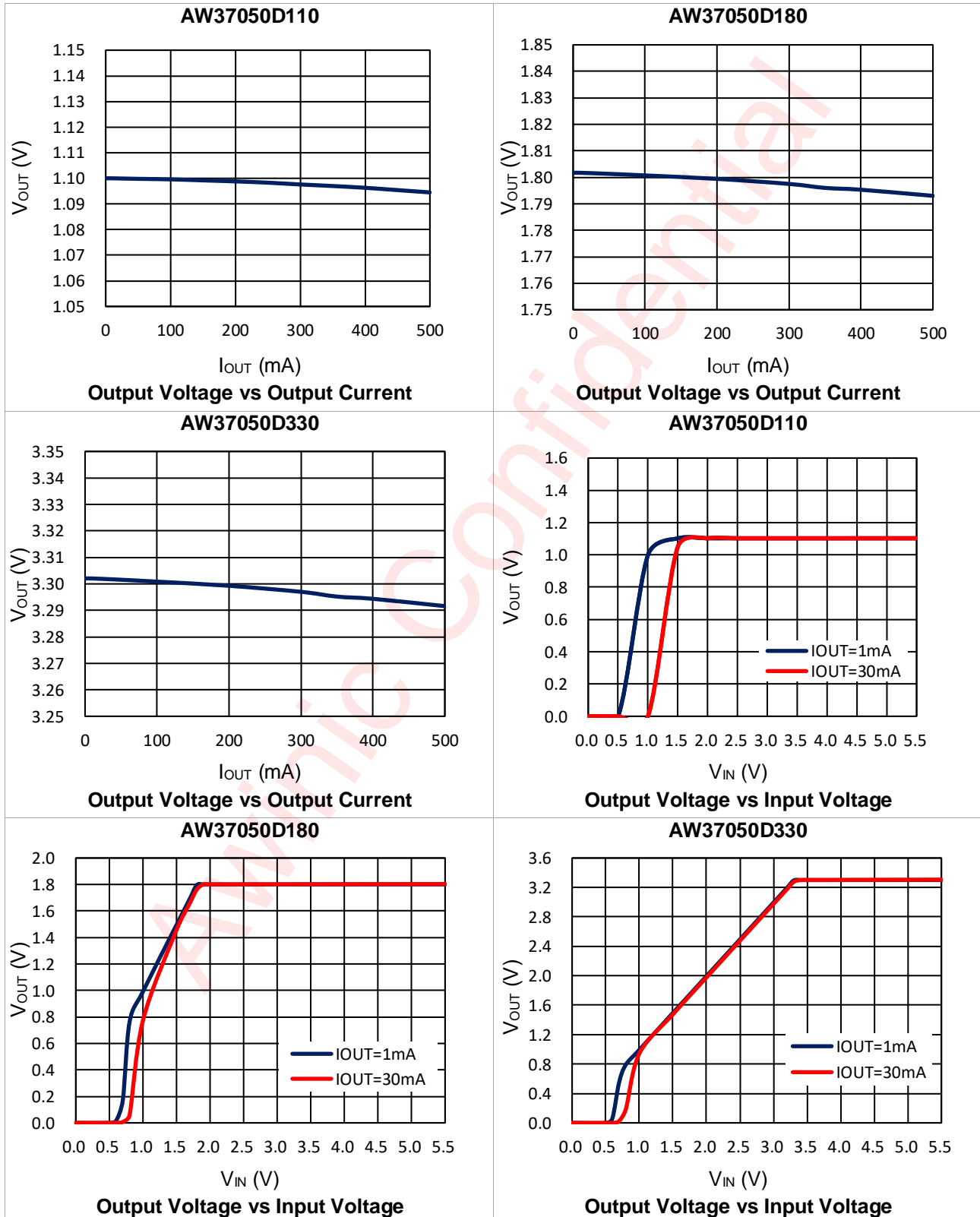
## Electrical Characteristics

$V_{IN}=V_{OUT(SET)}+1V$ ,  $V_{CE}>1V$ ,  $I_{OUT}=1mA$ ,  $C_{IN}=C_{OUT}=1\mu F$ ,  $T_A=25^\circ C$  (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{IN}$	Input Voltage Range		1.4		5.5	V
$V_{OUT\_ACC}$	Output Voltage Accuracy	$T_A=25^\circ C$	-1		1	%
		$-40^\circ C \leq T_A \leq 85^\circ C$	-2		2	
$LOAD_{Reg}$	Load Regulation	$1mA \leq I_{OUT} \leq 500mA$		5	30	mV
$LINE_{Reg}$	Line Regulation	$V_{OUT(SET)}+0.5V \leq V_{IN} \leq 5.5V$		1	5	mV
$V_{dropout}$	Dropout Voltage	$I_{OUT}=500mA$ , When $V_{OUT}$ falls 100mV below $V_{OUT(SET)}$	$V_{OUT(SET)}=1.1V$	1001		mV
			$V_{OUT(SET)}=1.2V$	904		
			$V_{OUT(SET)}=1.8V$	530		
			$V_{OUT(SET)}=2.5V$	363		
			$V_{OUT(SET)}=2.8V$	319		
			$V_{OUT(SET)}=3.0V$	297		
			$V_{OUT(SET)}=3.3V$	275		
$I_{SD}$	Shutdown Current	$V_{CE}<0.4V$		0.1	1	$\mu A$
$I_Q$	Quiescent Current	$I_{OUT}=0mA$		50	100	$\mu A$
$V_{CEH}$	CE Input Voltage "H"	$-40^\circ C \leq T_A \leq 85^\circ C$	1			V
$V_{CEL}$	CE Input Voltage "L"	$-40^\circ C \leq T_A \leq 85^\circ C$			0.4	V
PSRR	Power Supply Ripple Rejection	$I_{OUT}=30mA$ , $f=1kHz$ $V_{OUT(SET)}=1.8V$		90		dB
$V_N$	Output Voltage Noise	$I_{OUT}=30mA$ BW=10Hz to 100kHz	$V_{OUT(SET)}=1.1V$	21		$\mu V_{rms}$
			$V_{OUT(SET)}=1.8V$	33		
			$V_{OUT(SET)}=3.3V$	46		
$I_{CL}$	Output Current Limit	$V_{OUT}=90\% \cdot V_{OUT(SET)}$	500			mA
$I_{SC}$	Short Current Limit	$V_{OUT}<10\% \cdot V_{OUT(SET)}$		150		mA
VTC	Output Voltage Temperature Coefficient	$-40^\circ C \leq T_A \leq 85^\circ C$		$\pm 40$		ppm/ $^\circ C$
$R_{DISC}$	Auto Discharge Resistance	$V_{IN}=4V$ , $V_{CE}<0.4V$ , $V_{OUT}=2.8V$		130		$\Omega$
$I_{CE}$	CE Pull Down Current			140		nA
$T_{SDH}$	Thermal Shutdown Threshold	Temperature Rising		160		$^\circ C$
$T_{SDL}$	Thermal Shutdown Reset Threshold	Temperature Falling		130		$^\circ C$

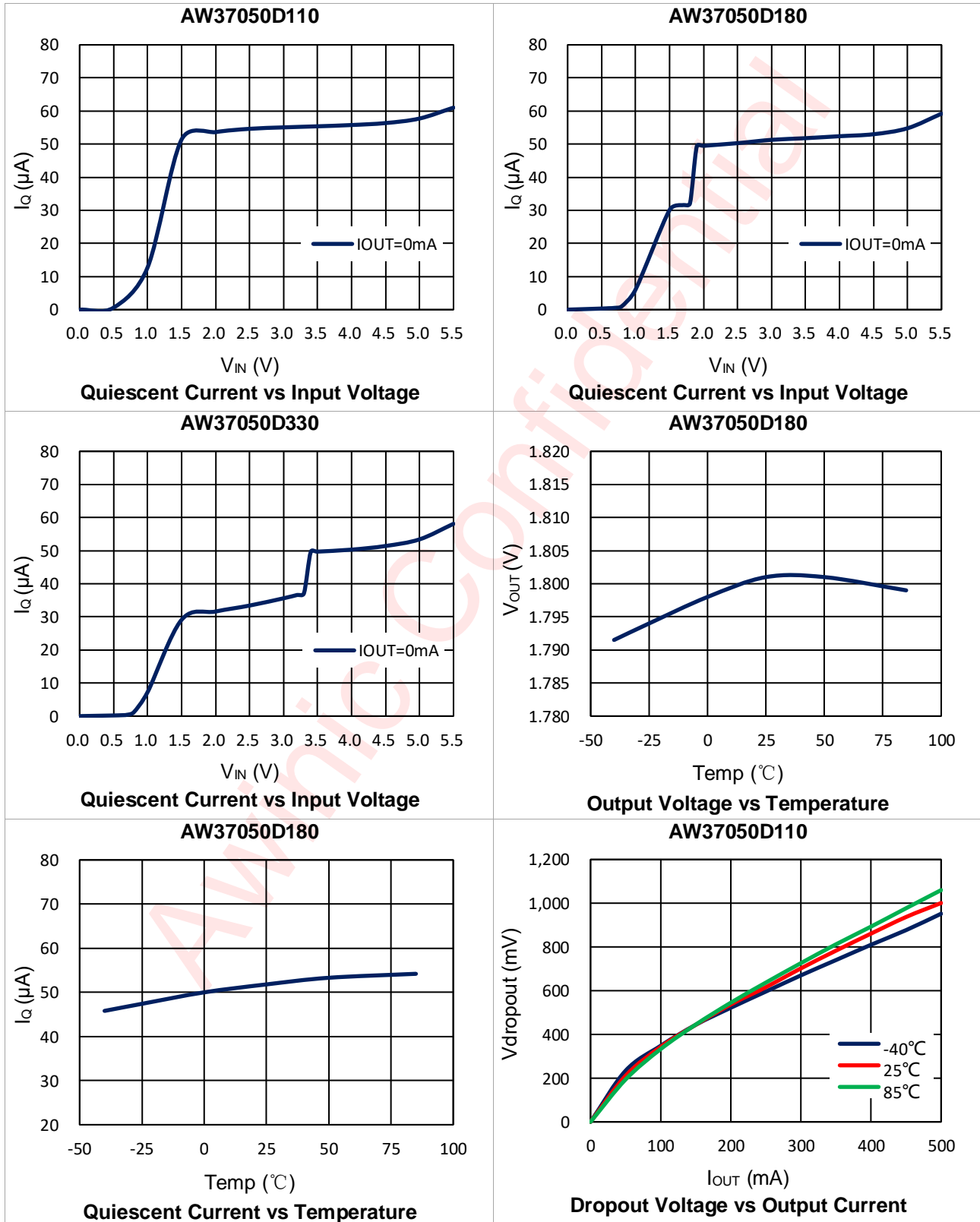
## Typical Characteristics

$V_{IN}=V_{OUT(SET)}+1V$ ,  $V_{CE}>1V$ ,  $I_{OUT}=1mA$ ,  $C_{IN}=C_{OUT}=1\mu F$ ,  $T_A=25^\circ C$ , In Typical Application Circuit, unless otherwise noted.



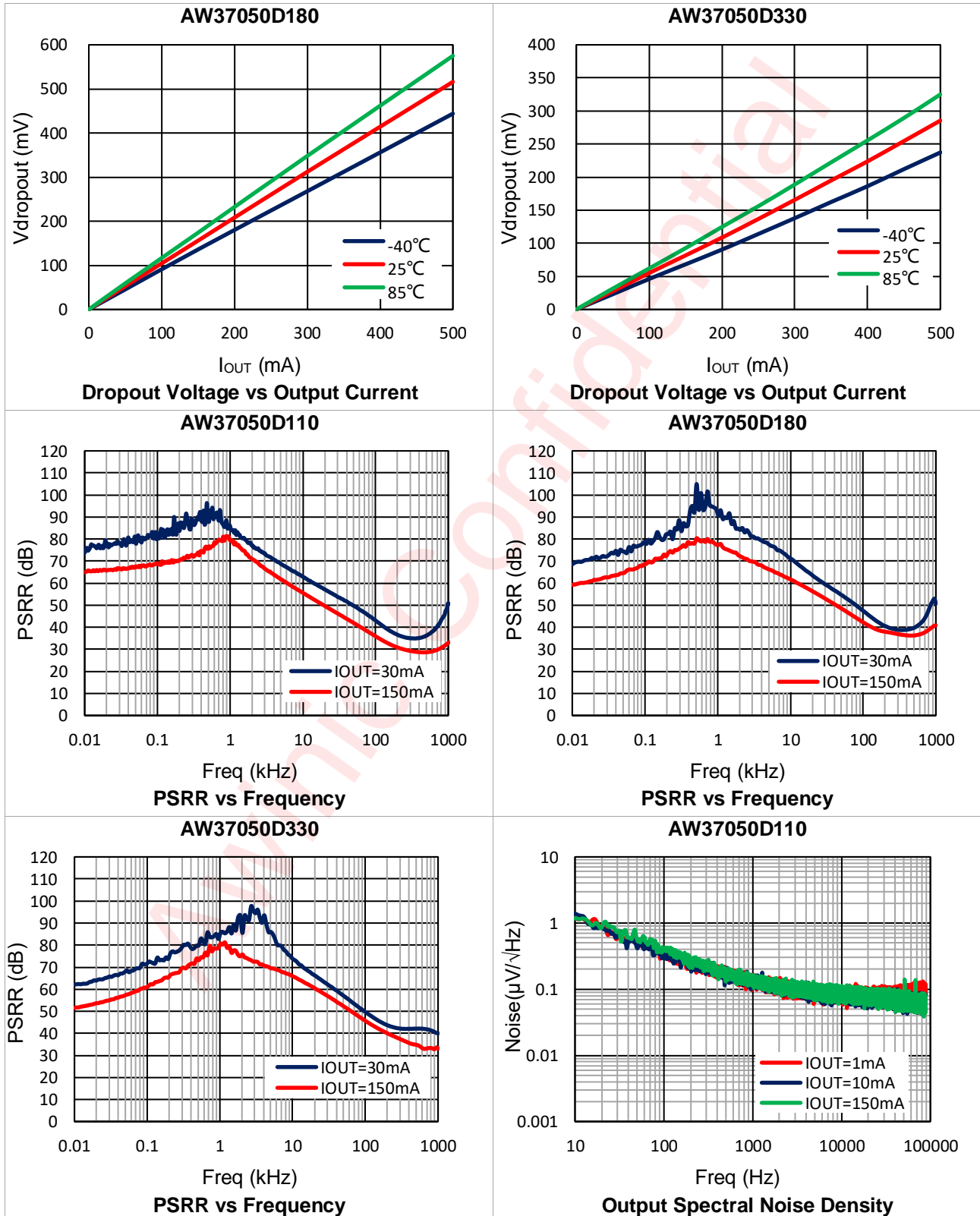
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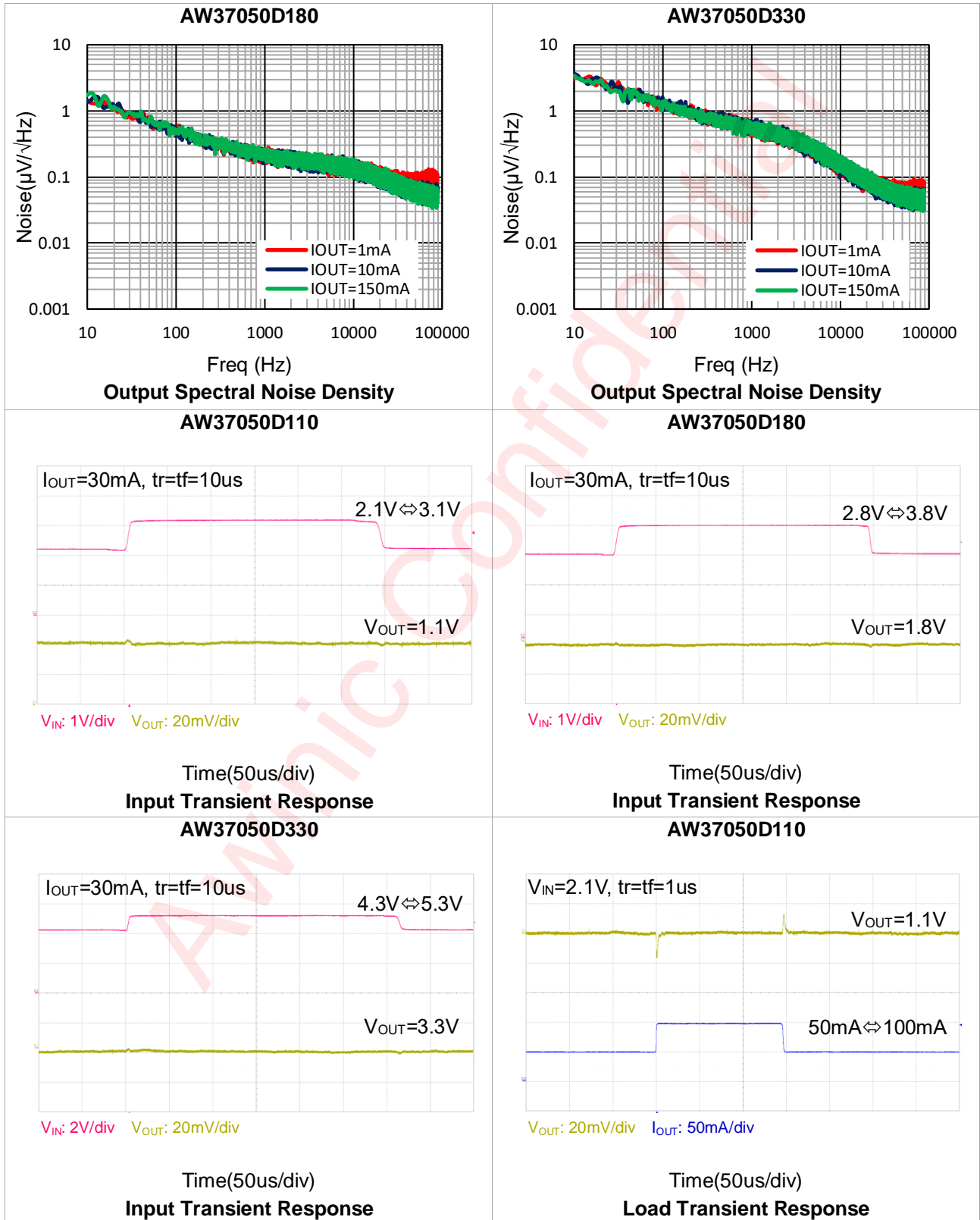
### Typical Characteristics (Continued)

$V_{IN}=V_{OUT(SET)}+1V$ ,  $V_{CE}>1V$ ,  $I_{OUT}=1mA$ ,  $C_{IN}=C_{OUT}=1\mu F$ ,  $T_A=25^\circ C$ , In Typical Application Circuit, unless otherwise noted.



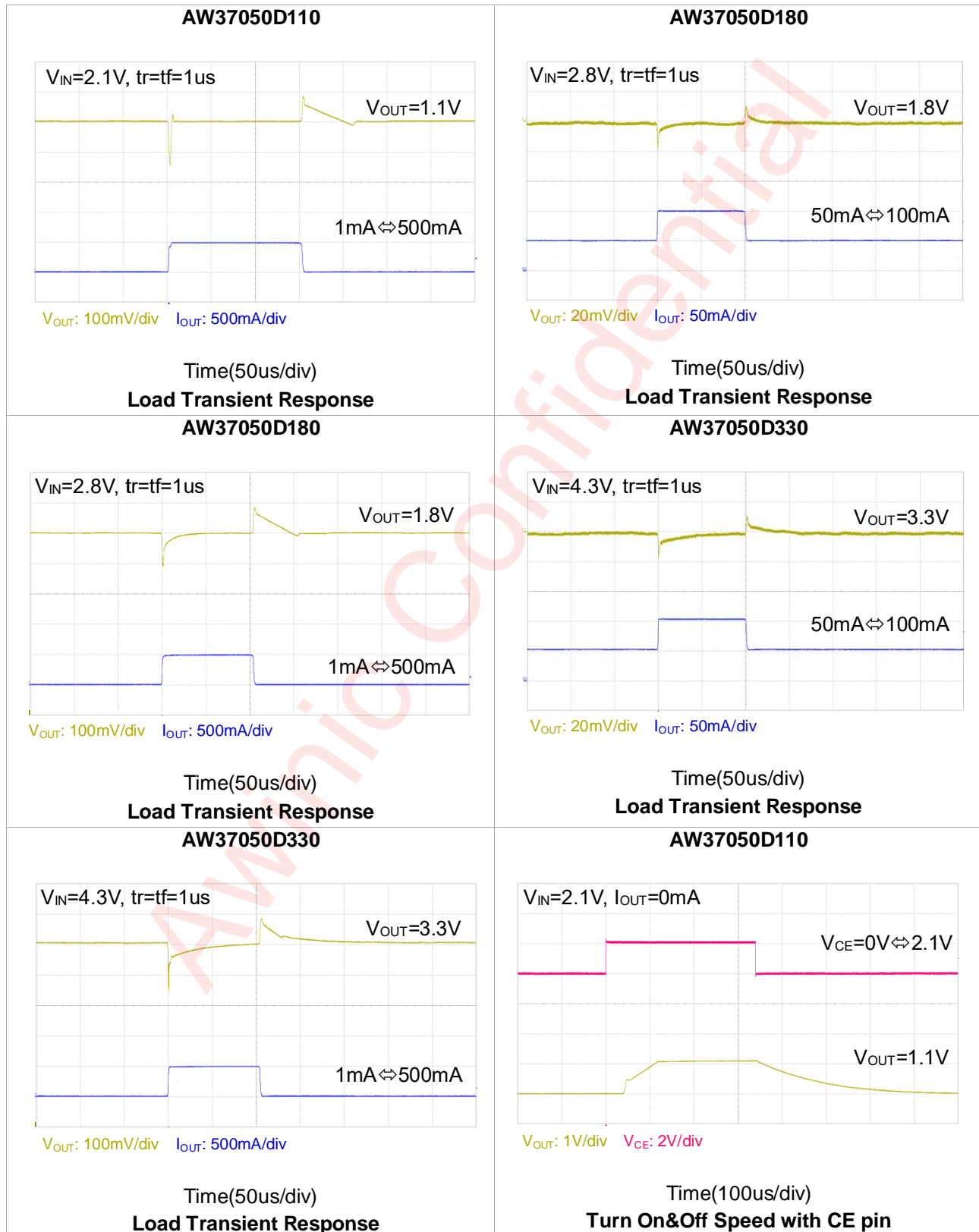
## Typical Characteristics (Continued)

$V_{IN}=V_{OUT(SET)}+1V$ ,  $V_{CE}>1V$ ,  $I_{OUT}=1mA$ ,  $C_{IN}=C_{OUT}=1\mu F$ ,  $T_A=25^\circ C$ , In Typical Application Circuit, unless otherwise noted.



## Typical Characteristics (Continued)

$V_{IN}=V_{OUT(SET)}+1V$ ,  $V_{CE}>1V$ ,  $I_{OUT}=1mA$ ,  $C_{IN}=C_{OUT}=1\mu F$ ,  $T_A=25^\circ C$ , In Typical Application Circuit, unless otherwise noted.



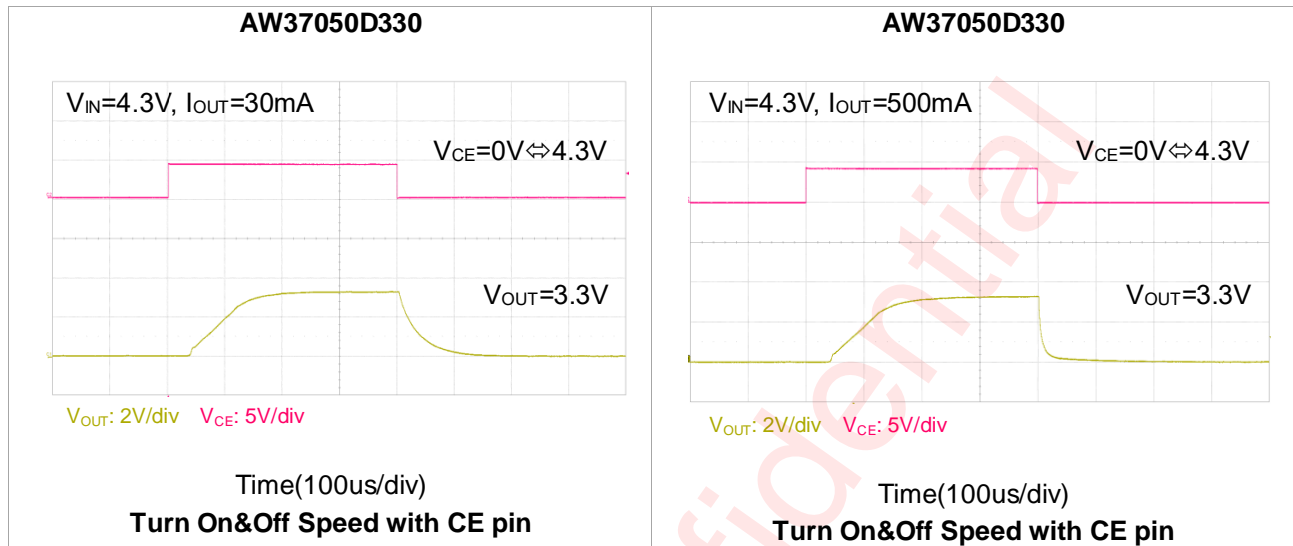
## Typical Characteristics (Continued)

$V_{IN}=V_{OUT(SET)}+1V$ ,  $V_{CE}>1V$ ,  $I_{OUT}=1mA$ ,  $C_{IN}=C_{OUT}=1\mu F$ ,  $T_A=25^\circ C$ , In Typical Application Circuit, unless otherwise noted.



## Typical Characteristics (Continued)

$V_{IN}=V_{OUT(SET)}+1V$ ,  $V_{CE}>1V$ ,  $I_{OUT}=1mA$ ,  $C_{IN}=C_{OUT}=1\mu F$ ,  $T_A=25^\circ C$ , In Typical Application Circuit, unless otherwise noted.



## Detailed Functional Description

AW37050YXXX is a low dropout voltage regulator. After powered on, with CE pin assertion, feedback voltage signal from the integrated resistor network and a voltage related to the voltage reference are transmit to positive input terminal and negative input terminal of an error amplifier (EA) respectively. The output signal of EA is used to control the open-state of power MOSFET. After soft-start, feedback voltage signal compares with the established reference voltage, making output voltage stable and accurate. AW37050YXXX integrates function of load transient accelerating, making LDO obtain excellent dynamic load transient response performance.

### Enable Operation

AW37050YXXX uses CE pin to realize enable operation. Applying proper value of voltage to CE pin can make IC enable/disable.

If the voltage of CE pin is less than 0.4V, AW37050YXXX is guaranteed to be disabled. In this state, function modules of IC and power MOSFET are turned off. And the auto discharge function is enabled making output discharge through a on-state NMOSFET to Ground. In disable state, AW37050YXXX only consumes a typical 10nA current.

If the voltage of CE pin is more than 1V, AW37050YXXX is guaranteed to be enabled. In this state, the auto discharge function is disabled, and AW37050YXXX regulates output voltage to the designed value of voltage. A 140nA pull down current to Ground is built-in at CE pin, making sure that the IC is disabled when CE pin floats. If Enable function is not required, CE pin should be connected directly to IN pin.

### Output Current Limit

AW37050YXXX integrates output current limit function, protecting IC from excessive current.

When the load is excessively heavy, AW37050YXXX limits the current flowing through the IC to a typical 700mA current. This value is specially designed, so that IC is protected properly and the output capability of 500mA is not influenced either.

Meanwhile, AW37050YXXX integrates a 150mA fold-back current limit function, lowering the system dissipation when output overload or short to Ground.

### Thermal Shutdown

AW37050YXXX integrates thermal shutdown function, protect IC from excessively high temperature.

When the chip temperature exceeds 160°C, AW37050YXXX detects it as an over-temperature event, triggering thermal shutdown, which will turn off the main function module, including power MOSFET. This inhibits increase of chip's temperature. IC would keep the protection-state on until the chip's temperature falls below to 130°C. At this moment, the over-temperature protection-state is released, IC resumes to work again. The hysteresis avoids IC's turning off and on frequently around the the Thermal Shutdown threshold.

### Auto Discharge

AW37050YXXX makes output voltage discharge quickly when in CE disable state or thermal shutdown state, benefit from integrating auto discharge function. Auto discharge function is implemented by integrated a NMOSFET of typical 130Ω R<sub>dson</sub> route from Output to Ground, and the route is get through in CE disable state or thermal shutdown state. This feature prevents residual charge voltage on the output capacitor, which may impact proper power up of the system connected to the converter. It should be noted that auto discharge function is optional according to different specs.

## Application Information

### Power Dissipation and Device Operation

The permissible power dissipation is dependent on the ambient temperature  $T_A$  and the junction-to-ambient thermal resistance  $R_{\theta JA}$ .

The absolute maximum allowable power dissipation for the device in a given package can be calculated using Equation below, where  $T_{J\_MAX} = 150^\circ\text{C}$  :

$$PD_{MAX\_ABS} = (T_{J\_MAX} - T_A) / R_{\theta JA}$$

The recommended maximum allowable power dissipation for the device in a given package can be calculated using Equation below, where  $T_{J\_REC} = 125^\circ\text{C}$  :

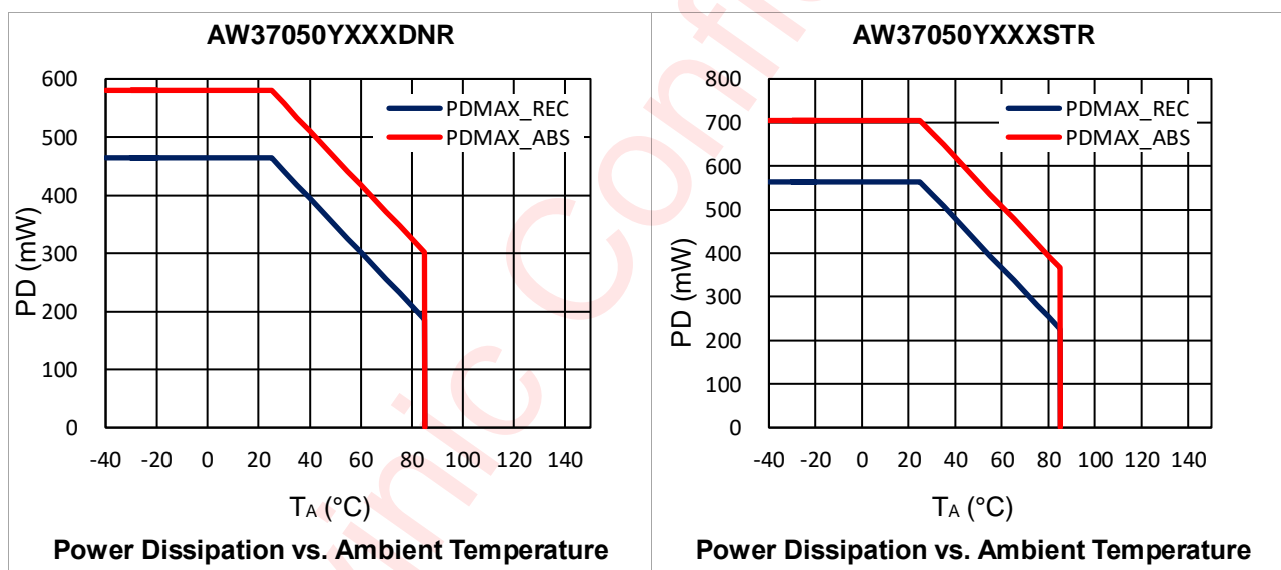
$$PD_{MAX\_REC} = (T_{J\_REC} - T_A) / R_{\theta JA}$$

The actual power being dissipated in the device can be represented by Equation below:

$$PD_{ACT} = (V_{IN} - V_{OUT}) \times I_{OUT}$$

These equations above establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device.

The graphs of Power Dissipation vs. Ambient Temperature are showed below :



The above graphs show the maximum power dissipation of the respective package at  $T_{J\_REC} = 125^\circ\text{C}$  and  $T_{J\_MAX} = 150^\circ\text{C}$ . Operating the device in the region between  $PD_{MAX\_REC}$  and  $PD_{MAX\_ABS}$  might have a negative influence on its lifetime.

### Capacitors Selection

#### IN pin: Input Capacitor $C_{IN}$

AW37050YXXX advises to use a  $1\mu\text{F}$  or more X5R or X7R ceramic capacitor at IN pin as shown in Typical Application Circuit.

#### OUT pin: Output Capacitor $C_{OUT}$

AW37050YXXX advises to use a  $1\mu\text{F}$  or more X5R or X7R ceramic capacitor at OUT pin as shown in Typical Application Circuit.

## Recommended Components List

Component	PART No.	DESCRIPTION	MFR	TYP.	UNIT
C <sub>IN</sub>	GRM155R61A105KE15	10V, X5R, 0402	MURATA	1	μF
C <sub>OUT</sub>	GRM155R61A105KE15	10V, X5R, 0402	MURATA	1	μF

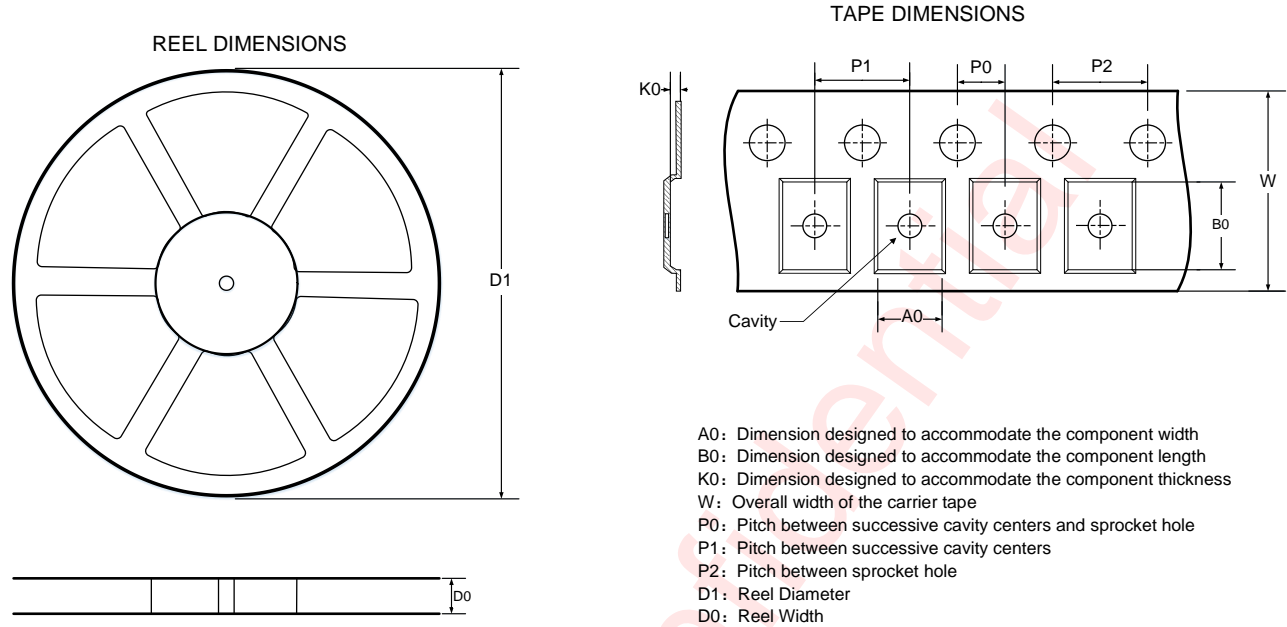
## PCB Layout Consideration

The performance of a power source circuit using this device is highly dependent on a peripheral circuit. To obtain the optimal performance, a peripheral component or the device mounted on PCB should not exceed its rated voltage, rated current or rated power. When designing a peripheral circuit, guidelines below for PCB layout of AW37050YXXX should be obeyed:

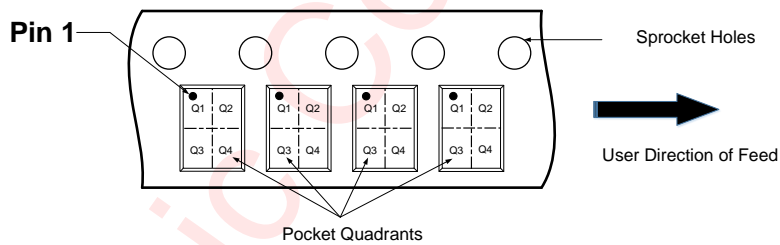
1. All peripheral components should be placed as close to the chip as possible. C<sub>IN</sub> and C<sub>OUT</sub> should be close to IN and OUT pins respectively. Avoid connecting device and chip pins with two different layers of copper, use the same layer of copper instead.
2. IN and OUT pin are the large current input and output of the chip, make IN, OUT, and meanwhile GND lines sufficient.
3. The connection lines between the planes of C<sub>IN</sub> or C<sub>OUT</sub> and respective chip pin should be as short and wide as possible, to reduce noise and EMI interference, or it may cause noise pickup or unstable operation.
4. The exposed plane of chip and GND pins must be connected to the large-area ground layer of PCB directly, meanwhile place sufficient vias below the exposed plane. Thus we can decrease the thermal resistor on the board to optimize heat-diffusion performance.

## Tape And Reel Information

DFN 1mmX1mm-4L



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



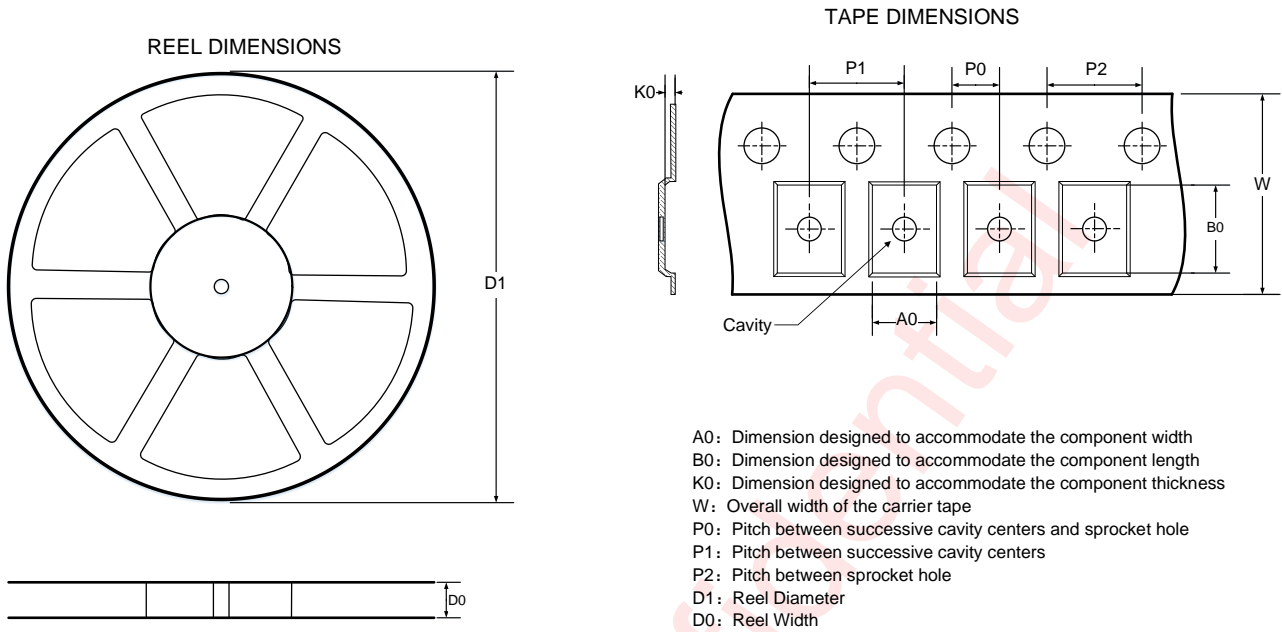
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

### DIMENSIONS AND PIN1 ORIENTATION

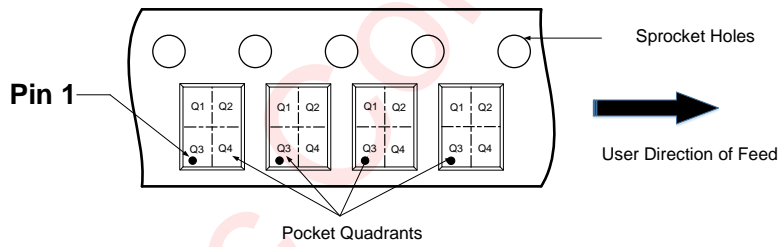
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.14	1.17	0.56	2	4	4	8	Q1

All dimensions are nominal

SOT 23-5L



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

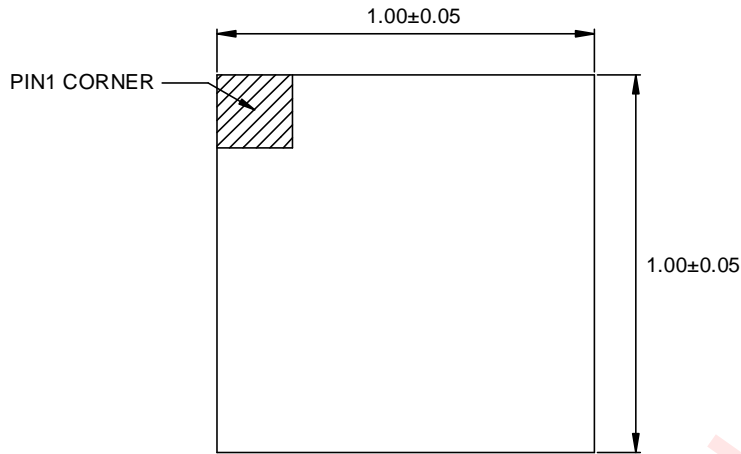
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	3.3	3.2	1.4	2	4	4	8	Q3

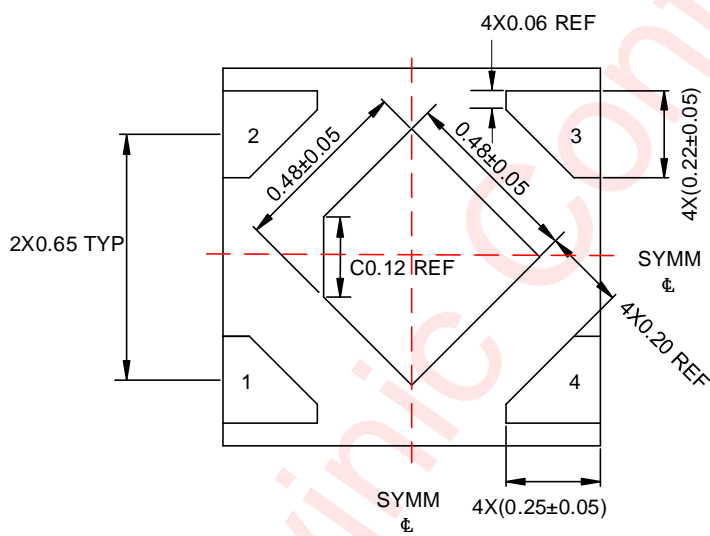
All dimensions are nominal

## Package Description

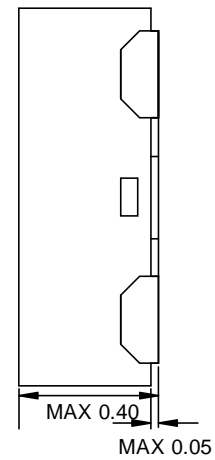
DFN 1mmX1mm-4L



Top View



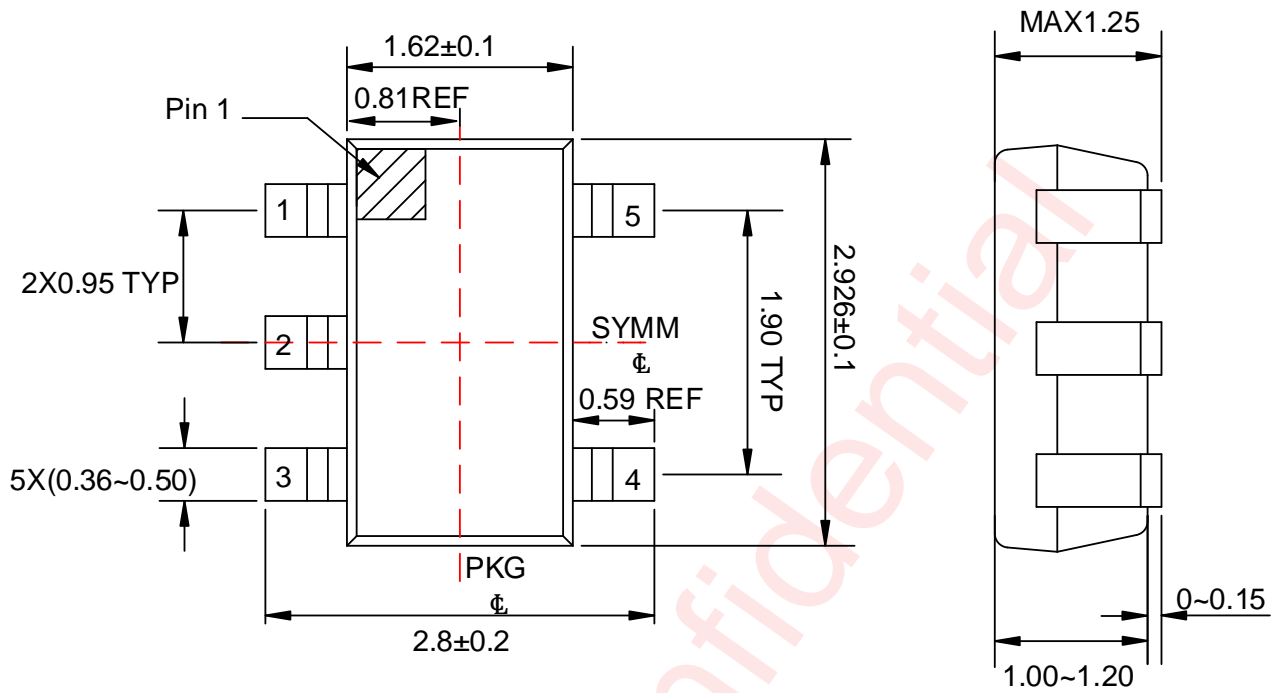
Bottom View



Side View

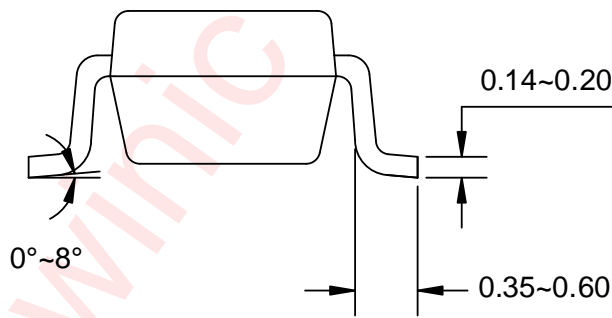
Unit:mm

SOT 23-5L



Top View

Side View

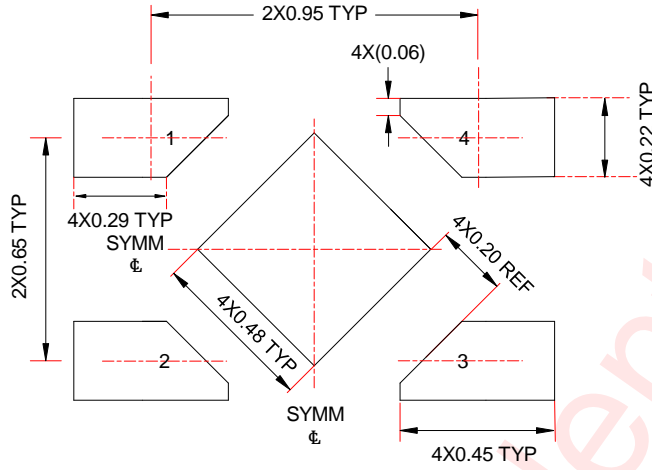


Side View

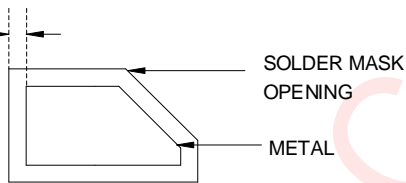
Unit: mm

### Land Pattern Data

DFN 1mmX1mm-4L

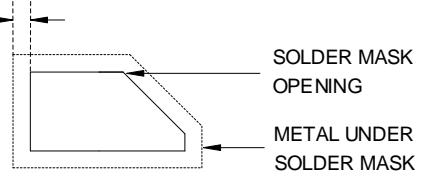


0.05 MAX  
ALL AROUND



NON SOLDER MASK DEFINED

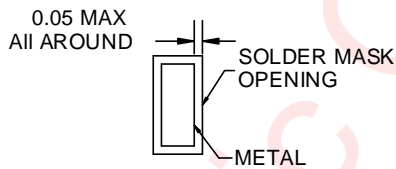
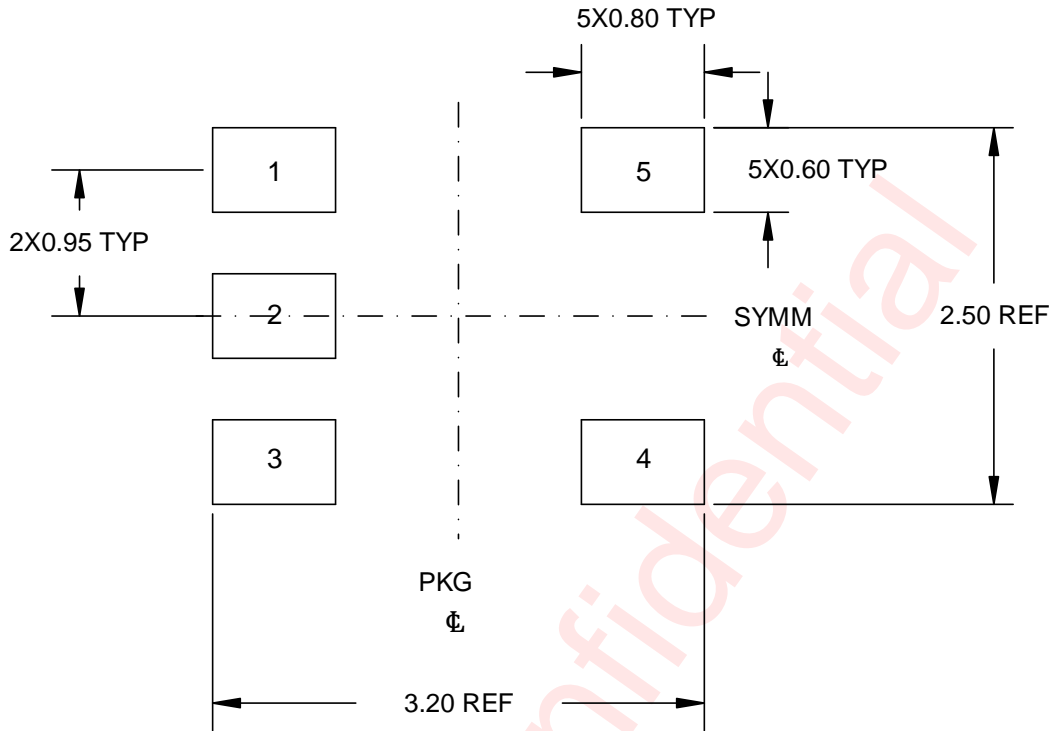
0.05 MIN  
ALL AROUND



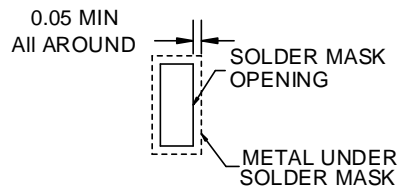
SOLDER MASK DEFINED

UNIT : mm

SOT 23-5L



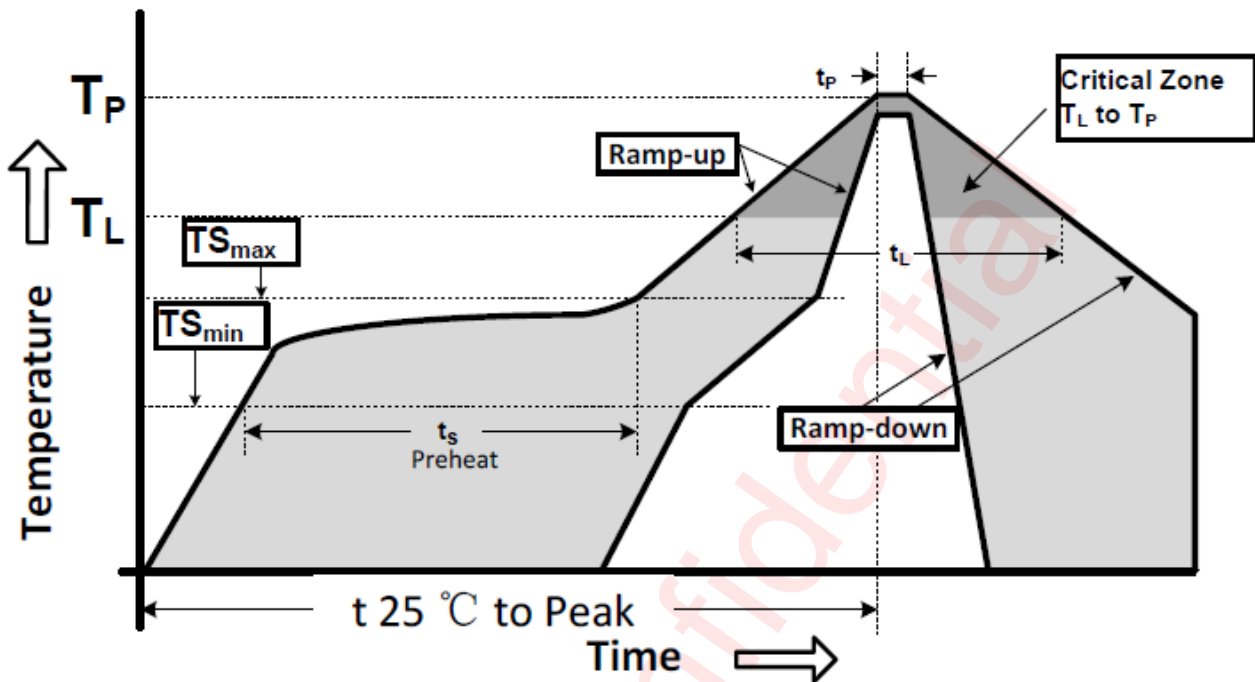
NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

## Reflow



Reflow Note	Spec
Ramp-up rate ( $T_{S_{max}}$ to $T_P$ )	3°C/second max.
Preheat temperature ( $T_{S_{min}}$ to $T_{S_{max}}$ )	150°C to 200°C
Preheat time ( $t_s$ )	60 – 180 seconds
Time above $T_L$ , 217°C ( $t_L$ )	60 – 150 seconds
Peak temperature ( $T_P$ )	260°C
Time within 5°C of peak temperature( $t_p$ )	20 – 40 seconds
Ramp-down rate	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

## Revision History

Version	Date	Change Record
V1.0	Jan. 2021	Officially released
V1.1	Jul. 2021	Add SOT 23-5L package; Add electrical characteristics of 1.1V
V1.2	Apr. 2022	Add test standard of Vdropout in Electrical Characteristics; Correct Test Condition of HBM; Replenish and update Thermal Metric parameters in Absolute Maximum Ratings; Add graphs of Power Dissipation vs. Ambient Temperature; Add reflow curve
V1.3	Aug. 2022	Update Tape And Reel Information of DFN 1mmX1mm-4L and SOT 23-5L packages; Update Package Description of SOT 23-5L package
V1.4	Apr. 2024	Update the description of the diagram(P16);Update the package description of DFN 1mmX1mm-4L.(P20)

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