30W, 4.5V to 26V, High efficiency Stereo Class D Audio Amplifier with I2C Control

Features

- Wide Voltage Range: 4.5V - 26V
- Output Power:
  - BTL mode: 2×30W@8Ω, 24V,THD+N<1%
  - PBTL mode: 1×60W@4Ω, 24V,THD+N<1%
- Low THD+N: 0.03% at 1W, 1kHz input, 8Ω
- 17mA Idle Current in Low-Loss Mode
- Overall efficiency up to 94%
- Multiple switching frequencies
  - AM avoidance
  - Master/Slave synchronization
  - Up to 1.2MHz switching frequency
- Programmable Power Limit
- Support 1.8V/3.3V I²C Control Gain, Spread Spectrum,Thermal Foldback and Phase shift etc.
- Support parallel BTL Mode and MONO Mode
- Integrated self-protection：over-voltage, under-voltage, over-temperature, DC-detect and short-circuit protection
- ETSSOP 11mm×8.1mm -32L Package

Applications

- Speaker bar、After-market automotive、CRT TV and Consumer Audio Applications

General Description

AW83119 is a stereo efficient, Class-D audio power amplifier for driving speakers up to 60W/4Ω in PBTL mode. The AW83119 can run 2×30W/8Ω without heat sink on a dual layer PCB.

The AW83119 advanced oscillator/PLL circuit employs a multiple switching frequency option to avoid AM interferences; this is achieved together with an option of Master/Slave mode, making it possible to synchronize multiple devices.

The AW83119 controls internal registers through the I²C interface. Registers parameters include Gain, MONO mode, Spread Spectrum, Mute, Thermal Foldback and Phase shift parameters etc.

The AW83119 built-in over-voltage, under-voltage protection, DC protection, thermal protection and short-circuit protection, effectively prevent it from being damaged.

AW83119 is available in ETSSOP 11mm×8.1mm-32L package.

Typical Application Circuit

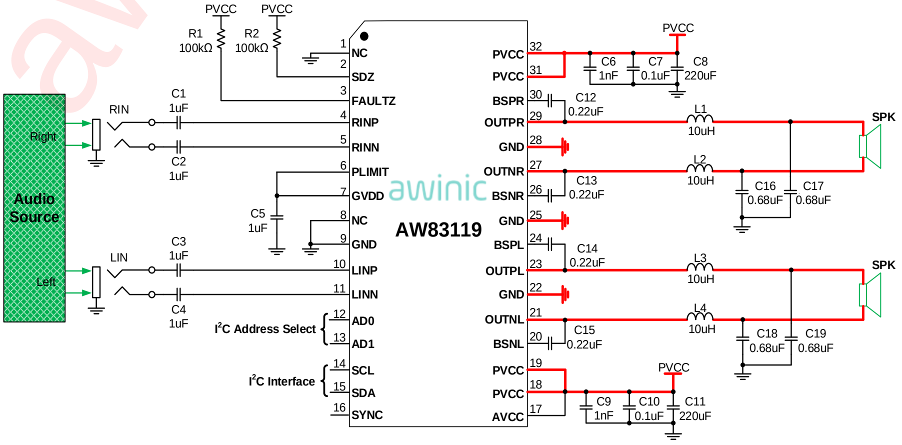
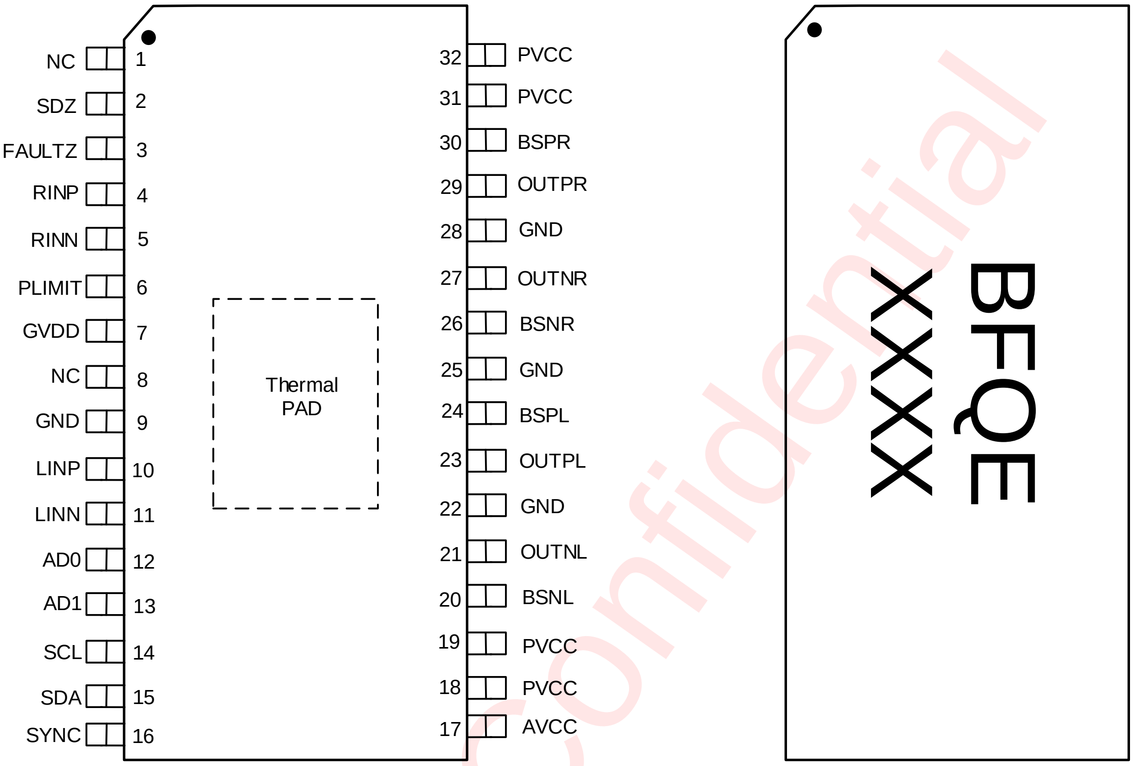


Figure 1 Typical Application Circuit of AW83119

Pin Configuration And Top Mark



AW83119TSR PIN Configuration
(Top View)

AW83119TSR MARKING
(Top View)

BFQE - AW83119TSR
XXXX - Production Tracing Code

Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	NC	No Connect Pin. Can be shorted to GND or left open.
2	SDZ	Shutdown logic input for audio amp (LOW = outputs Hi-Z, Registers will are cleared, HIGH = outputs enabled). TTL logic levels with compliance to PVCC.
3	FAULTZ	General fault reporting including Over-temp, DC Detect. Open drain. FAULTZ = High, normal operation, FAULTZ = LOW, fault condition.
4	RINP	Positive audio input for right channel. Biased at 2.75V.
5	RINN	Negative audio input for right channel. Biased at 2.75V.
6	PLIMIT	Power limit level control. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit.
7	GVDD	Internally generated FET gate drive supply. Nominal voltage is 5.75V.

8	NC	No Connect Pin. Can be shorted to GND or left open.
9	GND	Ground
10	LINP	Positive audio input for left channel. Biased at 2.75V. Connect to GND for PBTL mode.
11	LINN	Negative audio input for left channel. Biased at 2.75V. Connect to GND for PBTL mode.
12	AD0	I^{2}C address pin0. TTL logic levels with compliance to GVDD.
13	AD1	I^{2}C address pin1. TTL logic levels with compliance to GVDD.
14	SCL	I^{2}C-bus clock input.
15	SDA	I^{2}C-bus data input/output.
16	SYNC	Clock input/output for synchronizing multiple class-D devices. Not connect for Master mode.
17	AVCC	Analog supply
18	PVCC	Power supply
19	PVCC	Power supply
20	BSNL	Bootstrap supply (BST) for left channel output, negative high-side FET.
21	OUTNL	Class-D H-bridge negative output for left channel.
22	GND	Power Ground.
23	OUTPL	Class-D H-bridge positive output for left channel.
24	BSPL	Bootstrap supply (BST) for left channel output, positive high-side FET.
25	GND	Power Ground.
26	BSNR	Bootstrap supply (BST) for right channel output, negative high-side FET.
27	OUTNR	Class-D H-bridge negative output for right channel.
28	GND	Power Ground.
29	OUTPR	Class-D H-bridge positive output for right channel.
30	BSPR	Bootstrap supply (BST) for right channel output, positive high-side FET.
31,32	PVCC	Power supply.

Functional Block Diagram

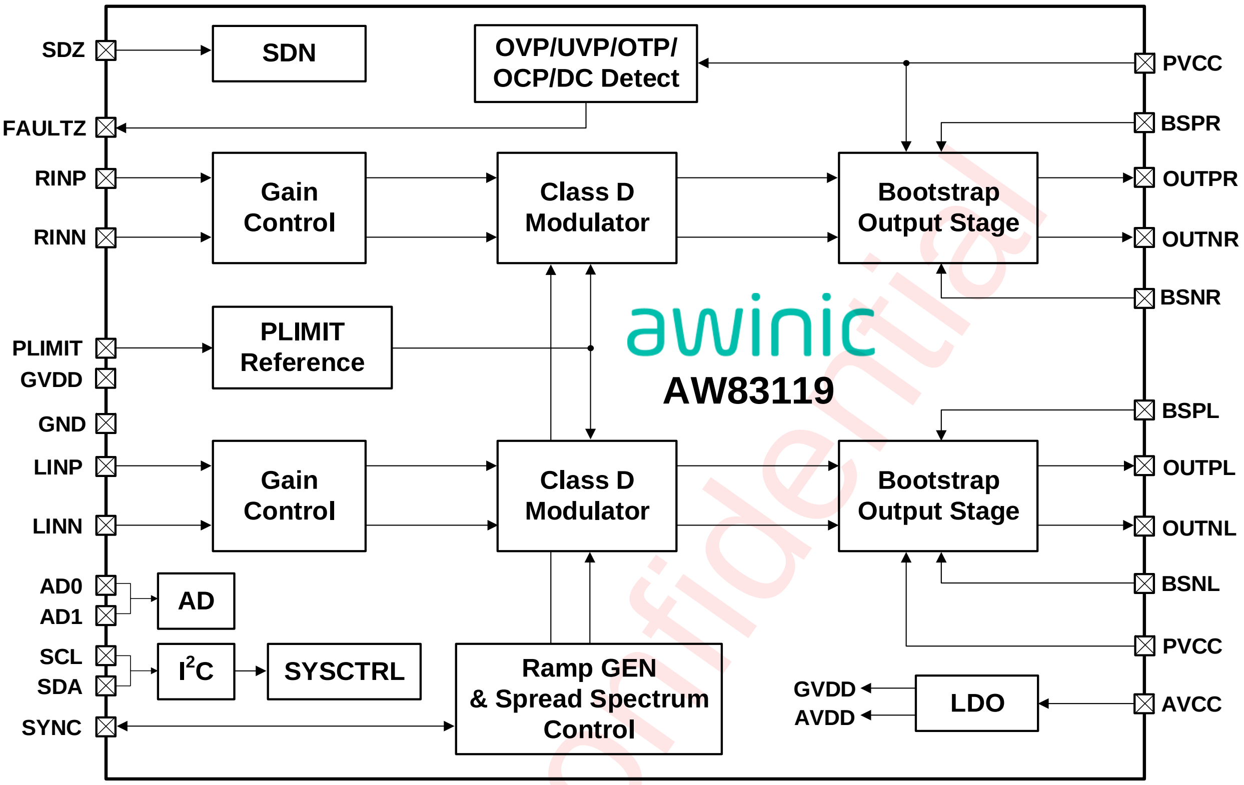


Figure 3 AW83119 Functional Diagram

Typical Application Circuits

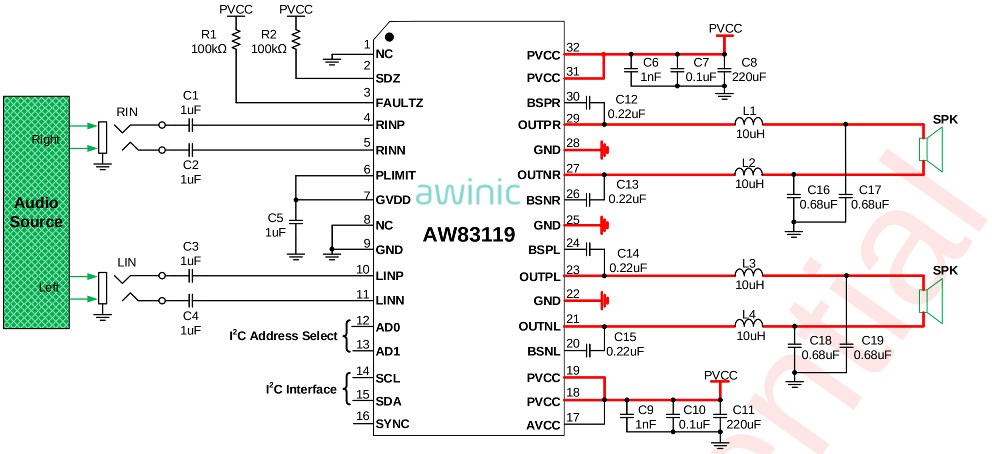


Figure 4 AW83119 Typical Application Diagram

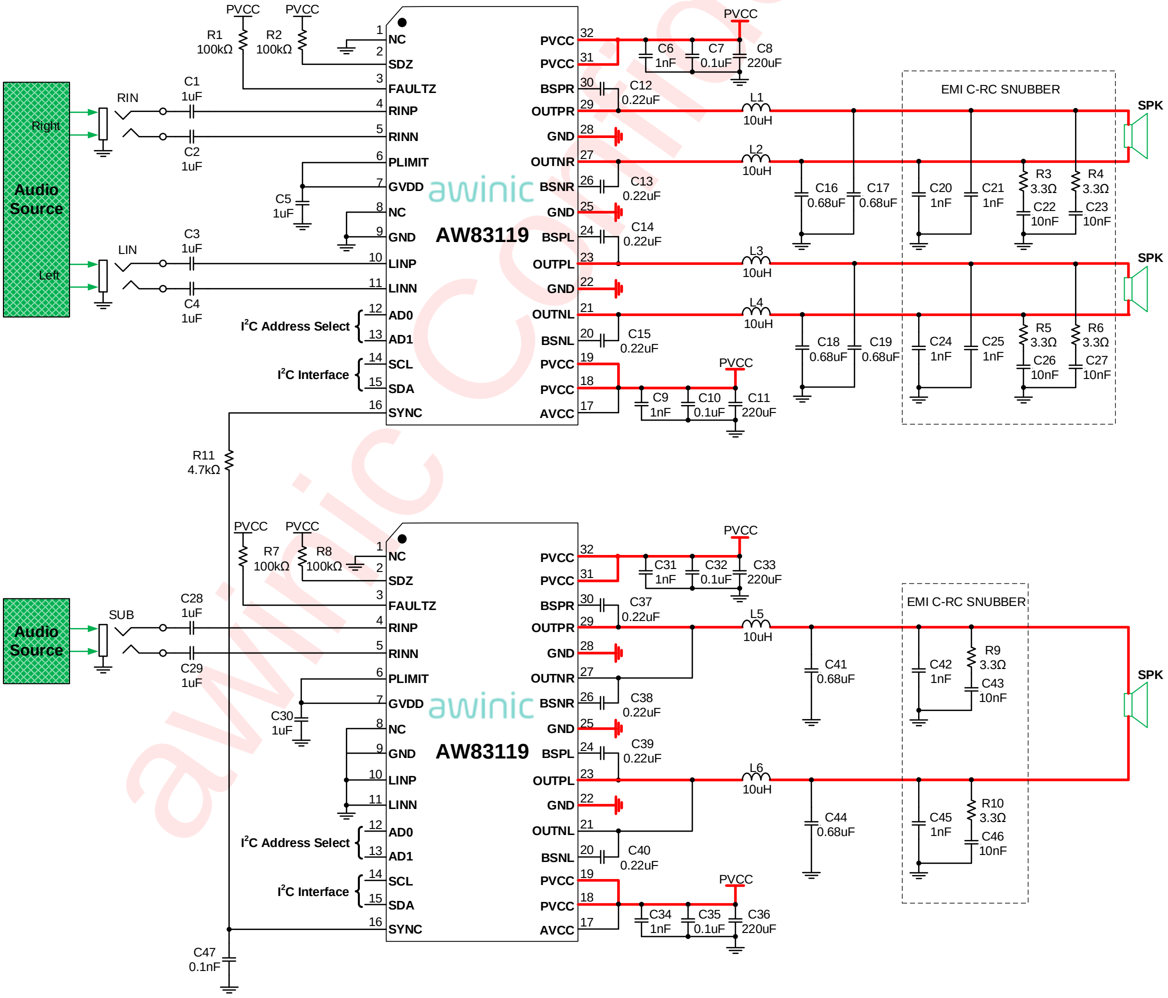


Figure 5 AW83119 2.1 Master and Slave Application Diagram[1]

Note1: In order to avoid conflict with other I2C device address in AW83119 2.1 Master and Slave Application, can pull up or pull down AD0 and AD1 pins of AW83119 to set the I2C device address, respectively.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW83119TSR	-40°C～85°C	ETSSOP 11mmX8.1mm -32L	BFQE	MSL3	ROHS+HF	2500 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage range	PVCC, AVCC	-0.3V to 30V
Input voltage range	INPL, INNL, INPR, INNR, AD0, AD1, SCL, SDA	-0.3V to 6V
	PLIMIT, SYNC	-0.3V to GVDD+0.3V
	SDZ	-0.3V to PVCC+0.3V
Output voltage range	FAULTZ	-0.3V to PVCC+0.3V
	GVDD, OUTNL, OUTPL, OUTNR, OUTPR	-0.3V to PVCC+0.3V
Junction-to-ambient thermal resistance θ_{JA}		20.34°C /W
Operating free-air temperature range		-40°C to 85°C
Maximum operating junction temperature T_{JMAX}		165°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD(Including CDM HBM MM)(NOTE 2)		
PVCC PIN HBM		±2kV
Other PIN HBM		±2kV
CDM		±1.5kV
Latch-up		
Test condition: JESD78E		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001

Electrical Characteristics

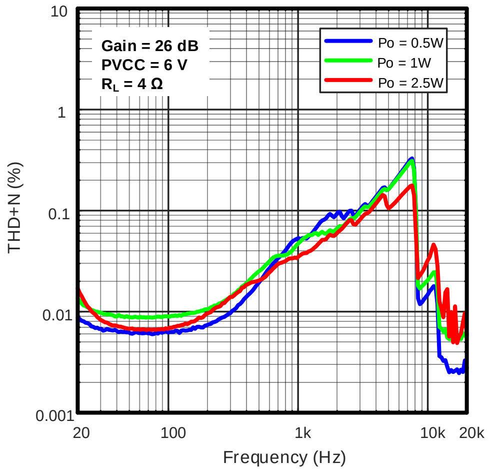
AVCC=PVCC=12V to 24V, RL=4Ω, T_A=25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	PVCC, AVCC	4.5		26	V
V_{IH}	High-level input voltage	SDZ, SYNC	2			V
		AD0, AD1, SDA, SCL	1.3			V
V_{IL}	Low-level input voltage	SDZ, SYNC			0.8	V
		AD0, AD1, SDA, SCL			0.8	V
V_{OL}	Low-level output voltage	FAULTZ, $R_{PULL-UP}$=100kΩ, PVCC=26V			0.8	V
I_{IH}	High-level input current	SDZ (V_I=2V, PVCC=18V)			5	μA
R_L(BTL)	Minimum load impedance	Output filter: L=10μH, C=680nF	3.2	4		Ω
R_L(PBTL)		Output filter: L=10μH, C=1μF	1.6	2		Ω
L_O	Output-filter inductance	Minimum output filter inductance under short-circuit condition	2			μH
DC						
$\|V_{OS}\|$	Class-D output offset voltage (measured differentially)	VI=0V, Gain=36dB			30	mV
I_{CC}	Quiescent supply current	SDZ=2V, No load or filter, PVCC=12V		17		mA
		SDZ=2V, No load or filter, PVCC=24V		23		
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	SDZ=0.8V, No load or filter, PVCC=12V		20		μA
		SDZ=0.8V, No load or filter, PVCC=24V		30		
$r_{DS(on)}$	Drain-source on-state resistance, measured pin to pin	PVCC=21V, I_{out}=500mA, T_J=25°C		100		mΩ
G	Gain (BTL)	MAST_SLV=0,GAIN[1:0]=00		20		dB
		MAST_SLV=0,GAIN[1:0]=01		26		
		MAST_SLV=0,GAIN[1:0]=10		32		
		MAST_SLV=0,GAIN[1:0]=11		36		
	Gain (SLV)	MAST_SLV=1,GAIN[1:0]=00		20		
		MAST_SLV=1,GAIN[1:0]=01		26		
		MAST_SLV=1,GAIN[1:0]=10		32		
		MAST_SLV=1,GAIN[1:0]=11		36		
t_{on}	Turn-on time	SDZ=2V		40		ms
t_{off}	Turn-off time	SDZ=0.8V		2		μs

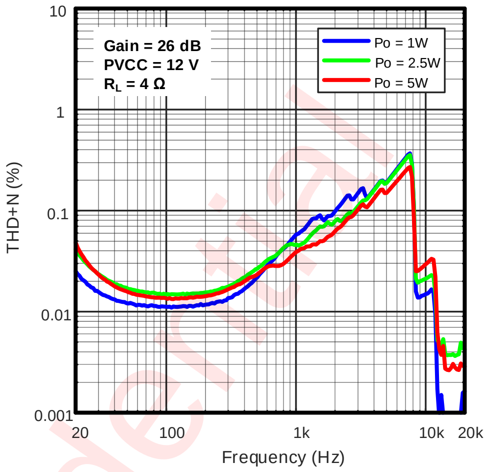
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
GVDD	Gate drive supply	I_{GVDD}<200μA	5.4	5.75	6.6	V
V_O	Output voltage maximum under PLIMIT control	V_{PLIMIT}=2V, V_I=1Vrms	8.5	10	11.5	V
AC						
PSRR	Power supply ripple rejection	200mVpp ripple at 1kHz，Gain=20dB，Inputs AC-coupled to GND		70		dB
P_O	Continuous output power	THD+N=10%, f=1kHz, PVCC=15V		25.5		W
		THD+N=10%, f=1kHz, PVCC=21V		53.5		
THD+N	Total harmonic distortion + noise	VCC=21V, f=1kHz, PO=25W		0.05		%
Vn	Output integrated noise	20-20kHz, A-weighted filter, Gain=20dB		65		μV
				-84		dBV
	Crosstalk	V_O=1Vrms, Gain=20dB, f=1kHz		-100		dB
SNR	Signal-to-noise ratio	THD+N<1%, f=1kHz, Gain=20dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency	FSW[2:0]=000		400		kHz
		FSW[2:0]=001		500		
		FSW[2:0]=010		600		
		FSW[2:0]=011		1000		
		FSW[2:0]=100		1200		
		FSW[2:0]=101		300		
		FSW[2:0]=110	Reserved			
		FSW[2:0]=111	Reserved			
T_{OT}	Thermal trip point			160		°C
$T_{OT,\ hys}$	Thermal hysteresis			25		°C
I_{OC}	Over current trip point			9.5		A

Typical Characteristics

fosc=400kHz, BD Mode, T_A=25°C (unless otherwise noted).



THD+N (BTL) vs Frequency



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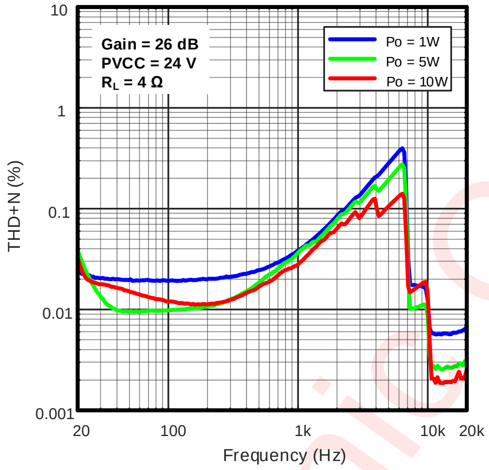

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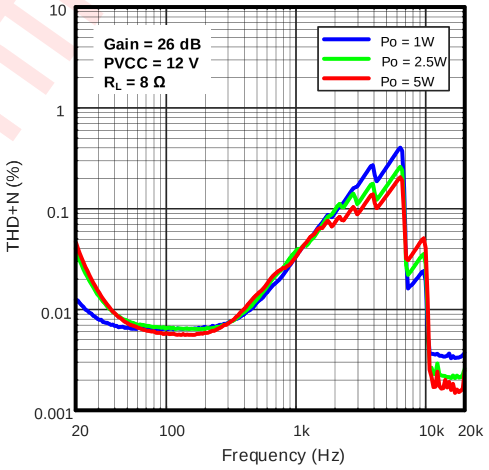

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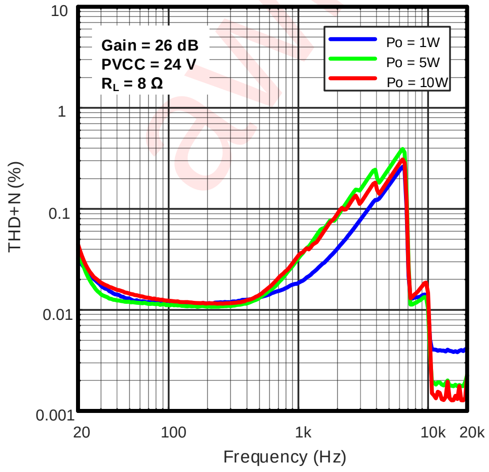

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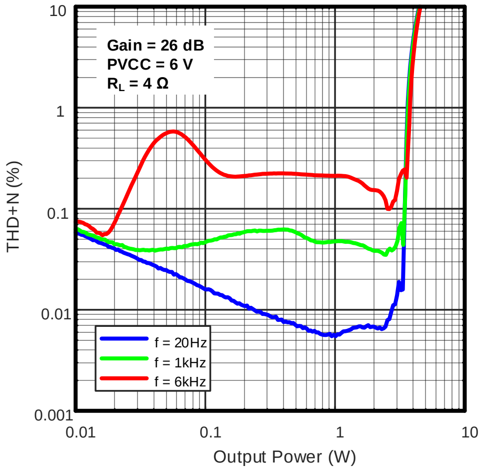
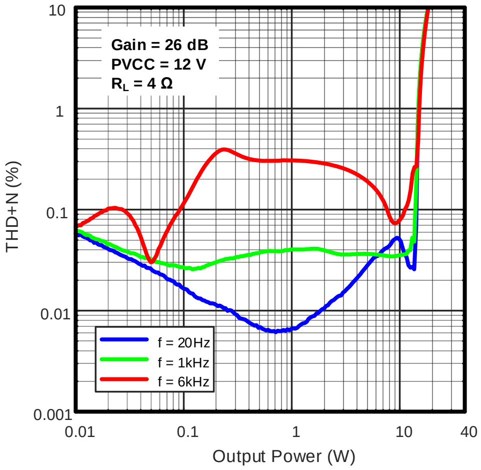


THD+N (BTL) vs Po



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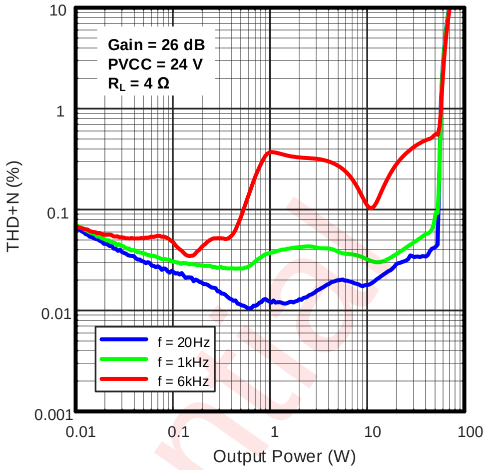

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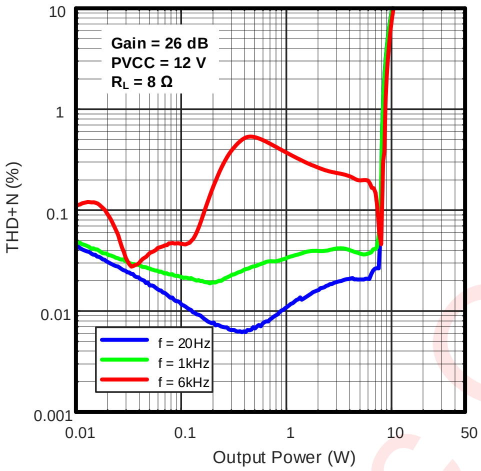

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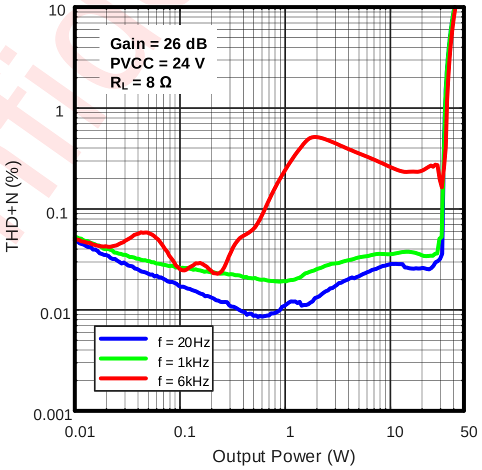

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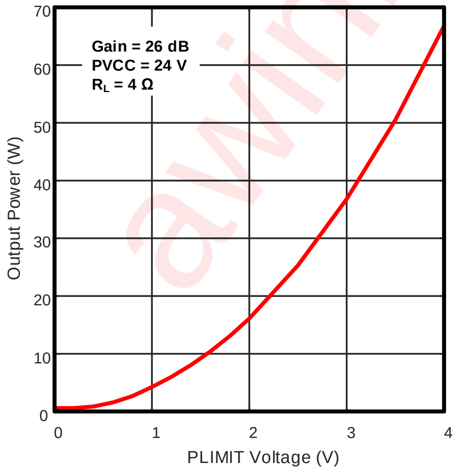
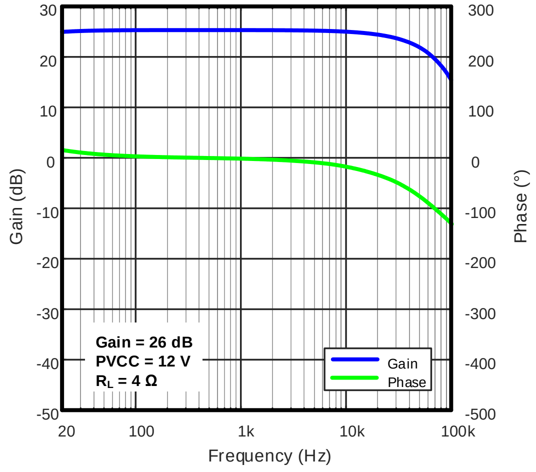
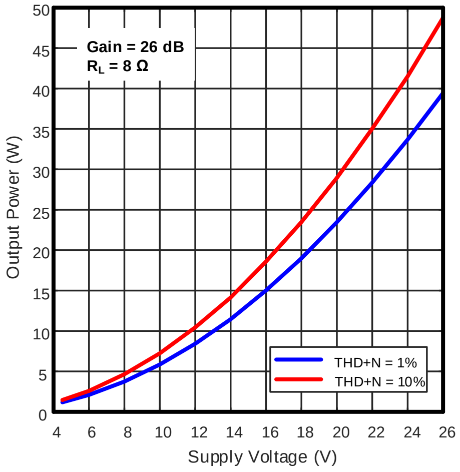


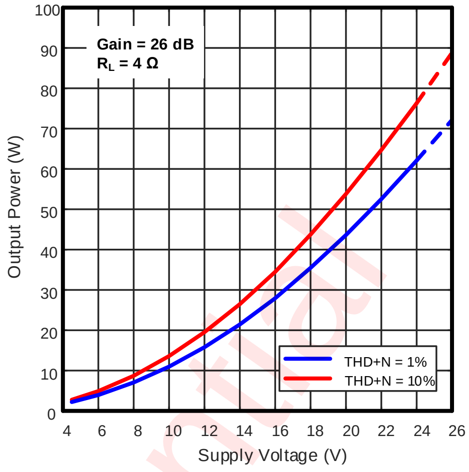
Po (BTL) vs PLIMIT Voltage



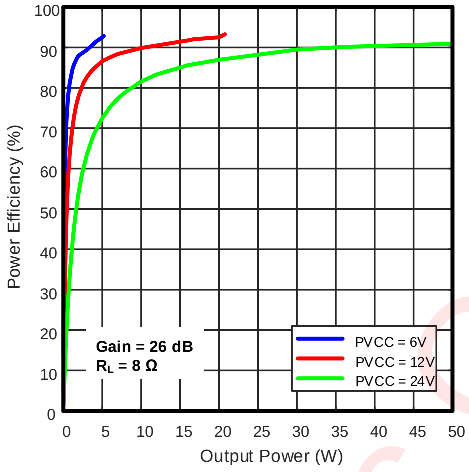
Gain/Phase (BTL) vs Frequency



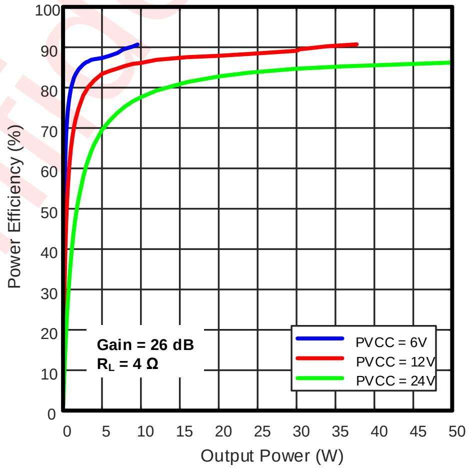
Po (BTL) vs Supply Voltage



Po (BTL) vs Supply Voltage



Efficiency (BTL) vs Po



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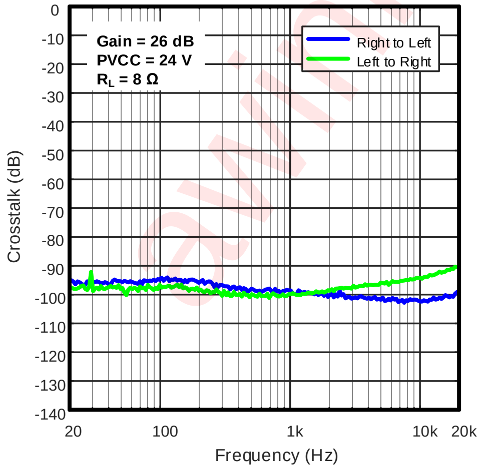
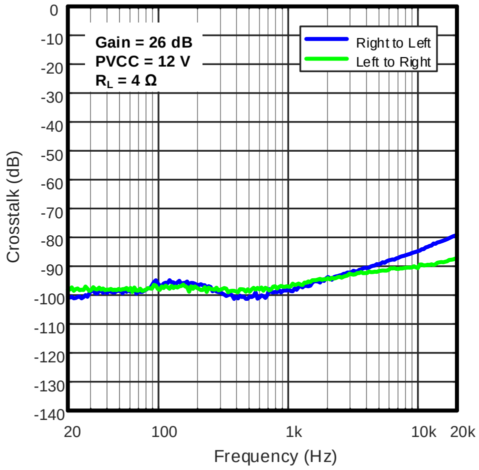
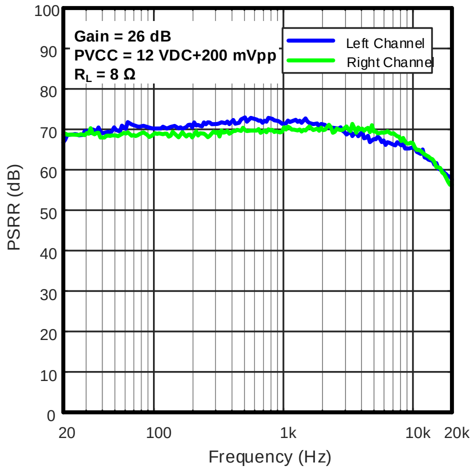


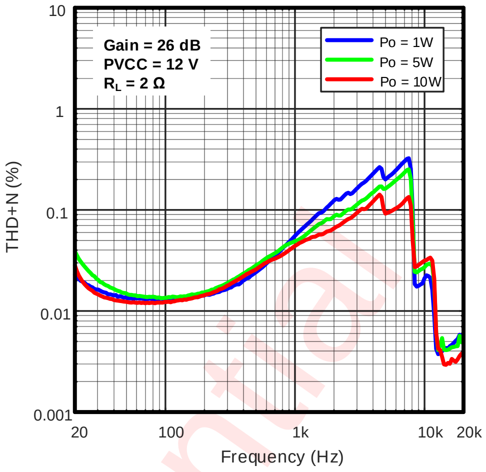
Crosstalk (BTL) vs Frequency



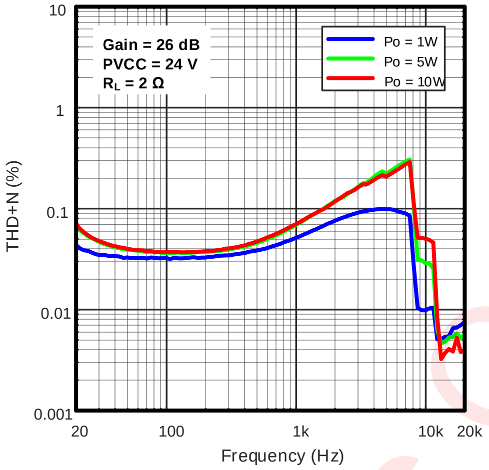
Crosstalk (BTL) vs Frequency



PSRR (BTL) vs Frequency



THD+N (PBTL) vs Frequency



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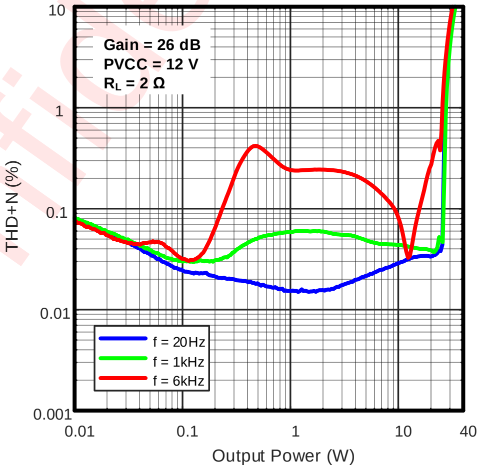
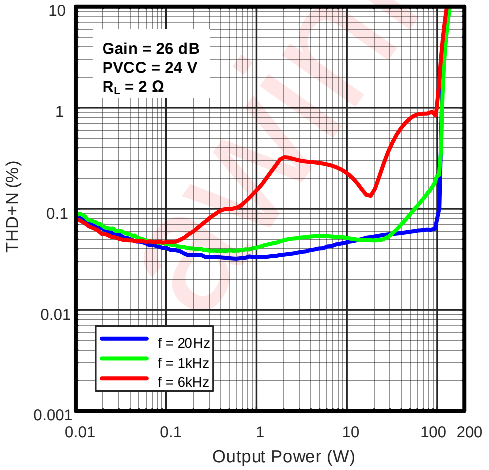
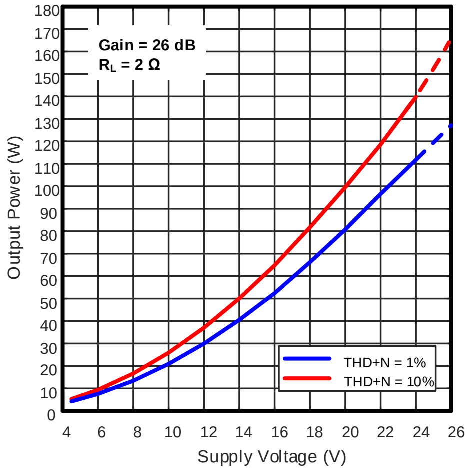


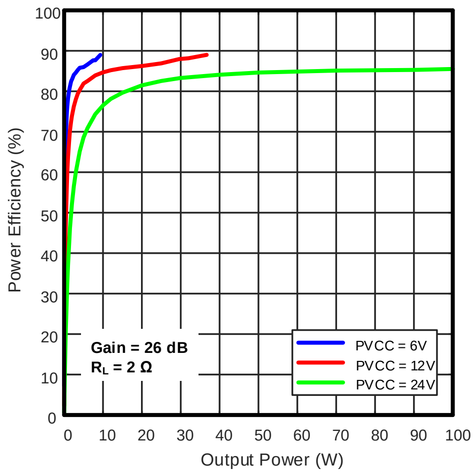
THD+N (PBTL) vs Po



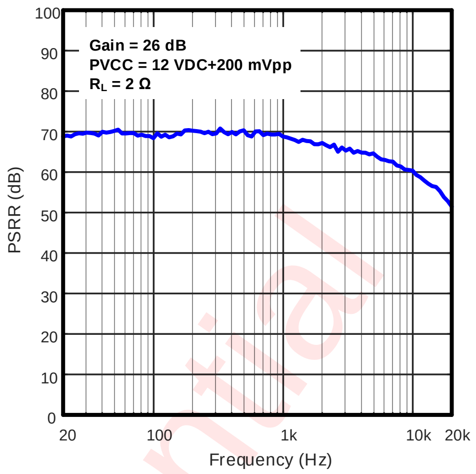
THD+N (PBTL) vs Po



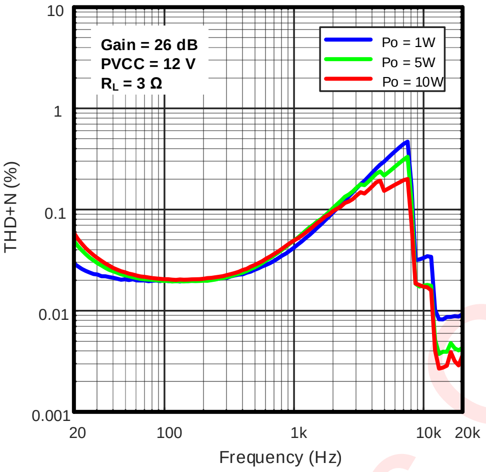
Po (PBTL) vs Supply Voltage



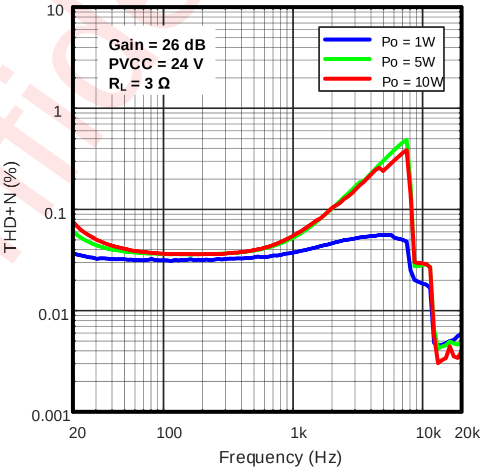
Efficiency (PBTL) vs Po



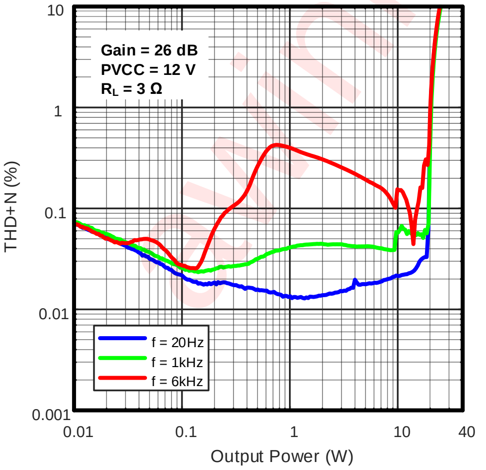
PSRR (PBTL) vs Frequency



THD+N (PBTL) vs Frequency



THD+N (PBTL) vs Frequency



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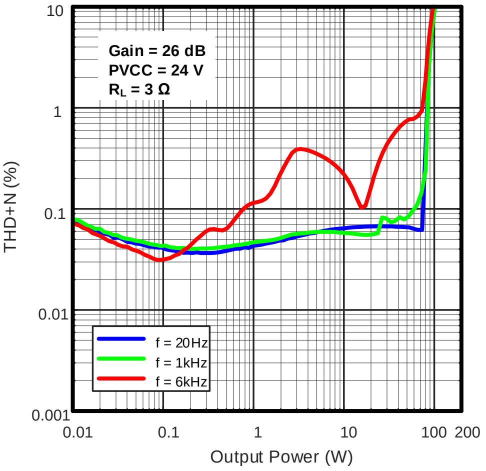
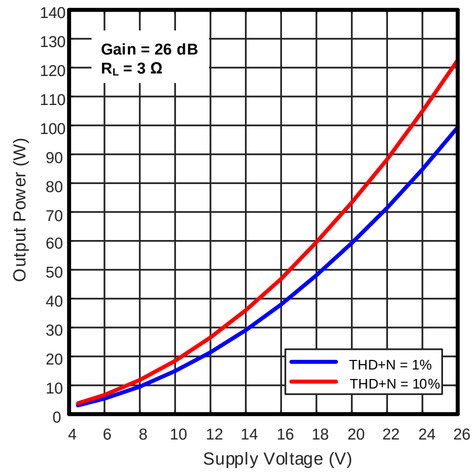
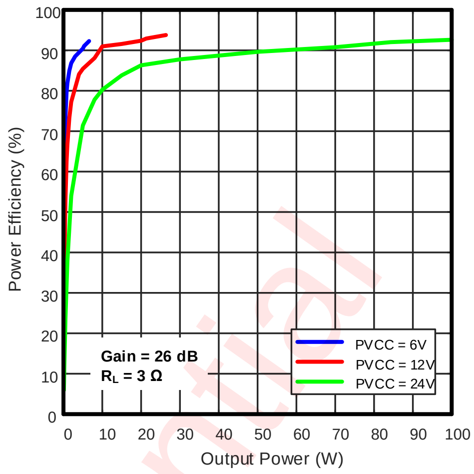


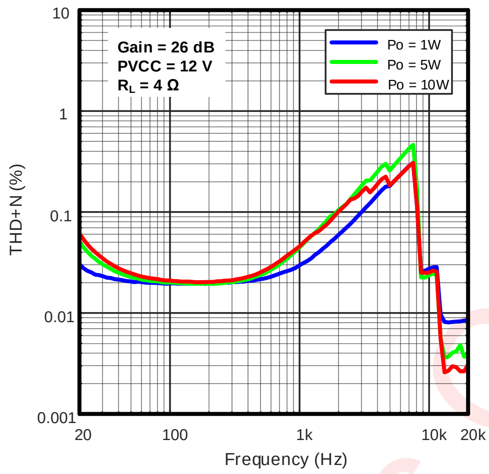
THD+N (PBTL) vs Po



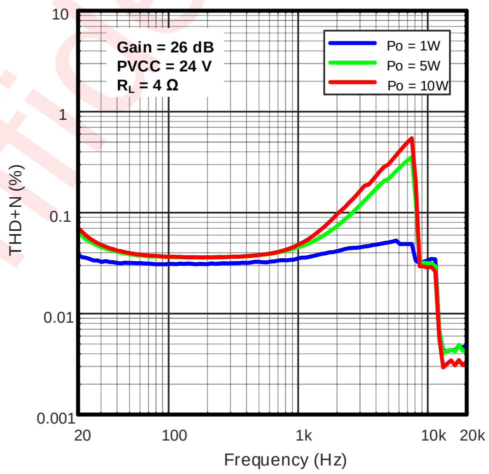
Po (PBTL) vs Supply Voltage



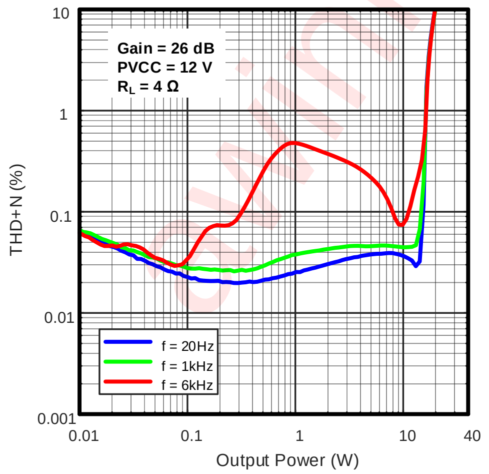
Efficiency (PBTL) vs Po



THD+N (PBTL) vs Frequency



THD+N (PBTL) vs Frequency



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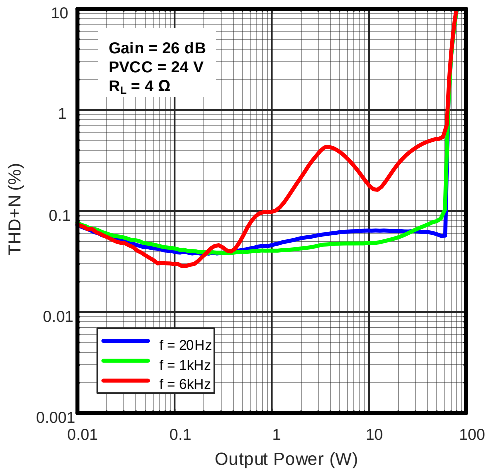
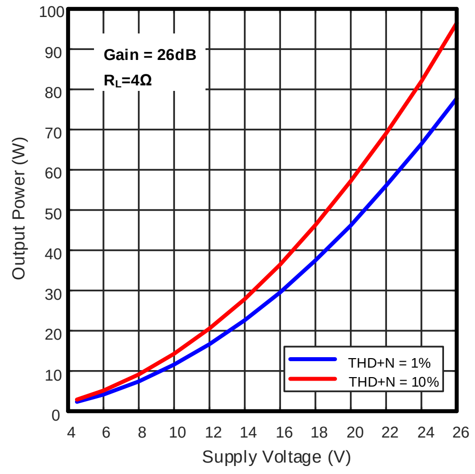
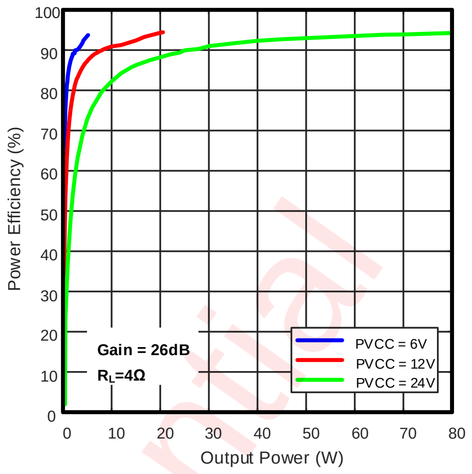


THD+N (PBTL) vs Po



Po (PBTL) vs Supply Voltage



Efficiency (PBTL) vs Po

Note: Dashed lines represent thermally limited region for the continuous output power.

Detailed Functional Description

The AW83119 device is a highly efficient and highly integrated Class D audio amplifier with I^2C control. The amplifier is designed for driving 60W/4Ω speakers in PBTL mode, and driving 2×30W/8Ω speakers in dual channel BTL mode under 4.5~26V PVCC supply voltage.

Gain Setting and Master/Slave Mode

The gain of the AW83119 is selected via register GAIN (Register Address 0x00h –D[6:5]). Master or Slave mode is set via register MAST_SLV (Register Address 0x00h –D[4]). The first four stages sets the GAIN in Master mode in gains of 20, 26, 32, 36 dB respectively, while the next four stages sets the GAIN in Slave mode in gains of 20, 26, 32, 36 dB respectively. Table 1 lists the recommended register values and the state and gain:

Table 1 Gain and Master/Slave

MASTER / SLAVE MODE	MAST_SLV	GAIN[1:0]	GAIN	INPUT IMPEDANCE
Master	0	00	20 dB	60 kΩ
Master	0	01	26 dB	30 kΩ
Master	0	10	32 dB	15 kΩ
Master	0	11	36 dB	9 kΩ
Slave	1	00	20 dB	60 kΩ
Slave	1	01	26 dB	30 kΩ
Slave	1	10	32 dB	15 kΩ
Slave	1	11	36 dB	9 kΩ

In Master mode, SYNC terminal is an output, in Slave mode, SYNC terminal is an input for a clock input. TTL logic levels with compliance to GVDD. If SYNC terminal is provided by an external platform as a clock input in Slave mode, it must be given before SDZ goes high level voltage.

Startup and Shutdown Operation

The AW83119 employs a shutdown mode of operation designed to reduce supply current (Icc) to the absolute minimum level during periods of nonuse for power conservation. The SDZ input terminal should be held high during normal operation when the amplifier is in use. Pulling SDZ low will put the outputs to mute and the amplifier to enter a low-current state. It is not recommended to leave SDZ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply.

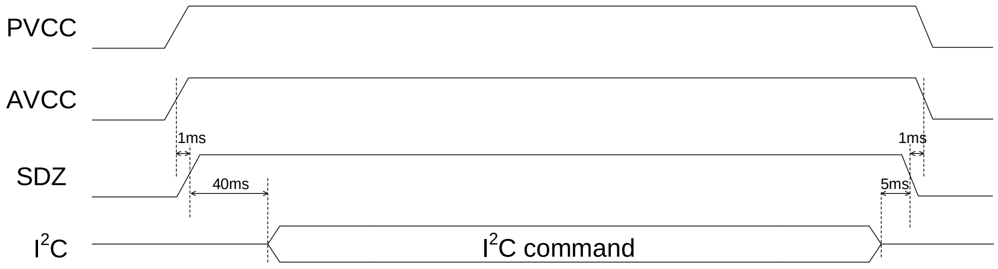


Figure 6 Startup and shutdown Sequence

Differential Inputs

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the AW83119 with a differential source, connect the positive lead of the audio source to the RINP or LINP input and the negative lead from the audio source to the RINN or LINN input. To use the AW83119 with a single-ended source, ac ground the negative input through a capacitor equal in value to the input capacitor on positive and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible. This is to allow the input dc blocking capacitors to become completely charged during the 10 ms power-up time. If the input capacitors are not allowed to completely charge, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.

Device Protection System

The AW83119 contains a complete set of protection circuits carefully designed to make system design efficient as well as to protect the device against any kind of permanent failures due to short circuits, overload, over temperature, and under-voltage. The FAULTZ pin will signal if an error is detected according to Table 2:

Table 2 Fault Reporting

FAULT	TRIGGERING CONDITION (typical value)	FAULTZ	ACTION	SELF-CLEARING/ LATCHED
Under Voltage on PVCC	PVCC < 4.1V	-	Output high impedance	Self-clearing
Over Voltage on PVCC	PVCC > 29V	-	Output high impedance	Self-clearing
Over Current	Output short or short to PVCC or GND	Low	Output high impedance	Latched
Over Temperature	T_j> 160℃	Low	Output high impedance	Latched
Too High DC Offset	DC output voltage	Low	Output high impedance	Latched

Short-Circuit Protection and Automatic Recovery Feature

The AW83119 has protection from over current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the FAULTZ pin as a low state. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged. The AW83119 can automatic recovery from the short circuit protection latch.

Thermal Protection

Thermal protection on the AW83119 prevents damage to the device when the internal die temperature exceeds 160°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal trip point, the device enters into the shutdown state and the outputs are disabled. This is a latched fault.

Thermal protection faults are reported on the FAULTZ terminal as a low state. The AW83119 can automatic recovery from the thermal protection latch.

Thermal Foldback

The Thermal Foldback (TFB), is designed to protect AW83119 from excessive die temperature increases, in case the device operates beyond the recommended temperature/power limit, or with a weaker thermal system design than recommended. It allows the AW83119 to play as loud as possible without triggering unexpected thermal shutdown. When the die temperature triggers the over-temperature warning level (140°C), an internal AGC (Automatic Gain Control) will reduce the gain gradually. Once the die temperature drops below the over-temperature warning level, the device's gain gradually returns to the former setting. The TFB gain regulation speed (attack time and release time) settings are the same as a regular AGC, which is also configurable with register TFB_AT_SEL (0x01h) and TFB_RT_SEL (0x01h).

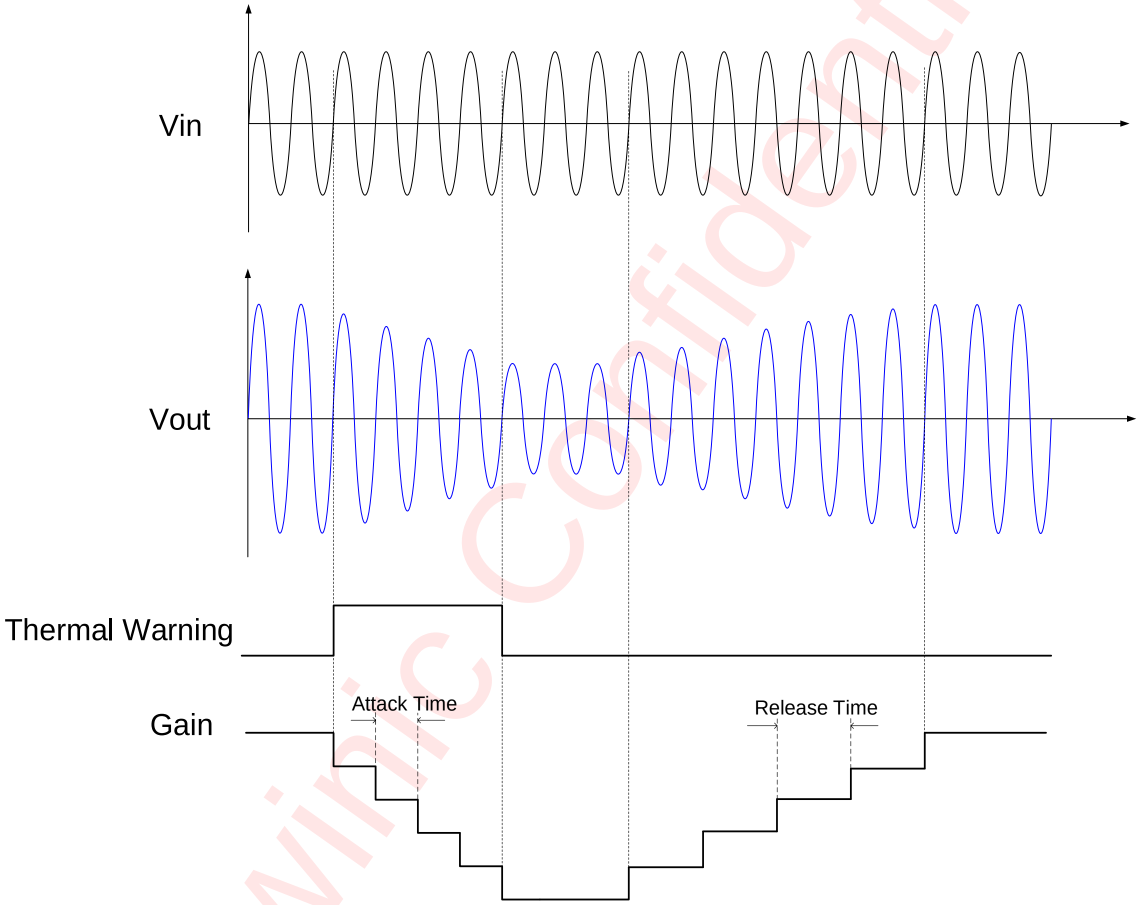


Figure 7 Thermal Foldback Operation Principle

DC Detect Protection

The AW83119 has circuitry which will protect the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault will be reported on the FAULT pin as a low state. The DC Detect fault will also cause the amplifier to shutdown by changing the state of the outputs to Hi-Z. AW83119 can automatic recovery from the DC Detect protection latch.

A DC Detect Fault is issued when the output differential duty-cycle of either channel exceeds 63% for more than 625 msec at the same polarity. Table 3 below shows some examples of the typical DC Detect Protection threshold for several values of the supply voltage. This feature protects the speaker from large DC currents or AC currents less than 2Hz. To avoid nuisance faults due to the DC detect circuit, hold the SDZ pin low at power up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

Table 3 lists the minimum output offset voltage required to trigger the DC detect. The outputs must remain at or above the voltage listed in the table for more than 625 msec to trigger the DC detect.

Table 3 DC Detect Threshold

PVCC(V)	VOS-OUTPUT OFFSET VOLTAGE（V）
4.5	1.17
6	1.56
12	3.12
18	4.68

PLIMIT Operation

The AW83119 has a built-in voltage limiter that can be used to limit the output voltage level below the supply rail, the amplifier simply operates as if it was powered by a lower supply voltage, and thereby limits the output power. Add a resister divider from GVDD to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Add a 1μF capacitor from pin PLIMIT to ground to ensure stability.

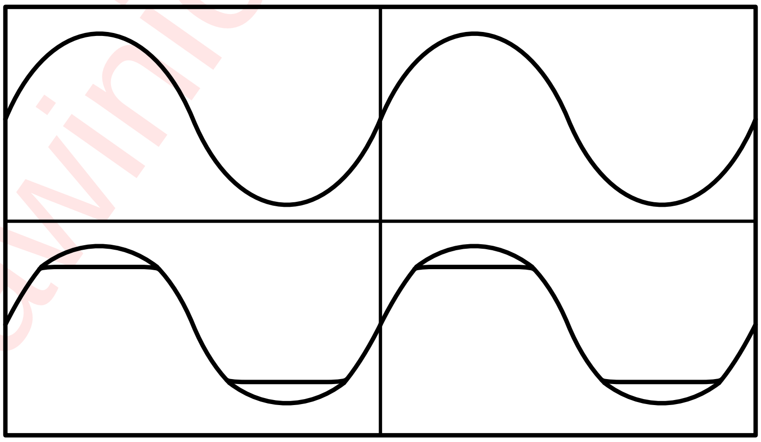


Figure 8 Power Limit Example

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to a fixed maximum value. This limit can be thought of as a “virtual” voltage rail which is lower than the supply connected to PVCC. This “virtual” rail is approximately 5 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT}(unclipped) = \frac{\left(\left(\frac{R_L}{R_L + 2 * R_S}\right) * V_P\right)^2}{2 * R_L}$$

where

R_L is the load resistance.

R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.

V_P is the peak amplitude, $V_P = 5 \times$ PLIMIT voltage.

Table 4 Power Limit Voltage

PVCC (V)	PLIMIT VOLTAGE (V)[1]	R to GND	R to GVDD	OUTPUT VOLTAGE (V_{rms})
12	1.2	18 kΩ	68 kΩ	6.19
12	1.84	24 kΩ	51 kΩ	9.02
12	GVDD	Open	Short	10.71
24	2	24 kΩ	45 kΩ	9.53
24	2.7	45 kΩ	51 kΩ	12.45
24	GVDD	Open	Short	18.06

(1) PLIMIT measurements taken with EVM gain set to 26dB and input voltage set to $1V_{rms}$.

Device Modulation Scheme

The AW83119 has the option of running in either BD modulation or Low-Loss modulation; this is set by register EN_LLM (0x00h).

EN_LLM=0: BD modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0V to the supply voltage. The OUTP and OUTN are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0V throughout most of the switch period, reducing the switching current, which reduces any I^2R losses in the load.

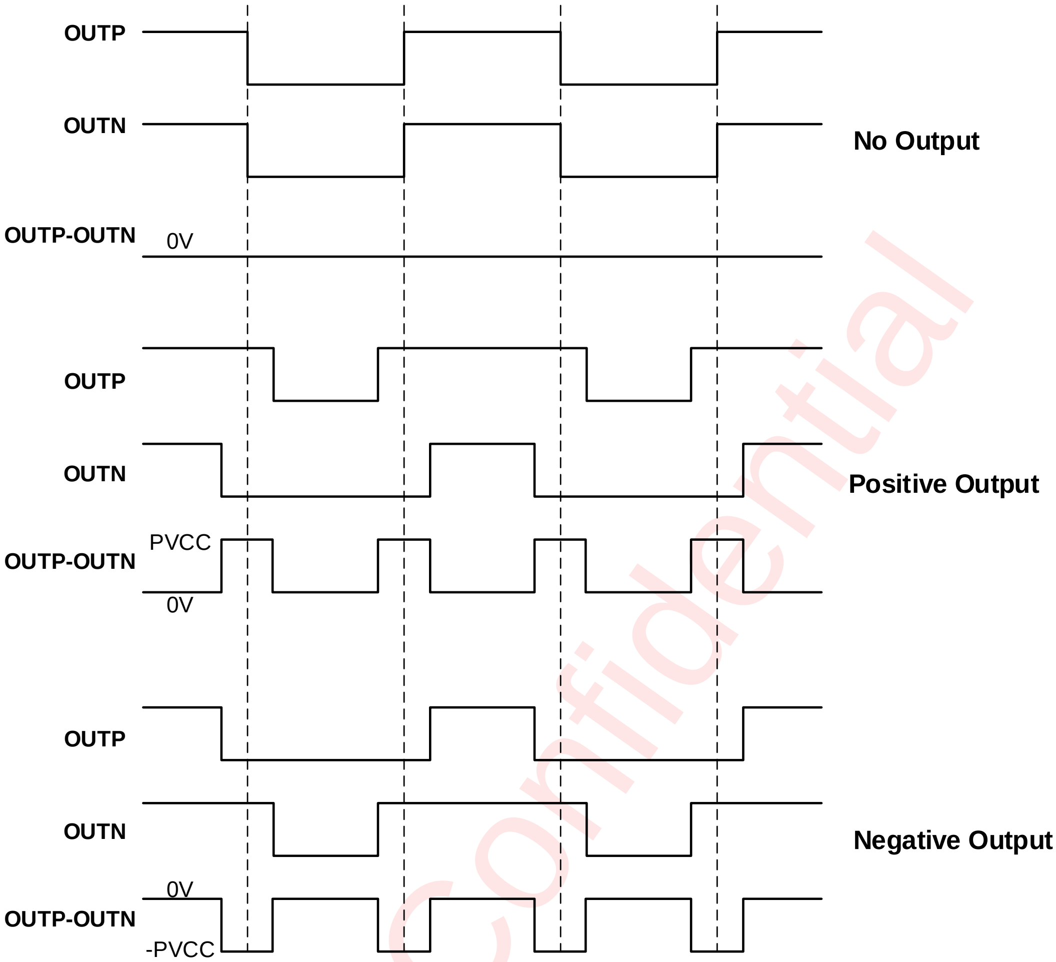


Figure 9 BD Mode Modulation

EN_LLM=1: Low-Loss modulation

The Low-Loss mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In Low-Loss mode the outputs operate at 20% modulation during idle conditions. When an audio signal is applied one output will decrease and one will increase. The decreasing output signal will quickly rail to GND at which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses. The THD penalty in Low-Loss mode is minimized by the high performance feedback loop. The resulting audio signal at each half output has a discontinuity each time the output rails to GND. This can cause ringing in the audio reconstruction filter unless care is taken in the selection of the filter components and type of filter used.

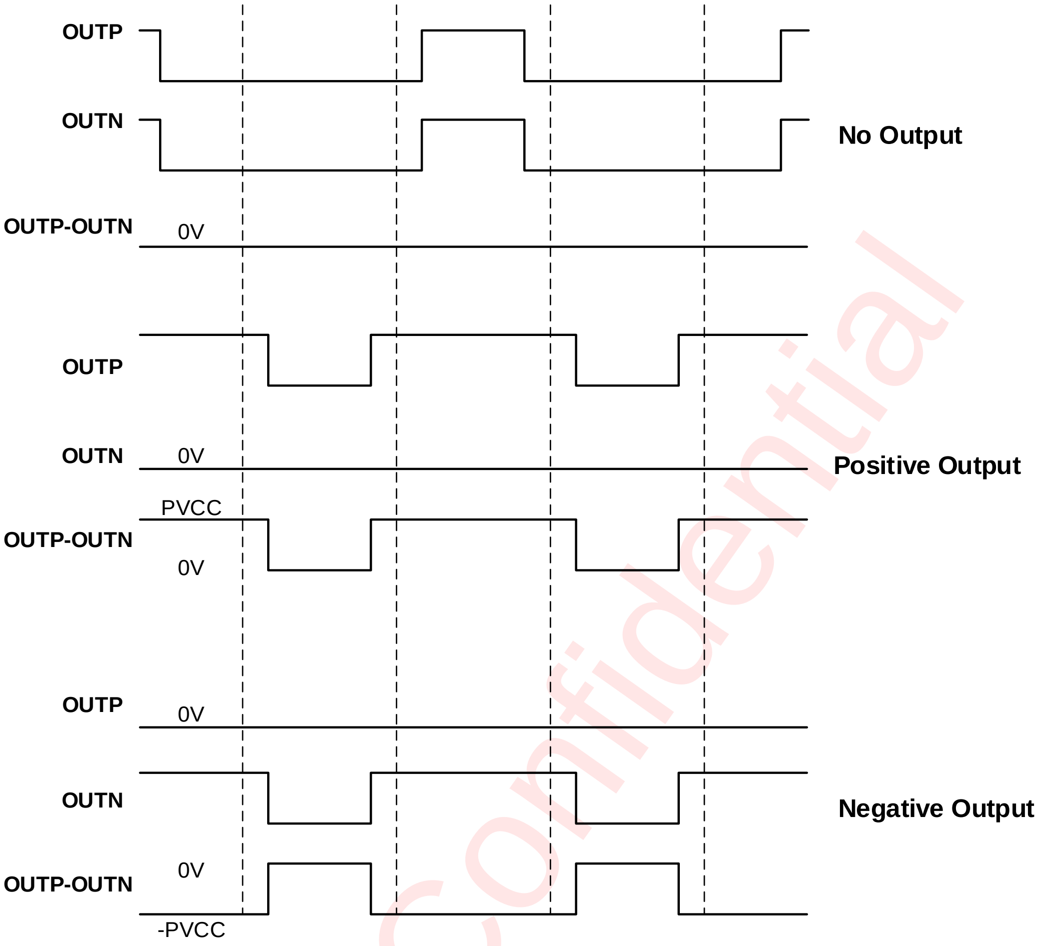


Figure 10 Low-Loss Mode Modulation

AM Avoidance EMI Reduction

To reduce interference in the AM radio band, the AW83119 has the ability to change the modulation frequency via register FSW (0x00h). The recommended frequencies are listed in Table 5. The fundamental frequency and its second harmonic straddle the AM radio band listed. This eliminates the tones that can be present due to the modulation frequency being demodulated by the AM radio.

Table 5 AM Frequencies

US	EUROPEAN	Modulation Frequency(kHz)	FSW[2]	FSW[1]	FSW[0]
AM Frequency(kHz)	AM Frequency(kHz)				
	522-540	300	1	0	1
540-917	540-914	1200	1	0	0
917-1125	914-1122	600	0	1	0
1125-1375	1122-1373	1000	0	1	1
1375-1547	1373-1548	1000	0	1	1
1547-1700	1548-1701	1000	0	1	1

Spread Spectrum

AW83119 supports spread spectrum(1) control the modulation frequency to improve EMI performance. User need configure register SS_CON (0x02h) to enable spread spectrum, select spread spectrum frequency with register FSW (0x00h). AW83119 spread spectrum range is 12%.

Output spectrums of the AW83119 is different whether or enable spread spectrum by configure register SS_CON (0x02h). Figure 12 is output spectrum of FSW=001, SS_CON=0, and Figure 13 is output spectrum when SS_CON=1, FSW=001, fsw=500kHz±12%.

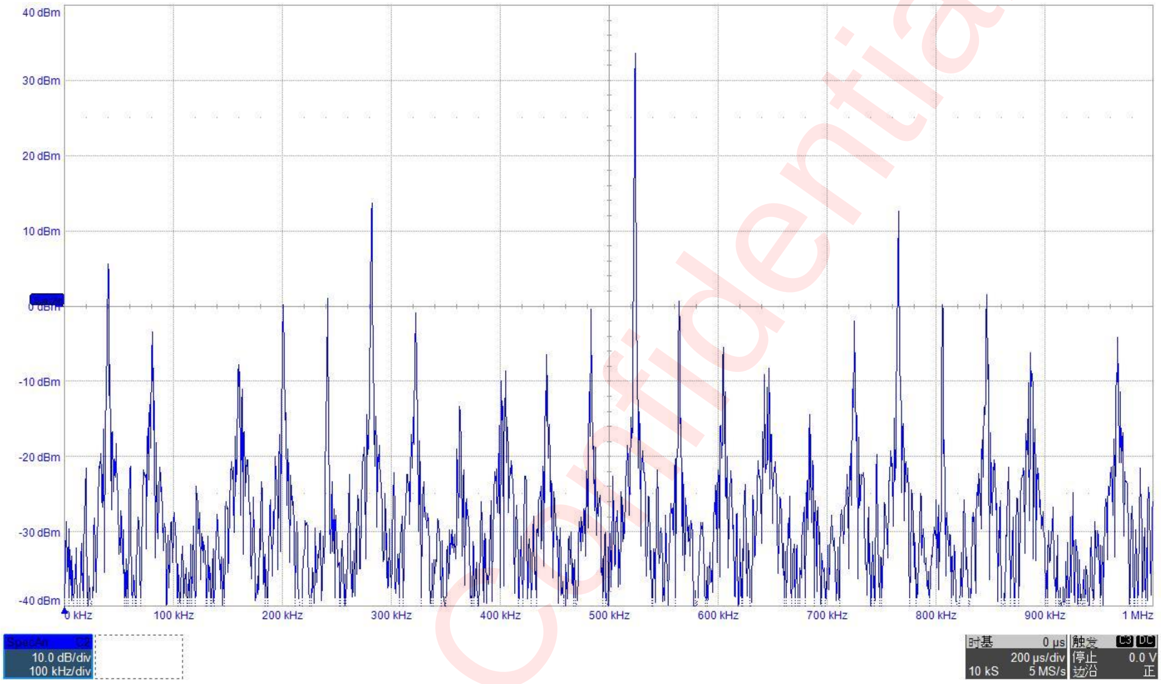


Figure 11 FSW=001, fsw=500kHz, Output spectrum of the AW83119

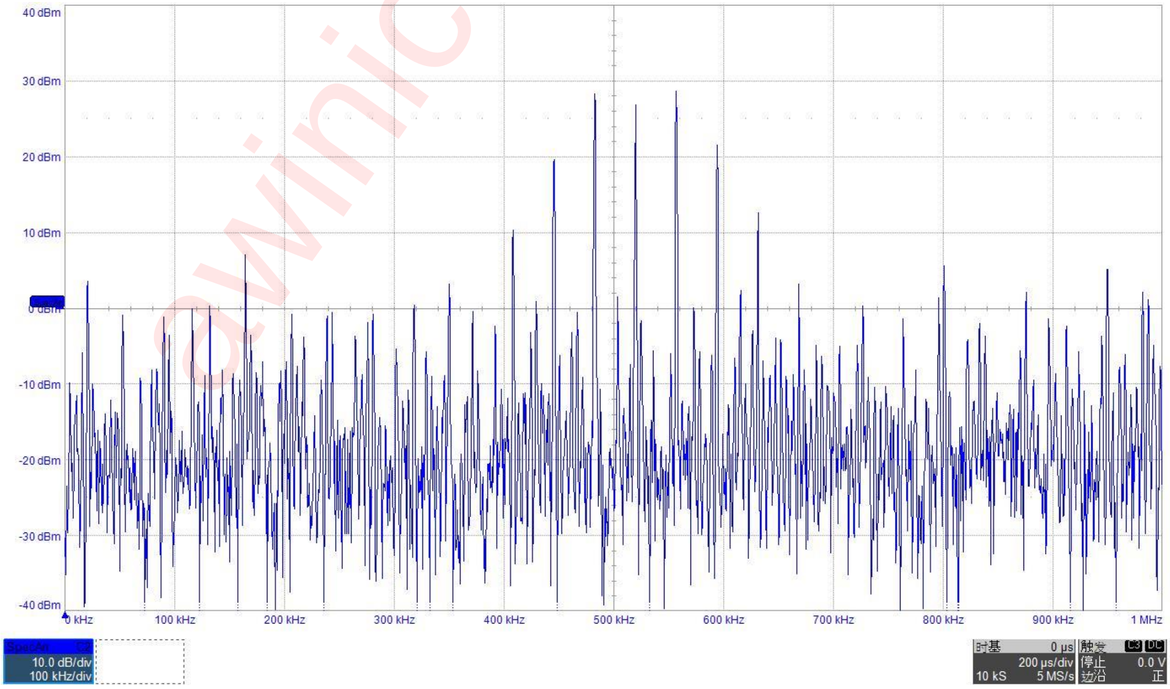


Figure 12 FSW=001, fsw=500kHz±12%, Output spectrum of the AW83119

(1) It is noted that Slave Mode does not supported spread spectrum control the modulation frequency.

Phase Shift

AW83119 supports channel to channel 45/90/135/180-degree PWM phase shift to minimize the EMI. Configure register PWM_PHASE_CON (0x01h) to control the degree of PWM phase shift.

Channel to channel phase shift control the phase of output PWM such that the idle output PWM waveforms of the two audio channels are 45/90/135/180-degree PWM phase shift. Channel to channel phase shift does not affect the audio signal, or its polarity.

PBTL Mode

The AW83119 can be connected in PBTL mode enabling up to 100W output power. This is done by:

1) Connect INPL and INNL directly to Ground (without capacitors) this sets the device in PBTL mode during power up.

2) Analog input signal is applied to INPR and INNR.

3) Connect OUTPR and OUTNR together for the positive speaker terminal and OUTNL and OUTPL together for negative pin.

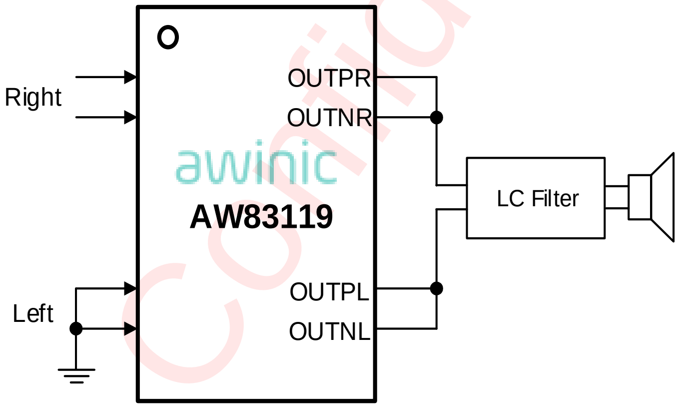


Figure 13 PBTL Mode

MONO Mode

The AW83119 can be connected in MONO mode to cut the idle power-loss nearly by half. This is done by:

1) Configure register MONO_EN=1 (0x00h) this sets the device in MONO mode.

2) Analog input signal is applied to INPL and INNL.

3) Connect OUTPL and OUTNL to speaker just like normal BTL mode.

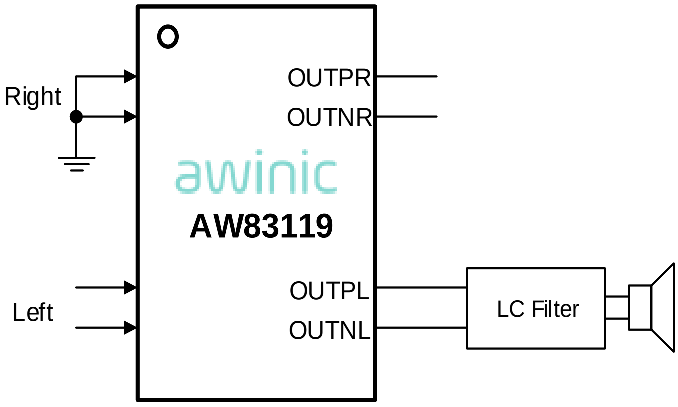


Figure 14 MONO Mode

I^{2}C Timing feature

Parameter			MIN	TYP	MAX	UNIT
No.	Sym	Name				
1	f_{SCL}	SCL Clock frequency			400	kHz
2	t_{LOW}	SCL Low level Duration	1.3			μs
3	t_{HIGH}	SCL High level Duration	0.6			μs
4	t_{RISE}	SCL, SDA rise time			0.3	μs
5	t_{FALL}	SCL, SDA fall time			0.3	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			μs
7	$t_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			μs
9	t_{BUF}	the Bus idle time START state to STOP state	1.3			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			μs
11	$t_{HD:DAT}$	SDA hold time	10			ns

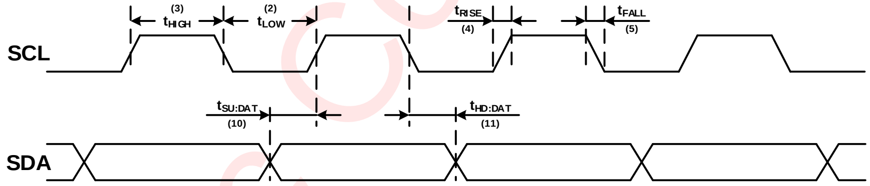


Figure 15 SCL and SDA timing relationships in the data transmission process

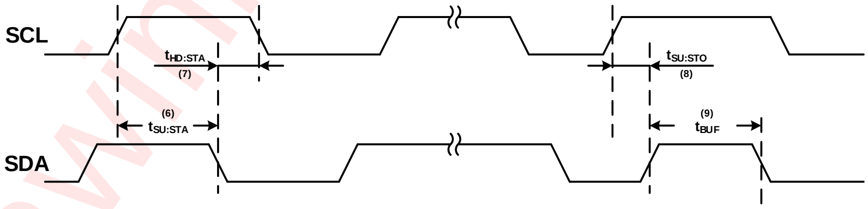


Figure 16 The Timing Relationship between START and STOP State

General I^{2}C Operation

The I^{2}C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The device is addressed by a unique 7-bit address; the same device can send and receive data. In addition, Communications equipment has distinguish master from slave device: In the communication process, only the master device can initiate a transfer and terminate data and generate a corresponding clock signal. The devices using the address access during transmission can be seen as a slave device.

SDA and SCL connect to the power supply through the current source or pull-up resistor. SDA and SCL default is a high level. All data to start transmission and end of transmission requires the main device to issue START state and STOP status:

START state：The SCL maintain a high level, SDA from high to low level

STOP state：The SCL maintain a high level, SDA pulled low to high level

Start and Stop states can be only generated by the master device. In addition, if the device does not produce STOP state after the data transmission is completed, instead re-generate a START state (Repeated START, Sr), and it is believed that this bus is still in the process of data transmission. Functionally, Sr state and START state is the same. As shown in Figure 17.

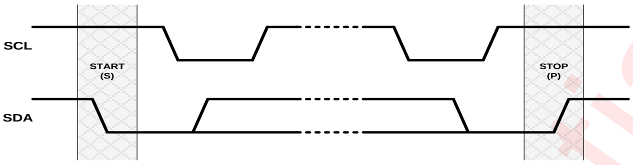


Figure 17 START and STOP State Generation Process

In the data transmission process, when the clock line SCL maintains a high level, the data line SDA must remain the same. Only when the SCL maintain a low level, the data line SDA can be changed, as shown in Figure 18. Each transmission of information on the SDA is 9 bits as a unit. The first eight bits are the data to be transmitted, and the first one is the most significant bit (Most Significant Bit, MSB), the ninth bit is an confirmation bit (Acknowledge, ACK or A), as shown in Figure 19. When the SDA transmits a low level in ninth clock pulse, it means the acknowledgment bit is 1, namely the current transmission of 8 bits data are confirmed, otherwise it means that the data transmission has not been confirmed. Any amount of data can be transferred between START and STOP state.

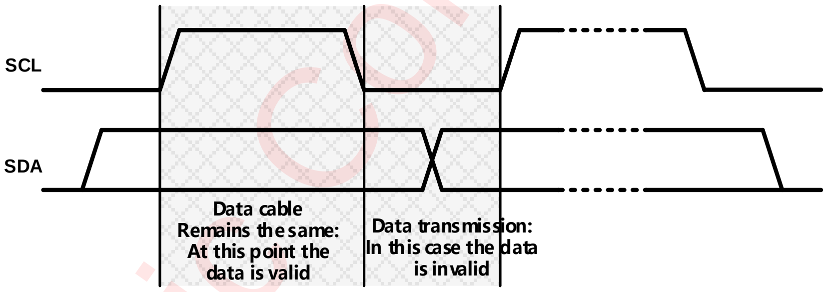


Figure 18 The Data Transfer Rules on the I2C Bus

The whole process of actual data transmission is shown in Figure 19. When generating a START condition, the master device sends an 8-bit data, including a 7-bit slave addresses (Slave Address), and followed by a "read / write" flag ($R/\overline{W}$). The flag is used to specify the direction of transmission of subsequent data. The master device will produce the STOP state to end the process after the data transmission is completed. However, if the master device intends to continue data transmission, you can directly send a Repeated START state, without the need to use the STOP state to end transmission.

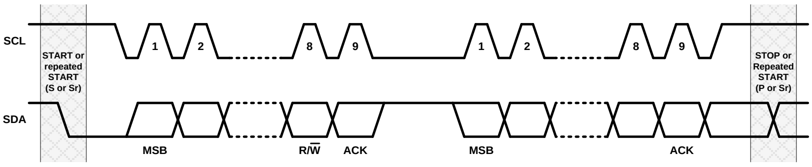


Figure 19 Data Transmission on the I2C Bus

I²C Read/Write Processes

The following describes two kinds of ways of the I²C bus data transmission:

Write Process

Writing process refers to the master device write data into the slave device. In this process, the transfer direction of the data is always unchanged from the master device to the slave device. All acknowledge bits are transferred by the slave device, in particular, AW83119 as the slave device, the transmission process in accordance with the following steps, as shown in Figure 20:

Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.

Master device transmits the 7-bits device address of the slave device, followed by the "read / write" flag (flag R/$\overline{W}$ = 0);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device transmits the 8-bit AW83119 register address to which the first data byte will written；

The slave device asserts an acknowledgment (ACK) bit to confirm the register address is correct;

Master sends 8 bits of data to register which needs to be written;

The slave device asserts an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

If the master device needs to continue transmitting data, it does not need further to send the register address for AW83119, within AW83119 each send confirmation bit(ACK) regret automatic accumulation register address then only need to repeat the sixth step and seven step:

The master device generates the STOP state to end the data transmission.

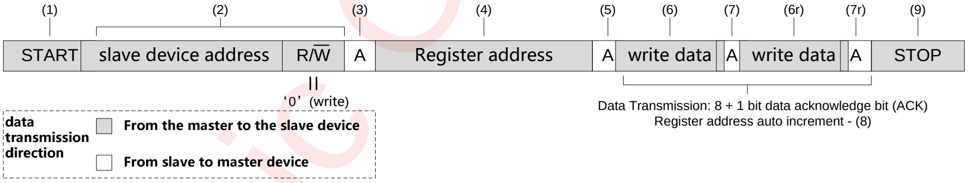


Figure 20 Writing Process (Data Transmission Direction Remains the Same)

Read Process

Reading process refers to the slave device reading data back to the master device. In this process, the direction of data transmission will change. Before and after the change, the master device sends START state and slave address twice, and sends the opposite "read/write" flag. In particular, AW83119 as the slave device, the transmission process carried out by following steps listed in Figure 21:

Master device asserts a start condition;

Master device transmits the 7 bits address of AW83119, and followed by a "read / write" flag (R/$\overline{W}$ = 0);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device sends the 8bit address that the AW83119 register needs to read the data;

The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;

The master device restarts the data transfer process by continuously generating STOP state and START state or a separate Repeated START.

Master sends 7-bits address of the slave device and followed by a read / write flag (flag R/$\overline{W}$ = 1) again.

The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not.

The master transmits 8 bits of data to register which needs to be read;

The slave device sends an acknowledgment bit (ACK) to confirm whether the data is sent successfully.

AW83119 automatically increment register address once after the slave sent each acknowledge bit (ACK).

The master device generates the STOP state to end the data transmission.

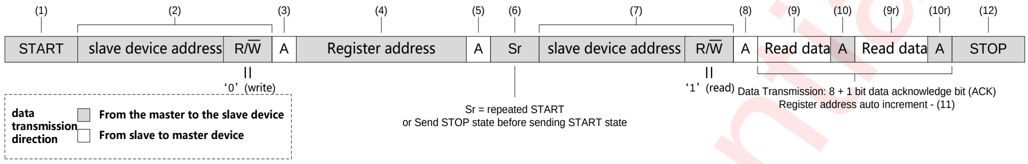


Figure 21 Reading Process (Data Transmission Direction Remains the Same)

Register Configuration

Register List

Write 55AA to the 08 register of the AW83119 to reset the register.

ADDR	NAME	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	**PINSET**	**RW**	0	0	0	0	0	0	0	EN_LLM	MONO_EN	GAIN		MAST_SLV	FSW			MUTE	0x0021
0x01	**CUSTOM0**	**RW**	0	0	0	0	0	0	0	0	TFB_RT_SEL			TFB_AT_SEL			PWM_PHASE_CON		0x0090
0x02	**CUSTOM1**	**RW**	TEST_EN		TFB_GAIN	0	VCOM_CON	SS_CON	0	1	0	CON_EDGE		DT_CON			0	0	0xC128
0x08	**SYSST**	**RO**	MAST_SLV__S	0	1	0	0	TFB_S	OCOT_S	DC_S	0	0	UVP_OVP_S	1	MONO_MD_S	LOWLOSS_MD_S	0	0	0x2010
0x09	**SYSINT**	**RC**	MAST_SLV__I	0	0	0	0	TFB_I	OCOT_I	DC_I	0	0	UVP_OVP_I	0	MONO_MD_I	LOWLOSS_MD_I	0	0	0x0000

AW83119's I^2C address is 10110A1A0H, as shown in Table 6, in order to avoid conflict with other I^2C devices address, you can pull up or pull down AD1 and AD0 pins of AW83119 to set the value of A1 and A0, respectively. The following lists specific information about all visible registers, including default values and programmable ranges.

Table 6 AW83119 Address Byte

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	0	1	1	0	A1	A0	R/W

According to the above table, if A1A0=00, the I2C device address is defined as '1011000'(58H). A1A0=01, the I2C device address is defined as '1011001'(59H). A1A0=10, the I2C device address is defined as '1011010'(5AH). A1A0=11, the I2C device address is defined as '1011011'(5BH).

Register Detailed Description

PINSET: (Address 00h)

Bit	Symbol	R/W	Description	Default
15:10	IDCODE	R	Chip ID will be returned after reading.	00
9	RESERVED	R	Reserved.	0
8	EN_LLM	RW	Full-wave or Unilateral modulation mode select. 0: BD Mode 1: Low-Loss Mode	0
7	MONO_EN	RW	Stereo or Mono mode select. 0: Stereo 1: Mono	0
6:5	GAIN	RW	Gain select. 00: 20dB 01: 26dB 10: 32dB 11: 36dB	01
4	MAST_SLV	RW	Master or Slave mode select. 0: Master 1: Slave	0

3:1	FSW	RW	Frequency modulation control signal. 000: 400kHz 001: 500kHz 010: 600kHz 011: 1000kHz 100: 1200kHz 101: 300kHz 110: Reserved 111: Reserved	000
0	MUTE	RW	Mute enable control. 1: Enable 0: Disable	1

CUSTOM0: (Address 01h)

Bit	Symbol	R/W	Description	Default
15:8	RESERVED	R	Reserved.	00000000
7:5	TFB_RT_SEL	RW	TFB release time setting. 000: 40.96ms/step 001: 81.92ms/step 010: 163.84ms/step 011: 327.68ms/step 100: 655.36ms/step 101: 1310.72ms/step 110: 2621.44ms/step 111: Reserved	100
4:2	TFB_AT_SEL	RW	TFB attack time setting. 000: 20.48ms/step 001: 40.96ms/step 010: 81.92ms/step 011: 163.84ms/step 100: 327.68ms/step 101: 655.36ms/step 110: 1310.72ms/step 111: Reserved	100
1:0	PWM_PHASE_CON	RW	Adjust the phase difference of the two-channel triangle wave. 00: 0° 01: 180° 10: 90° 11: 45°	00

CUSTOM1: (Address 02h)

Bit	Symbol	R/W	Description	Default
15:14	TFB_EN	RW	AGC test mode setting. 00: TFB enable 01: Reserved 10: Reserved 11: TFB disable	11
13	TFB_GAIN	RW	Gain=20dB/32dB/36dB, whether to enable TFB. 0: TFB can be used only when Gain=26dB 1: TFB can be used when Gain=20dB/26dB/32dB/36dB	0
12	RESERVED	R	Reserved.	0
11	VCOM_CON	RW	The duty cycle in Low-Loss Mode. 0: 20% 1: 25%	0

10	SS_CON	RW	Spread spectrum control signal. 0: disable 1: enable	0
9:7	RESERVED	R	Reserved.	010
6:5	CON_EDGE	RW	Output PWM fall/rise time control. 00: Reserved 01:12ns 10: 18ns 11: 24ns	01
4:2	DT_CON	RW	Output PWM deadtime control. 000: Reserved 001: Reserved 010: 20ns (12ns) 011: 30ns (12ns) 100: 35ns (18ns) 101: 55ns (18ns) 110: 65ns (24ns) 111: 75ns (24ns)	010
1:0	RESERVED	R	Reserved.	00

SYSST: (Address 08h)

Bit	Symbol	R/W	Description	Default
15	MAST_SLV_S	RO	Master or Slave mode status. 0: Master 1: Slave	0
14:11	RESERVED	R	Reserved.	0100
10	TFB_S	RO	Over temperature and limit amplitude status. 0: Normal 1: over temperature	0
9	OCOT_S	RO	OTOC status. 0: Normal 1: OT/OC occurring	0
8	DC_S	RO	DC status. 0: Normal 1: DC occurring	0
7:6	RESERVED	R	Reserved.	00
5	UVP_OVP_S	RO	UVP or OVP status. 0: Normal 1: UVP or OVP occurring	0
4	RESERVED	R	Reserved.	1
3	MONO_MD_S	RO	Single channel mode status. 0: Normal 1: MONO mode	0
2	LOWLOSS_MD_S	RO	Low-Loss mode status. 0: Normal 1: Low-Loss mode	0
1	RESERVED	R	Reserved.	0
0	RESERVED	R	Reserved.	0

SYSINT: (Address 09h)

Bit	Symbol	R/W	Description	Default
15	MAST_SLV_I	RC	Interrupt indicator for MAST_SLV_S.	0
14:11	RESERVED	R	Reserved.	0000

10	TFB_I	RC	Interrupt indicator for TFB_S.	0
9	OCOT_I	RC	Interrupt indicator for OCOT_S.	0
8	DC_I	RC	Interrupt indicator for DC_S.	0
7:6	RESERVED	R	Reserved.	00
5	UVP_OVP_I	RC	Interrupt indicator for UVP_OVP_S.	0
4	RESERVED	R	Reserved.	0
3	MONO_MD_I	RC	Interrupt indicator for MONO_MD_S.	0
2	LOWLOSS_MD_I	RC	Interrupt indicator for LOWLOSS_MD_S.	0
1	RESERVED	R	Reserved.	0
0	RESERVED	R	Reserved.	0

Application Information

Capacitors Selection

Input Capacitor (input high-pass cutoff frequency)

The AW83119 input stage is a fully differential input stage and the input impedance changes with the gain setting from 9 kΩ at 36 dB gain to 60 kΩ at 20 dB gain. Table 7 lists the values from min to max gain. The tolerance of the input resistor value is ±20% so the minimum value will be higher than 7.2 kΩ. The inputs need to be AC-coupled to minimize the output dc-offset and ensure correct ramping of the output voltages during power-ON and power-OFF. The input ac-coupling capacitor together with the input impedance forms a high-pass filter with the following cur-off frequency:

$$f = \frac{1}{2\pi Z_i C_i}$$

If a flat bass response is required down to 20 Hz the recommended cut-off frequency is a tenth of that, 2 Hz. Table 7 lists the recommended ac-couplings capacitors for each gain step. If a -3 dB is accepted at 20 Hz 10 times lower capacitors can used.

Table 7 Recommended Input AC-Coupling Capacitors

GAIN	INPUT IMPEDANCE	INPUT CAPACITANCE	HIGH-PASS FILTER
20 dB	60 kΩ	1.5 μF	1.8 Hz
26 dB	30 kΩ	3.3 μF	1.6 Hz
32 dB	15 kΩ	5.6 μF	1.9 Hz
36 dB	9 kΩ	10 μF	1.8 Hz

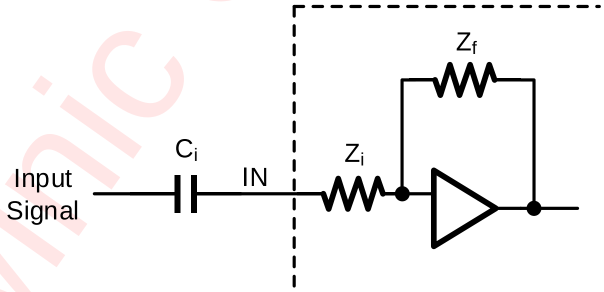


Figure 22 Input Capacitor and Impedance

The input capacitors used should be a type with low leakage, like quality electrolytic, tantalum or ceramic. If a polarized type is used the positive connection should face the input pins which are biased to 2.75 Vdc.

GVDD Decoupling Capacitor

The GVDD supply is used to power the gates of the output full bridge transistors. It can also be used to supply the PLIMIT voltage dividers. AW83119 advises to decouple GVDD with a X5R ceramic 1μF capacitor to GND. The GVDD supply is not intended to be used for external supply. It is recommended to limit the current consumption by using resistor voltage dividers for PLIMIT of 100 kΩ or more.

Supply Decoupling Capacitor

Good quality decoupling capacitors can improve the efficiency and the best performance of the power amplifier. At the same time, in order to get good high frequency transient performance in a high-speed switching application, the ESR value of the capacitor should be as small as possible. In AW83119 applications, low ESR (equivalent-series-resistance) X5R or better ratings ceramic capacitors are recommended. Consider temperature, ripple current, and voltage overshoots when selecting decoupling capacitors. Also, these decoupling capacitors should be located near the PVCC and GND connections to the device in order to minimize series inductances. Select the bulk capacitors at the PVCC for proper voltage margin and adequate capacitance to support the requirements. In practice, with a well-designed power supply, two 220μF, 50V capacitors should be sufficient. One capacitor should be placed near the PVCC at each side of the device.

Bootstrap Capacitor

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220nF, 25V ceramic capacitor of quality X5R or better, must be connected from each output to its corresponding bootstrap input. The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

LC Filter Selection

The main reason that the traditional class-D amplifier-based on AD modulation needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is 2×PVCC, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

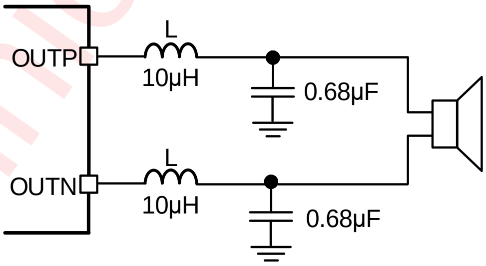


Figure 23 Output LC Filters

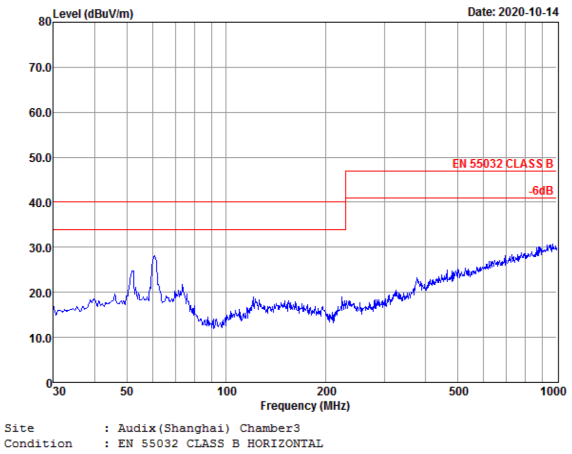
An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

Additional EMC improvements may be obtained by adding snubber networks from each of the class-D outputs to ground. Suggested values for a simple RC series snubber network would be 10Ω in series with a 220pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the audio amplifier. Take care to evaluate the stress on the component in the snubber network especially if the amplifier is running at high PVCC. Also, make sure the layout of the snubber network is tight and returns directly to the GND pins on the IC.

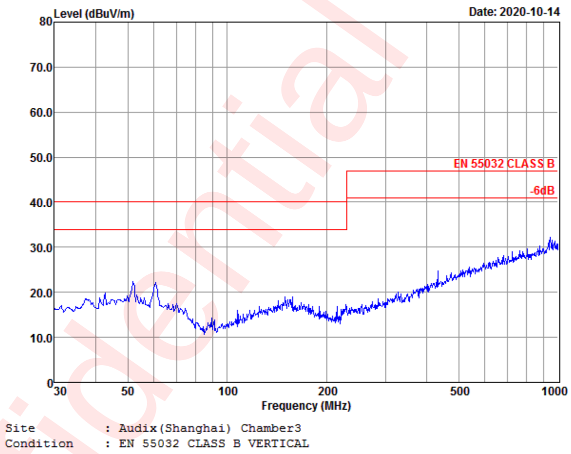
Application Performance Curves

EN55022 Radiated Emissions Results

AW83119 DEMO, PVCC=12V, 8Ω speakers, speaker cable length is 1m, FSW[2:0]=001, SS_CON=1, Spread Spectrum frequency is 500kHz, Spread Spectrum range is 12%, Po=1W.



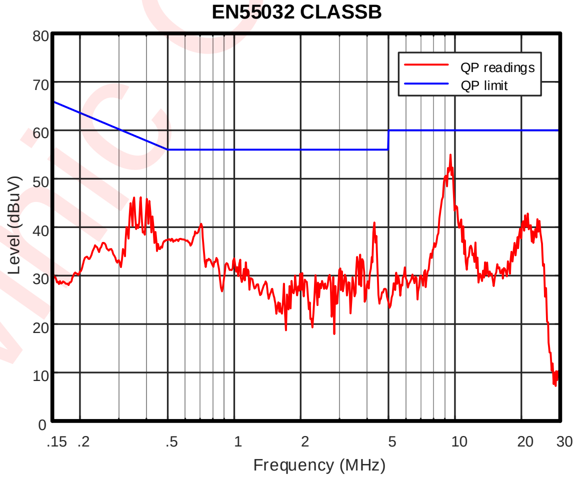
Radiated Emission - Horizontal



Radiated Emission - Vertical

EN55032 Conducted Emissions Results

AW83119 DEMO, PVCC=12V, 8Ω speakers, speaker cable length is 1m, FSW[2:0]=001, SS_CON=1, Spread Spectrum frequency is 500kHz, Spread Spectrum range is 12%, Po=4W.



Conducted Emission - Line

PCB Layout Consideration

AW83119 is a high efficiency, stereo class-D audio amplifier with wide voltage range, to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

1. The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (220μF or greater) bulk power supply decoupling capacitors should be placed near the AW83119 on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the IC GND pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220pF and 1nF and a large mid-frequency cap of value between 100nF and 1μF also of good quality to the PVCC connections at each end of the chip.
2. The PVCC decoupling capacitors should connect to GND. All ground should be connected at the IC GND, which should be used as a central ground connection or star ground for the AW83119.
3. The LC filter should be placed as close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded.
4. Place the AW83119 device away from the edge of the PCB when possible to ensure that the heat can travel away from the device on all four sides.
5. Because the ground pins are the best conductors of heat in the package, maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible.
6. Ensure the vias do not cut off power current flow from the power supply through the planes on internal layers. If needed, remove some vias that are farthest from the AW83119 to open up the current path to and from the device.

Layout Example

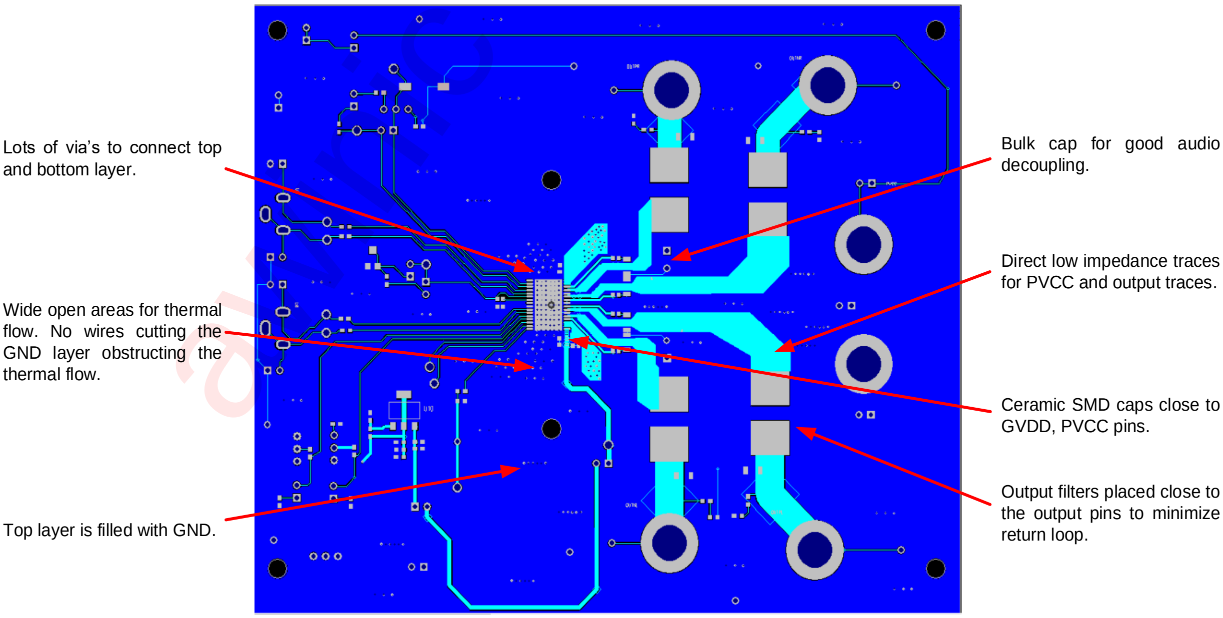
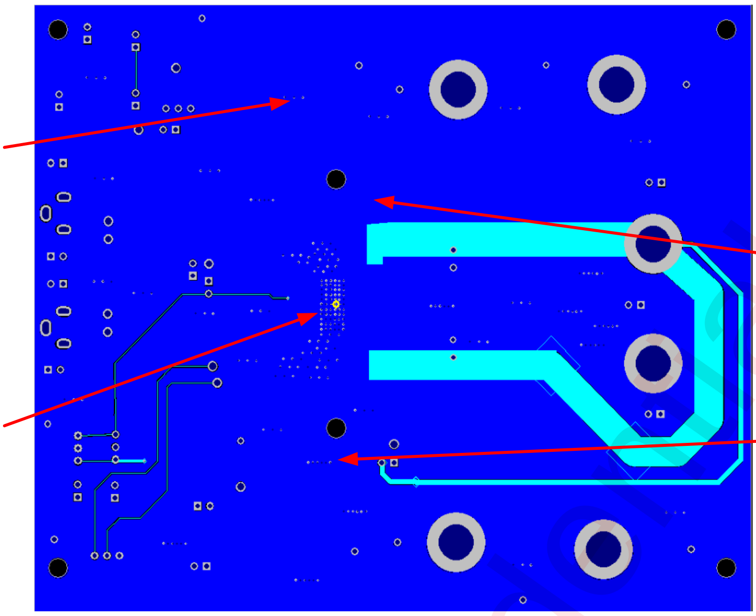


Figure 24 Layout Example Top



Via's along the PCB edge.

Lots of via's to connect top and bottom layer.

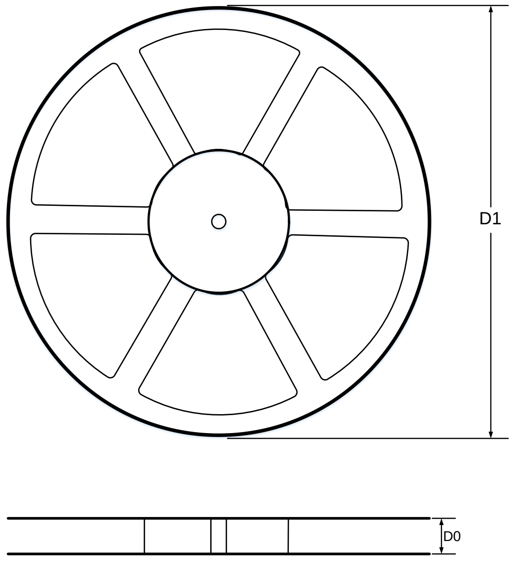
Solid GND plane for low impedance return path.

Bottom layer is filled with GND.

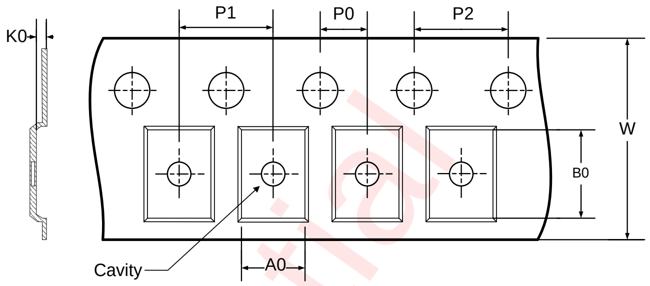
Figure 25 Layout Example Bottom

Tape And Reel Information

REEL DIMENSIONS

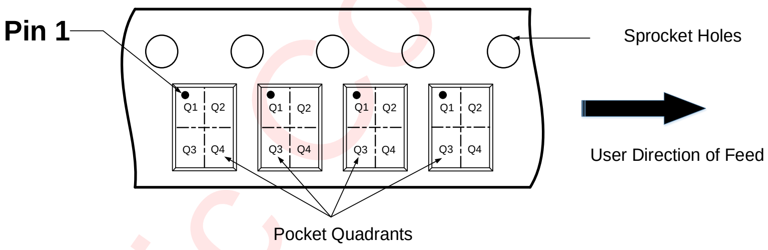


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



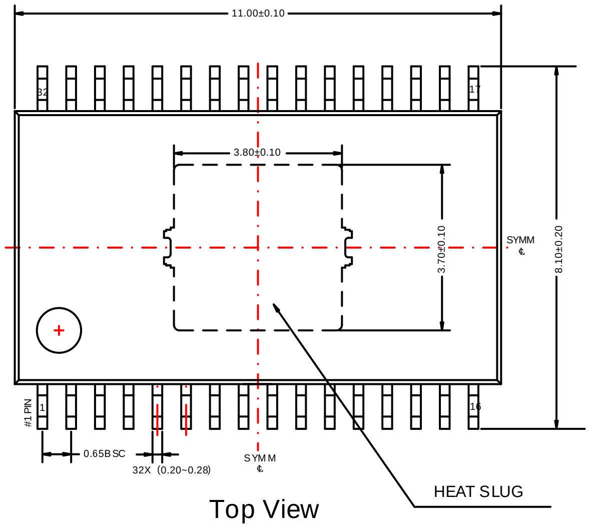
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

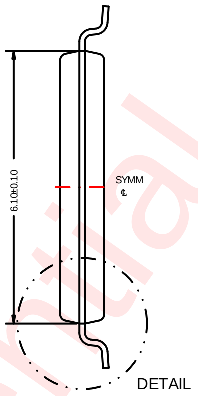
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	24.4	8.6	11.5	1.6	2	12	4	24	Q1

All dimensions are nominal

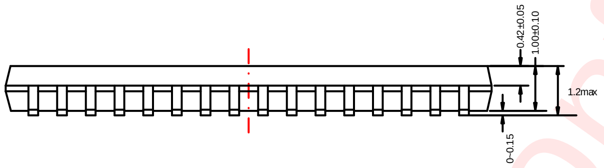
Package Description



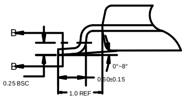
Top View



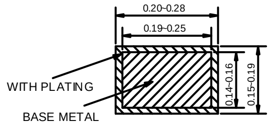
Side View



Side View



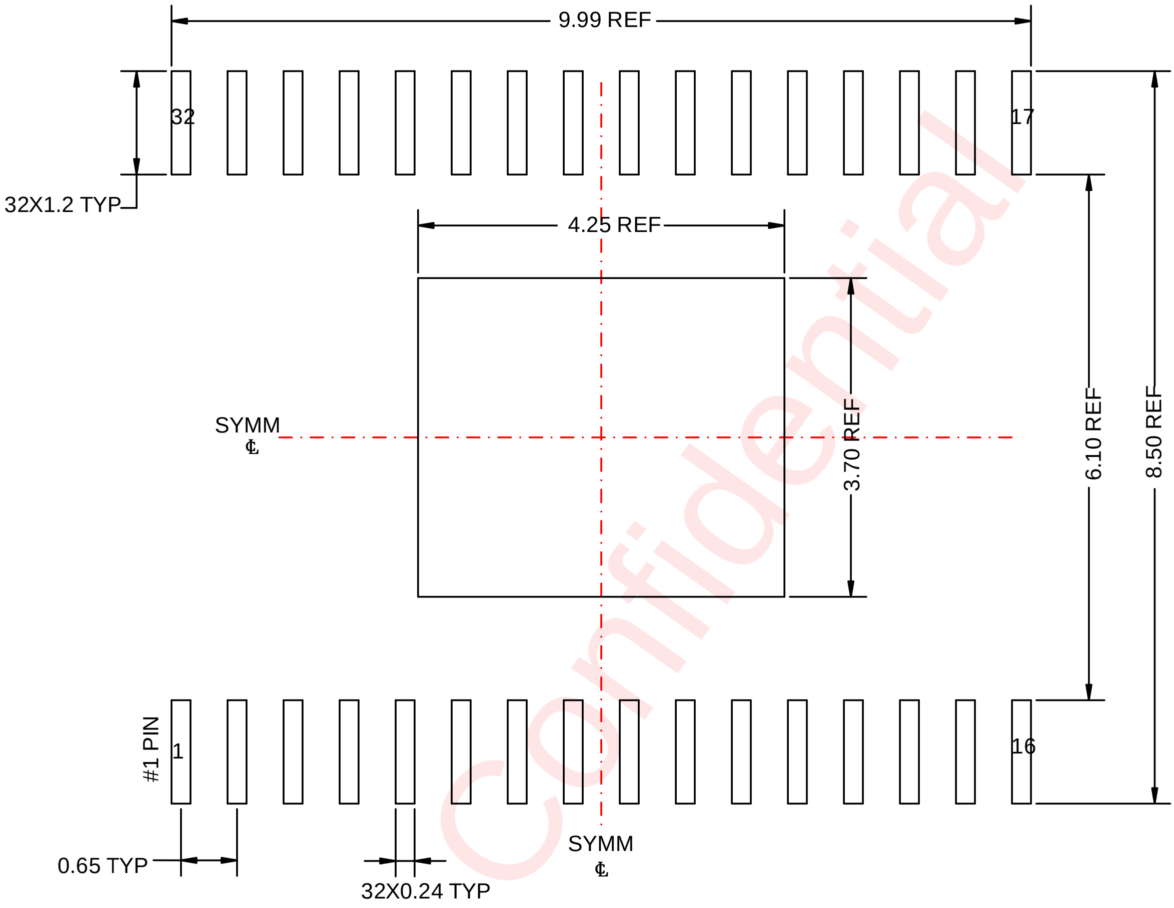
DETAIL

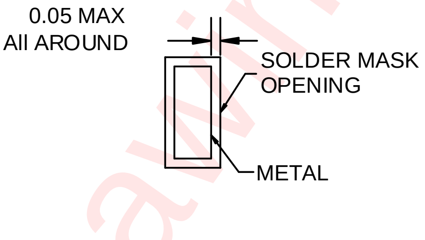


SECTION B-B

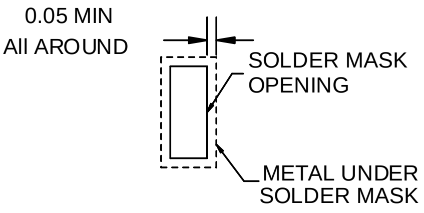
UNIT:mm

Land Pattern Data





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Version Information

Version	Date	Description
V1.0	2020-12-22	AW83119TSR datasheet V1.0
V1.1	2024-01-12	Update IDCODE

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