32-bit MCU Integrated ARM®Cortex™-M0+ and 10 Chanels ADC

Features

- 24MHz ARM®Cortex™-M0+
- 4KB LDROM, 60KB Flash, 16KB SRAM
- Selectable Gains of 1, …, 2048
- 100 K SPS 14-bit SAR ADC
- 12-bit offset calibration DAC
- CRC32 and High-speed divider
- 2 x 32-bit timer, 2 watch-dog
- Support 1MHz I²C, UART
- I²C 7-bit slave address：0x5C
- Max 10 analog input channel, 16 GPIO pins
- Power-on reset, Low voltage detection
- Low voltage reset and temperature detection
- Support In-System Programming (ISP) & In-Circuit Programming (ICP)
- Low power mode
- AEC-Q100 Temperature Range：

  Grade2 (-40℃~105℃)
- WBQFN 5.0mmX5.0mmX0.75mm-40L package

General Description

AW86803QNR-Q1 is a SoC for automotive smartface, light Synchronized with Sound application and so on, which is integrated ARM®Cortex™-M0+ core. It has embedded 60k byte program flash (APROM), 4k byte boot program space LDROM, 16k byte SRAM. It integrated timer, watch dog, 1 AFE module, 1 I²C module, 1 UART module and 1 GPIO module.

AW86803QNR-Q1 support ISP (In-System Programming) and ICP (In-Circuit Programming). System startup interval is configurable, and it can be configured to boot from ROM, LDROM or SRAM.

Applications

Automotive smartface applicaton

Light Synchronized with Sound

Typical Application Circuit

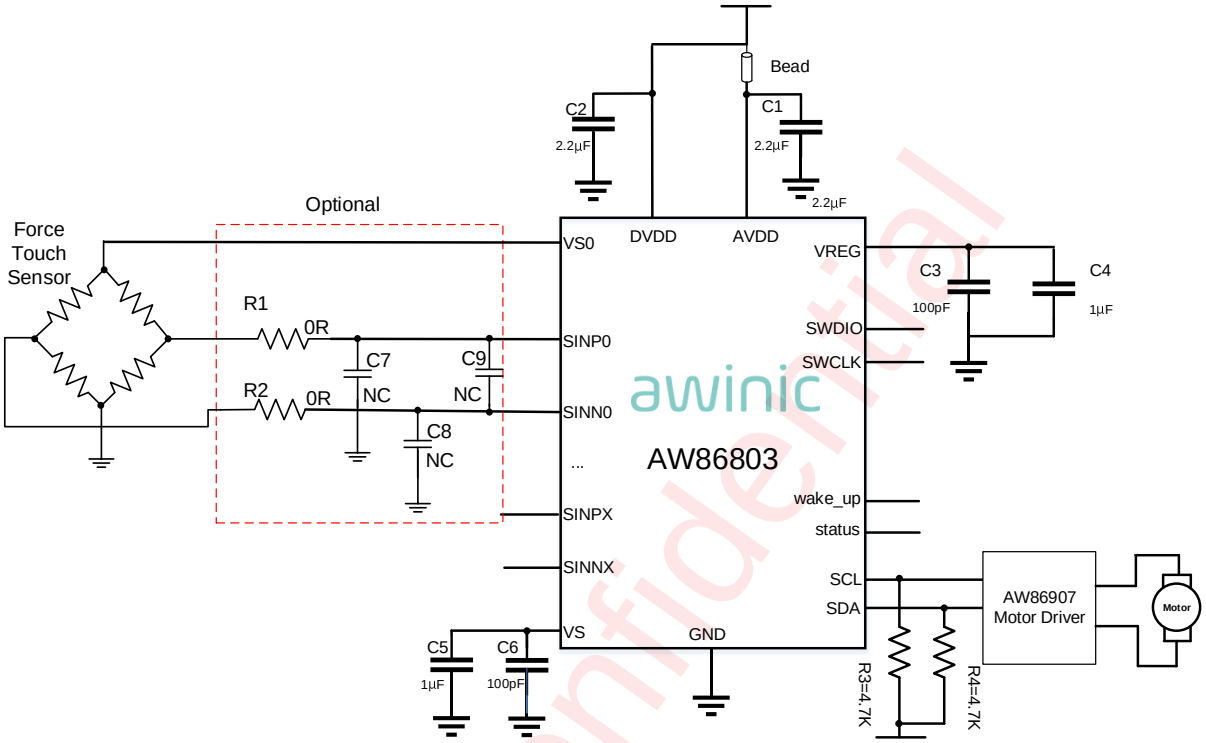


Figure 1 AW86803QNR-Q1 Typical Application Circuit for automotive smartface

Notice:

1. For force application, it recommends to reserve optional circuit to prevent EMI issue.
2. As a slave, the wake_up and status pin need to connect to host.
3. It can control the motor Driver to drive haptic module.

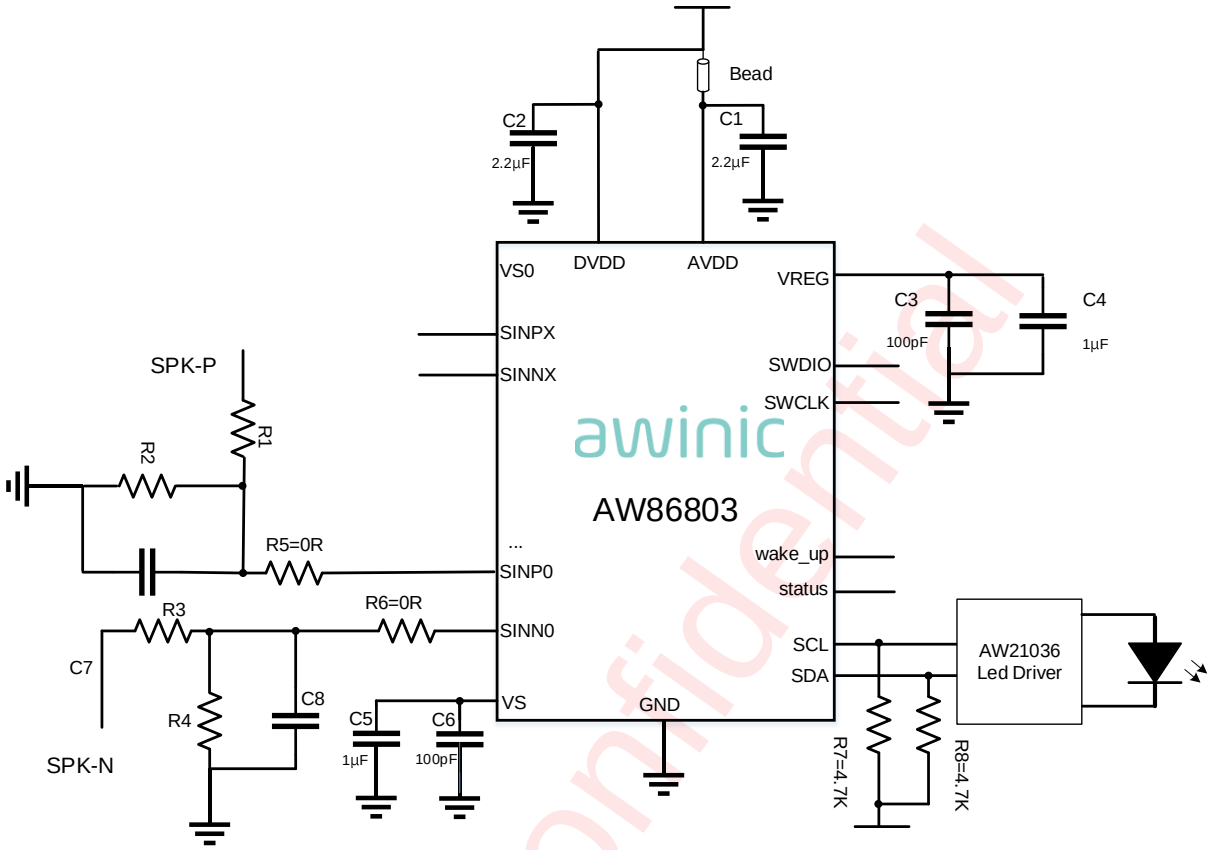


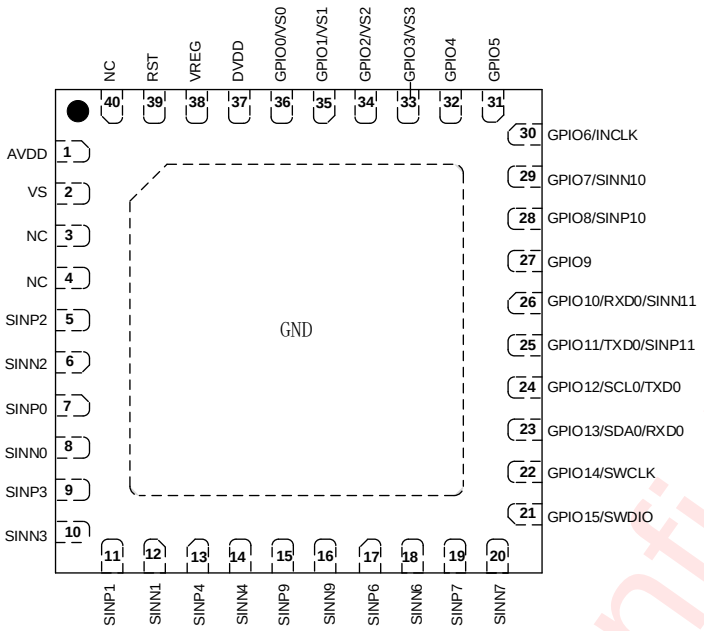
Figure 2 AW86803QNR-Q1 Typical Application Circuit for light synchronized with sound

Notice:

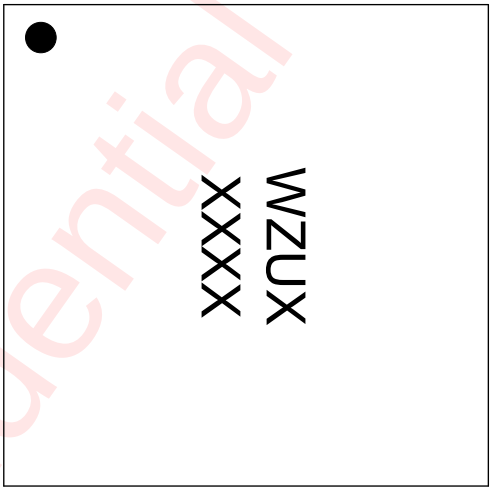
1. For this application, at the front end of input, we need to add low filter and divider circuit to keep the SINPX, SINNX in the safe voltage.
2. As a slave, the wake_up and status pin need to connect to host.

Pin Configuration And Top Mark

AW86803QNR-Q1
(Top View)



AW86803QNR-Q1 Marking
(Top View)



WZUX - AW86803QNR-Q1
XXXX - Production Tracing Code

Figure 3 AW86803QNR-Q1 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	AVDD	Analog power
2	VS	VS Regulated output
3	NC	Not Connected
4	NC	Not Connected
5	SINP2	Sensor Channel 2 Positive Input
6	SINN2	Sensor Channel 2 Negative Input
7	SINP0	Sensor Channel 0 Positive Input
8	SINN0	Sensor Channel 0 Negative Input
9	SINP3	Sensor Channel 3 Positive Input
10	SINN3	Sensor Channel 3 Negative Input
11	SINP1	Sensor Channel 1 Positive Input
12	SINN1	Sensor Channel 1 Negative Input
13	SINP4	Sensor Channel 4 Positive Input
14	SINN4	Sensor Channel 4 Negative Input
15	SINP9	Sensor Channel 9 Positive Input
16	SINN9	Sensor Channel 9 Negative Input
17	SINP6	Sensor Channel 6 Positive Input
18	SINN6	Sensor Channel 6 Negative Input
19	SINP7	Sensor Channel 7 Positive Input
20	SINN7	Sensor Channel 7 Negative Input
21	GPIO15/ SWDIO	GPIO15，push-pull output / SW DEBUG DATA
22	GPIO14/ SWCLK	GPIO14，push-pull output / SW DEBUG CLK
23	GPIO13/ SDA0/ RXD0	GPIO13，open-drain output / I²C0 DATA/ UART0 RXD
24	GPIO12/ SCL0/ TXD0	GPIO12，open-drain output / I²C0 CLK/ UART0 TXD
25	GPIO11/ TXD0 / SINP11	GPIO11，open-drain output / UART0 TXD / Sensor Channel 11 Positive Input
26	GPIO10/ RXD0/ SINN11	GPIO10，open-drain output / UART0 RXD / Sensor Channel 11 Negative Input
27	GPIO9	GPIO9，open-drain output

28	GPIO8 / SINP10	GPIO8，open-drain output / Sensor Channel 10 Positive Input
29	GPIO7 / SINN10	GPIO7，open-drain output / Sensor Channel 10 Negative Input
30	GPIO6/ INCLK	GPIO6，open-drain output / External clock input pin
31	GPIO5	GPIO5，open-drain output
32	GPIO4	GPIO4，open-drain output
33	GPIO3/ VS3	GPIO3，push-pull output / VS3 output
34	GPIO2/ VS2	GPIO2，push-pull output / VS2 output
35	GPIO1/ VS1	GPIO1，push-pull output / VS1 output
36	GPIO0/ VS0	GPIO0，push-pull output / VS0 output
37	DVDD	Digital power
38	VREG	LDO output pin，needs to be connected to 1μf capacitor
39	RST	Reset input，active high
40	NC	Not Connected
	GND	Ground

Functional Block Diagram

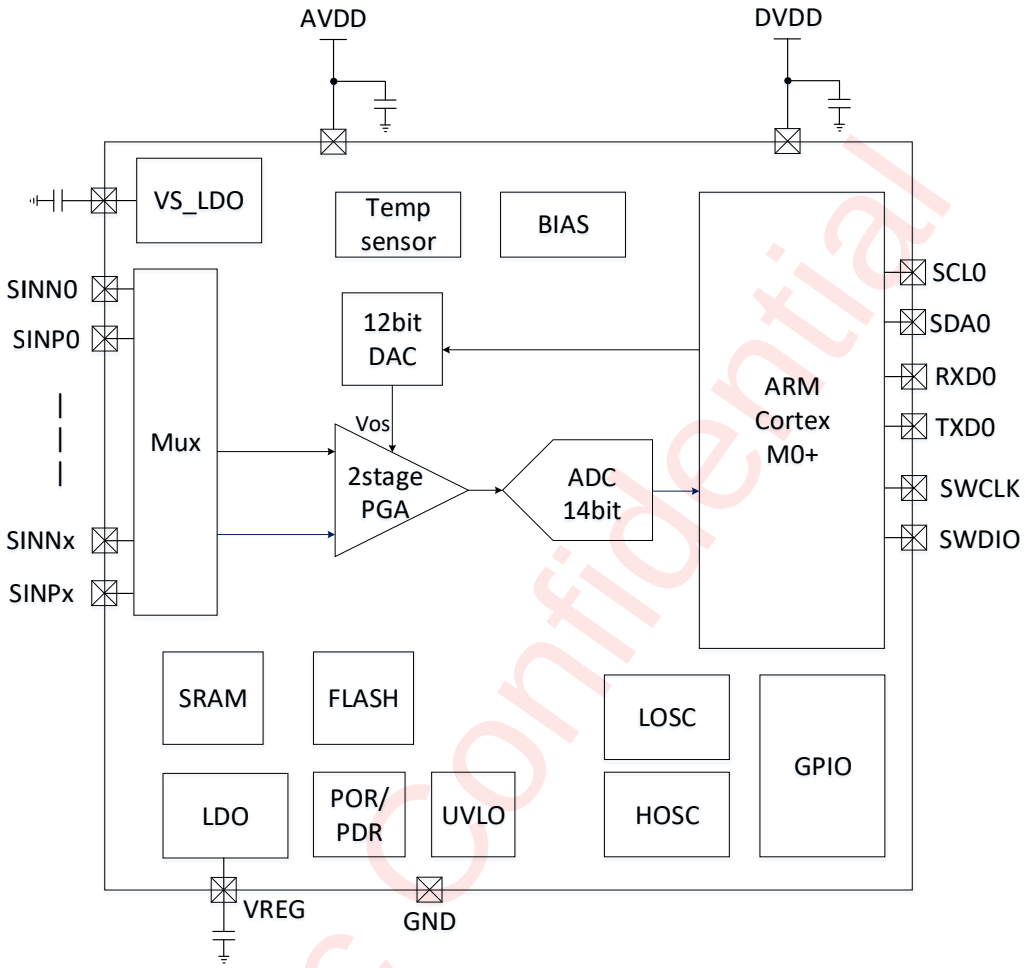


Figure 4 AW86803QNR-Q1 Function Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW86803QNR-Q1	-40℃~105℃	WBQFN 5.0mmX5.0mm X0.75mm-40L	WZUX	MSL3	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

Parameter	Range
Supply voltage range AVDD	-0.3V to 6.0V
Supply voltage range DVDD	-0.3V to 6.0V
SINPX, SINNX, GPIO	-0.3V to VDD+0.3V
Digital power supply VREG	-0.3V to 1.65V
Package Thermal Resistance θ_{JA}	60°C/W
Ambient Temperature Range	-40°C to 105°C
Maximum Junction Temperature T_{JMAX}	150°C
Storage Temperature Range T_{STG}	-65°C to 150°C
Lead Temperature（Soldering 10 Seconds）	260°C
ESD Rating (NOTE 2 3)	
HBM（Human Body Model）	±2kV
CDM(Charge Device Model)	±1.5kV
Latch-up	
Test Condition: JESD78E	+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE 2：The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE 3：Charge Device Model test method: ESDA/JEDEC JS-002-2018.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD	Analog supply voltage	2.5	3.3	5.5	V
DVDD	Analog supply voltage	2	3.3	5.5	V
C_{AVDD}	Input capacitance		2.2		μF
C_{DVDD}	Input capacitance		2.2		μF
C_{VS1}	VS Decoupling capacitor	1			μF
C_{REG1}	VREG Decoupling capacitor	1			μF
T_A	Operating free-air temperature range	-40	25	105	°C

Electrical Characteristics

AVDD=3.3V, DVDD=3.3V, RST=0, TA=25°C for typical values (unless otherwise noted)

Parameter		Test Conditions	Min	Typical	Max	Unit
AVDD	Analog supply voltage		2.5		5.5	V
DVDD	Digital supply voltage		2		5.5	V
V_{IH}	Logic input high level		1.35			V
V_{IL}	Logic input low level				0.35	V
V_{OL}	Logic output low level	I_{OUT}=4mA			0.4	V
V_{OH}	Logic output high level	I_{OUT}=0.8mA	AVDD-0.4			V
I_{SD}(1)	Shutdown current	RST =3.3V		0.03		μA
I_{LP1}	Power down mode supply current	POR+LOSC Turn on		3		μA
I_{LP2}	Deep sleep mode supply current	POR+LOSC+LDO Turn on		7		μA
I_{LP3}	Sleep mode supply current	CPU Power consumption in sleep mode		1.2		mA
I_Q	Quiescent current			4.5		mA
T_{SD}	Over temperature protection threshold			160		℃
T_{SDR}	Over temperature protection recovery threshold			130		℃
24MHz HOSC						
F_{HOSC}	HOSC working frequency			24		MHz
R_{HOSC}	HOSC Accuracy		-2		2	%
35kHz LOSC						
F_{LOSC}	LOSC working frequency			35		kHz
R_{LOSC}	LOSC Accuracy		-15		15	%
14bit SAR ADC						
V_{ADIN}(4)	Input voltage		0		AVDD	V
V_{REF}	ADC Reference voltage			AVDD		V
F_{ADC}	Conversion rate			100		Ksps
PGA(Signal input path)						
V_{CMI}(4)	Common mode input voltage		0.1		AVDD-1	V
V_{DMI}(4)	Differential input voltage				AVDD/ G_{PGA}	V
G_{PGA_min}	PGA gain min			1		
G_{PGA_max}	PGA gain max			2048		
GE	Gain error			10		%

Parameter		Test Conditions	Min	Typical	Max	Unit
R_{IN}	Differential input impedance			17		MΩ
ISOch-ch	Channel isolation			80		dB
CMRR	Common mode rejection ratio	1.5 mVPP on SIN, 200Hz		105		dB
PSRR	Power supply rejection ratio	200Hz		50		dB
V_{OS}	Input offset voltage			±1		mV
DAC						
R_{DAC}	Resolution			12		bit
M_{DAC}	Monotonic			11		bit
V_{EOSI}	Equivalent offset calibration range		-540×K(2)		+540×K(2)	mV
LDO						
V_{REG}	LDO output voltage		1.35	1.5	1.65	V
C_{REG}	LDO Decoupling capacitor		1			μF
VS						
V_S	VS output voltage		2.4		3.1	V
C_{VS}	VS Decoupling capacitor		1			μF
I_{VSH}(3)	High supply current of VS turns on			100		mA
UVLO						
V_{UV}	Undervoltage detection voltage			2.3		V
V_{UVH}	Under-voltage protection hysteresis voltage			100		mV
POR						
V_{POR}	Power-on reset voltage			1.6		V
Temperature Sense						
T_R	Temperature detection range		-40		105	℃
R_{TS}	Temperature detection accuracy		-3		3	℃

(1) Does not include reset leakage

(2) K= （VS/3）K_{pga}，（K_{pga} =1（G_{pga1}≤64），K_{pga} =1/2（G_{pga1}=128），K_{pga} =1/4（G_{pga1}=256））*

(3) High supply current pulse of VS turns on less than 60 μs

(4) Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

I²C Interface TIMING

Parameter			Super-fast mode			UNIT
No.	Symbol	Name	MIN	TYP	MAX	
1	f_{SCL}	SCL Clock frequency		400	1000	kHz
2	t_{LOW}	SCL Low level Duration	0.5			μs
3	t_{HIGH}	SCL High level Duration	0.3			μs
4	t_{RISE}	SCL, SDA rise time			0.1	μs
5	t_{FALL}	SCL, SDA fall time			0.1	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.3			μs
7	$t_{HD:STA}$	(Repeat-start) Start condition hold time	0.3			μs
8	$t_{SU:STO}$	Stop condition setup time	0.3			μs
9	t_{BUF}	the Bus idle time START state to STOP state	0.5			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			μs
11	$t_{HD:DAT}$	SDA hold time	10			ns

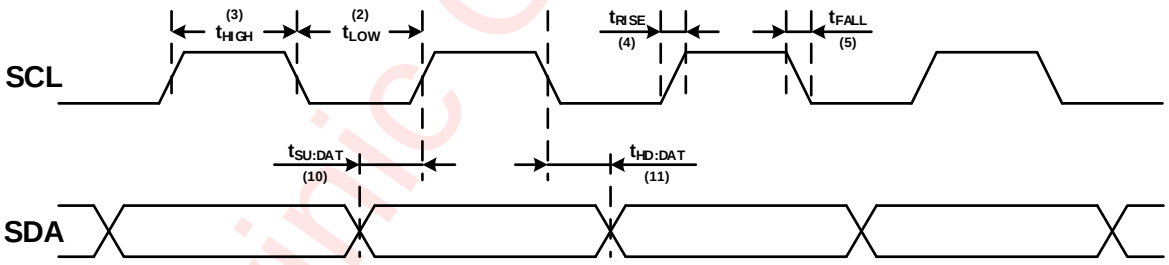


Figure 5 SCL and SDA timing relationships in the data transmission process

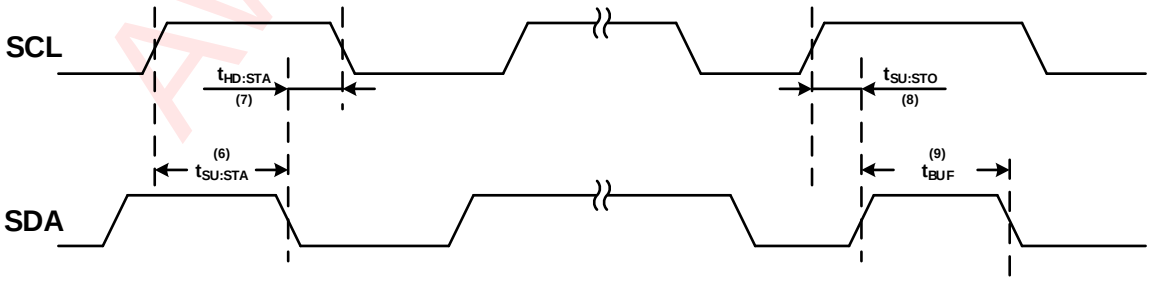


Figure 6 The timing relationship between START and STOP state

I²C Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

I²C Register address is 32-bit and register data is 32-bit. Note that I²C also support 8-bit data transfer. Writing

process of I²C is showed as below picture.

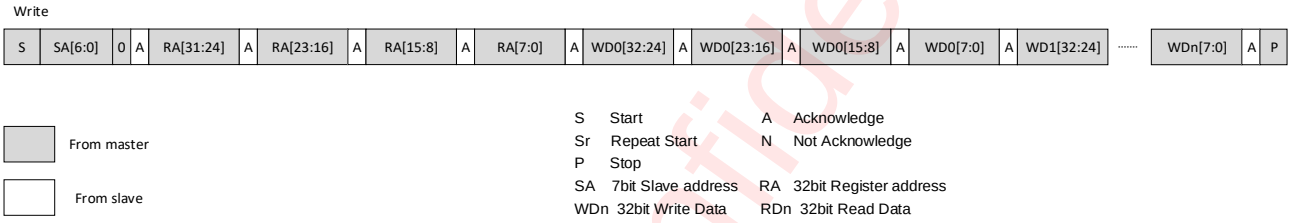


Figure 7 I²C Write Byte Cycle

I²C Read Cycle

I²C supports read operation data format with repeated start conditions, so there are two formats of I²C read operations. Read process of I²C is showed as below picture

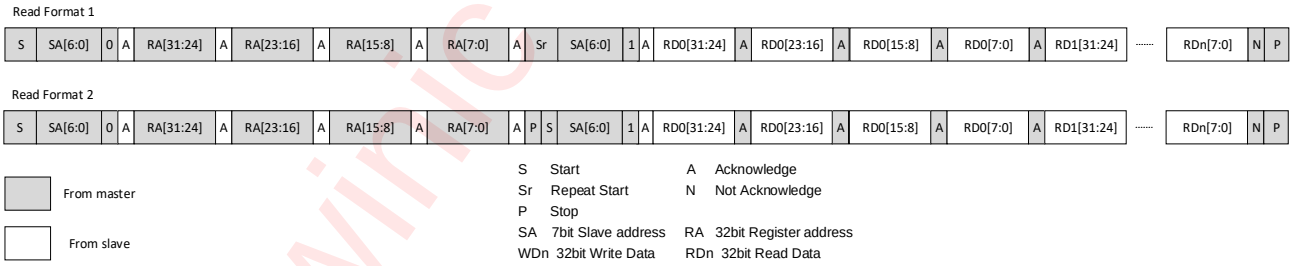


Figure 8 I²C Read Byte Cycle

Detailed Functional Description

Power On And Power Down Sequence

The power on and power down sequence of this device is illustrated in the following figure:

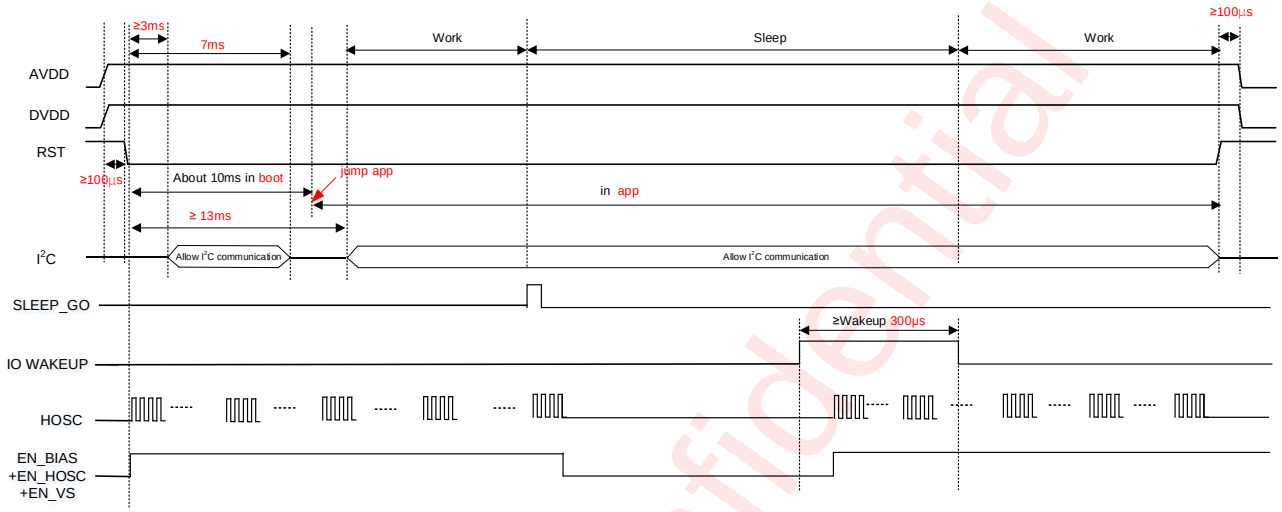


Figure 9 Power On and Power Down Sequence

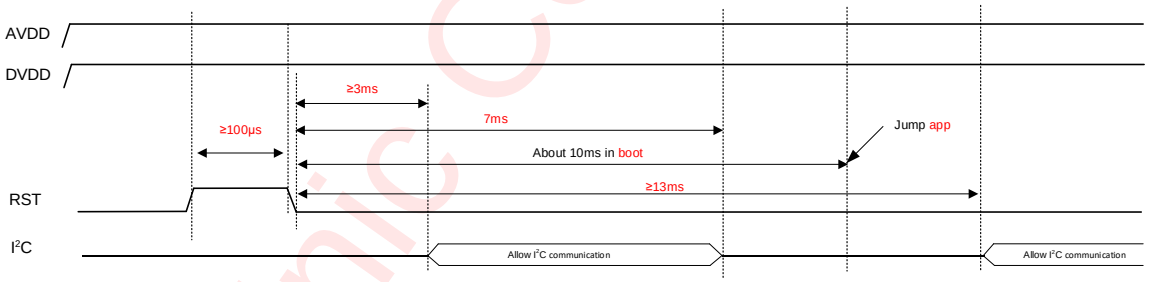


Figure 10 RST Sequence

ARM®Cortex™-M0+

The Cortex™-M0+ processor is a 32-bit multi-level configurable RISC processor.It has AMBA-AHB-Lite interface and Nested Vectored Interrupt Controller(NVIC),with optional hardware debugging function,can execute Thumb instructions and is compatible with other Cortex-M series.This processor supports two operation modes Thread mode Handler mode.When an exception occurs,the processor enters Handler mode.Exception return can only occur in Handler mode.When reset,the processor will enter Thread mode,the processor can also enter Thread mode when an abnormal return. Compared with Cortex™-M0 processor, The Cortex™-M0+ processor has higher energy consumption efficient.

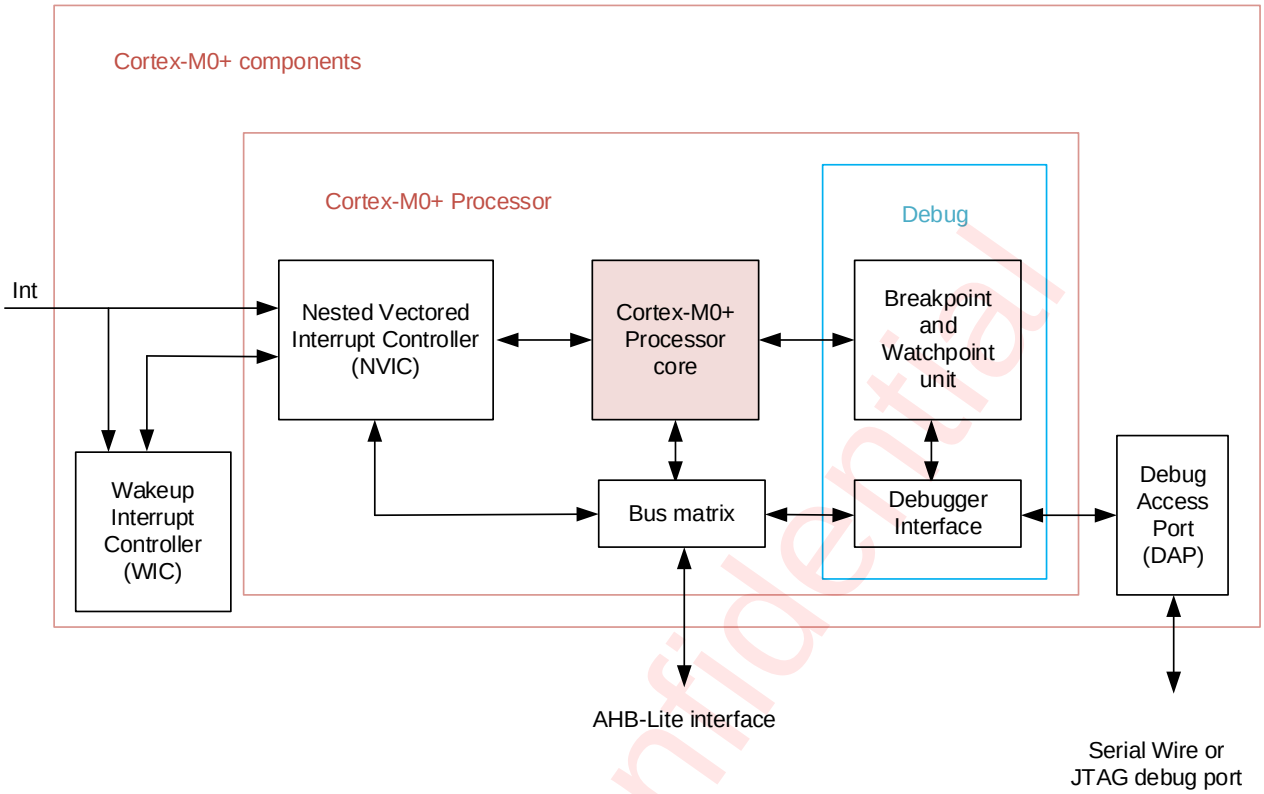


Figure 11 Cortex-M0+ core

Cortex-M0+ core features

The system supports little-endian data access and provides a single instruction 32-bit hardware multiplier.

NVIC provides 32 external interrupts with 4-level interrupt priority. There is a dedicated non-maskable interrupt NMI. The system supports level and pulse interrupt trigger. Interrupt wakeup register WIC, support ultra-low power sleep mode.

Debug: there are 4 hardware breakpoints, 2 observation points, program count sampling register for non-invasive code analysis, single-step vector capture capability.

Bus interface: The system provides a single 32-bit AMBA-3, AHB-lite system interface that integrates all system peripherals and memory and Single 32-bit slave port supporting DAP (Debug Access Port).

- Low gate count processor with the following features
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compatible with 24-bit systick timer
  - 32-bit hardware divider
  - Supports little-endian data access
  - Deterministic, fixed delay interrupt handling capability
  - Abnormal mode (C-ABI), ARMv6-M (C-ABI) compatible with C application binary interface, allowing users to implement interrupt handling with pure C language functions
  - Use wait for interrupt (WFI), wait for event instruction (WFE), or directly enter low-power sleep mode when returning from interrupt

- NVIC characteristics
  - 32 external interrupt inputs, each with 4 priority levels
  - Non-maskable interrupt input
  - Supporting level and pulse trigger interrupt
  - Interrupt wake controller (WIC), supporting ultra-low power sleep mode
- Bus interface
  - Single 32-bit AMBA-3, AHB-Lite system interface provides convenient integration for all system peripherals and memory
  - Single 32-bit slave port supporting DAP (Debug Access Port)
- Debug
  - 4 hardware breakpoints
  - 2 observation points
  - Program count sampling register for non-intrusive code (PCSR)
  - Single step and vector capture capabilities

System memory map

The chip provides 4G byte addressing space, only supports little-endian data format, unified addressing of ROM, SRAM and controller registers.

Flash memory space		
0x0100_1000 – 0x0100_FFFF	FLASH_BA	FLASH Memory space (60KB)
LDROM memory space		
0x0100_0000– 0x0100_0FFF	LDROM_BA	LDROM Memory space (4KB)
ROM memory space		
0x1000_0000– 0x1000_0FFF	ROM_BA	ROM Memory space (4KB)
SRAM memory space		
0x2000_0000 – 0x2000_3FFF	SRAM_BA	SRAM Memory space (16KB)
AHB controller memory space (0x5000_0000 – 0x502F_FFFF)		
0x5000_0000 – 0x5000_1FFF	GCR_BA	System Management Control Register
0x5000_2000 – 0x5000_23FF	PWR_BA	Power Management Unit Register （Contains SWDT function register）
0x5000_2400 – 0x5000_27FF	RST_BA	Reset management unit register
0x5000_2800 – 0x5000_2BFF	CLK_BA	Clock management unit register
0x5000_C000 – 0x5000_DFFF	FMC_BA	Flash Memory control register
0x5000_E000 – 0x5000_FFFF	RMC_BA	SRAM Memory control register
0x5001_4000 – 0x5001_7FFF	HDIV_BA	Hardware divider control register
0x5002_4000 – 0x5002_7FFF	CRC_BA	CRC control register

APB controller memory space (0x4000_0000 – 0x401F_FFFF)		
0x4000_0000 – 0x4000_0FFF	WDT0_BA	Watchdog0 control register
0x4000_1000 – 0x4000_1FFF	WDT1_BA	Watchdog1 control register
0x4000_3000 – 0x4000_3FFF	UART0_BA	UART0 control register
0x4000_4000 – 0x4000_4FFF	TMR0_BA	Timer 0 control register
0x4000_5000 – 0x4000_5FFF	TMR1_BA	Timer 1 control register
0x4000_6000 – 0x4000_6FFF	I^2C0_BA	I^2C0 Interface control register
0x4000_8000 – 0x4000_8FFF	AFE0_BA	AFE0 control register
0x4000_9000 – 0x4000_9FFF	GPIOA_BA	GPIOA control register
System control space (SCS) (0xE000_E000 – 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System timer control register (SysTick)
0xE000_E100 – 0xE000_ECFF	SCS_BA	Nested Vectored Interrupt ControlRegisters(External interrupt control register)
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System control register

System interruption

Cortex™-M0+ provides an interrupt controller for managing exceptions, NVIC, and is closely connected with the processor.

Cortex™-M0+ provides an interrupt controller as a complete part of the exception model, named it nested vector interrupt controller.

NVIC supports 4-level discrete interrupt priority. When any interrupt request is received, the start address of the ISR register is taken from the interrupt vector table in memory. NVIC automatically saves the processing status to the stack and saves value of the registers "PC, PSR, LR" , RO ~ R3, R12 ".

At the end of the ISR, NVIC will restore the value of the relevant register from the stack, and then perform normal operations, so it takes a small amount of time to process the interrupt request.

The base address of the vector table is 0x00000000. The vector table includes the initial value of the stack after reset and the entry address of all exception handling situations and the order of the vector numbers for handling exceptions.

NVIC supports "Tail chaining" to handle interrupts. After an interrupt is processed, there is no need to resume the scene and the next one is processed immediately. This can reduce the interrupt waiting time and improve the efficiency of interrupt processing.

NVIC also supports "late arrival" to handle interrupts. If the current interrupt is saving the context and has not entered the interrupt processing function, a higher priority interrupt occurs, NVIC will handle the higher priority interrupt, and do not need to save again Context, which can improve real-time.

number and priority of interrupt vector

Exception Name	number	priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Set aside	4~10	Set aside
SVCall	11	Configurable
Set aside	12~13	Set aside
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16~47	Configurable

Exception number	IRQ number	Exception name	Source of anomaly	Interrupt description	Wake up deep sleep mode
1~15			System abnormality		
16	0	UVLO	UVLO	Undervoltage interrupt	No
17	1	TMR0_INT	TMR0	Timer 0 interrupt	Yes
18	2	TMR1_INT	TMR1	Timer 1 interrupt	Yes
19	3	UART0_INT	UART0	UART0 interrupt	Yes
20	4	I^2C0_INT	I^2C0	I^2C0 interrupt	Yes
21	5	AFE0_INT	AFE0	AFE0 interrupt	No
22	6	AFE0_CMP0_INT	AFE0_CMP0	AFE0 interrupt	No
23	7	AFE0_CMP1_INT	AFE0_CMP1	AFE0 interrupt	No
24	8	GPIOA_INT	GPIOA	GPIOA interrupt	Yes
25	9	RMC_INT	RMC	RAM Parity failed interrupt	No
26	10	FMC_INT	FMC		No
27	11	WDT0_INT	WDT0	Watchdog 0	Yes
28	12	SWDT_INT	SWDT	Smart watchdog	Yes
29	13	WDT1_INT	WDT1	Watchdog 1	Yes

Clock

The functions of the clock management unit module (CMU) mainly include: detecting whether the clock is OK according to the clock enable; after the alternative clock is OK, one of the external pin clock, the internal low-speed clock, and the internal high-speed clock is selected as the internal system clock according to the selector.

The CMU will also enable the clock gate control of the system clock, cpu clock and peripheral clock according to the low power consumption mode

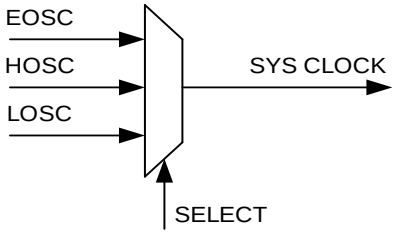


Figure 12 Clock

Reset

Select chip reset, digital system reset (MCU reset), CPU reset, peripheral module reset according to hard reset and register configuration

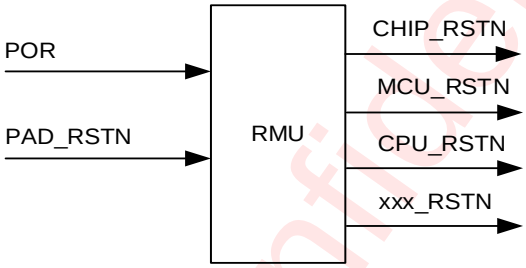


Figure 13 Reset

AFE

The AFE module includes two PGAs, one 12-bit DAC and one 14-bit ADC

- 14-bit SAR ADC,13-bit accuracy guarantee
- 12 external sensor inputs, 4 internal inputs (VS, VS/2, TEMP, GND)
- 16 channels
- 100KHz SPS
- Support the conversion result of 2's complement format / unsigned format / original format
- Provide multiple working modes
  1. Single conversion mode. Complete a conversion on the designated channel
  2. Single cycle scan mode. Complete a conversion on all designated channels
  3. Finite cycle scan mode1. Each channel switches to the next channel after a specified number of conversions
  4. Finite cycle scan mode2. Each channel converts once and then enters the next channel in turn, converting a specified number of times in total
  5. Infinite scan mode. Continuously execute single-cycle scan mode until software stops A/D conversion
  6. Burst Mode. Continue on a single designated channel and store the results in FIFO in sequence
- The conversion result can be compared with the specified value, the user can set whether to generate an interrupt when matching
- Built-in Level 2 PGA, the first stage PGA gain coefficient can be configured as 1/16/32/64/128/256, The second stage PGA gain coefficient can be configured as 1/2/3/4/5/6/7/8

➢ Built-in 12-bit DAC for offset voltage calibration

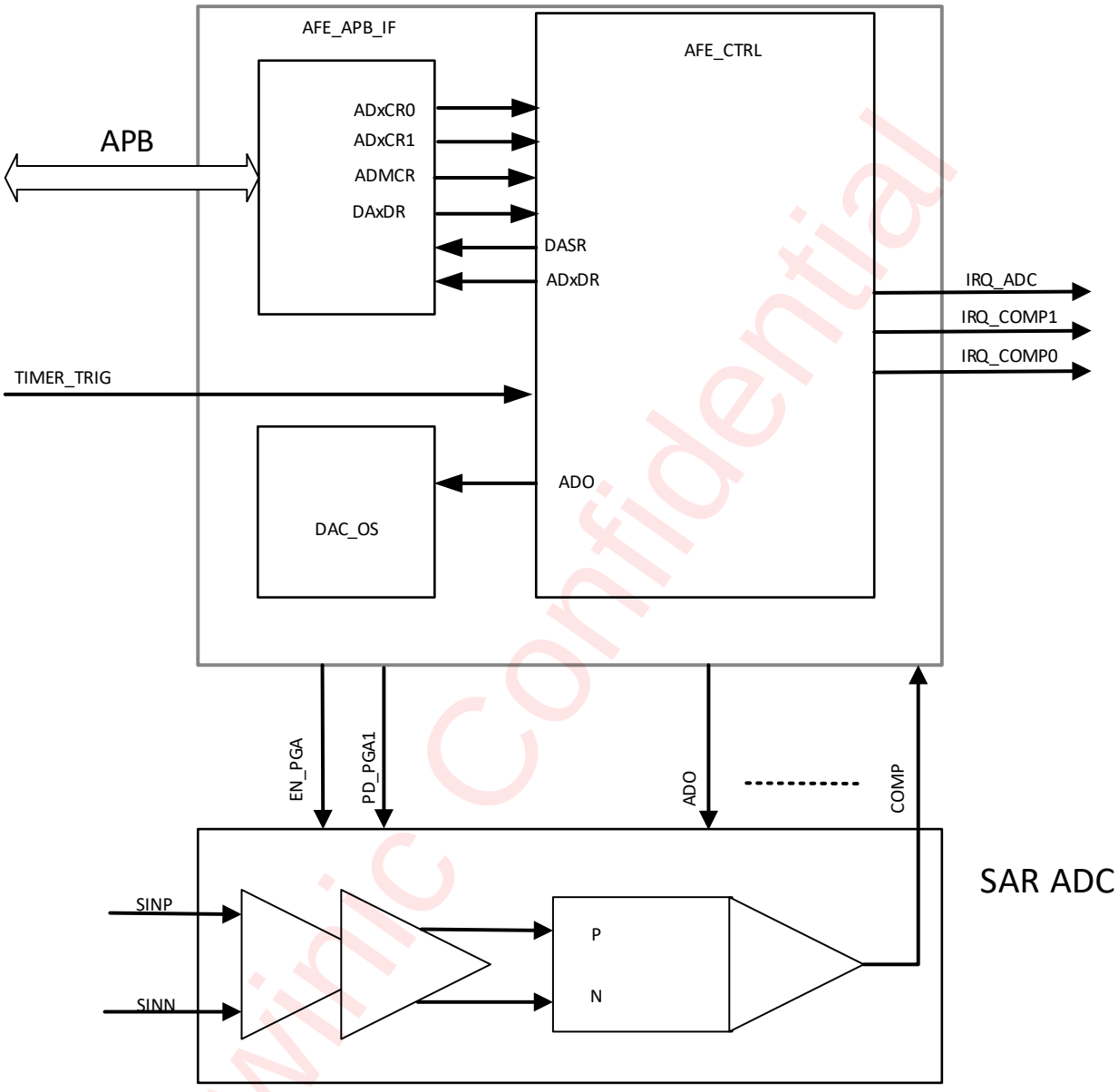


Figure 14 AFE

Register Configuration

Register List

BASE	NAME	Description
0x01001000	**FLASH**	FLASH MAIN space
0x01000000	**LDROM**	LDROM Module
0x10000000	**ROM**	ROM Module
0x20000000	**SRAM**	SRAM Module
0x50000000	**SYS**	SYS Module
0x50002000	**PWR**	PWR Module
0x50002400	**RST**	RST Module
0x50002800	**CLK**	CLK Module
0x5000C000	**FMC**	FMC Module
0x5000E000	**RMC**	RMC Module
0x50014000	**HDIV**	HDIV Module
0x50024000	**CRC**	CRC Module
0x40000000	**WDT0**	WDT0 Module
0x40001000	**WDT1**	WDT1 Module
0x40003000	**UART**	UART Module
0x40004000	**TIMER0**	TMR0 Module
0x40005000	**TIMER1**	TMR1 Module
0x40006000	**I²C0**	I²C0 Module
0x40008000	**AFE**	AFE Module
0x40009000	**GPIO**	GPIO Module
0xE000E100	**NVIC**	NVIC Module

SYS: (Base Addr 0x50000000)

OFFSET	NAME	R/W	Description	Default
0x00	CHIP_ID	**RO**	Chip id	0x41571923
0x04	DATE	**RO**	Date information	0x20191115
0x08	FLS_ID	**RO**	Flash id	0x00086803
0x0C	FLS_DATE	**RO**	Flash date information	0x20191225
0x20	CFG_MOD	**R/W**	System configure register	0x5A5A00FC
0x40	BIAS_EN	**R/W**	Bias enable	0x00000001
0x5C	D2A_SPACE	**R/W**	digital to analog interface reservation configuration	0x00000000
0x80	PA_MFC_MUX	**R/W**	PA pin multifunction configuration register	0x00000000
0x84	PA_ADJ_DEG	**R/W**	PA13 pin deglitch time configure	0x00000000
0x88	PA_ADJ_OD	**R/W**	PA4-PA13 pin open-drain output time configure	0x00000000
0x8C	PA_IN_EN	**R/W**	PA0-PA13 pin input enable configure	0x0000FFFF
0x94	PA_OD_EN	**R/W**	PA0-PA15 pin open-drain enable configure	0x00000000
0x98	PA_SMIT_EN	**R/W**	PA0-PA15 pin input interfce schmitt trigger enable configure	0x0000FFFF
0x9C	PA_FAST	**R/W**	PA0-PA15 pin fast lane enable configure	0x00000000
0xA0	PA_PD_RES	**R/W**	PA0-PA3, PA14-PA15 pin pull-down resistor configure	0x00000000

0xA4	PA_SR_CTRL1	**R/W**	PA0-PA3, PA14-PA15 pin output delay configure register1	0x0000FFFF
0xA8	PA_SR_CTRL2	**R/W**	PA0-PA3, PA14-PA15 pin output delay configure register2	0x00000000
0xAC	PA_PU_RES	**R/W**	PA0-PA3, PA14-PA15 pin pull-up resistor configure	0x00000000
0x400	WR_PROT_KEY	**R/W**	system protection key register	0x00000000
0x404	SYS_WR_PROT	**RO**	system write protection key register	0x00000001

PWR: (Base Addr 0x50002000)

OFFSET	NAME	R/W	Description	Default
0x00	SLP_MOD	**R/W**	Chip low power mode	0x00000000
0x04	SLP_DLY	**R/W**	configure delay to enter low power mode	0x00000000
0x08	PD_EN	**R/W**	power-down mode enable	0x00000000
0x0C	SLP_EN	**R/W**	sleep mode enable	0x00000000
0x10	SLP_GO	**R/W**	start low power mode	0x00000000
0x20	SWDT_EN	**R/W**	swdt enable.it is automatically enable work in low power mode	0x00000000
0x24	SWDT_LOAD_EN	**R/W**	swdt reload count value enable. enabling needs to last at least 100 us	0x00000000
0x28	SWDT_LOAD_CNT	**R/W**	swdt reload count value.the upper 12 bits are the load count value, and the lower 4 bits are not configurable (N*16*LOSC clock cycle(about 30us))	0x0000000A
0x2C	SWDT_INTR_CLR	**R/W**	swdt interrupt clear	0x00000000
0x44	LDO_CUR	**R/W**	ldo current adjustment	0x00000004
0x80	VS_ADJ	**R/W**	VS voltage adjustment	0x00000002
0x88	VS_EN	**R/W**	output voltage enable	0x00000000
0xC0	UVLO_ADJ	**R/W**	uvlo adjustment	0x00000002
0xC4	UVLO_HVR	**R/W**	uvlo high voltage reset control	0x00000000
0xCC	UVLO_EN	**R/W**	uvlo enable	0x00000000
0xD0	UVLO_STAT	**R/W**	uvlo state register	0x000001FF
0x100	SRAM_SEL	**R/W**	sram enable	0x000000FF

RST: (Base Addr 0x50002400)

OFFSET	NAME	R/W	Description	Default
0x00	PDR_EN	**R/W**	PDR module enable	0x00000001
0x04	CHIP_RSTN	**R/W**	Chip reset control register	0x00000001
0x08	MCU_RSTN	**R/W**	Digital reset control register	0x00000001
0x0C	CPU_RSTN	**R/W**	Cpu reset control register	0x00000001
0x40	AFE_RSTN	**R/W**	Afe module reset	0x00000001
0x44	I^2C_RSTN	**R/W**	I2c module reset	0x00000001
0x48	CRC_RSTN	**R/W**	Crc module reset	0x00000001
0x4C	HDIV_RSTN	**R/W**	Hdiv module reset	0x00000001
0x50	UART_RSTN	**R/W**	Uart module reset	0x00000001
0x54	TMR0_RSTN	**R/W**	Timer0 module reset	0x00000001

0x58	TMR1_RSTN	**R/W**	Timer1 module reset	0x00000001
0x5C	GPIO_RSTN	**R/W**	gpio module reset	0x00000001
0x80	WDT_RSTN_EN	**R/W**	reset enable	0x0000000E
CLK: (Base Addr 0x50002800)				
OFFSET	**NAME**	**R/W**	**Description**	**Default**
0x08	OSC_EN	**R/W**	Osc enable	0x00000007
0x0C	HOSC_EN	**R/W**	Internal high-speed osc clk enable	0x00000001
0x10	HOSC_MOD	**R/W**	Internal high-speed osc clk frequency configuration	0x00000000
0x14	SYS_CLK_MUX	**R/W**	system clock source selection	0x00000001
0x18	ADC_CLK_DIV	**R/W**	adc clk frequency configuration	0x00000006
0x1C	ISP_CLK_EN	**R/W**	isp module clock enable	0x00000001
0x20	ADC_CLK_EN	**R/W**	adc module clock enable	0x00000001
0x24	WDT0_CLK_EN	**R/W**	wdt0 module clock enable	0x00000001
0x28	WDT1_CLK_EN	**R/W**	wdt1 module clock enable	0x00000001
0x2C	WDT2_CLK_EN	**R/W**	wdt2 module clock enable	0x00000001
0x34	SEL_SYS_CLK	**RO**	system clock selection results.	0x0000001B
0x40	AFE_CLK_EN	**R/W**	afe module clock enable	0x00000001
0x44	I^2C_CLK_EN	**R/W**	i2c module clock enable	0x00000001
0x48	CRC_CLK_EN	**R/W**	crc module clock enable	0x00000001
0x4C	HDIV_CLK_EN	**R/W**	hdiv module clock enable	0x00000001
0x50	UART_CLK_EN	**R/W**	uart module clock enable	0x00000001
0x54	TMR0_CLK_EN	**R/W**	timer0 module clock enable	0x00000001
0x58	TMR1_CLK_EN	**R/W**	timer1 module clock enable	0x00000001
0x5C	GPIO_CLK_EN	**R/W**	gpio module clock enable	0x00000001
FMC: (Base Addr 0x5000C000)				
OFFSET	**NAME**	**R/W**	**Description**	**Default**
0x00	ISP_CR	**R/W**	Isp control register	0x00000016
0x04	ISP_ADR	**R/W**	Flash address register	0x00000000
0x08	ISP_WDAT0	**R/W**	Isp write data register (for write one word)	0x00000000
0x0C	ISP_RDAT0	**RO**	Isp read data register (for read one word)	0x00000000
0x10	ISP_CMD	**R/W**	isp instruction register	0x000002f8
0x14	ISP_GO	**R/W**	isp trigger register	0x00000000
0x40	T_NVS	**R/W**	PROG/ERASE/CEb/NVR/Address to WEb Setup time	0x00000096
0x44	T_PGS	**R/W**	WEb low to PROG2 high Setup time	0x00000096
0x48	T_PROG	**R/W**	Byte Program Time	0x00000096
0x4C	T_RCV	**R/W**	WEb High to PROG/ERASE Low Setup time	0x00000096
0x50	T_RW	**R/W**	Latency to next operation after PROG/ ERASE low	0x00000003

0x54	T_ERASE	**R/W**	erase operation execution time	0x000186A0
0x58	T_WAKEUP	**R/W**	wake-up time	0x000000fa
0x80	ISP_WDAT0	**R/W**	Isp write data register 1st words	0x00000000
0x84	ISP_WDAT1	**R/W**	Isp write data register 2nd words	0x00000000
0x88	ISP_WDAT2	**R/W**	Isp write data register 3rd words	0x00000000
0x8C	ISP_WDAT3	**R/W**	Isp write data register 4th words	0x00000000
0x90	ISP_WDAT4	**R/W**	Isp write data register 5th words	0x00000000
0x94	ISP_WDAT5	**R/W**	Isp write data register 6th words	0x00000000
0x98	ISP_WDAT6	**R/W**	Isp write data register 7th words	0x00000000
0x9C	ISP_WDAT7	**R/W**	Isp write data register 8th words	0x00000000
0xA0	ISP_WDAT8	**R/W**	Isp write data register 9th words	0x00000000
0xA4	ISP_WDAT9	**R/W**	Isp write data register 10th words	0x00000000
0xA8	ISP_WDAT10	**R/W**	Isp write data register 11th words	0x00000000
0xAC	ISP_WDAT11	**R/W**	Isp write data register 12th words	0x00000000
0xB0	ISP_WDAT12	**R/W**	Isp write data register 13th words	0x00000000
0xB4	ISP_WDAT13	**R/W**	Isp write data register 14th words	0x00000000
0xB8	ISP_WDAT14	**R/W**	Isp write data register 15th words	0x00000000
0xBC	ISP_WDAT15	**R/W**	Isp write data register 16th words	0x00000000
0xC0	ISP_RDAT0	**RO**	Isp read data register (first word)	0x00000000
0xC4	ISP_RDAT1	**RO**	Isp read data register (second word)	0x00000000
0xC8	ISP_RDAT2	**RO**	Isp read data register (3th word)	0x00000000
0xCC	ISP_RDAT3	**RO**	Isp read data register (4th word)	0x00000000
0xD0	ISP_RDAT4	**RO**	Isp read data register (5th word)	0x00000000
0xD4	ISP_RDAT5	**RO**	Isp read data register (6th word)	0x00000000
0xD8	ISP_RDAT6	**RO**	Isp read data register (7th word)	0x00000000
0xDC	ISP_RDAT7	**RO**	Isp read data register (8th word)	0x00000000
0xE0	ISP_RDAT8	**RO**	Isp read data register (9th word)	0x00000000
0xE4	ISP_RDAT9	**RO**	Isp read data register (10th word)	0x00000000
0xE8	ISP_RDAT10	**RO**	Isp read data register (11th word)	0x00000000
0xEC	ISP_RDAT11	**RO**	Isp read data register (12th word)	0x00000000
0xF0	ISP_RDAT12	**RO**	Isp read data register (13th word)	0x00000000
0xF4	ISP_RDAT13	**RO**	Isp read data register (14th word)	0x00000000
0xF8	ISP_RDAT14	**RO**	Isp read data register (15th word)	0x00000000
0xFC	ISP_RDAT15	**RO**	Isp read data register (16th word)	0x00000000
RMC: (Base Addr 0x5000E000)				
OFFSET	**NAME**	**R/W**	**Description**	**Default**
0x00	RM_CON	**R/W**	Sram control register	0x00000000
HDIV: (Base Addr 0x50014000)				
OFFSET	**NAME**	**R/W**	**Description**	**Default**

0x00	DIVIDEND	**R/W**	dividend register	0x00000000
0x04	DIVISOR	**R/W**	divisor register	0x00000001
0x08	DIVIVQUO	**RO**	quotient register	0x00000000
0x0C	DIVREM	**RO**	remainder register	0x00000000
0x10	DIVSTS	**RO**	status register	0x00000000

CRC: (Base Addr 0x50024000)

OFFSET	NAME	R/W	Description	Default
0x00	CRC_DR	**R/W**	data register	0x00000000
0x04	CRC_IDR	**R/W**	temporary data storage register	0x00000000
0x08	CRC_CR	**R/W**	control register	0x00000000
0x10	CRC_INIT	**R/W**	initial value register	0x00000000
0x14	CRC_XOR	**R/W**	xor result register	0xFFFFFFFF

WDT0: (Base Addr 0x40000000)

OFFSET	NAME	R/W	Description	Default
0x00	WDT_CTRL	**R/W**	Control register	0x00000002
0x04	WDT_PERIOD	**R/W**	Timeout range register	0x00000000
0x08	WDT_CUR_CNT	**R/W**	Current counter value register	0x0000FFFF
0x0C	WDT_RESTART	**WO**	Counter restart register	0x00000000
0x10	WDT_STATUS	**RO**	Interrupt status register	0x00000000
0x14	WDT_ICR	**RO**	Interrupt clear register	0x00000000

WDT1: (Base Addr 0x40001000)

OFFSET	NAME	R/W	Description	Default
0x00	WDT1_CTRL	**R/W**	Control register	0x00000002
0x04	WDT1_PERIOD	**R/W**	Timeout range register	0x00000000
0x08	WDT1_CUR_CNT	**R/W**	Current counter value register	0x0000FFFF
0x0C	WDT1_RESTART	**WO**	Counter restart register	0x00000000
0x10	WDT1_STATUS	**RO**	Interrupt status register	0x00000000
0x14	WDT1_ICR	**RO**	Interrupt clear register	0x00000000

UART: (Base Addr 0x40003000)

OFFSET	NAME	R/W	Description	Default
0x00	DIV_LL	**R/W**	Divisor Latch (Low)	0x00000000
0x04	INTEN	**R/W**	Interrupt Enable Register	0x00000000
0x08	FIFO_CTRL	**WO**	FIFO Control Register	0x00000000
0x0C	LINE_CTRL	**R/W**	Line Control Register	0x00000000
0x14	LINE_STATUS	**RO**	Line Status Register	0x00000060

0x70	FIFO_ACC	**R/W**	FIFO Access Register	0x00000000
0x74	TXFIFO_RD	**RO**	Transmit FIFO Read	0x00000000
0x78	RXFIFO_WR	**WO**	Receive FIFO Write	0x00000000
0x7C	UART_STATUS	**RO**	UART Status Register	0x00000006
0x80	TXFIFO_LEV	**RO**	Transmit FIFO Level	0x00000000
0x84	RXFIFO_LEV	**RO**	Receive FIFO Level	0x00000000

TIMER0: (Base Addr 0x40004000)

OFFSET	NAME	R/W	Description	Default
0x00	TIM0_LOADCNT	**R/W**	Value to be loaded into Timer	0x00000000
0x04	TIM0_CURVAL	**RO**	Current Value of Timer	0x00000000
0x08	*TIM0_CTRL*	**R/W**	Control Register for Timer	0x00000000
0x0c	TIM0_ICR	**RO**	clears all active interrupts and then Returns all zeroes (0)	0x00000000
0x10	TIM0_STATUS	**RO**	The interrupt status of timer0 in the component.	0x00000000

TIMER1: (Base Addr 0x40005000)

OFFSET	NAME	R/W	Description	Default
0x00	TIM1_LOADCNT	**R/W**	Value to be loaded into Timer	0x00000000
0x04	TIM1_CURVAL	**RO**	Current Value of Timer	0x00000000
0x08	TIM1_CTRL	**R/W**	Control Register for Timer	0x00000000
0x0c	TIM1_ICR	**RO**	Returns all zeroes (0) and clears all active interrupts	0x00000000
0x10	TIM1_STATUS	**RO**	The interrupt status of timer1 in the component.	0x00000000

I²C0: (Base Addr 0x40006000)

OFFSET	NAME	R/W	Description	Default
0x00	I²C_CONTROL	**R/W**	I²C Control	0x0000007F
0x04	I²C_TAR_ADDR	**R/W**	I²C Target Address	0x00001055
0x08	I²C_SLV_ADDR	**R/W**	I²C Slave Address	0x00000055
0x10	I²C_DA_BUF_CMD	**R/W**	I²C Rx/Tx Data Buffer and Command	0x00000000
0x14	I²C_ST_SCLH_CNT	**R/W**	Standard speed I²C Clock SCL High level Count value	0x00000190
0x18	I²C_ST_SCLL_CNT	**R/W**	Standard speed I²C Clock SCL Low level Count value	0x000001D6
0x1C	I²C_FT_SCLH_CNT	**R/W**	Fast speed I²C Clock SCL High level Count value	0x0000003C
0x20	I²C_FT_SCLL_CNT	**R/W**	Fast speed I²C Clock SCL Low level Count value	0x00000082
0x2C	I²C_INT_STATUS	**RO**	I²C Interrupt Status	0x00000000
0x30	I²C_INT_FLAG	**R/W**	I²C Interrupt Mask	0x00000000
0x34	I²C_RAW_INT_STATUS	**RO**	I²C Raw Interrupt Status	0x00000000
0x38	I²C_RX_FIFO_TH	**R/W**	I²C Receive FIFO Threshold	0x00000000
0x3C	I²C_TX_FIFO_TH	**R/W**	I²C Transmit FIFO Threshold	0x00000000
0x40	I²C_CLR_INT	**RO**	Clear Combined and Individual Interrupts	0x00000000
0x44	I²C_CLR_RX_UD_INT	**RO**	Clear RX_UNDER Interrupt	0x00000000
0x48	I²C_CLR_RX_OV_INT	**RO**	Clear RX_OVER Interrupt	0x00000000

0x4C	I²C_CLR_TX_OV_INT	**RO**	Clear TX_OVER Interrupt	0x00000000
0x50	I²C_CLR_RD_REQ_INT	**RO**	Clear RD_REQ Interrupt	0x00000000
0x54	I²C_CLR_TX_ABRT_INT	**RO**	Clear TX_ABRT Interrupt	0x00000000
0x58	I²C_CLR_RX_DONE_INT	**RO**	Clear RX_DONE Interrupt	0x00000000
0x5C	I²C_CLR_ACTIVITY_INT	**RO**	Clear ACTIVITY Interrupt	0x00000000
0x60	I²C_CLR_STOP_DET_INT	**RO**	Clear STOP_DET Interrupt	0x00000000
0x64	I²C_CLR_STAR_DET_INT	**RO**	Clear START_DET Interrupt	0x00000000
0x68	I²C_CLR_GEN_CAL_INT	**RO**	Clear GEN_CALL Interrupt	0x00000000
0x6C	I²C_ENABLE	**R/W**	I²C Enable	0x00000000
0x70	I²C_STATUS	**RO**	I²C Status register	0x00000006
0x74	I²C_TX_FIFO_LEVEL	**RO**	Transmit FIFO Level Register	0x00000000
0x78	I²C_RX_FIFO_LEVEL	**RO**	Receive FIFO Level Register	0x00000000
0x7C	I²C_SDA_HOLD_TIME	**R/W**	SDA hold time length register	0x00000001
0x80	I²C_TX_ABRT_STATUS	**R/W**	I²C Transmit Abort Status Register	0x00000000
0x94	I²C_SDA_SETUP_TIME	**R/W**	I²C SDA Setup Register	0x00000064
0x98	I²C_ACK_GEN_CALL	**R/W**	I²C ACK General Call Register	0x00000001
0x9C	I²C_ENABLE_STATUS	**RO**	I²C Enable Status Register	0x00000000
0xA0	I²C_FS_SPK_LIMIT	**R/W**	ISS and FS spike suppression limit	0x00000005
0xA4	I²C_HS_SPK_LIMIT	**R/W**	HS spike suppression limit	0x00000001

AFE: (Base Addr 0x40008000)

OFFSET	NAME	R/W	Description	Default
0x00	ADCH0CR0	**R/W**	channel 0 ADC configuration register0	0x00003FFF
0x04	ADCH0CR1	**R/W**	channel 0 ADC configuration register1	0x43640023
0x08	DACH0CR	**R/W**	channel 0 DAC configuration register	0x00000900
0x0C	DACH0DR	**R/W**	channel 0 DAC data register0	0x00000000
0x10	ADCH0DR	**RO**	channel 0 ADC data register	0x00000000
0x20	ADCH1CR0	**R/W**	channel 1 ADC configuration register0	0x00003FFF
0x24	ADCH1CR1	**R/W**	channel 1 ADC configuration register1	0x43640023
0x28	DACH1CR	**R/W**	channel 1 DAC configuration register	0x00000900
0x2C	DACH1DR	**R/W**	channel 1 DAC data register0	0x00000000
0x30	ADCH1DR	**RO**	channel 1 ADC data register	0x00000000
0x40	ADCH2CR0	**R/W**	channel 2 ADC configuration register0	0x00003FFF
0x44	ADCH2CR1	**R/W**	channel 2 ADC configuration register1	0x43640023
0x48	DACH2CR	**R/W**	channel 2 DAC configuration register	0x00000900
0x4C	DACH2DR	**R/W**	channel 2 DAC data register0	0x00000000
0x50	ADCH2DR	**RO**	channel 2 ADC data register	0x00000000
0x60	ADCH3CR0	**R/W**	channel 3 ADC configuration register0	0x00003FFF
0x64	ADCH3CR1	**R/W**	channel 3 ADC configuration register1	0x43640023
0x68	DACH3CR	**R/W**	channel 3 DAC configuration register	0x00000900

0x6C	DACH3DR	**R/W**	channel 3 DAC data register0	0x00000000
0x70	ADCH3DR	**RO**	channel 3 ADC data register	0x00000000
0x80	ADCH4CR0	**R/W**	channel 4 ADC configuration register0	0x00003FFF
0x84	ADCH4CR1	**R/W**	channel 4 ADC configuration register1	0x43640023
0x88	DACH4CR	**R/W**	channel 4 DAC configuration register	0x00000900
0x8C	DACH4DR	**R/W**	channel 4 DAC data register0	0x00000000
0x90	ADCH4DR	**RO**	channel 4 ADC data register	0x00000000
0xA0	ADCH5CR0	**R/W**	channel 5 ADC configuration register0	0x00003FFF
0xA4	ADCH5CR1	**R/W**	channel 5 ADC configuration register1	0x43640023
0xA8	DACH5CR	**R/W**	channel 5 DAC configuration register	0x00000900
0xAC	DACH5DR	**R/W**	channel 5 DAC data register0	0x00000000
0xB0	ADCH5DR	**RO**	channel 5 ADC data register	0x00000000
0xC0	ADCH6CR0	**R/W**	channel 6 ADC configuration register0	0x00003FFF
0xC4	ADCH6CR1	**R/W**	channel 6 ADC configuration register1	0x43640023
0xC8	DACH6CR	**R/W**	channel 6 DAC configuration register	0x00000900
0xCC	DACH6DR	**R/W**	channel 6 DAC data register0	0x00000000
0xD0	ADCH6DR	**RO**	channel 6 ADC data register	0x00000000
0xE0	ADCH7CR0	**R/W**	channel 7 ADC configuration register0	0x00003FFF
0xE4	ADCH7CR1	**R/W**	channel 7 ADC configuration register1	0x43640023
0xE8	DACH7CR	**R/W**	channel 7 DAC configuration register	0x00000900
0xEC	DACH7DR	**R/W**	channel 7 DAC data register0	0x00000000
0xF0	ADCH7DR	**RO**	channel 7 ADC data register	0x00000000
0x100	ADCH8CR0	**R/W**	channel 8 ADC configuration register0	0x00003FFF
0x104	ADCH8CR1	**R/W**	channel 8 ADC configuration register1	0x43640023
0x108	DACH8CR	**R/W**	channel 8 DAC configuration register	0x00000900
0x10C	DACH8DR	**R/W**	channel 8 DAC data register0	0x00000000
0x110	ADCH8DR	**RO**	channel 8 ADC data register	0x00000000
0x120	ADCH9CR0	**R/W**	channel 9 ADC configuration register0	0x00003FFF
0x124	ADCH9CR1	**R/W**	channel 9 ADC configuration register1	0x43640023
0x128	DACH9CR	**R/W**	channel 9 DAC configuration register	0x00000900
0x12C	DACH9DR	**R/W**	channel 9 DAC data register0	0x00000000
0x130	ADCH9DR	**RO**	channel 9 ADC data register	0x00000000
0x140	ADCH10CR0	**R/W**	channel 10 ADC configuration register0	0x00003FFF
0x144	ADCH10CR1	**R/W**	channel 10 ADC configuration register1	0x43640023
0x148	DACH10CR	**R/W**	channel 10 DAC configuration register	0x00000900
0x14C	DACH10DR	**R/W**	channel 10 DAC data register0	0x00000000
0x150	ADCH10DR	**RO**	channel 10 ADC data register	0x00000000
0x160	ADCH11CR0	**R/W**	channel 11 ADC configuration register0	0x00003FFF
0x164	ADCH11CR1	**R/W**	channel 11 ADC configuration register1	0x43640023
0x168	DACH11CR	**R/W**	channel 11 DAC configuration register	0x00000900
0x16C	DACH11DR	**R/W**	channel 11 DAC data register0	0x00000000

0x170	ADCH11DR	**RO**	channel 11 ADC data register	0x00000000
0x180	ADCH12CR0	**R/W**	channel 12 ADC configuration register0	0x00003FFF
0x184	ADCH12CR1	**R/W**	channel 12 ADC configuration register1	0x43640023
0x188	DACH12CR	**R/W**	channel 12 DAC configuration register	0x00000900
0x18C	DACH12DR	**R/W**	channel 12 DAC data register0	0x00000000
0x190	ADCH12DR	**RO**	channel 12 ADC data register	0x00000000
0x1A0	ADCH13CR0	**R/W**	channel 13 ADC configuration register0	0x00003FFF
0x1A4	ADCH13CR1	**R/W**	channel 13 ADC configuration register1	0x43640023
0x1A8	DACH13CR	**R/W**	channel 13 DAC configuration register	0x00000900
0x1AC	DACH13DR	**R/W**	channel 13 DAC data register0	0x00000000
0x1B0	ADCH13DR	**RO**	channel 13 ADC data register	0x00000000
0x1C0	ADCH14CR0	**R/W**	channel 14 ADC configuration register0	0x00003FFF
0x1C4	ADCH14CR1	**R/W**	channel 14 ADC configuration register1	0x43640023
0x1C8	DACH14CR	**R/W**	channel 14 DAC configuration register	0x00000900
0x1CC	DACH14DR	**R/W**	channel 14 DAC data register0	0x00000000
0x1D0	ADCH14DR	**RO**	channel 14 ADC data register	0x00000000
0x1E0	ADCH15CR0	**R/W**	channel 15 ADC configuration register0	0x00003FFF
0x1E4	ADCH15CR1	**R/W**	channel 15 ADC configuration register1	0x43640023
0x1E8	DACH15CR	**R/W**	channel 15 DAC configuration register	0x00000900
0x1EC	DACH15DR	**R/W**	channel 15 DAC data register0	0x00000000
0x1F0	ADCH15DR	**RO**	channel 15 ADC data register	0x00000000
0x400	ADMCR	**R/W**	ADC mode control register	0x00000000
0x404	ADTDR	**R/W**	ADC trigger delay control register	0x00280000
0x408	ADSR	**R/W**	ADC status register	0x00000000
0x40C	ADCMPCR0	**R/W**	ADC compare register0	0x00000000
0x410	ADCMPCR1	**R/W**	ADC compare register1	0x00000000
0x414	ADCHEN	**R/W**	channel enable register	0x00000000
0x418	DAOSDR	**R/W**	DAC offset calibration register	0x00000000

GPIO: (Base Addr 0x40009000)

OFFSET	NAME	R/W	Description	Default
0x00	GPIO_ODR	**R/W**	GPIO output data register	0x00000000
0x04	GPIO_OER	**R/W**	GPIO output enable register	0x00000000
0x30	GPIO_INTR	**R/W**	GPIO interrupt enable register	0x00000000
0x34	GPIO_INTMR	**R/W**	GPIO interrupt mask register	0x00000000
0x38	GPIO_INTLR	**R/W**	GPIO interrupt level register	0x00000000
0x3C	GPIO_INTPR	**R/W**	GPIO interrupt polarity register	0x00000000
0x40	GPIO_INTSR	**RO**	GPIO interrupt status register	0x00000000
0x44	GPIO_INTRSR	**RO**	GPIO raw interrupt status register	0x00000000
0x4C	GPIO_ICR	**R/W**	GPIO interrupt clear register	0x00000000
0x50	GPIO_IDR	**RO**	GPIO input data register	0x00000000

0x68	GPIO_INTBER	**R/W**	GPIO interrupt both edge register	0x00000000
NVIC: (Base Addr 0xE000E100)				
OFFSET	**NAME**	**R/W**	**Description**	**Default**
0x00	NVIC_ISER	**R/W**	IRQ0-IRQ11 Set-Enable control register	0x00000000
0x80	NVIC_ICER	**R/W**	IRQ0-IRQ11 Clear-Enable control register	0x00000000
0x100	NVIC_ISPR	**R/W**	IRQ0-IRQ11 Set-Pending control register	0x00000000
0x180	NVIC_ICPR	**R/W**	IRQ0-IRQ11 Clear-Pending control register	0x00000000
0x300	NVIC_IPR0	**R/W**	IRQ0-IRQ3 priority control register	0x00000000
0x304	NVIC_IPR1	**R/W**	IRQ4-IRQ7 priority control register	0x00000000
0x308	NVIC_IPR2	**R/W**	IRQ8-IRQ11 priority control register	0x00000000

Register Detailed Description

SYS: (Base Addr 0x50000000)

CHIP_ID: (Offset 00h)

Bit	Symbol	R/W	Description	Default
31:0	ID	RO	Chip ID (41571923h) will be returned after read.	0x41571923

DATE: (Offset 04h)

Bit	Symbol	R/W	Description	Default
31:0	REG_DATE	RO	Project date information	0x20191115

FLS_ID: (Offset 08h)

Bit	Symbol	R/W	Description	Default
31:0	FLASH ID	RO	flash id information	0x00086803

FLS_DATE: (Offset 0Ch)

Bit	Symbol	R/W	Description	Default
31:0	FLASH DATE	RO	flash date information	0x20191225

CFG_MOD: (Offset 20h)

Bit	Symbol	R/W	Description	Default
31:16	CFG_FROM_FLS	RW	configuration from Flash or register 0x5A5A: from flash	0x5A5A
15:8	Reserved	RO	Reserved	0x0
7:4	CFG_FLS_PROG_FLG	RO	FLASH configuration flag 0x0: configuration finish	0xF
3:2	FLS_BOOT_MOD	RO	Flash Configure startup mode 0b00: ROM 0b01: FLASH LDROM 0b10: SRAM 0b11: SRAM	0x3

1:0	BOOT_MOD_CBS	RW	Register configure startup mode 0b00: ROM 0b01: FLASH LDROM 0b10: SRAM 0b11: SRAM	0x0

BIAS_EN: (Offset 40h)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RW	Reserved	0
0	EN	RW	Configuration bias switch enable 0: disable 1: enable	0x1

D2A_SPACE: (Offset 5Ch)

Bit	Symbol	R/W	Description	Default
31:0	SPACE	RW	Digital-to-analog interface reservation configuration	0x0

PA_MFC_MUX: (Offset 80h)

Bit	Symbol	R/W	Description	Default
31:30	MUX15	RW	GPIO 15pin multi-function configuration. 0b00: SWDIO 0b01: GPIO15 0b10: GPIO15 0b11: GPIO15	0x0
29:28	MUX14	RW	GPIO 14pin multi-function configuration. 0b00: SWCLK 0b01: GPIO14 0b10: GPIO14 0b11: GPIO14	0x0
27:26	MUX13	RW	GPIO 13pin multi-function configuration. 0b00: SDA0 0b01: UART_RXD 0b10: GPIO13 0b11: GPIO13	0x0
25:24	MUX12	RW	GPIO 12pin multi-function configuration. 0b00: SCL0 0b01: UART_TXD 0b10: GPIO12 0b11: GPIO12	0x0
23:22	MUX11	RW	GPIO 11pin multi-function configuration. 0b00: SDA1 0b01: AINP11 0b10: UART_TXD 0b11: GPIO11	0x0
21:20	MUX10	RW	GPIO 10pin multi-function configuration. 0b00: SCL1 0b01: AINN11 0b10: UART_RXD 0b11: GPIO10	0x0

19:18	MUX9	RW	GPIO 9pin multi-function configuration. 0b00: GPIO9 0b01: GPIO9 0b10: GPIO9 0b11: GPIO9	0x0
17:16	MUX8	RW	GPIO 8pin multi-function configuration. 0b00: GPIO8 0b01: AINP10 0b10: GPIO8 0b11: GPIO8	0x0
15:14	MUX7	RW	GPIO 7pin multi-function configuration. 0b00: GPIO7 0b01: AINN10 0b10: GPIO7 0b11: GPIO7	0x0
13:12	MUX6	RW	GPIO 6pin multi-function configuration. 0b00: GPIO6 0b01: EOSC_CLK 0b11: GPIO6	0x0
11:10	MUX5	RW	GPIO 5pin multi-function configuration. 0b00: GPIO5 0b01: TEST_CLK 0b10: GPIO5 0b11: GPIO5	0x0
9:8	MUX4	RW	GPIO 4pin multi-function configuration. 0b00: GPIO4 0b10: GPIO4 0b11: GPIO4	0x0
7:6	MUX3	RW	GPIO 3pin multi-function configuration. 0b00: GPIO3 0b01: VS 0b10: GPIO3 0b11: GPIO3	0x0
5:4	MUX2	RW	GPIO 2pin multi-function configuration. 0b00: GPIO2 0b01: VS 0b10: GPIO2 0b11: GPIO2	0x0
3:2	MUX1	RW	GPIO 1pin multi-function configuration. 0b00: GPIO1 0b01: VS 0b10: GPIO1 0b11: GPIO1	0x0
1:0	MUX0	RW	GPIO 0pin multi-function configuration. 0b00: GPIO0 0b01: VS 0b10: GPIO0 0b11: GPIO0	0x0

PA_ADJ_DEG: (Offset 84h)

Bit	Symbol	R/W	Description	Default

31:16	Reserved	RO	Reserved	0
15:0	ADJ_DEG	RW	GPIO13 pin deglitch time configuration. 0:I²C 1:UART	0x0

PA_ADJ_OD: (Offset 88h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0
13	ADJ_OD13	RW	GPIO13 pin open-drain output delay time control. 0:20ns 1:2ns	0x0
12	ADJ_OD12	RW	GPIO12 pin open-drain output delay time control. 0:20ns 1:2ns	0x0
11	ADJ_OD11	RW	GPIO11 pin open-drain output delay time control. 0:20ns 1:2ns	0x0
10	ADJ_OD10	RW	GPIO10 pin open-drain output delay time control. 0:20ns 1:2ns	0x0
9	ADJ_OD9	RW	GPIO9 pin open-drain output delay time control. 0:20ns 1:2ns	0x0
8	ADJ_OD8	RW	GPIO8 pin open-drain output delay time control. 0:20ns 1:2ns	0x0
7	ADJ_OD7	RW	GPIO7 pin open-drain output delay time control. 0:20ns 1:2ns	0x0
6	ADJ_OD6	RW	GPIO6 pin open-drain output delay time control. 0:20ns 1:2ns	0x0
5	ADJ_OD5	RW	GPIO5 pin open-drain output delay time control. 0:20ns 1:2ns	0x0
4	ADJ_OD4	RW	GPIO4 pin open-drain output delay time control. 0:20ns 1:2ns	0x0
3:0	Reserved	RO	Reserved	0

PA_IN_EN: (Offset 8Ch)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0
15:14	Reserved	RO	Reserved	0x3
13	IN_EN13	RW	GPIO13 pin input enable control. (GPIO14 and GPIO15 are used for debug interface) 0:disable 1:enable	0x1

12	IN_EN12	RW	GPIO12 pin input enable control. (GPIO14 and GPIO15 are used for debug interface) 0:disable 1:enable	0x1
11	IN_EN11	RW	GPIO11 pin input enable control. (GPIO14 and GPIO15 are used for debug interface) 0:disable 1:enable	0x1
10	IN_EN10	RW	GPIO10 pin input enable control. (GPIO14 and GPIO15 are used for debug interface) 0:disable 1:enable	0x1
9	IN_EN9	RW	GPIO9 pin input enable control. (GPIO14 and GPIO15 are used for debug interface) 0:disable 1:enable	0x1
8	IN_EN8	RW	GPIO8 pin input enable control. (GPIO14 and GPIO15 are used for debug interface) 0:disable 1:enable	0x1
7	IN_EN7	RW	GPIO7 pin input enable control. (GPIO14 and GPIO15 are used for debug interface) 0:disable 1:enable	0x1
6	IN_EN6	RW	GPIO6 pin input enable control. (GPIO14 and GPIO15 are used for debug interface) 0:disable 1:enable	0x1
5	IN_EN5	RW	GPIO5 pin input enable control. (GPIO14 and GPIO15 are used for debug interface) 0:disable 1:enable	0x1
4	IN_EN4	RW	GPIO4 pin input enable control. (GPIO14 and GPIO15 are used for debug interface) 0:disable 1:enable	0x1
3	IN_EN3	RW	GPIO3 pin input enable control. (GPIO14 and GPIO15 are used for debug interface) 0:disable 1:enable	0x1

2	IN_EN2	RW	GPIO2 pin input enable control. (GPIO14 and GPIO15 are used for debug interface) 0:disable 1:enable	0x1
1	IN_EN1	RW	GPIO1 pin input enable control. (GPIO14 and GPIO15 are used for debug interface) 0:disable 1:enable	0x1
0	IN_EN0	RW	GPIO0 pin input enable control. (GPIO14 and GPIO15 are used for debug interface) 0:disable 1:enable	0x1

PA_OD_EN: (Offset 94h)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0
15	OD_EN15	RW	GPIO15 pin open-drain output enable. 0:push_pull 1:open_drain	0x0
14	OD_EN14	RW	GPIO14 pin open-drain output enable. 0:push_pull 1:open_drain	0x0
13	OD_EN13	RW	GPIO13 pin open-drain output enable. 0:disable OD 1:open_drain	0x0
12	OD_EN12	RW	GPIO12 pin open-drain output enable. 0:disable OD 1:open_drain	0x0
11	OD_EN11	RW	GPIO11 pin open-drain output enable. 0:disable OD 1:open_drain	0x0
10	OD_EN10	RW	GPIO10 pin open-drain output enable. 0:disable OD 1:open_drain	0x0
9	OD_EN9	RW	GPIO9 pin open-drain output enable. 0:disable OD 1:open_drain	0x0
8	OD_EN8	RW	GPIO8 pin open-drain output enable. 0:disable OD 1:open_drain	0x0
7	OD_EN7	RW	GPIO7 pin open-drain output enable. 0:disable OD 1:open_drain	0x0
6	OD_EN6	RW	GPIO6 pin open-drain output enable. 0:disable OD 1:open_drain	0x0

5	OD_EN5	RW	GPIO5 pin open-drain output enable. 0:disable OD 1:open_drain	0x0
4	OD_EN4	RW	GPIO4 pin open-drain output enable. 0:disable OD 1:open_drain	0x0
3	OD_EN3	RW	GPIO3 pin open-drain output enable. 0:push_pull 1:open_drain	0x0
2	OD_EN2	RW	GPIO2 pin open-drain output enable. 0:push_pull 1:open_drain	0x0
1	OD_EN1	RW	GPIO1 pin open-drain output enable. 0:push_pull 1:open_drain	0x0
0	OD_EN0	RW	GPIO0 pin open-drain output enable. 0:push_pull 1:open_drain	0x0

PA_SMIT_EN: (Offset 98h)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0
15	SMIT_EN15	RW	GPIO15 pin input interface schmitt trigger enable control. 0:disable. 1:enable	0x1
14	SMIT_EN14	RW	GPIO14 pin input interface schmitt trigger enable control. 0:disable. 1:enable	0x1
13	SMIT_EN13	RW	GPIO13 pin input interface schmitt trigger enable control. 0:disable. 1:enable	0x1
12	SMIT_EN12	RW	GPIO12 pin input interface schmitt trigger enable control. 0:disable. 1:enable	0x1
11	SMIT_EN11	RW	GPIO11 pin input interface schmitt trigger enable control. 0:disable. 1:enable	0x1
10	SMIT_EN10	RW	GPIO10 pin input interface schmitt trigger enable control. 0:disable. 1:enable	0x1
9	SMIT_EN9	RW	GPIO9 pin input interface schmitt trigger enable control. 0:disable. 1:enable	0x1

8	SMIT_EN8	RW	GPIO8 pin input interface schmitt trigger enable control. 0:disable. 1:enable	0x1
7	SMIT_EN7	RW	GPIO7 pin input interface schmitt trigger enable control. 0:disable. 1:enable	0x1
6	SMIT_EN6	RW	GPIO6 pin input interface schmitt trigger enable control. 0:disable. 1:enable	0x1
5	SMIT_EN5	RW	GPIO5 pin input interface schmitt trigger enable control. 0:disable. 1:enable	0x1
4	SMIT_EN4	RW	GPIO4 pin input interface schmitt trigger enable control. 0:disable. 1:enable	0x1
3	SMIT_EN3	RW	GPIO3 pin input interface schmitt trigger enable control. 0:disable. 1:enable	0x1
2	SMIT_EN2	RW	GPIO2 pin input interface schmitt trigger enable control. 0:disable. 1:enable	0x1
1	SMIT_EN1	RW	GPIO1 pin input interface schmitt trigger enable control. 0:disable. 1:enable	0x1
0	SMIT_EN0	RW	GPIO0 pin input interface schmitt trigger enable control. 0:disable. 1:enable	0x1

PA_FAST: (Offset 9Ch)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0
15	FAST_MODE15	RW	GPIO15 pin fast lane enable control. 0:slow. 1:fast	0x0
14	FAST_MODE14	RW	GPIO14 pin fast lane enable control. 0:slow. 1:fast	0x0
13	FAST_MODE13	RW	GPIO13 pin fast lane enable control. 0:slow. 1:fast	0x0
12	FAST_MODE12	RW	GPIO12 pin fast lane enable control. 0:slow. 1:fast	0x0
11	FAST_MODE11	RW	GPIO11 pin fast lane enable control. 0:slow. 1:fast	0x0

10	FAST_MODE10	RW	GPIO10 pin fast lane enable control. 0:slow. 1:fast	0x0
9	FAST_MODE9	RW	GPIO9 pin fast lane enable control. 0:slow. 1:fast	0x0
8	FAST_MODE8	RW	GPIO8 pin fast lane enable control. 0:slow. 1:fast	0x0
7	FAST_MODE7	RW	GPIO7 pin fast lane enable control. 0:slow. 1:fast	0x0
6	FAST_MODE6	RW	GPIO6 pin fast lane enable control. 0:slow. 1:fast	0x0
5	FAST_MODE5	RW	GPIO5 pin fast lane enable control. 0:slow. 1:fast	0x0
4	FAST_MODE4	RW	GPIO4 pin fast lane enable control. 0:slow. 1:fast	0x0
3	FAST_MODE3	RW	GPIO3 pin fast lane enable control. 0:slow. 1:fast	0x0
2	FAST_MODE2	RW	GPIO2 pin fast lane enable control. 0:slow. 1:fast	0x0
1	FAST_MODE1	RW	GPIO1 pin fast lane enable control. 0:slow. 1:fast	0x0
0	FAST_MODE0	RW	GPIO0 pin fast lane enable control. 0:slow. 1:fast	0x0

PA_PD_RES: (Offset A0h)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0
15	PD_RES15	RW	GPIO15 pin pull-down resistor control. 0:no pull-down resistor. 1:pull-down resistor	0x0
14	PD_RES14	RW	GPIO14 pin pull-down resistor control. 0:no pull-down resistor. 1:pull-down resistor	0x0
13:4	Reserved	RO	Reserved	0
3	PD_RES3	RW	GPIO3 pin pull-down resistor control. 0:no pull-down resistor. 1:pull-down resistor	0x0
2	PD_RES2	RW	GPIO2 pin pull-down resistor control. 0:no pull-down resistor. 1:pull-down resistor	0x0

1	PD_RES1	RW	GPIO1 pin pull-down resistor control. 0:no pull-down resistor. 1:pull-down resistor	0x0
0	PD_RES0	RW	GPIO0 pin pull-down resistor control. 0:no pull-down resistor. 1:pull-down resistor	0x0

PA_SR_CTRL1: (Offset A4h)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0
15	CTRL1_15	RW	GPIO15 pin output delay control.[CTRL2_X: CTRL1_X], X=15 0b00: 110ns 0b01: 21ns 0b10: 9ns 0b11: 3ns	0x1
14	CTRL1_14	RW	GPIO14 pin output delay control.[CTRL2_X: CTRL1_X], X=14 0b00: 110ns 0b01: 21ns 0b10: 9ns 0b11: 3ns	0x1
13:4	Reserved	RO	Reserved	0x3ff
3	CTRL1_3	RW	GPIO3 pin output delay control.[CTRL2_X: CTRL1_X], X=3 0b00: 110ns 0b01: 21ns 0b10: 9ns 0b11: 3ns	0x1
2	CTRL1_2	RW	GPIO2 pin output delay control.[CTRL2_X: CTRL1_X], X=2 0b00: 110ns 0b01: 21ns 0b10: 9ns 0b11: 3ns	0x1
1	CTRL1_1	RW	GPIO1 pin output delay control.[CTRL2_X: CTRL1_X], X=1 0b00: 110ns 0b01: 21ns 0b10: 9ns 0b11: 3ns	0x1
0	CTRL1_0	RW	GPIO0 pin output delay control.[CTRL2_X: CTRL1_X], X=0 0b00: 110ns 0b01: 21ns 0b10: 9ns 0b11: 3ns	0x1

PA_SR_CTRL2: (Offset A8h)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0

15	CTRL2_15	RW	GPIO15 pin output delay control.[CTRL2_X: CTRL1_X], X=15 0b00: 110ns 0b01: 21ns 0b10: 9ns 0b11: 3ns	0x0
14	CTRL2_14	RW	GPIO14 pin output delay control.[CTRL2_X: CTRL1_X], X=14 0b00: 110ns 0b01: 21ns 0b10: 9ns 0b11: 3ns	0x0
31:4	Reserved	RO	Reserved	0
3	CTRL2_3	RW	GPIO3 pin output delay control.[CTRL2_X: CTRL1_X], X=3 0b00: 110ns 0b01: 21ns 0b10: 9ns 0b11: 3ns	0x0
2	CTRL2_2	RW	GPIO2 pin output delay control.[CTRL2_X: CTRL1_X], X=2 0b00: 110ns 0b01: 21ns 0b10: 9ns 0b11: 3ns	0x0
1	CTRL2_1	RW	GPIO1 pin output delay control.[CTRL2_X: CTRL1_X], X=1 0b00: 110ns 0b01: 21ns 0b10: 9ns 0b11: 3ns	0x0
0	CTRL2_0	RW	GPIO0 pin output delay control.[CTRL2_X: CTRL1_X], X=0 0b00: 110ns 0b01: 21ns 0b10: 9ns 0b11: 3ns	0x0

PA_PU_RES: (Offset ACh)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0
15	PU_RES15	RW	GPIO15 pin pull-up resistor control. 0:no pull-up resistor 1:pull-up resistor	0x0
14	PU_RES14	RW	GPIO14 pin pull-up resistor control. 0:no pull-up resistor 1:pull-up resistor	0x0
13:4	Reserved	RO	Reserved	0
3	PU_RES3	RW	GPIO3 pin pull-up resistor control. 0:no pull-up resistor 1:pull-up resistor	0x0
2	PU_RES2	RW	GPIO2 pin pull-up resistor control. 0:no pull-up resistor 1:pull-up resistor	0x0

1	PU_RES1	RW	GPIO1 pin pull-up resistor control. 0:no pull-up resistor 1:pull-up resistor	0x0
0	PU_RES0	RW	GPIO0 pin pull-up resistor control. 0:no pull-up resistor 1:pull-up resistor	0x0

WR_PROT_KEY: (Offset 400h)

Bit	Symbol	R/W	Description	Default
31:8	KEY_SHIFT	RO	The system protects the KEY register.Only the lower 8 bits can be written at a time,and then lower 24 bits are shifted to 31:8 bits.Once the write sequence is :0x41574943,write protection is released, all system protected registers can be written. System write-protected registers are flows: sys_reg: CFG_MOD, FLS_TRIM, TEMP_TRIM, LOSC_TRIM, HOSC_TRIM, LDO_TRIM, rst_reg: PDR_EN, CHIP_RSTN, MCU_RSTN, CPU_RSTN, clk_reg: OSC_EN, HOSC_EN, HOSC_MOD, SYS_CLK_MUX, ADC_CLK_DIV, ISP_CLK_EN, ADC_CLK_EN,SEL_SYS_CLK, WDT0_CLK_EN, WDT1_CLK_EN, WDT2_CLK_EN, pwr_reg: SLP_MOD, SLP_DLY, PD_EN, SLP_EN, SLP_GO, SWDT_EN, SWDT_LOAD_EN, SWDT_LOAD_CNT, SWDT_INTR_CLR, LDO_CUR, VS_ADJ, UVLO_ADJ, UVLO_HVR, UVLO_EN, SRAM_EN fmc_reg: ISP_CR, ISP_ADR, ISP_WDAT0—ISP_WDAT15, ISP_CMD, ISP_GO, T_NVS, T_PGS, T_PROG, T_RCV, T_RW, T_ERASE, T_WAKEUP rmc_reg: RM_CON	0x0
7:0	KEY	RW	Write lower 8 bits	0x0

SYS_WR_PROT: (Offset 404h)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0
0	PROT_FLAG	RO	When the WR_PROT_KET register is written to the 0x41574943 sequence,the protection is released.0 means the protection is released.	0x1

PWR: (Base Addr 0x50002000)

SLP_MOD: (Offset 00h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:2	Reserved	RO	Reserved	0
1:0	CFG_SLP_MOD	RW	Chip low power mode . 0b00: normal mode 0b01: cpu sleep mode 0b10:deep sleeping mode (turn off the high-speed oscillator) 0b11:power-down mode	0x00000000

SLP_DLY: (Offset 04h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:16	Reserved	RO	Reserved	0
15:0	CFG_SLP_DLY	RW	configure delay to enter low power mode .calculated in system clock cycles（N* HOSC clock cycle）	0x0

PD_EN: (Offset 08h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:1	Reserved	RO	Reserved	0
0	CFG_PD_EN	RW	power-down mode enable. 1:enable 0:disable	0x0

SLP_EN: (Offset 0Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:1	Reserved	RO	Reserved	0
0	CFG_SLP_EN	RW	sleep mode enable . 0:disable 1:enable	0x0

SLP_GO: (Offset 10h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:1	Reserved	RO	Reserved	0
0	CFG_SLP_GO	RW	start low power mode 0: disable 1: go	0x0

SWDT_EN: (Offset 20h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:1	Reserved	RO	Reserved	0
0	CFG_SWDT_EN	RW	swdt enable.it is automatically enable work in low power mode 0: disable 1: enable	0x0

SWDT_LOAD_EN: (Offset 24h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:1	Reserved	RO	Reserved	0
0	CFG_LOAD_EN	RW	swdt reload count value enable .enabling needs to last at least 100 μs 0: disable 1:enable	0x0

SWDT_LOAD_CNT: (Offset 28h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:16	Reserved	RO	Reserved	0
15:4	CFG_LOAD_CNT	RW	swdt reload count value.the upper 12 bits are the load count value, and the lower 4 bits are not configurable (N*16*LOSC clock cycle(about 30μs))	0x0
3:0	CFG_LOAD_L_CNT	RW	the lower 4 bits are the unit configuration value for the low power mode on-delay(N* LOSC clock cycle(about 30μs))	0xA

SWDT_INTR_CLR: (Offset 2Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:1	Reserved	RO	Reserved	0
0	CFG_INTR_CLR	RW	swdt interrupt clear . 0:no effect 1:clear	0x0

LDO_CUR: (Offset 44h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:4	Reserved	RO	Reserved	0
3	CFG_LDO_RLOAD	RW	ldo output 2 μA quiescent current, not used by default 0:disable 1: enable	0x0
2:0	CFG_LDO_CUR	RW	ldo current adjustment . 0b000: 0μA 0b001: 0.8μA 0b010: 1.2μA 0b011: 2μA 0b100: 2μA 0b101: 2.8μA 0b110: 3.2μA 0b111: 4μA	0x4

VS_ADJ: (Offset 80h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:2	Reserved	RO	Reserved	0
1:0	CFG_VS_ADJ	RW	VS voltage adjustment. 0b00: 2.4V 0b01: 2.8V 0b10: 3.0V 0b11: 3.1V	0x2

VS_EN: (Offset 88h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:2	Reserved	RO	Reserved	0
1:0	CFG_VS_EN	RW	output voltage enable. 0:disable 1:enable	0x0

UVLO_ADJ: (Offset C0h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:3	Reserved	RO	Reserved	0
2:0	CFG_UVLO_ADJ	RW	uvlo adjustment. 0b000: 1.78/1.87 0b001: 1.93/2.03 0b010: 2.3/2.43 0b011: 2.61/2.7 0b100: 3.01/3.13 0b101: 3.57/3.67 0b110: 3.93/4.04 0b111: 6.4/6.5	0x2

UVLO_HVR: (Offset C4h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:1	Reserved	RO	Reserved	0
0	CFG_UVLO_HVR	RW	uvlo high voltage reset control. 0: 3.93/4.04 1: 6.4/6.5	0x0

UVLO_EN: (Offset CCh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:1	Reserved	RO	Reserved	0
0	CFG_UVLO_EN	RW	uvlo enable 0: disable 1:enable	0x0

UVLO_STAT: (Offset D0h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:18	Reserved	RO	Reserved	0
17	UVLO_INTR	RW	sram sel si	0x0
16	UVLO_FLAG	RO	cnt over flag 0: no uvlo req 1: uvlo req	0x0
15:0	CFG_FILT_VALUE	RW	config UVLO delay filter counter value	0x1FFF

SRAM_SEL: (Offset 100h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:8	Reserved	RO	Reserved	0
7:0	CFG_SRAM_SEL	RW	sram power on select signal	0xFF

RST: (Base Addr 0x50002400)				
PDR_EN: (Offset 00h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:1	Reserved	RO	Reserved	0
1:0	CFG_PDR_EN	RW	PDR module enable. 0: disable 1: enable	0x1

CHIP_RSTN: (Offset 04h)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0
0	CFG_CHIP_RSTN	RW	Chip reset control register 0: RESET 1: no effect	0x1

MCU_RSTN: (Offset 08h)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0
0	CFG_MCU_RSTN	RW	Digital reset control register 0: RESET 1: no effect	0x1

CPU_RSTN: (Offset 0Ch)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0
0	CFG_CPU_RSTN	RW	Cpu reset control register 0: RESET 1: no effect	0x1

AFE_RSTN: (Offset 40h)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0
0	CFG_AFE_RSTN	RW	Afe module reset . 0: RESET 1: no effect	0x1

I^2C_RSTN: (Offset 44h)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0
0	CFG_I^2C_RSTN	RW	I2c module reset . 0: RESET 1: no effect	0x1

CRC_RSTN: (Offset 48h)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0
0	CFG_CRC_RSTN	RW	Crc module reset . 0: RESET 1: no effect	0x1

HDIV_RSTN: (Offset 4Ch)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0
0	CFG_HDIV_RSTN	RW	Hdiv module reset . 0: RESET 1: no effect	0x1

UART_RSTN: (Offset 50h)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0
0	CFG_UART_RSTN	RW	Uart module reset . 0: RESET 1: no effect	0x1

TMR0_RSTN: (Offset 54h)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0
0	CFG_TMR0_RSTN	RW	Timer0 module reset . 0: RESET 1: no effect	0x1

TMR1_RSTN: (Offset 58h)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0
0	CFG_TMR1_RSTN	RW	Timer1 module reset . 0: RESET 1: no effect	0x1

GPIO_RSTN: (Offset 5Ch)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0
0	CFG_GPIO_RSTN	RW	Gpio module reset . 0: RESET 1: no effect	0x1

WDT_RSTN_EN: (Offset 80h)

Bit	Symbol	R/W	Description	Default
31:6	Reserved	RO	Reserved	0
5	CFG_EN_CPU_RST	RW	Cpu reset enable 0: disable 1: enable	0x0
4	CFG_EN_RMC_RST	RW	Sram reset enable 0: disable 1: enable	0x0
3	CFG_EN_SWDT_RST	RW	Swdt reset enable 0: disable 1: enable	0x1
2	CFG_EN_WDT0_RST	RW	wdt0 reset enable 0: disable 1: enable	0x1
1	CFG_EN_WDT1_RST	RW	wdt1 reset enable 0: disable 1: enable	0x1
1	CFG_EN_UVLO_RST	RW	Uvlo reset enable 0: disable 1: enable	0x1

CLK: (Base Addr 0x50002800)				
OSC_EN: (Offset 08h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:4	Reserved	RO	Reserved	0
3	Reserved	RO	Reserved	0x0
2	CFG_BIAS_EN	RW	Bias enable switch 0: disable 1: enable	0x1
1	CFG_EOSC_EN	RW	External osc clk enable 0: disable 1: enable	0x1
0	CFG_LOSC_EN	RW	Internal low-speed osc clk enable 0: disable 1: enable	0x1

HOSC_EN: (Offset 0Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:1	Reserved	RO	Reserved	0
0	CFG_HOSC_EN	RW	internal high-speed osc clk enable 0: disable 1: enable	0x1

HOSC_MOD: (Offset 10h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:2	Reserved	RO	Reserved	0
1:0	CFG_HOSC_MOD	RW	internal high-speed osc clk frequency configuration. 0b00: 24Mhz 0b01: 32Mhz 0b10: 40Mhz 0b11: 48Mhz	0x0

SYS_CLK_MUX: (Offset 14h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:2	Reserved	RO	Reserved	0
1:0	CFG_CLK_MUX	RW	system clock source selection . 0b00: Internal low-speed osc clk 0b01: internal high-speed osc clk 0b10: External osc clk 0b11: External osc clk	0x1

ADC_CLK_DIV: (Offset 18h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:16	Reserved	RO	Reserved	0
15:0	CFG_ADC_CLK_DIV	RW	adc clk frequency configuration. 0,1 : undivided. N: clock frequency divided into N times. ADC SPS is : system clock frequeny /frequency divided coefficient/40. for example : 24M/6/40=100K sps	0x6

ISP_CLK_EN: (Offset 1Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:1	Reserved	RO	Reserved	0
0	CFG_ISP_CLK_EN	RW	isp module clock enable 0: disable 1: enable	0x1

ADC_CLK_EN: (Offset 20h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:1	Reserved	RO	Reserved	0
0	CFG_ADC_CLK_EN	RW	adc module clock enable 0: disable 1: enable	0x1

WDT0_CLK_EN: (Offset 24h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:1	Reserved	RO	Reserved	0
0	CFG_WDT0_CLK_EN	RW	wdt0 module clock enable 0: disable 1: enable	0x1

WDT1_CLK_EN: (Offset 28h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:1	Reserved	RO	Reserved	0
0	CFG_WDT1_CLK_EN	RW	wdt1 module clock enable 0: disable 1: enable	0x1

WDT2_CLK_EN: (Offset 2Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:1	Reserved	RO	Reserved	0
0	CFG_WDT2_CLK_EN	RW	wdt2 module clock enable 0: disable 1: enable	0x1

SEL_SYS_CLK: (Offset 34h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:6	Reserved	RO	Reserved	0
5:4	SEL_CLK_RUSULT	RO	system clock selection results. 0b00: losc_clk 0b01: hosc_clk 0b10: eosc_clk 0b11: eosc_clk	0x1
3	SEL_CLK_OK	RO	selection clock is ok 0: fail 1: ok	0x1
2	EOSC_OK	RO	eosc clock is ok 0: fail 1: ok	0x0

1	HOSC_OK	RO	internal hosc clock is ok 0: fail 1: ok	0x1
0	LOSC_OK	RO	internal losc clock is ok 0: fail 1: ok	0x1

AFE_CLK_EN: (Offset 40h)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0
0	CFG_AFE_CLK_EN	RW	afe module clock enable 0: disable 1: enable	0x1

I²C_CLK_EN: (Offset 44h)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0
0	CFG_I²C_CLK_EN	RW	i2c module clock enable 0: disable 1: enable	0x1

CRC_CLK_EN: (Offset 48h)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0
0	CFG_CRC_CLK_EN	RW	crc module clock enable 0: disable 1: enable	0x1

HDIV_CLK_EN: (Offset 4Ch)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0
0	CFG_HDIV_CLK_EN	RW	hdiv module clock enable 0: disable 1: enable	0x1

UART_CLK_EN: (Offset 50h)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0
0	CFG_UART_CLK_EN	RW	uart module clock enable 0: disable 1: enable	0x1

TMR0_CLK_EN: (Offset 54h)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0
0	CFG_TMR0_CLK_EN	RW	tmr0 module clock enable 0: disable 1: enable	0x1

TMR1_CLK_EN: (Offset 58h)

Bit	Symbol	R/W	Description	Default

31:1	Reserved	RO	Reserved	0
0	CFG_TMR1_CLK_EN	RW	tmr1 module clock enable 0: disable 1: enable	0x1

GPIO_CLK_EN: (Offset 5Ch)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0
0	CFG_GPIO_CLK_EN	RW	GPIO module clock enable 0: disable 1: enable	0x1

FMC: (Base Addr 0x5000C000)

ISP_CR: (Offset 00h)

Bit	Symbol	R/W	Description	Default
31:6	Reserved	RO	Reserved	0
5	Reserved	RW	Reserved	0x0
4	Reserved	RW	Reserved	0x1
3	ISP_DPSTB_EN	RW	standby mode enable 0: disable 1: enable	0x0
2	ISP_APROM_EN	RW	aprom update enable 0: disable 1: enable	0x1
1	ISP_CFGDAT_EN	RW	configure data enable 0: disable 1: enable	0x1
0	ISP_EN	RW	isp enable 0: disable 1: enable	0x0

ISP_ADR: (Offset 04h)

Bit	Symbol	R/W	Description	Default
31:0	FLASH ADDR	RW	flash address	0x0

ISP_WDAT0: (Offset 08h)

Bit	Symbol	R/W	Description	Default
31:0	WR_DATA0_S	RW	isp write data (write one word)	0x0

ISP_RDAT0: (Offset 0Ch)

Bit	Symbol	R/W	Description	Default
31:0	RD_DATA0_S	RO	isp read data (read one word)	0x0

ISP_CMD: (Offset 10h)

Bit	Symbol	R/W	Description	Default
31:13	Reserved	RO	Reserved	0
12	Reserved	RW	Reserved	0x0

11	Reserved	RW	Reserved	0x0
10	Reserved	RW	Reserved	0x0
9	ISP_NVR	RW	isp selected NVR 0: no select 1: select	0x1
8	ISP_CHIP	RW	isp selected CHIP 0: no select 1: select	0x0
7:4	ISP_RW_LEN	RW	isp data length 0x0 : 1 word 0xf: 16 words	0xf
3:0	CMD	RW	isp instruction 0x0: read 0x2: write 0x4: erase 0x8: load trim	0x8

ISP_GO: (Offset 14h)

Bit	Symbol	R/W	Description	Default
31:13	Reserved	RO	Reserved	0
12	CMD_GO	RW	0: free 1: busy	0x0

T_NVS: (Offset 40h)

Bit	Symbol	R/W	Description	Default
31:0	NVS	RW	PROG/ERASE/CEb/NVR/Address to WEb Setup time	0x96

T_PGS: (Offset 44h)

Bit	Symbol	R/W	Description	Default
31:0	PGS	RW	W Eb low to PROG2 high Setup time	0x96

T_PROG: (Offset 48h)

Bit	Symbol	R/W	Description	Default
31:0	PROG	RW	Byte Program Time	0x96

T_RCV: (Offset 4Ch)

Bit	Symbol	R/W	Description	Default
31:0	RCV	RW	WEb High to PROG/ERASE Low Setup time	0x96

T_RW: (Offset 50h)

Bit	Symbol	R/W	Description	Default
31:0	RW	RW	Latency to next operation after PROG/ ERASE low	0x3

T_ERASE: (Offset 54h)

Bit	Symbol	R/W	Description	Default
31:0	ERASE	RW	erase operation execution time	0x186A0

T_WAKEUP: (Offset 58h)

Bit	Symbol	R/W	Description	Default
31:0	WAKEUP	RW	wake-up time	0xFA

ISP_WDAT0: (Offset 80h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	WDATA0	RW	isp write data	0x0

ISP_WDAT1: (Offset 84h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	WDATA1	RW	isp write data	0x0

ISP_WDAT2: (Offset 88h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	WDATA2	RW	isp write data	0x0

ISP_WDAT3: (Offset 8Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	WDATA3	RW	isp write data	0x0

ISP_WDAT4: (Offset 90h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	WDATA4	RW	isp write data	0x0

ISP_WDAT5: (Offset 94h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	WDATA5	RW	isp write data	0x0

ISP_WDAT6: (Offset 98h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	WDATA6	RW	isp write data	0x0

ISP_WDAT7: (Offset 9Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	WDATA7	RW	isp write data	0x0

ISP_WDAT8: (Offset A0h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	WDATA8	RW	isp write data	0x0

ISP_WDAT9: (Offset A4h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	WDATA9	RW	isp write data	0x0

ISP_WDAT10: (Offset A8h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	WDATA10	RW	isp write data	0x0

ISP_WDAT11: (Offset ACh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	WDATA11	RW	isp write data	0x0

ISP_WDAT12: (Offset B0h)

Bit	Symbol	R/W	Description	Default
31:0	WDATA12	RW	isp write data	0x0

ISP_WDAT13: (Offset B4h)

Bit	Symbol	R/W	Description	Default
31:0	WDATA13	RW	isp write data	0x0

ISP_WDAT14: (Offset B8h)

Bit	Symbol	R/W	Description	Default
31:0	WDATA14	RW	isp write data	0x0

ISP_WDAT15: (Offset BCh)

Bit	Symbol	R/W	Description	Default
31:0	WDATA15	RW	isp write data	0x0

ISP_RDAT0: (Offset C0h)

Bit	Symbol	R/W	Description	Default
31:0	RDATA0	RO	isp read data	0x0

ISP_RDAT1: (Offset C4h)

Bit	Symbol	R/W	Description	Default
31:0	RDATA1	RO	isp read data	0x0

ISP_RDAT2: (Offset C8h)

Bit	Symbol	R/W	Description	Default
31:0	RDATA2	RO	isp read data	0x0

ISP_RDAT3: (Offset CCh)

Bit	Symbol	R/W	Description	Default
31:0	RDATA3	RO	isp read data	0x0

ISP_RDAT4: (Offset D0h)

Bit	Symbol	R/W	Description	Default
31:0	RDATA4	RO	isp read data	0x0

ISP_RDAT5: (Offset D4h)

Bit	Symbol	R/W	Description	Default
31:0	RDATA5	RO	isp read data	0x0

ISP_RDAT6: (Offset D8h)

Bit	Symbol	R/W	Description	Default
31:0	RDATA6	RO	isp read data	0x0

ISP_RDAT7: (Offset DCh)

Bit	Symbol	R/W	Description	Default
31:0	RDATA7	RO	isp read data	0x0

ISP_RDAT8: (Offset E0h)

Bit	Symbol	R/W	Description	Default
31:0	RDATA8	RO	isp read data	0x0

ISP_RDAT9: (Offset E4h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	RDATA9	RO	isp read data	0x0

ISP_RDAT10: (Offset E8h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	RDATA10	RO	isp read data	0x0

ISP_RDAT11: (Offset ECh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	RDATA11	RO	isp read data	0x0

ISP_RDAT12: (Offset F0h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	RDATA12	RO	isp read data	0x0

ISP_RDAT13: (Offset F4h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	RDATA13	RO	isp read data	0x0

ISP_RDAT14: (Offset F8h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	RDATA14	RO	isp read data	0x0

ISP_RDAT15: (Offset FCh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	RDATA15	RO	isp read data	0x0

RMC: (Base Addr 0x5000E000)				
RM_CON: (Offset 00h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:9	Reserved	RO	Reserved	0x0
8	SRAM_PEF	RW	SRAM check mark.this bit is set automatically by the hardware when a SRAM check error is detected.it is cleared when writing 1 to this bit 0: check error 1: clear bit	0x0
7:2	Reserved	RO	Reserved	0x0
1	RSTEN	RW	SRAM check error triggers MCU reset. 0:disable trigger reset 1:enable trigger reset	0x0
0	NMI_IE	RW	NMI interrupt triggered by SRAM check error. 0:disable trigger interrupt 1: enable trigger interrupt	0x0

HDIV: (Base Addr 0x50014000)				
DIVIDEND: (Offset 00h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	DENT	RW	this register is used to store dividend	0x0

DIVISOR: (Offset 04h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	SOR	RW	this register is used to store divisor	0x1

DIVIVQUO: (Offset 08h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	QUO	RO	quotient register	0x0

DIVREM: (Offset 0Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	REM	RO	remainder register	0x0

DIVSTS: (Offset 10h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:2	Reserved	RO	Reserved	0x0
1	SOR_OK	RO	check divisor 0: divisor is not equal 0 1: divisor is equal to 0	0x0
0	FINISH	RO	status register 0: busy 1: finish	0x0

CRC: (Base Addr 0x50024000)				
CRC_DR: (Offset 00h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	DR	RW	store new data to be calculated	0x0

CRC_IDR: (Offset 04h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	IDR	RW	store temporary data	0x0

CRC_CR: (Offset 08h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:10	Reserved	RO	Reserved	0x0
9	OUT_XOR	RW	output xor control signal. 0: no xor 1: xor	0x0

8	REV_CRC	RW	flip control signal. 0: no flip 1:flip	0x0
7	REV_OUT	RW	flip output data. 0: no flip 1: flip	0x0
6:5	REV_IN	RW	flip input data. 0b00: no flip 0b01: flip by byte 0b10: flip by halfword 0b11: flip by word	0x0
4	LOAD	RW	data reload control,load the value in CRC_INIT into the current calculation,cleared by hardware 0: loading completed 1: loading	0x0
3:2	Reserved	RO	Reserved	0x0
1:0	BYTE_VALID	RW	input data valid byte position 0b00: byte 0b01: halfword 0b10 : word 0b11: word	0x0

CRC_INIT: (Offset 10h)

Bit	Symbol	R/W	Description	Default
31:0	INIT	RW	CRC initial data	0x0

CRC_XOR: (Offset 14h)

Bit	Symbol	R/W	Description	Default
31:0	XOR	RW	this register is used to store the CRC XOR value	0xFFFFFFFF

WDT0: (Base Addr 0x40000000)

WDT_CTRL: (Offset 00h)

Bit	Symbol	R/W	Description	Default
31:5	Reserved	RO	Reserved	0x0

4:2	RST_LEN	RW	Reset pulse length. Writes have no effect when the configuration parameter WDT_HC_RPL is 1, making the register bits read-only. This is used to select the number of pclk cycles for which the system reset stays asserted. The range of values available is 2 to 256 pclk cycles. 0b000: 2 pclk cycles 0b001: 4 pclk cycles 0b010: 8 pclk cycles 0b011: 16 pclk cycles 0b100: 32 pclk cycles 0b101: 64 pclk cycles 0b110: 128 pclk cycles 0b111: 256 pclk cycles	0x0
1	MODE	RW	Response mode. Writes have no effect when the parameter WDT_HC_RMOD = 1,thus this register becomes read-only. Selects the output response generated to a timeout. 0: Generate reset. 1: special reset.	0x1
0	WDT_EN	RW	WDT enable. Writable when the configuration parameter WDT_ALWAYS_EN =0, otherwise, it is readable. This bit is used to enable and disable the DW_apb_wdt. When disabled,the counter does not decrement. Thus, no interrupts or system resets are generated. Once this bit has been enabled, it can be cleared only by a system reset. 0: WDT disabled. 1: WDT enabled.	0x0

WDT_PERIOD: (Offset 04h)

Bit	Symbol	R/W	Description	Default
31:4	Reserved	RO	Reserved	0x0

3:0	TOP	RW	Timeout period. Writes have no effect when the configuration parameter WDT_HC_TOP = 1, thus making this register read-only. This field is used to select the timeout period from which the watchdog counter restarts. A change of the timeout period takes effect only after the next counter restart (kick). The range of values is limited by the WDT_CNT_WIDTH. If TOP is programmed to select a range that is greater than the counter width, the timeout period is truncated to fit to the counter width. This affects only the non-user specified values as users are limited to these boundaries during configuration. The range of values available for a 32-bit watchdog counter are: Where i = TOP and t = timeout period For i = 0 to 15 if WDT_USE_FIX_TOP==1 t = 2(16 + i) else t = WDT_USER_TOP_(i)	0x0

WDT_CUR_CNT: (Offset 08h)

Bit	Symbol	R/W	Description	Default
31:0	CURRENT_COUNT	RO	This register, when read, is the current value of the internal counter. This value is read coherently when ever it is read, which is relevant when the APB_DATA_WIDTH is less than the counterwidth.	0xFFFF

WDT_RESTART: (Offset 0Ch)

Bit	Symbol	R/W	Description	Default
31:8	Reserved	RO	Reserved	0x0
7:0	RESTART	WO	This register is used to restart the WDT counter. As a safety feature to prevent accidental restarts, the value 0x76 must be written. A restart also clears the WDT interrupt. Reading this register returns zero.	0x0

WDT_STATUS: (Offset 10h)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0x0
0	INTERRUPT_STATUS0	RO	This register shows the interrupt status of the WDT. 0: Interrupt is inactive 1: Interrupt is active	0x0

WDT_ICR: (Offset 14h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:1	Reserved	RO	Reserved	0x0
0	INTERRUPT_CLEAR	RO	Clears the watchdog interrupt. This can be used to clear the interrupt without restarting the watchdog counter. 0: disable 1: clear wdt int	0x0

WDT1: (Base Addr 0x40001000)				
WDT1_CTRL: (Offset 00h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:5	Reserved	RO	Reserved	0x0
4:2	RST_LEN	RW	Reset pulse length. Writes have no effect when the configuration parameter WDT_HC_RPL is 1, making the register bits read-only. This is used to select the number of pclk cycles for which the system reset stays asserted. The range of values available is 2 to 256 pclk cycles. 0b000: 2 pclk cycles 0b001: 4 pclk cycles 0b010: 8 pclk cycles 0b011: 16 pclk cycles 0b100: 32 pclk cycles 0b101: 64 pclk cycles 0b110: 128 pclk cycles 0b111: 256 pclk cycles	0x0
1	MODE	RW	Response mode. Writes have no effect when the parameter WDT_HC_RMOD = 1,thus this register becomes read-only. Selects the output response generated to a timeout. 0: Generate reset. 1: special reset.	0x1
0	WDT_EN	RW	WDT enable. Writable when the configuration parameter WDT_ALWAYS_EN =0, otherwise, it is readable. This bit is used to enable and disable the DW_apb_wdt. When disabled,the counter does not decrement. Thus, no interrupts or system resets are generated. Once this bit has been enabled, it can be cleared only by a system reset. 0: WDT disabled. 1: WDT enabled.	0x0

WDT1_PERIOD: (Offset 04h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:4	Reserved	RO	Reserved	0x0
3:0	TOP	RW	Timeout period. Writes have no effect when the configuration parameter WDT_HC_TOP = 1, thus making this register read-only. This field is used to select the timeout period from which the watchdog counter restarts. A change of the timeout period takes effect only after the next counter restart (kick). The range of values is limited by the WDT_CNT_WIDTH. If TOP is programmed to select a range that is greater than the counter width, the timeout period is truncated to fit to the counter width. This affects only the non-user specified values as users are limited to these boundaries during configuration. The range of values available for a 32-bit watchdog counter are: Where i = TOP and t = timeout period For i = 0 to 15 if WDT_USE_FIX_TOP==1 t = 2(16 + i) else t = WDT_USER_TOP_(i)	0x0

WDT1_CUR_CNT: (Offset 08h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	CURRENT_COUNT	RO	This register, when read, is the current value of the internal counter. This value is read coherently when ever it is read, which is relevant when the APB_DATA_WIDTH is less than the counterwidth.	0xFFFF

WDT1_RESTART: (Offset 0Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:8	Reserved	RO	Reserved	0x0
7:0	RESTART	WO	This register is used to restart the WDT counter. As a safety feature to prevent accidental restarts, the value 0x76 must be written. A restart also clears the WDT interrupt. Reading this register returns zero.	0x0

WDT1_STATUS: (Offset 10h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:1	Reserved	RO	Reserved	0x0

0	INTERRUPT_STATUS	RO	This register shows the interrupt status of the WDT. 0: Interrupt is inactive 1: Interrupt is active	0x0

WDT1_ICR: (Offset 14h)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0x0
0	INTERRUPT_CLEAR	RO	Clears the watchdog interrupt. This can be used to clear the interrupt without restarting the watchdog counter. 0: disable 1: clear wdt int	0x0

UART: (Base Addr 0x40003000)

DIV_LL: (Offset 00h)

Bit	Symbol	R/W	Description	Default
31:8	Reserved	RO	Reserved	0x0
7:0	DIVISOR_LATCH_L	RW	FUNCTION1: this register can be accessed only when the DLAB bit (LINE_CTRL[7]) is set. Divisor Latch register that contains the baud rate divisor for the UART. The output baud rate is equal to the serial clock (pclk if one clock design, sclk if two clock design (Asynchronous Serial Clock Support is enabled) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) /(16 * divisor). Note that with the Divisor Latch Registers set to 0, the baud clock is disabled and no serial communications occur. FUNCTION2: This register can be accessed only when the DLAB bit (LINE_CTRL[7]) is cleared Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the LINE STATUS Register (LINE_STATUS) is set. FUNCTION3: Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the LINE STATUS Register (LINE_STATUS) is set.	0x0000

INTEN: (Offset 04h)

Bit	Symbol	R/W	Description	Default
31:8	Reserved	RO	Reserved	0x0

7	PTIME	RW	Programmable THRE(Trans mitter Holding Register Empty) Interrupt This is used to enable/disable the generation of THRE Interrupt. 0: disabled 1: enabled	0x0
6:4	Reserved	RO	Reserved	0x0
3	EDSSI	RW	Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0: disabled 1: enabled	0x0
2	ELSI	RW	Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver LINE STATUS Interrupt. This is the highest priority interrupt. 0: disabled 1: enabled	0x0
1	ETBEI	RW	Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0: disabled 1: enabled	0x0
0	ERBFI	RW	Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 0: disabled 1: enabled	0x0

FIFO_CTRL: (Offset 08h)

Bit	Symbol	R/W	Description	Default
31:8	Reserved	RO	Reserved	0x0
7:6	RCVR_TRIGGER	WO	RCVR Trigger. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. 0b00: 1 character in the FIFO 0b01: FIFO 1/4 full 0b10: FIFO 1/2full 0b11: FIFO 2 less than full	0x0
5:4	TX_EMPTY_TRIGGER	WO	This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. 0b00: FIFO empty 0b01: 2 characters in the FIFO 0b10: FIFO 1/4 full 0b11: FIFO 1/2 full	0x0

3	DMA_MODE	WO	DMA Mode. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (Additional DMA signals not included). 0: mode 0 1: mode 1	0x0
2	XMIT_FIFO_RESET	WO	XMIT FIFO Reset. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (Additional DMA signals included). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. 0: xmit fifo unreset 1: xmit fifo reset	0x0
1	RCVR_FIFO_RESET	WO	RCVR FIFO Reset. This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (Additional DMA signals included). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. 0: rcvr fifo un-reset 1: rcvr fifo reset	0x0
0	FIFO_ENABLE	WO	FIFO Enable. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset. 0: disable 1 : enable	0x0

LINE_CTRL: (Offset 0Ch)

Bit	Symbol	R/W	Description	Default
31:8	Reserved	RO	Reserved	0x0
7	DLAB	RW	Divisor Latch Access Bit. If Configures the peripheral not to be fully 16550-compatible, then writeable only when UART is not busy (UART_STATUS[0] is 0); otherwise always writable, always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH/LPDLL and LPDLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. 0: disable divisor latch register 1: enable divisor latch register	0x0

6	BREAK	RW	Break Control Bit.This is used to cause a break condition to be transmitted to the receiving device. If set to 1, the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by Modem Control Register[4], the sout line is forced low until the Break bit is cleared. If IrDA SIR Mode Support and active (Modem Control Register[6] set to 1) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low. 0: un-cause break condition 1: cause break condition	0x0
5	STICK_PARITY	RW	Stick Parity. If CONFIGURES THE PERIPHERAL NOT TO BE FULLY 16550-COMPATIBLE, then writeable only when UART is not busy (UART_STATUS[0] is 0); otherwise always writable, always readable. This bit is used to force parity value. When PEN, EPS, and Stick Parity are set to 1, the parity bit is transmitted and checked as logic 0. If PEN and Stick Parity are set to 1 and EPS is a logic 0, then parity bit is transmitted and checked as a logic 1. If this bit is set to 0, Stick Parity is disabled. 0: stick parity disable 1: stick parity enable	0x0
4	EPS	RW	Even Parity Select. If CONFIGURES THE PERIPHERAL NOT TO BE FULLY 16550-COMPATIBLE, then writeable only when UART is not busy (UART_STATUS[0] is 0); otherwise always writable, always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to 1). If set to 1, an even number of logic 1s is transmitted or checked. If set to 0, an odd number of logic 1s is transmitted or checked. 0: select odd parity 1: select even parity	0x0
3	PEN	RW	Parity Enable. If CONFIGURES THE PERIPHERAL NOT TO BE FULLY 16550-COMPATIBLE, then writeable only when UART is not busy (UART_STATUS[0] is 0); otherwise always writable, always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0: parity disabled 1: parity enabled	0x0

2	STOP	RW	Number of stop bits. If CONFIGURES THE PERIPHERAL NOT TO BE FULLY 16550-COMPATIBLE, then writeable only when UART is not busy (UART_STATUS[0] is 0); otherwise always writable, always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to 0, one stop bit is transmitted in the serial data. If set to 1 and the data bits are set to 5 (LINE_CTRL[1:0] set to 0) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0: 1 stop bit 1: 1.5 stop bits	0x0
1:0	DLS	RW	Data Length Select. If CONFIGURES THE PERIPHERAL NOT TO BE FULLY 16550-COMPATIBLE, then writeable only when UART is not busy (UART_STATUS[0] is 0); otherwise always writable, always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 0b00: 5 bits 0b01: 6bits 0b10: 7bits 0b11: 8 bits	0x0

LINE_STATUS: (Offset 14h)

Bit	Symbol	R/W	Description	Default
31:8	Reserved	RO	Reserved	0x00000000
7	RFE	RO	Receiver FIFO Error bit. This bit is only relevant when Receiver and Transmitter FIFO depth in bytes != NONE AND FIFOs are enabled (FIFO Control Register[0] set to 1). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. 0: no error in RX FIFO 1: error in RX FIFO This bit is cleared when the LINE_STATUS is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.	0x0
6	TEMT	RO	Transmitter Empty bit. If in FIFO mode (Receiver and Transmitter FIFO depth in bytes != NONE) and FIFOs enabled (FIFO Control Register[0] set to 1), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in non-FIFO mode or FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty. 0: unempty 1: empty	0x1

5	THRE	RO	Transmit Holding Register Empty bit. If THRE Interrupt mode not available or THRE mode is disabled (Interrupt Enable Register[7] set to 0) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the Transmit Holding Register or TX FIFO is empty. This bit is set whenever data is transferred from the Transmit Holding Register or TX FIFO to the transmitter shift register and no new data has been written to the Transmit Holding Register or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE Interrupt mode AND Receiver and Transmitter FIFO depth in bytes != NONE and both modes are active (Interrupt Enable Register[7] set to 1 and FIFO Control Register[0] set to 1 respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FIFO Control Register[5:4] threshold setting. 0: full 1: empty	0x1
4	BI	RO	Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (IrDA SIR Mode Not Support), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode (IrDA SIR Mode Support), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all 0s, to be received by the UART. In FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LINE_STATUS clears the BI bit. In non-FIFO mode, the BI indication occurs immediately and persists until the LINE_STATUS is read. NOTE: If a FIFO is full when a break condition is received, a FIFO overrun occurs. The break condition and all the information associated with it—parity and framing errors—is discarded; any information that a break character was received is lost. 0: no break 1: break	0x0

3	FE	RO	Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit; that is, data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LINE_STATUS[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LINE_STATUS[4]). This happens because the break character implicitly generates a framing error by holding the sin input to logic 0 for longer than the duration of a character. 0: no framing error 1: framing error Reading the LINE_STATUS clears the FE bit.	0x0
2	PE	RO	Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LINE_CTRL[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LINE_STATUS[2]) can be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LINE_STATUS[4]). In this situation, the Parity Error bit is set if parity generation and detection is enabled (LINE_CTRL[3]=1) and the parity is set to odd (LINE_CTRL[4]=0). 0: no parity error 1: parity error Reading the LINE_STATUS clears the PE bit.	0x0
1	OE	RO	Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RECEIVE BUFFER REGISTER. When this happens, the data in the RECEIVE BUFFER REGISTER is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0: no overrun error 1: overrun error Reading the LINE_STATUS clears the OE bit.	0x0

0	DR	RO	Data Ready bit. This is used to indicate that the receiver contains at least one character in the RECEIVE BUFFER REGISTER or the receiver FIFO. 0: no data ready 1: data ready This bit is cleared when the RECEIVE BUFFER REGISTER is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.	0x0

FIFO_ACC: (Offset 70h)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0x0
0	FIFO_ACCESS	RW	Writes have no effect when FIFO_ACCESS = No, always readable. This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RECEIVE BUFFER REGISTER to be written by the master and the Transmit Holding Register to be read by the master. 0: FIFO access mode disabled 1: FIFO access mode enabled Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty	0x0

TXFIFO_RD: (Offset 74h)

Bit	Symbol	R/W	Description	Default
31:8	Reserved	RO	Reserved	0x0
7:0	TRANS_FIFO_READ	RO	Transmit FIFO Read. These bits are only valid when FIFO access mode is enabled (FIFO Access Register[0] is set to 1). When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO. When FIFOs are not implemented or not enabled, reading this register gives the data in the Transmit Holding Register.	0x0

RXFIFO_WR: (Offset 78h)

Bit	Symbol	R/W	Description	Default
31:10	Reserved	RO	Reserved	0x0
9	RFFE	WO	Receive FIFO Framing Error. These bits are only valid when FIFO access mode is enabled (FIFO Access Register[0] is set to 1). When FIFOs are implemented and enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write framing error detection information to the Receive Buffer Register. 0: framing un-error 1: framing error	0x0

8	RFPE	WO	Receive FIFO Parity Error. These bits are only valid when FIFO access mode is enabled (FIFO Access Register[0] is set to 1). When FIFOs are implemented and enabled, this bit is used to write parity error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write parity error detection information to the Receive Buffer Register. 0: parity un-error 1: parity error	0x0
7:0	RFWD	WO	Receive FIFO Write Data. These bits are only valid when FIFO access mode is enabled (FIFO Access Register[0] is set to 1). When FIFOs are implemented and enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not implemented or not enabled, the data that is written to the RFWD is pushed into the Receive Buffer Register.	0x0

UART_STATUS: (Offset 7Ch)

Bit	Symbol	R/W	Description	Default
31:5	Reserved	RO	Reserved	0x0
4	RFF	RO	Receive FIFO Full. This bit is only valid whenFIFO Status registers included. This is used to indicate that the receive FIFO is completely full. 0: Receive FIFO not full 1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.	0x0
3	RFNE	RO	Receive FIFO Not Empty. This bit is only valid whenFIFO Status registers included. This is used to indicate that the receive FIFO contains one or more entries. 0: Receive FIFO is empty 1: Receive FIFO not empty This bit is cleared when the RX FIFO is empty.	0x0
2	TFE	RO	Transmit FIFO Empty. This bit is only valid whenFIFO Status registers included. This is used to indicate that the transmit FIFO is completely empty. 0: Transmit FIFO not empty 1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.	0x1
1	TFNF	RO	Transmit FIFO Not Full. This bit is only valid whenFIFO Status registers included. This is used to indicate that the transmit FIFO in not full. 0: Transmit FIFO is full 1: Transmit FIFO not full This bit is cleared when the TX FIFO is full.	0x1

0	BUSY	RO	UART Busy. This bit is valid only when CONFIGURES THE PERIPHERAL NOT TO BE FULLY 16550-COMPATIBLE and indicates that a serial transfer is in progress; when cleared, indicates that the uart is idle or inactive. 0: idle 1: busy This bit will be set to 1 (busy) under any of the following conditions: 1. Transmission in progress on serial interface 2. Transmit data present in Transmit Holding Register, when FIFO access mode is not being used (FIFO Access Register = 0) and the baud divisor is non-zero ({DLH,DLL} does not equal 0) when the divisor latch access bit is 0 (LINE_CTRL.DLAB = 0) 3. Reception in progress on the interface 4. Receive data present in RECEIVE BUFFER REGISTER, when FIFO access mode is not being used (FIFO Access Register = 0) NOTE: It is possible for the UART Busy bit to be cleared even though a new character may have been sent from another device. That is, if the UART has no data in Transmit Holding Register and RECEIVE BUFFER REGISTER and there is no transmission in progress and a start bit of a new character has just reached the uart. This is due to the fact that a valid start is not seen until the middle of the bit period and this duration is dependent on the baud divisor that has been programmed. If a second system clock has been implemented (Asynchronous Serial Clock Support is enabledd), the assertion of this bit is also delayed by several cycles of the slower clock.	0x0

TXFIFO_LEV: (Offset 80h)

Bit	Symbol	R/W	Description	Default
31:4	Reserved	RO	Reserved	0x0
3:0	TRANS_FIFO_LEVEL	RO	Transmit FIFO Level. This is indicates the number of data entries in the transmit FIFO.	0x0

RXFIFO_LEV: (Offset 84h)

Bit	Symbol	R/W	Description	Default
31:4	Reserved	RO	Reserved	0x0
3:0	RECEIVE_FIFO_LEVEL	RO	Receive FIFO Level. This is indicates the number of data entries in the receive FIFO.	0x0

TIMER0: (Base Addr 0x40004000)

TIM0_LOADCNT: (Offset 00h)

Bit	Symbol	R/W	Description	Default
31:0	LOAD_COUNT0	RW	Value to be loaded into TimerN. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.	0x0

TIM0_CURVAL: (Offset 04h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	CURRENT_VALUE0	RO	Current Value of Timer. This register is supported only when timer_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value	0x0

TIM0_CTRL: (Offset 08h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:3	Reserved	RO	Reserved	0x0
2	TMR_INT_MASK0	RW	Timer interrupt mask for Timer 0: not masked 1: masked	0x0
1	TMR_MODE0	RW	Timer mode for Timer 0: free-running mode 1: user-defined count mode	0x0
0	TMR_ENABLE0	RW	Timer enable bit for Timer 0: disable 1: enable	0x0

TIM0_ICR: (Offset 0Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:1	Reserved	RO	Reserved	0x0
0	TMR_END_OF_INT0	RO	Reading from this register returns all zeroes (0) and clears the interrupt from Timer.	0x0

TIM0_STATUS: (Offset 10h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:1	Reserved	RO	Reserved	0x0
0	TMR_INT_STAT0	RO	Contains the interrupt status of all timers in the component. If a bit of this register is 0, then the corresponding timer interrupt is not active –and the corresponding interrupt could be on either the timer_intr bus or the timer_intr_n bus, depending on the interrupt polarity you have chosen. Similarly, if a bit of this register is 1, then the corresponding interrupt bit has been set in the relevant interrupt bus. In both cases, the status reported is the status after the interrupt mask has been applied. Reading from this register does not clear any active interrupts: 0: not active 1: active after	0x0

TIMER1: (Base Addr 0x40005000)				
TIM1_LOADCNT: (Offset 00h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	LOAD_COUNT1	RW	Value to be loaded into TimerN. This is the value from which	0x0

			counting commences. Any value written to this register is loaded into the associated timer.	

TIM1_CURVAL: (Offset 04h)

Bit	Symbol	R/W	Description	Default
31:0	CURRENT_VALUE1	RO	Current Value of Timer. This register is supported only when timer_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value	0x0

TIM1_CTRL: (Offset 08h)

Bit	Symbol	R/W	Description	Default
31:3	Reserved	RO	Reserved	0x0
2	TMR_INT_MASK1	RW	Timer interrupt mask for Timer 0: not masked 1: masked	0x0
1	TMR_MODE1	RW	Timer mode for Timer 0: free-running mode 1: user-defined count mode	0x0
0	TMR_ENABLE1	RW	Timer enable bit for Timer 0: disable 1: enable	0x0

TIM1_ICR: (Offset 0Ch)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0x0
0	TMR_END_OF_INT1	RO	Reading from this register returns all zeroes (0) and clears the interrupt from Timer.	0x0

TIM1_STATUS: (Offset 10h)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0x0
0	TMR_INT_STAT1	RO	Contains the interrupt status of all timers in the component. If a bit of this register is 0, then the corresponding timer interrupt is not active –and the corresponding interrupt could be on either the timer_intr bus or the timer_intr_n bus, depending on the interrupt polarity you have chosen. Similarly, if a bit of this register is 1, then the corresponding interrupt bit has been set in the relevant interrupt bus. In both cases, the status reported is the status after the interrupt mask has been applied. Reading from this register does not clear any active interrupts: 0: not active 1: active after	0x0

I²C: (Base Addr 0x40006000)				
I²C_CONTROL: (Offset 00h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:7	Reserved	RO	Reserved	0x0
6	SLV_DISABLE	RW	This bit controls whether I²C has its slave disabled, which means once the presetn signal is applied, then this bit takes on the value of the configuration parameter 0. You have the choI2Ce of having the slave enabled or disabled after reset is applied, which means software does not have to configure the slave. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), i2c functions only as a master and does not perform any action that requires a slave. 0: slave is enabled 1: slave is disabled	0x1
5	RESTART_EN	RW	Determines whether RESTART conditions may be sent when acting as a master. Some older slaves do not support handling RESTART conditions; however, RESTART conditions are used in severaL i2c operations. 0: disable 1: enable	0x1
4	10BITADDR_MS	RW	If the 0 configuration parameter is set to “No” (0), this bit is 1 and controls whether the i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If0 is set to “Yes” (1), the function of this bit is handled by bit 12 of I²C_TAR_ADDR register, and becomes a read-only . 0: 7-bit addressing 1: 10-bit addressing Dependencies: If0 = 1, then this bit is read-only. If0 = 0, then this bit can be read or write.	0x1
3	10BITADDR_SLV	RW	When acting as a slave, this bit controls whether the i2c responds to 7- or 10-bit addresses. 0: 7-bit addressing 1: 10-bit addressing	0x1

2:1	SPEED	RW	These bits control at which speed the i2c operates; its setting is relevant only if one is operating the i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to 2'b11; otherwise, hardware updates this register with the value of 2'b11. 0b01: standard mode 0b10: fast mode 0b11: high speed mode	0x3
0	MASTER_MOD	RW	This bit controls whether the i2c master is enabled. 0: master disabled 1: master enabled	0x1

I²C_TAR_ADDR: (Offset 04h)

Bit	Symbol	R/W	Description	Default
31:13	Reserved	RW	Reserved	0x0
12	10BITADR_MAST	RW	This bit controls whether the i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. 0: 7-bit addressing 1: 10-bit addressing	0x1
11	SPECIAL	RW	This bit Indicates whether software performs a General Call or START BYTE command. 0: general call 1: start byte	0x0
10	GC_OR_START	RW	If bit 11 (SPECIAL) is set to 1, then this bit Indicates whether a General Call or START byte command is to be performed by the i2c. 0: General Call Address 1: start byte	0x0
9:0	TAR_ADDR	RW	This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.	0x55

I²C_SLV_ADDR: (Offset 08h)

Bit	Symbol	R/W	Description	Default
31:10	Reserved	RO	Reserved	0x0

9:0	SLV_ADDR	RW	The I²C_SLV_ADDR holds the slave address when the I²C is operating as a slave. For 7-bit addressing, only I²C_SLV_ADDR[6:0] is used. This register can be written only when the I²C interface is disabled, which corresponds to I²C_ENABLE[0] being set to 0. Writes at other times have no effect.	0x5C

I²C_DA_BUF_CMD: (Offset 10h)

Bit	Symbol	R/W	Description	Default
31:11	Reserved	RO	Reserved	0x0
10	RESTART	WO	This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if enable of i2c master empty fifo hold is configured to 1. 1 – If enable of i2c restart is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if enable of i2c restart is 0, a STOP followed by a START is issued instead. 0 – If enable of i2c restart is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if enable of i2c restart is 0, a STOP followed by a START is issued instead. 0: restart is un-issued 1: restart is issued	0x0
9	STOP	WO	This bit controls whether a STOP is issued after the byte is sent or received. This bit is available only if enable of i2c master empty fifo hold is configured to 1. 1 – STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. 0 – STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO. 0: stop is un-issued 1: stop is issued	0x0

8	CMD	WO	This bit controls whether a read or a write is performed. This bit does not control the direction when the i2c acts as a slave. It controls only the direction when it acts as a master. 0: Write 1: Read	0x0
7:0	DAT	RW	This register contains the data to be transmitted or received on the I²C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the i2c. However, when you read this register, these bits return the value of data received on the i2c interface.	0x0

I²C_ST_SCLH_CNT: (Offset 14h)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0x0
15:0	ST_SCL_HCNT	RW	This register must be set before any I²C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. This register can be written only when the I²C interface is disabled which corresponds to I²C_ENABLE[0] being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with width of APB data = 8, the order of programming is important to ensure the correct operation of the i2c. The lower byte must be programmed first. Then the upper byte is programmed. When the configuration parameter i2c high count is set to 1, this register is read only.	0x190

I²C_ST_SCLL_CNT: (Offset 18h)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0x0

15:0	ST_SCL_LCNT	RW	This register must be set before any I²C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. This register can be written only when the I²C interface is disabled which corresponds to I²C_ENABLE[0] being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted, results in 8 being set. For designs with width of APB data = 8, the order of programming is important to ensure the correct operation of i2c. The lower byte must be programmed first, and then the upper byte is programmed. When the configuration parameter i2c high count is set to 1, this register is read only.	0x1D6

I²C_FS_SCLH_CNT: (Offset 1Ch)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0x0
15:0	FS_SCL_HCNT	RW	This register must be set before any I²C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read-only returning 0s if 2'b11 = standard. This register can be written only when the I²C interface is disabled, which corresponds to I²C_ENABLE[0] being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with width of APB data == 8 the order of programming is important to ensure the correct operation of the i2c. The lower byte must be programmed first. Then the upper byte is programmed. When the configuration parameter i2c high count is set to 1, this register is read only.	0x03C

I²C_FS_SCLL_CNT: (Offset 20h)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0x0

15:0	FS_SCL_LCNT	RW	This register must be set before any I²C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read-only returning 0s if 2'b11 = standard. This register can be written only when the I²C interface is disabled, which corresponds to I²C_ENABLE[0] being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with width of APB data = 8 the order of programming is important to ensure the correct operation of the i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8. When the configuration parameter i2c high count is set to 1, this register is read only.	0x082

I²C_INT_STATUS: (Offset 2Ch)

Bit	Symbol	R/W	Description	Default
31:12	Reserved	RO	Reserved	0x0
11	R_GEN_ALL	RO	Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling i2c or when the CPU reads bit 0 of the I²C_CLR_GEN_CAL_INT register. i2c stores the received data in the Rx buffer. 0: address is unreceived 1: address is received	0x0
10	R_START_DET	RO	Indicates whether a START or RESTART condition has occurred on the I²C interface regardless of whether i2c is operating in slave or master mode. 0: start condition un-occurred 1: start condition occurred	0x0
9	R_STOP_DET	RO	Indicates whether a STOP condition has occurred on the I²C interface regardless of whether i2c is operating in slave or master mode. 0: stop condition un-occurred 1: stop condition occurred	0x0

8	R_ACTIVITY	RO	This bit captures i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the i2c Reading the I²C_CLR_ACTIVITY_INT register Reading the I²C_CLR_INT register System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the i2c module is idle, this bit remains set until cleared, indI2Cating that there was activity on the bus. 0: un-activity 1: activity	0x0
7	R_RX_DONE	RO	When the i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indI2Cating that the transmission is done. 0: not slave transmitter 1: slave transmitter	0x0
6	R_TX_ABRT	RO	This bit Indicates if i2c, as an I²C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I²C master or an I²C slave, and is referred to as a “transmit abort”. When this bit is set to 1, the I²C_TX_ABRT_STATUS register Indicates the reason why the transmit abort takes places. 0: not i2c transmitter 1: i2c transmitter	0x0
5	R_RD_REQ	RO	This bit is set to 1 when i2c is acting as a slave and another I²C master is attempting to read data from i2c. The i2c holds the I²C bus in a wait state (SCL=0) until this interrupt is servI2Ced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the I²C_DA_BUF_CMDregister. This bit is set to 0 just after the processor reads the I²C_CLR_RD_REQ_INTregister. 0: no request 1: request data	0x0

4	R_TX_EMPTY	RO	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the I²C_TX_TL register. It is automatI2Cally cleared by hardware when the buffer level goes above the threshold. When I²C_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer activity, then with I²C_en=0, this bit is set to 0. 0: not below the threshold 1: below the threshold value	0x0
3	R_TX_OVER	RO	Set during transmit if the transmit buffer is filled to I²C_TX_BUFFER_DEPTH and the processor attempts to issue another I²C command by writing to the I²C_DA_BUF_CMDregister. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when I²C_en goes to 0, this interrupt is cleared. 0: state maching is idle 1: state maching is going	0x0
2	R_RX_FULL	RO	Set when the receive buffer reaches or goes above the RX_TL threshold in the I²C_RX_FIFO_LEVEL register. It is automatI2Cally cleared by hardware when buffer level goes below the threshold. If the module is disabled (I²C_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once I²C_ENABLE[0] is set to 0, regardless of the activity that continues 0: set I²C_ENABLE 0 1: I²C_ENABLE is 1	0x0
1	R_RX_OVER	RO	Set if the receive buffer is completely filled to I²C_RX_BUFFER_DEPTH and an additional byte is received from an external I²C devI2Ce. The i2c acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (I²C_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when I²C_en goes to 0, this interrupt is cleared. 0: receive no overflow 1: receive overflow	0x0

0	R_RX_UNDER	RO	Set if the processor attempts to read the receive buffer when it is empty by reading from the I²C_DA_BUF_CMDregister. If the module is disabled (I²C_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when I²C_en goes to 0, this interrupt is cleared. 0: I²C_ENABLE is 0 1: keep level	0x0

I²C_INT_FLAG: (Offset 30h)

Bit	Symbol	R/W	Description	Default
31:12	Reserved	RO	Reserved	0x0
11	M_GEN_ALL	RW	These bits mask their corresponding interrupt status bits in the I²C_INT_STATUS register. 0: diasble 1: enable	0x0
10	M_START_DET	RW	These bits mask their corresponding interrupt status bits in the I²C_INT_STATUS register. 0: diasble 1: enable	0x0
9	M_STOP_DET	RW	These bits mask their corresponding interrupt status bits in the I²C_INT_STATUS register. 0: diasble 1: enable	0x0
8	M_ACTIVITY	RW	These bits mask their corresponding interrupt status bits in the I²C_INT_STATUS register. 0: diasble 1: enable	0x0
7	M_RX_DONE	RW	These bits mask their corresponding interrupt status bits in the I²C_INT_STATUS register. 0: diasble 1: enable	0x0
6	M_TX_ABRT	RW	These bits mask their corresponding interrupt status bits in the I²C_INT_STATUS register. 0: diasble 1: enable	0x0

5	M_RD_REQ	RW	These bits mask their corresponding interrupt status bits in the I²C_INT_STATUS register. 0: diasble 1: enable	0x0
4	M_TX_EMPTY	RW	These bits mask their corresponding interrupt status bits in the I²C_INT_STATUS register. 0: diasble 1: enable	0x0
3	M_TX_OVER	RW	These bits mask their corresponding interrupt status bits in the I²C_INT_STATUS register. 0: diasble 1: enable	0x0
2	M_RX_FULL	RW	These bits mask their corresponding interrupt status bits in the I²C_INT_STATUS register. 0: diasble 1: enable	0x0
1	M_RX_OVER	RW	These bits mask their corresponding interrupt status bits in the I²C_INT_STATUS register. 0: diasble 1: enable	0x0
0	M_RX_UNDER	RW	These bits mask their corresponding interrupt status bits in the I²C_INT_STATUS register. 0: diasble 1: enable	0x0

I²C_RAW_INT_STATUS: (Offset 34h)

Bit	Symbol	R/W	Description	Default
31:12	Reserved	RO	Reserved	0x0
11	GEN_ALL	RO	Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling i2c or when the CPU reads bit 0 of the I²C_CLR_GEN_CAL_INT register. i2c stores the received data in the Rx buffer. 0: diasble 1: enable	0x0

10	START_DET	RO	Indicates whether a START or RESTART condition has occurred on the I²C interface regardless of whether i2c is operating in slave or master mode. 0: diasble 1: enable	0x0
9	STOP_DET	RO	Indicates whether a STOP condition has occurred on the I²C interface regardless of whether i2c is operating in slave or master mode. 0: diasble 1: enable	0x0
8	S_ACTIVITY	RO	This bit captures i2c activity and stays set until it is cleared. There are four ways to clear it: 1.Disabling the i2c 2.Reading the I²C_CLR_ACTIVITY_INT register 3.Reading the I²C_CLR_INT register 4.System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the i2c module is idle, this bit remains set until cleared,indI2Cating that there was activity on the bus. 0: diasble 1: enable	0x0
7	RX_DONE	RO	When the i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indI2Cating that the transmission is done. 0: diasble 1: enable	0x0
6	TX_ABRT	RO	This bit Indicates if i2c, as an I²C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I²C master or an I²C slave, and is referred to as a “transmit abort”. When this bit is set to 1, the I²C_TX_ABRT_STATUS register Indicates the reason why the transmit abort takes places. 0: diasble 1: enable	0x0

5	RD_REQ	RO	This bit is set to 1 when i2c is acting as a slave and another I²C master is attempting to read data from i2c. The i2c holds the I²C bus in a wait state (SCL=0) until this interrupt is servI2Ced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the I²C_DA_BUF_CMDregister. This bit is set to 0 just after the processor reads the I²C_CLR_RD_REQ_INTregister. 0: diasble 1: enable	0x0
4	TX_EMPTY	RO	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the I²C_TX_TL register. It is automatI2Cally cleared by hardware when the buffer level goes above the threshold. When I²C_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer activity, then with I²C_en=0, this bit is set to 0. 0: diasble 1: enable	0x0
3	TX_OVER	RO	Set during transmit if the transmit buffer is filled to I²C_TX_BUFFER_DEPTH and the processor attempts to issue another I²C command by writing to the I²C_DA_BUF_CMDregister. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when I²C_en goes to 0, this interrupt is cleared. 0: diasble 1: enable	0x0
2	RX_FULL	RO	Set when the receive buffer reaches or goes above the RX_TL threshold in the I²C_RX_FIFO_LEVEL register. It is automatI2Cally cleared by hardware when buffer level goes below the threshold. If the module is disabled (I²C_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once I²C_ENABLE[0] is set to 0, regardless of the activity that continues. 0: diasble 1: enable	0x0

1	RX_OVER	RO	Set if the receive buffer is completely filled to I²C_RX_BUFFER_DEPTH and an additional byte is received from an external I²C devI2Ce. The i2c acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (I²C_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when I²C_en goes to 0, this interrupt is cleared. 0: diasble 1: enable	0x0
0	RX_UNDER	RO	Set if the processor attempts to read the receive buffer when it is empty by reading from the I²C_DA_BUF_CMDregister. If the module is disabled (I²C_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when I²C_en goes to 0, this interrupt is cleared. 0: diasble 1: enable	0x0

I²C_RX_FIFO_TH: (Offset 38h)

Bit	Symbol	R/W	Description	Default
15:8	Reserved	RO	Reserved	0x0
7:0	RX_TL	RW	Receive FIFO Threshold Level Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in I²C_RAW_INT_STATUS register). The valid range is 0-255, with the additional restrI2Ction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 1 entry, and a value of 255 sets the threshold for 256 entries.	0x0

I²C_TX_FIFO_TH: (Offset 3Ch)

Bit	Symbol	R/W	Description	Default
15:8	Reserved	RO	Reserved	0x0

7:0	TX_TL	RW	Transmit FIFO Threshold Level Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in I²C_RAW_INT_STATUS register). The valid range is 0-255, with the additional restrI2Ction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries.	0x0

I²C_CLR_INT: (Offset 40h)

Bit	Symbol	R/W	Description	Default
15:1	Reserved	RO	Reserved	0x0
0	CLR_INTR	RO	Read this register to clear the combined interrupt, all individual interrupts, and the I²C_TX_ABRT_STATUS register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the I²C_TX_ABRT_STATUS register for an exception to clearing I²C_TX_ABRT_STATUS.	0x0

I²C_CLR_RX_UD_INT: (Offset 44h)

Bit	Symbol	R/W	Description	Default
15:1	Reserved	RO	Reserved	0x0
0	CLR_RX_UNDER	RO	Read this register to clear the RX_UNDER interrupt (bit 0) of the I²C_RAW_INT_STATUS register.	0x0

I²C_CLR_RX_OV_INT: (Offset 48h)

Bit	Symbol	R/W	Description	Default
15:1	Reserved	RO	Reserved	0x0
0	CLR_RX_OVER	RO	Read this register to clear the RX_OVER interrupt (bit 1) of the I²C_RAW_INT_STATUS register.	0x0

I²C_CLR_TX_OV_INT: (Offset 4Ch)

Bit	Symbol	R/W	Description	Default
15:1	Reserved	RO	Reserved	0x0
0	CLR_TX_OVER	RO	Read this register to clear the RX_OVER interrupt (bit 1) of the I²C_RAW_INT_STATUS register.	0x0

I²C_CLR_RD_REQ_INT: (Offset 50h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:1	Reserved	RO	Reserved	0x0
0	CLR_RD_REQ	RO	Read this register to clear the RD_REQ interrupt (bit 5) of the I²C_RAW_INT_STATUS register.	0x0

I²C_CLR_TX_ABRT_INT: (Offset 54h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:1	Reserved	RO	Reserved	0x0
0	CLR_TX_ABRT	RO	Read this register to clear the TX_ABRT interrupt (bit 6) of the I²C_RAW_INT_STATUS register, and the I²C_TX_ABRT_STATUS register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the I²C_TX_ABRT_STATUS register for an exception to clearing I²C_TX_ABRT_STATUS.	0x0

I²C_CLR_RX_DONE_INT: (Offset 58h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:1	Reserved	RO	Reserved	0x0
0	CLR_RX_DONE	RO	Read this register to clear the RX_DONE interrupt (bit 7) of the I²C_RAW_INT_STATUS register	0x0

I²C_CLR_ACTIVITY_INT: (Offset 5Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:1	Reserved	RO	Reserved	0x0
0	CLR_ACTIVITY	RO	Reading this register clears the ACTIVITY interrupt if the I²C is not active anymore. If the I²C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatI2Cally cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the I²C_RAW_INT_STATUS register.	0x0

I²C_CLR_STOP_DET_INT: (Offset 60h)

Bit	Symbol	R/W	Description	Default
15:1	Reserved	RO	Reserved	0x0
0	CLR_STOP_DET	RO	Read this register to clear the STOP_DET interrupt (bit 9) of the I²C_RAW_INT_STATUS register.	0x0

I²C_CLR_STAR_DET_INT: (Offset 64h)

Bit	Symbol	R/W	Description	Default
15:1	Reserved	RO	Reserved	0x0
0	CLR_START_DET	RO	Read this register to clear the START_DET interrupt (bit 10) of the I²C_RAW_INT_STATUS register.	0x0

I²C_CLR_GEN_CAL_INT: (Offset 68h)

Bit	Symbol	R/W	Description	Default
15:1	Reserved	RO	Reserved	0x0
0	CLR_GEN_CALL	RO	Read this register to clear the GEN_CALL interrupt (bit 11) of I²C_RAW_INT_STATUS register.	0x0

I²C_ENABLE: (Offset 6Ch)

Bit	Symbol	R/W	Description	Default
15:2	Reserved	RO	Reserved	0x0
1	ABORT	RW	When set, the controller initiates the transfer abort. The software can abort the I²C transfer in master mode by setting this bit. The software can set this bit only when ENABLE is already set; otherwise, the controller ignores any write to ABORT bit. The software cannot clear the ABORT bit once set. In response to an ABORT, the controller issues a STOP and flushes the Tx FIFO after completing the current transfer, then sets the TX_ABORT interrupt after the abort operation. The ABORT bit is cleared automatI2Cally after the abort operation. 0: ABORT done 1: ABORT operation in progress	0x0
0	ENABLE	RW	Controls whether the i2c is enabled. 0: disable i2c 1: enable i2c.	0x0

I²C_STATUS: (Offset 70h)

Bit	Symbol	R/W	Description	Default
31:7	Reserved	RO	Reserved	0x0
6	SLV_ACTIVITY	RO	Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set. 0: Slave FSM is IDLE 1: Slave FSM is is Active.	0x0
5	MST_ACTIVITY	RO	Master FSM Activity Status. When the Master Finite State Machine (FSM) is not inthe IDLE state, this bit is set. 0: Master FSM is IDLE 1: Master FSM is Active	0x0
4	RFF	RO	Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. 0: Receive FIFO not full 1: Receive FIFO full	0x0
3	RFNE	RO	Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. 0: Receive FIFO empty 1: Receive FIFO not empty	0x0
2	TFE	RO	Transmit FIFO Completely Empty. When the transmit FIFO is completely empty,this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. 0: Transmit FIFO not empty 1: Transmit FIFO is empty	0x1
1	TFNF	RO	Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. 0: Transmit FIFO is full 1: Transmit FIFO not full	0x1
0	ACTIVITY	RO	I^2C Activity Status. 0: unactivity 1: activity	0x0

I^2C_TX_FIFO_LEVEL: (Offset 74h)

Bit	Symbol	R/W	Description	Default
31:4	Reserved	RO	Reserved	0x0
3:0	TXFLR	RO	Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.	0x0

I²C_RX_FIFO_LEVEL: (Offset 78h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:4	Reserved	RO	Reserved	0x0
3:0	RXFLR	RO	Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.	0x0

I²C_SDA_HOLD_TIME: (Offset 7Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:16	Reserved	RO	Reserved	0x0
15:0	SDA_HOLD	RW	Sets the required SDA hold time in units of I²C_clk period.	0x1

I²C_TX_ABRT_STATUS: (Offset 80h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:24	TX_FLUSH_CNT	RW	This field preserves the TXFLR value prior to the last TX_ABRT event. It is cleared whenever I²C is disabled.	0x0
23:17	Reserved	RO	Reserved	0x0
16	ABRT_USER_ABRT	RO	This is a master-mode-only bit. Master has detected the transfer abort (I²C_ENABLE[1]). 0: master mode undetected 1: master mode detected	0x0
15	ABRT_SLVRD_INTX	RO	When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of I²C_DA_BUF_CMDregister 0: unrespond slave mode request 1: respond slave mode request	0x0
14	ABRT_SLV_ARBLOST	RO	Slave lost the bus while transmitting data to a remote master. I²C_TX_ABRT_STATUS[12] is set at the same time. 0: slave un-lost bus 1: slave lost bus	0x0
13	ABRT_SLVFLUSH_TX	RO	Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO. 0: do not refresh data 1: refresh data	0x0
12	ARB_LOST	RO	Master has lost arbitration, or if I²C_TX_ABRT_STATUS[14] is also set, then the slave transmitter has lost arbitration. 0: master un-lost arbitration	0x0

			1: master lost arbitration	
11	ABRT_MASTER_DIS	RO	User tries to initiate a Master operation with the Master mode disabled. 0: un-initiate master operation 1: initiate master operation	0x0
10	ABRT_10BIT_STRT	RO	The restart is disabled(enable of i2c restart bit (I²C_CONTROL[5]) = 0) and the master sends a read command in 10-bit addressing mode 0: restart is enable 1: 10 bit address	0x0
9	ABRT_SBYTE_STRT	RO	To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (I²C_CONTROL[5]=1), the SPECIAL bit must be cleared (I²C_TAR_ADDR[11]), or the GC_OR_START bit must be cleared (I²C_TAR_ADDR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets re-asserted. 0: restart is enable 1: start byte	0x0
8	ABRT_HS_STRT	RO	The restart is disabled(enable of i2c restart bit (I²C_CONTROL[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode. 0: restart is enable 1: high speed mode	0x0
7	ABRT_SBYTE_ACK	RO	Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). 0: unsent start byte 1: sent start byte	0x0
6	ABRT_HS_ACKDET	RO	Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). 0: un hign speed mode 1: high speed mode	0x0
5	ABRT_GCALL_READ	RO	i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (I²C_DATA_CMD[9] is set to 1). 0: unsent general call 1: sent general call	0x0

4	ABRT_GCALL_ACK	RO	i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call. 0: slave ack 1: no slave ack	0x0
3	ABRT_TXDATA_ACK	RO	This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s). 0: no master ack 1: master ack	0x0
2	ART_10A2_NACK	RO	Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave. 0: slv-ack 1: un-10bit address ack	0x0
1	ART_10A1_NACK	RO	Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave. 0: ack 1: un-10bit address ack	0x0
0	ABRT_7ADDR_ACK	RO	Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. 0: ack 1: un-7bit address slv-ack	0x0

I²C_SDA_SETUP_TIME: (Offset 94h)

Bit	Symbol	R/W	Description	Default
31:8	Reserved	RO	Reserved	0x0
7:0	SDA_SETUP	RW	SDA Setup. It is recommended that if the required delay is 1000ns, then for an I²C_clk frequency of 10 MHz, I²C_SDA_SETUP should be programmed to a value of 11. I²C_SDA_SETUP must be programmed with a minimum value of 2.	0x64

I²C_ACK_GEN_CALL: (Offset 98h)

Bit	Symbol	R/W	Description	Default
31:1	Reserved	RO	Reserved	0x0
0	ACK_GEN_CALL	RW	ACK General Call. When set to 1, i2c responds with a ACK (by asserting I²C_data_oe) when it receives a General Call. When set to 0, the i2c does not generate General Call interrupts. 0: un-generate call interrupt 1: ack general call	0x1

I²C_ENABLE_STATUS: (Offset 9Ch)

Bit	Symbol	R/W	Description	Default
31:3	Reserved	RO	Reserved	0x0
2	SLV_RX_DA_LOST	RO	Slave Received Data Lost. This bit Indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I²C transfer due to setting I²C_ENABLE[0] from 1 to 0. When read as 1, i2c is deemed to have been actively engaged in an aborted I²C transfer (with matching address) and the data phase of the I²C transfer has been entered, even though a data byte has been responded with a NACK. NOTE: If the remote I²C master terminates the transfer with a STOP condition before the i2c has a chance to NACK a transfer, and I²C_ENABLE[0] has been set to 0, then this bit is also set to 1. When read as 0, i2c is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer. 0: data is received 1: data lost	0x0
1	SLV_DIS_BUSY	RO	Slave Disabled While Busy (Transmit, Receive). This bit Indicates if a potential or active Slave operation has been aborted due to setting bit 0 of the I²C_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to bit 0 of I²C_ENABLE while: (a) i2c is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, i2c is deemed to have forced a NACK during any part of an I²C transfer, irrespective of whether the I²C address matches the slave address set in i2c (I²C_SLV_ADDR register) OR if the transfer is completed before bit 0 of I²C_ENABLE is set to 0, but has not taken effect. 0: slave activity 1: slave disable	0x0
0	I²C_EN	RO	I²C_en Status. This bit always reflects the value driven on the output port I²C_en. When read as 1, i2c is deemed to be in an enabled state. When read as 0, i2c is deemed completely inactive. 0: disable	0x0

			1: enable	

I²C_FS_SPK_LIMIT: (Offset A0h)

Bit	Symbol	R/W	Description	Default
31:8	Reserved	RO	Reserved	0x0
7:0	FSPKLEN	RW	This register must be set before any I²C bus transaction can take place to ensure stable operation. This register sets the duration, measured in I²C_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logI2C;. This register can be written only when the I²C interface is disabled, which corresponds to I²C_ENABLE[0] being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted, results in 1 being set.	0x5

I²C_HS_SPK_LIMIT: (Offset A4h)

Bit	Symbol	R/W	Description	Default
31:8	Reserved	RO	Reserved	0x0
7:0	HSPKLEN	RW	This register must be set before any I²C bus transaction can take place to ensure stable operation. This register sets the duration, measured in I²C_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logI2C;. This register can be written only when the I²C interface is disabled, which corresponds to I²C_ENABLE[0] being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted, results in 1 being set.	0x1

AFE: (Base Addr 0x40008000)

ADCH0CR0: (Offset 00h)

Bit	Symbol	R/W	Description	Default
31:29	Reserved	RO	Reserved	0x0

28:24	SP_MUX_0	RW	Positive terminal of DC voltage channel.(configure channel0,16 channels in total,the channel offset address is 0x20) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
23:21	Reserved	RO	Reserved	0x0
20:16	SN_MUX_0	RW	negative terminal of DC voltage channel.(configure channel0,16 channels in total,the channel offset address is 0x20) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
15	RED_OS_0	RW	offset Residual cancellation enable signal (configure channel0, 16channels in total,the channel offset address is 0x20) 0: no elimination of residuals 1: elimination of residuals	0x0
14	DMOF_0	RW	differential input mode output format(configure channel0,16 channels in total,the channel offset address is 0x20) 0: original code of result 1: complement of result	0x0
13	PD_DOUBLE_VIN_0	RW	in ADC single-ended mode, turn off the double-ended input (configure channel0,16 channels in total,the channel offset address is 0x20) 0: double-ended input 1: single-ended input	0x1
12	EN_DIFF_0	RW	ADC input working mode (configure channel0,15 channels in total,the channel offset address is 0x20) 0: single-ended mode 1: differential mode	0x1
11:8	PD_SW_IN_0	RW	PA3-PA0 analog switch control (configure channel0,16 channels in total,the channel offset address is 0x20) 0: strobe vs 1: disable	0xF

7:4	PD_AINP_0	RW	CHx sensor positive input selection (configure channel0,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 positive 0b0001: sensor1 positive 0b0010: sensor2 positive 0b0011: sensor3 positive 0b0100: sensor4 positive 0b0101: sensor5 positive 0b0110: sensor6 positive 0b0111: sensor7 positive 0b1000: sensor8 positive 0b1001: sensor9 positive 0b1010: sensor10 positive 0b1011:sensor11 positive	0xF
3:0	PD_AINN_0	RW	CHx sensor negative input selection (configure channel0,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 negative 0b0001: sensor1 negative 0b0010: sensor2 negative 0b0011: sensor3 negative 0b0100: sensor4 negative 0b0101: sensor5 negative 0b0110: sensor6 negative 0b0111: sensor7 negative 0b1000: sensor8 negative 0b1001: sensor9 negative 0b1010: sensor10 negative 0b1011:sensor11 negative	0xF

ADCH0CR1: (Offset 04h)

Bit	Symbol	R/W	Description	Default
31	Reserved	RO	Reserved	0x0
30:28	PGA_IBIASE_0	RW	PGA module overall current selection(configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1μA 0b001: 1.25μA 0b010: 1.5μA 0b011: 1.75μA 0b100: 2μA 0b101: 2.25μA 0b110: 2.5μA 0b111: 2.75μA	0x4
27	Reserved	RO	Reserved	0x0

26:24	BW_FILTER_0	RW	PGA RC filter output frequency selection(configure channel0,16channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 125kHz 0b001: 250kHz 0b010: 167kHz 0b011: 500kHz 0b100: 143kHz 0b101: 333kHz 0b110: 200kHz 0b111: 1000kHz	0x3
23:22	VREF_SEL_0	RW	VRP voltage selection(configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b00: 2.4v 0b01: 2.8v 0b10: 3.0v 0b11: 3.1v	0x1
21	VREF_GEN_SEL_0	RW	ADC refrence voltage selection(configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: AVDD 1: VRP	0x1
20	VCM_ADJ_0	RW	PGA output common mode voltage selection(configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: 0.5*AVDD 1: 0.5*AVDD-0.1	0x0
19	Reserved	RO	Reserved	0x0
18:16	ADC_IBIAS_0	RW	ADC BIAS current control(configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 2μA 0b001: 2.5μA 0b010: 3μA 0b011: 3.5μA 0b100: 4μA 0b101: 4.5μA 0b110: 5μA 0b111: 5.5μA	0x4
15:13	Reserved	RO	Reserved	0x0
12	INV_AD_0	RW	SAR ADC output flip enable (configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: no flip 1: flip	0x0
11	EN_PGA_0	RW	PGA enable switch (configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: disable 1: enable	0x0

10	PD_PGA1_0	RW	First level of PGA enable switch (configure channel0,16channels in total,the channel offset address is 0x20 *channel +0x4) 1: disable 0: enable	0x0
9	PD_PGA2_0	RW	second level of PGA enable switch (configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 1: disable 0: enable	0x0
8	PD_FILTER_0	RW	turn off the PGA2 filter (configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 1: turn off 0: turn on	0x0
7	Reserved	RO	Reserved	0x0
6:4	GAIN_PGA1_0	RW	First level of PGA gain selection(configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256 0b110: 256 0b111: 256	0x2
3	Reserved	RO	Reserved	0x0
2:0	GAIN_PGA2_0	RW	second level of PGA gain selection(configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

DACH0CR: (Offset 08h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13	EN_DAC_CAL_0	RW	enable digital DAC calibration loop operation(configure channel0,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0

12	EN_DAC_0	RW	enable calibration offset DAC (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0
11	EN_DAC_VIN_0	RW	turn on DAC negative current input(configure channel0,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: turn off 1: turn on	0x1
10	DIR_DAC_0	RW	DAC direction select (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable current direction 1: enable current direction	0x0
9	DIR_MODE0_0	RW	DAC direction select (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offset 1: enable affect offset	0x0
8	DIR_MODE1_0	RW	DAC direction select (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offsef 1: enable affect offset	0x1
7:2	Reserved	RO	Reserved	0x0
1:0	VDAC_RANGE_0	RW	DAC calibration offset range (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0x8) 0b00: ±0.540*VS/3 0b01: ±0.540*VS/4 0b10: ±0.540*VS/5 0b11: ±0.540*VS/6	0x0

DACH0DR: (Offset 0Ch)

Bit	Symbol	R/W	Description	Default
31:30	Reserved	RO	Reserved	0x0
29:16	AD_OS_0	RW	ADC OFFSET residual.directly save the Adc result,that is, the ADC code, and convert it to two's complement operation when used (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0
15:12	Reserved	RO	Reserved	0x0
11:0	DA_0	RW	D/A data register (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0

ADCH0DR: (Offset 10h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13:0	ADDR_0	RO	channel 0 value(configure channel0,16 channels in total,the channel offset address is 0x20*channel +0x10)	0x0

ADCH1CR0: (Offset 20h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:29	Reserved	RO	Reserved	0x0
28:24	SP_MUX_1	RW	Positive terminal of DC voltage channel.(configure channel0,16 channels in total,the channel offset address is 0x20) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
23:21	Reserved	RO	Reserved	0x0
20:16	SN_MUX_1	RW	negative terminal of DC voltage channel.(configure channel0,16 channels in total,the channel offset address is 0x20) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
15	RED_OS_1	RW	offset Residual cancellation enable signal (configure channel0, 16channels in total,the channel offset address is 0x20) 0: no elimination of residuals 1: elimination of residuals	0x0
14	DMOF_1	RW	differential input mode output format(configure channel0,16 channels in total,the channel offset address is 0x20) 0: original code of result 1: complement of result	0x0
13	PD_DOUBLE_VIN_1	RW	in ADC single-ended mode, turn off the double-ended input (configure channel0,16 channels in total,the channel offset address is 0x20) 0: double-ended input 1: single-ended input	0x1
12	EN_DIFF_1	RW	ADC input working mode (configure channel0,15 channels in total,the channel offset address is 0x20) 0: single-ended mode 1: differential mode	0x1
11:8	PD_SW_IN_1	RW	PA3-PA0 analog switch control (configure channel0,16 channels in total,the channel offset address is 0x20) 0: strobe vs 1: disable	0xF

7:4	PD_AINP_1	RW	CHx sensor positive input selection (configure channel0,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 positive 0b0001: sensor1 positive 0b0010: sensor2 positive 0b0011: sensor3 positive 0b0100: sensor4 positive 0b0101: sensor5 positive 0b0110: sensor6 positive 0b0111: sensor7 positive 0b1000: sensor8 positive 0b1001: sensor9 positive 0b1010: sensor10 positive 0b1011:sensor11 positive	0xF
3:0	PD_AINN_1	RW	CHx sensor negative input selection (configure channel0,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 negative 0b0001: sensor1 negative 0b0010: sensor2 negative 0b0011: sensor3 negative 0b0100: sensor4 negative 0b0101: sensor5 negative 0b0110: sensor6 negative 0b0111: sensor7 negative 0b1000: sensor8 negative 0b1001: sensor9 negative 0b1010: sensor10 negative 0b1011:sensor11 negative	0xF

ADCH1CR1: (Offset 24h)

Bit	Symbol	R/W	Description	Default
31	Reserved	RO	Reserved	0x0
30:28	PGA_IBIASE_1	RW	PGA module overall current selection(configure channel1,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1μA 0b001: 1.25μA 0b010: 1.5μA 0b011: 1.75μA 0b100: 2μA 0b101: 2.25μA 0b110: 2.5μA 0b111: 2.75μA	0x4
27	Reserved	RO	Reserved	0x0

26:24	BW_FILTER_1	RW	PGA RC filter output frequency selection(configure channel1,16channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 125kHz 0b001: 250kHz 0b010: 167kHz 0b011: 500kHz 0b100: 143kHz 0b101: 333kHz 0b110: 200kHz 0b111: 1000kHz	0x3
23:22	VREF_SEL_1	RW	VRP voltage selection(configure channel1,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b00: 2.4v 0b01: 2.8v 0b10: 3.0v 0b11: 3.1v	0x1
21	VREF_GEN_SEL_1	RW	ADC refrence voltage selection(configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: AVDD 1: VRP	0x1
20	VCM_ADJ_1	RW	PGA output common mode voltage selection(configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: 0.5*AVDD 1: 0.5*AVDD-0.1	0x0
19	Reserved	RO	Reserved	0x0
18:16	ADC_IBIAS_1	RW	ADC BIAS current control(configure channel1,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 2μA 0b001: 2.5μA 0b010: 3μA 0b011: 3.5μA 0b100: 4μA 0b101: 4.5μA 0b110: 5μA 0b111: 5.5μA	0x4
15:13	Reserved	RO	Reserved	0x0
12	INV_AD_1	RW	SAR ADC output flip enable (configure channel1,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: no flip 1: flip	0x0
11	EN_PGA_1	RW	PGA enable switch (configure channel1,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: disable 1: enable	0x0

10	PD_PGA1_1	RW	First level of PGA enable switch (configure channel0,16channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
9	PD_PGA2_1	RW	second level of PGA enable switch (configure channel1,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
8	PD_FILTER_1	RW	turn off the PGA2 filter (configure channel1,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: turn on 1: turn off	0x0
7	Reserved	RO	Reserved	0x0
6:4	GAIN_PGA1_1	RW	First level of PGA gain selection(configure channel1,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256 0b110: 256 0b111: 256	0x2
3	Reserved	RO	Reserved	0x0
2:0	GAIN_PGA2_1	RW	second level of PGA gain selection(configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

DACH1CR: (Offset 28h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13	EN_DAC_CAL_1	RW	enable digital DAC calibration loop operation(configure channel1,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0

12	EN_DAC_1	RW	enable calibration offset DAC (configure channel1,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0
11	EN_DAC_VIN_1	RW	turn on DAC negative current input(configure channel1,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: turn off 1: turn on	0x1
10	DIR_DAC_1	RW	DAC direction select (configure channel1,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable current direction 1: enable current direction	0x0
9	DIR_MODE0_1	RW	DAC direction select (configure channel1,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offset 1: enable affect offset	0x0
8	DIR_MODE1_1	RW	DAC direction select (configure channel1,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offsef 1: enable affect offset	0x1
7:2	Reserved	RO	Reserved	0x0
1:0	VDAC_RANGE_1	RW	DAC calibration offset range (configure channel1,16 channels in total,the channel offset address is 0x20*channel +0x8) 0b00: ±0.540*VS/3 0b01: ±0.540*VS/4 0b10: ±0.540*VS/5 0b11: ±0.540*VS/6	0x0

DACH1DR: (Offset 2Ch)

Bit	Symbol	R/W	Description	Default
31:30	Reserved	RO	Reserved	0x0
29:16	AD_OS_1	RW	ADC OFFSET residual.directly save the Adc result,that is, the ADC code, and convert it to two's complement operation when used (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0
15:12	Reserved	RO	Reserved	0x0
11:0	DA_1	RW	D/A data register (configure channel1,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0

ADCH1DR: (Offset 30h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13:0	ADDR_1	RO	channel 1 value(configure channel0,16 channels in total,the channel offset address is 0x20*channel +0x10)	0x0

ADCH2CR0: (Offset 40h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:29	Reserved	RO	Reserved	0x0
28:24	SP_MUX_2	RW	Positive terminal of DC voltage channel.(configure channel2,16 channels in total,the channel offset address is 0x20) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
23:21	Reserved	RO	Reserved	0x0
20:16	SN_MUX_2	RW	negative terminal of DC voltage channel.(configure channel2,16 channels in total,the channel offset address is 0x20) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
15	RED_OS_2	RW	offset Residual cancellation enable signal (configure channel2, 16channels in total,the channel offset address is 0x20) 0: no elimination of residuals 1: elimination of residuals	0x0
14	DMOF_2	RW	differential input mode output format(configure channel2,16 channels in total,the channel offset address is 0x20) 0: original code of result 1: complement of result	0x0
13	PD_DOUBLE_VIN_2	RW	in ADC single-ended mode, turn off the double-ended input (configure channel2,16 channels in total,the channel offset address is 0x20) 0: double-ended input 1: single-ended input	0x1
12	EN_DIFF_2	RW	ADC input working mode (configure channel2,15 channels in total,the channel offset address is 0x20) 0: single-ended mode 1: differential mode	0x1
11:8	PD_SW_IN_2	RW	PA3-PA0 analog switch control (configure channel2,16 channels in total,the channel offset address is 0x20) 0: strobe vs 1: disable	0xF

7:4	PD_AINP_2	RW	CHx sensor positive input selection (configure channel2,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 positive 0b0001: sensor1 positive 0b0010: sensor2 positive 0b0011: sensor3 positive 0b0100: sensor4 positive 0b0101: sensor5 positive 0b0110: sensor6 positive 0b0111: sensor7 positive 0b1000: sensor8 positive 0b1001: sensor9 positive 0b1010: sensor10 positive 0b1011:sensor11 positive	0xF
3:0	PD_AINN_2	RW	CHx sensor negative input selection (configure channel0,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 negative 0b0001: sensor1 negative 0b0010: sensor2 negative 0b0011: sensor3 negative 0b0100: sensor4 negative 0b0101: sensor5 negative 0b0110: sensor6 negative 0b0111: sensor7 negative 0b1000: sensor8 negative 0b1001: sensor9 negative 0b1010: sensor10 negative 0b1011:sensor11 negative	0xF

ADCH2CR1: (Offset 44h)

Bit	Symbol	R/W	Description	Default
31	Reserved	RO	Reserved	0x0
30:28	PGA_IBIASE_2	RW	PGA module overall current selection(configure channel2,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1μA 0b001: 1.25μA 0b010: 1.5μA 0b011: 1.75μA 0b100: 2μA 0b101: 2.25μA 0b110: 2.5μA 0b111: 2.75μA	0x4
27	Reserved	RO	Reserved	0x0

26:24	BW_FILTER_2	RW	PGA RC filter output frequency selection(configure channel2,16channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 125kHz 0b001: 250kHz 0b010: 167kHz 0b011: 500kHz 0b100: 143kHz 0b101: 333kHz 0b110: 200kHz 0b111: 1000kHz	0x3
23:22	VREF_SEL_2	RW	VRP voltage selection(configure channel2,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b00: 2.4v 0b01: 2.8v 0b10: 3.0v 0b11: 3.1v	0x1
21	VREF_GEN_SEL_2	RW	ADC refrence voltage selection(configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: AVDD 1: VRP	0x1
20	VCM_ADJ_2	RW	PGA output common mode voltage selection(configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: 0.5*AVDD 1: 0.5*AVDD-0.1	0x0
19	Reserved	RO	Reserved	0x0
18:16	ADC_IBIAS_2	RW	ADC BIAS current control(configure channel2,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 2μA 0b001: 2.5μA 0b010: 3μA 0b011: 3.5μA 0b100: 4μA 0b101: 4.5μA 0b110: 5μA 0b111: 5.5μA	0x4
15:13	Reserved	RO	Reserved	0x0
12	INV_AD_2	RW	SAR ADC output flip enable (configure channel2,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: no flip 1: flip	0x0
11	EN_PGA_2	RW	PGA enable switch (configure channel2,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: disable 1: enable	0x0

10	PD_PGA1_2	RW	First level of PGA enable switch (configure channel2,16channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
9	PD_PGA2_2	RW	second level of PGA enable switch (configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
8	PD_FILTER_2	RW	turn off the PGA2 filter (configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: turn on 1: turn off	0x0
7	Reserved	RO	Reserved	0x0
6:4	GAIN_PGA1_2	RW	First level of PGA gain selection(configure channel2,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256 0b110: 256 0b111: 256	0x2
3	Reserved	RO	Reserved	0x0
2:0	GAIN_PGA2_2	RW	second level of PGA gain selection(configure channel2,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

DACH2CR: (Offset 48h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13	EN_DAC_CAL_2	RW	enable digital DAC calibration loop operation(configure channel2,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0

12	EN_DAC_2	RW	enable calibration offset DAC (configure channel3,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0
11	EN_DAC_VIN_2	RW	turn on DAC negative current input(configure channel2,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: turn off 1: turn on	0x1
10	DIR_DAC_2	RW	DAC direction select (configure channel2,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable current direction 1: enable current direction	0x0
9	DIR_MODE0_2	RW	DAC direction select (configure channel2,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offset 1: enable affect offset	0x0
8	DIR_MODE1_2	RW	DAC direction select (configure channel2,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offsef 1: enable affect offset	0x1
7:2	Reserved	RO	Reserved	0x0
1:0	VDAC_RANGE_2	RW	DAC calibration offset range (configure channel2,16 channels in total,the channel offset address is 0x20*channel +0x8) 0b00: ±0.540*VS/3 0b01: ±0.540*VS/4 0b10: ±0.540*VS/5 0b11: ±0.540*VS/6	0x0

DACH2DR: (Offset 4Ch)

Bit	Symbol	R/W	Description	Default
31:30	Reserved	RO	Reserved	0x0
29:16	AD_OS_2	RW	ADC OFFSET residual.directly save the Adc result,that is, the ADC code, and convert it to two's complement operation when used (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0
15:12	Reserved	RO	Reserved	0x0
11:0	DA_2	RW	D/A data register (configure channel2,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0

ADCH2DR: (Offset 50h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13:0	ADDR_2	RO	channel 2 value(configure channel2,16 channels in total,the channel offset address is 0x20*channel +0x10)	0x0

ADCH3CR0: (Offset 60h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:29	Reserved	RO	Reserved	0x0
28:24	SP_MUX_3	RW	Positive terminal of DC voltage channel.(configure channel3,16 channels in total,the channel offset address is 0x20) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
23:21	Reserved	RO	Reserved	0x0
20:16	SN_MUX_3	RW	negative terminal of DC voltage channel.(configure channel3,16 channels in total,the channel offset address is 0x20) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
15	RED_OS_3	RW	offset Residual cancellation enable signal (configure channel3, 16channels in total,the channel offset address is 0x20) 0: no elimination of residuals 1: elimination of residuals	0x0
14	DMOF_3	RW	differential input mode output format(configure channel3,16 channels in total,the channel offset address is 0x20) 0: original code of result 1: complement of result	0x0
13	PD_DOUBLE_VIN_3	RW	in ADC single-ended mode, turn off the double-ended input (configure channel0,16 channels in total,the channel offset address is 0x20) 0: double-ended input 1: single-ended input	0x1
12	EN_DIFF_3	RW	ADC input working mode (configure channel3,15 channels in total,the channel offset address is 0x20) 0: single-ended mode 1: differential mode	0x1
11:8	PD_SW_IN_3	RW	PA3-PA0 analog switch control (configure channel3,16 channels in total,the channel offset address is 0x20) 0: strobe vs 1: disable	0xF

7:4	PD_AINP_3	RW	CHx sensor positive input selection (configure channel0,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 positive 0b0001: sensor1 positive 0b0010: sensor2 positive 0b0011: sensor3 positive 0b0100: sensor4 positive 0b0101: sensor5 positive 0b0110: sensor6 positive 0b0111: sensor7 positive 0b1000: sensor8 positive 0b1001: sensor9 positive 0b1010: sensor10 positive 0b1011:sensor11 positive	0xF
3:0	PD_AINN_3	RW	CHx sensor negative input selection (configure channel3,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 negative 0b0001: sensor1 negative 0b0010: sensor2 negative 0b0011: sensor3 negative 0b0100: sensor4 negative 0b0101: sensor5 negative 0b0110: sensor6 negative 0b0111: sensor7 negative 0b1000: sensor8 negative 0b1001: sensor9 negative 0b1010: sensor10 negative 0b1011:sensor11 negative	0xF

ADCH3CR1: (Offset 64h)

Bit	Symbol	R/W	Description	Default
31	Reserved	RO	Reserved	0x0
30:28	PGA_IBIASE_3	RW	PGA module overall current selection(configure channel3,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1μA 0b001: 1.25μA 0b010: 1.5μA 0b011: 1.75μA 0b100: 2μA 0b101: 2.25μA 0b110: 2.5μA 0b111: 2.75μA	0x4
27	Reserved	RO	Reserved	0x0

26:24	BW_FILTER_3	RW	PGA RC filter output frequency selection(configure channel3,16channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 125kHz 0b001: 250kHz 0b010: 167kHz 0b011: 500kHz 0b100: 143kHz 0b101: 333kHz 0b110: 200kHz 0b111: 1000kHz	0x3
23:22	VREF_SEL_3	RW	VRP voltage selection(configure channel3,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b00: 2.4v 0b01: 2.8v 0b10: 3.0v 0b11: 3.1v	0x1
21	VREF_GEN_SEL_3	RW	ADC refrence voltage selection(configure channel3,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: AVDD 1: VRP	0x1
20	VCM_ADJ_3	RW	PGA output common mode voltage selection(configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: 0.5*AVDD 1: 0.5*AVDD-0.1	0x0
19	Reserved	RO	Reserved	0x0
18:16	ADC_IBIAS_3	RW	ADC BIAS current control(configure channel3,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 2μA 0b001: 2.5μA 0b010: 3μA 0b011: 3.5μA 0b100: 4μA 0b101: 4.5μA 0b110: 5μA 0b111: 5.5μA	0x4
15:13	Reserved	RO	Reserved	0x0
12	INV_AD_3	RW	SAR ADC output flip enable (configure channel3,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: no flip 1: flip	0x0
11	EN_PGA_3	RW	PGA enable switch (configure channel3,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: disable 1: enable	0x0

10	PD_PGA1_3	RW	First level of PGA enable switch (configure channel3,16channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
9	PD_PGA2_3	RW	second level of PGA enable switch (configure channel3,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
8	PD_FILTER_3	RW	turn off the PGA2 filter (configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: turn on 1: turn off	0x0
7	Reserved	RO	Reserved	0x0
6:4	GAIN_PGA1_3	RW	First level of PGA gain selection(configure channel3,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256 0b110: 256 0b111: 256	0x2
3	Reserved	RO	Reserved	0x0
2:0	GAIN_PGA2_3	RW	second level of PGA gain selection(configure channel3,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

DACH3CR: (Offset 68h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13	EN_DAC_CAL_3	RW	enable digital DAC calibration loop operation(configure channel3,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0

12	EN_DAC_3	RW	enable calibration offset DAC (configure channel3,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0
11	EN_DAC_VIN_3	RW	turn on DAC negative current input(configure channel3,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: turn off 1: turn on	0x1
10	DIR_DAC_3	RW	DAC direction select (configure channel3,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable current direction 1: enable current direction	0x0
9	DIR_MODE0_3	RW	DAC direction select (configure channel3,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offset 1: enable affect offset	0x0
8	DIR_MODE1_3	RW	DAC direction select (configure channel3,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offsef 1: enable affect offset	0x1
7:2	Reserved	RO	Reserved	0x0
1:0	VDAC_RANGE_3	RW	DAC calibration offset range (configure channel3,16 channels in total,the channel offset address is 0x20*channel +0x8) 0b00: ±0.540*VS/3 0b01: ±0.540*VS/4 0b10: ±0.540*VS/5 0b11: ±0.540*VS/6	0x0

DACH3DR: (Offset 6Ch)

Bit	Symbol	R/W	Description	Default
31:30	Reserved	RO	Reserved	0x0
29:16	AD_OS_3	RW	ADC OFFSET residual.directly save the Adc result,that is, the ADC code, and convert it to two's complement operation when used (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0
15:12	Reserved	RO	Reserved	0x0
11:0	DA_3	RW	D/A data register (configure channel3,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0

ADCH3DR: (Offset 70h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13:0	ADDR_3	RO	channel 3 value(configure channel0,16 channels in total,the channel offset address is 0x20*channel +0x10)	0x0

ADCH4CR0: (Offset 80h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:29	Reserved	RO	Reserved	0x0
28:24	SP_MUX_4	RW	Positive terminal of DC voltage channel.(configure channel4,16 channels in total,the channel offset address is 0x20) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
23:21	Reserved	RO	Reserved	0x0
20:16	SN_MUX_4	RW	negative terminal of DC voltage channel.(configure channel4,16 channels in total,the channel offset address is 0x20) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
15	RED_OS_4	RW	offset Residual cancellation enable signal (configure channel4, 16channels in total,the channel offset address is 0x20) 0: no elimination of residuals 1: elimination of residuals	0x0
14	DMOF_4	RW	differential input mode output format(configure channel4,16 channels in total,the channel offset address is 0x20) 0: original code of result 1: complement of result.	0x0
13	PD_DOUBLE_VIN_4	RW	in ADC single-ended mode, turn off the double-ended input (configure channel4,16 channels in total,the channel offset address is 0x20) 0: double-ended input 1: single-ended input	0x1
12	EN_DIFF_4	RW	ADC input working mode (configure channel4,15 channels in total,the channel offset address is 0x20) 0: single-ended mode 1: differential mode	0x1
11:8	PD_SW_IN_4	RW	PA3-PA0 analog switch control (configure channel4,16 channels in total,the channel offset address is 0x20) 0: strobe vs 1: disable	0xF

7:4	PD_AINP_4	RW	CHx sensor positive input selection (configure channel0,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 positive 0b0001: sensor1 positive 0b0010: sensor2 positive 0b0011: sensor3 positive 0b0100: sensor4 positive 0b0101: sensor5 positive 0b0110: sensor6 positive 0b0111: sensor7 positive 0b1000: sensor8 positive 0b1001: sensor9 positive 0b1010: sensor10 positive 0b1011:sensor11 positive	0xF
3:0	PD_AINN_4	RW	CHx sensor negative input selection (configure channel4,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 negative 0b0001: sensor1 negative 0b0010: sensor2 negative 0b0011: sensor3 negative 0b0100: sensor4 negative 0b0101: sensor5 negative 0b0110: sensor6 negative 0b0111: sensor7 negative 0b1000: sensor8 negative 0b1001: sensor9 negative 0b1010: sensor10 negative 0b1011:sensor11 negative	0xF

ADCH4CR1: (Offset 84h)

Bit	Symbol	R/W	Description	Default
31	Reserved	RO	Reserved	0x0
30:28	PGA_IBIASE_4	RW	PGA module overall current selection(configure channel4,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1μA 0b001: 1.25μA 0b010: 1.5μA 0b011: 1.75μA 0b100: 2μA 0b101: 2.25μA 0b110: 2.5μA 0b111: 2.75μA	0x4
27	Reserved	RO	Reserved	0x0

26:24	BW_FILTER_4	RW	PGA RC filter output frequency selection(configure channel4,16channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 125kHz 0b001: 250kHz 0b010: 167kHz 0b011: 500kHz 0b100: 143kHz 0b101: 333kHz 0b110: 200kHz 0b111: 1000kHz	0x3
23:22	VREF_SEL_4	RW	VRP voltage selection(configure channel4,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b00: 2.4v 0b01: 2.8v 0b10: 3.0v 0b11: 3.1v	0x1
21	VREF_GEN_SEL_4	RW	ADC refrence voltage selection(configure channel4,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: AVDD 1: VRP	0x1
20	VCM_ADJ_4	RW	PGA output common mode voltage selection(configure channel4,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: 0.5*AVDD 1: 0.5*AVDD-0.1	0x0
19	Reserved	RO	Reserved	0x0
18:16	ADC_IBIAS_4	RW	ADC BIAS current control(configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 2μA 0b001: 2.5μA 0b010: 3μA 0b011: 3.5μA 0b100: 4μA 0b101: 4.5μA 0b110: 5μA 0b111: 5.5μA	0x4
15:13	Reserved	RO	Reserved	0x0
12	INV_AD_4	RW	SAR ADC output flip enable (configure channel4,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: no flip 1: flip	0x0
11	EN_PGA_4	RW	PGA enable switch (configure channel4,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: disable 1: enable	0x0

10	PD_PGA1_4	RW	First level of PGA enable switch (configure channel4,16channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
9	PD_PGA2_4	RW	second level of PGA enable switch (configure channel4,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
8	PD_FILTER_4	RW	turn off the PGA2 filter (configure channel4,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: turn on 1: turn off	0x0
7	Reserved	RO	Reserved	0x0
6:4	GAIN_PGA1_4	RW	First level of PGA gain selection(configure channel4,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256 0b110: 256 0b111: 256	0x2
3	Reserved	RO	Reserved	0x0
2:0	GAIN_PGA2_4	RW	second level of PGA gain selection(configure channel4,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

DACH4CR: (Offset 88h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13	EN_DAC_CAL_4	RW	enable digital DAC calibration loop operation(configure channel4,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0

12	EN_DAC_4	RW	enable calibration offset DAC (configure channel4,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0
11	EN_DAC_VIN_4	RW	turn on DAC negative current input(configure channel4,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: turn off 1: turn on	0x1
10	DIR_DAC_4	RW	DAC direction select (configure channel4,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable current direction 1: enable current direction	0x0
9	DIR_MODE0_4	RW	DAC direction select (configure channel4,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offset 1: enable affect offset	0x0
8	DIR_MODE1_4	RW	DAC direction select (configure channel4,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offsef 1: enable affect offset	0x1
7:2	Reserved	RO	Reserved	0x0
1:0	VDAC_RANGE_4	RW	DAC calibration offset range (configure channel4,16 channels in total,the channel offset address is 0x20*channel +0x8) 0b00: ±0.540*VS/3 0b01: ±0.540*VS/4 0b10: ±0.540*VS/5 0b11: ±0.540*VS/6	0x0

DACH4DR: (Offset 8Ch)

Bit	Symbol	R/W	Description	Default
31:30	Reserved	RO	Reserved	0x0
29:16	AD_OS_4	RW	ADC OFFSET residual.directly save the Adc result,that is, the ADC code, and convert it to two's complement operation when used (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0
15:12	Reserved	RO	Reserved	0x0
11:0	DA_4	RW	D/A data register (configure channel4,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0

ADCH4DR: (Offset 90h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13:0	ADDR_4	RO	channel 4 value(configure channel4,16 channels in total,the channel offset address is 0x20*channel +0x10)	0x0

ADCH5CR0: (Offset A0h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:29	Reserved	RO	Reserved	0x0
28:24	SP_MUX_5	RW	Positive terminal of DC voltage channel.(configure channel5,16channels in total,the channel offset address is 0x20) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
23:21	Reserved	RO	Reserved	0x0
20:16	SN_MUX_5	RW	negative terminal of DC voltage channel.(configure channel5,16 channels in total,the channel offset address is 0x20) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
15	RED_OS_5	RW	offset Residual cancellation enable signal (configure channel5, 16channels in total,the channel offset address is 0x20) 0: no elimination of residuals 1: elimination of residuals	0x0
14	DMOF_5	RW	differential input mode output format(configure channel5,16 channels in total,the channel offset address is 0x20) 0: original code of result 1: complement of result	0x0
13	PD_DOUBLE_VIN_5	RW	in ADC single-ended mode, turn off the double-ended input (configure channel5,16 channels in total,the channel offset address is 0x20) 0: double-ended input 1: single-ended input	0x1
12	EN_DIFF_5	RW	ADC input working mode (configure channel5,15 channels in total,the channel offset address is 0x20) 0: single-ended mode 1: differential mode	0x1
11:8	PD_SW_IN_5	RW	PA3-PA0 analog switch control (configure channel0,16 channels in total,the channel offset address is 0x20) 0: strobe vs 1: disable	0xF

7:4	PD_AINP_5	RW	CHx sensor positive input selection (configure channel5,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 positive 0b0001: sensor1 positive 0b0010: sensor2 positive 0b0011: sensor3 positive 0b0100: sensor4 positive 0b0101: sensor5 positive 0b0110: sensor6 positive 0b0111: sensor7 positive 0b1000: sensor8 positive 0b1001: sensor9 positive 0b1010: sensor10 positive 0b1011:sensor11 positive	0xF
3:0	PD_AINN_5	RW	CHx sensor negative input selection (configure channel5,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 negative 0b0001: sensor1 negative 0b0010: sensor2 negative 0b0011: sensor3 negative 0b0100: sensor4 negative 0b0101: sensor5 negative 0b0110: sensor6 negative 0b0111: sensor7 negative 0b1000: sensor8 negative 0b1001: sensor9 negative 0b1010: sensor10 negative 0b1011:sensor11 negative	0xF

ADCH5CR1: (Offset A4h)

Bit	Symbol	R/W	Description	Default
31	Reserved	RO	Reserved	0x0
30:28	PGA_IBIASE_5	RW	PGA module overall current selection(configure channel5,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1μA 0b001: 1.25μA 0b010: 1.5μA 0b011: 1.75μA 0b100: 2μA 0b101: 2.25μA 0b110: 2.5μA 0b111: 2.75μA	0x4
27	Reserved	RO	Reserved	0x0

26:24	BW_FILTER_5	RW	PGA RC filter output frequency selection(configure channel5,16channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 125kHz 0b001: 250kHz 0b010: 167kHz 0b011: 500kHz 0b100: 143kHz 0b101: 333kHz 0b110: 200kHz 0b111: 1000kHz	0x3
23:22	VREF_SEL_5	RW	VRP voltage selection(configure channel5,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b00: 2.4v 0b01: 2.8v 0b10: 3.0v 0b11: 3.1v	0x1
21	VREF_GEN_SEL_5	RW	ADC refrence voltage selection(configure channel5,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: AVDD 1: VRP	0x1
20	VCM_ADJ_5	RW	PGA output common mode voltage selection(configure channel5,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: 0.5*AVDD 1: 0.5*AVDD-0.1	0x0
19	Reserved	RO	Reserved	0x0
18:16	ADC_IBIAS_5	RW	ADC BIAS current control(configure channel5,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 2μA 0b001: 2.5μA 0b010: 3μA 0b011: 3.5μA 0b100: 4μA 0b101: 4.5μA 0b110: 5μA 0b111: 5.5μA	0x4
15:13	Reserved	RO	Reserved	0x0
12	INV_AD_5	RW	SAR ADC output flip enable (configure channel5,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: no flip 1: flip	0x0
11	EN_PGA_5	RW	PGA enable switch (configure channel5,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: disable 1: enable	0x0

10	PD_PGA1_5	RW	First level of PGA enable switch (configure channel5,16channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
9	PD_PGA2_5	RW	second level of PGA enable switch (configure channel5,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
8	PD_FILTER_5	RW	turn off the PGA2 filter (configure channel5,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: turn on 1: turn off	0x0
7	Reserved	RO	Reserved	0x0
6:4	GAIN_PGA1_5	RW	First level of PGA gain selection(configure channel5,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256 0b110: 256 0b111: 256	0x2
3	Reserved	RO	Reserved	0x0
2:0	GAIN_PGA2_5	RW	second level of PGA gain selection(configure channel5,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

DACH5CR: (Offset A8h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13	EN_DAC_CAL_5	RW	enable digital DAC calibration loop operation(configure channel5,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0

12	EN_DAC_5	RW	enable calibration offset DAC (configure channel5,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0
11	EN_DAC_VIN_5	RW	turn on DAC negative current input(configure channel5,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: turn off 1: turn on	0x1
10	DIR_DAC_5	RW	DAC direction select (configure channel5,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable current direction 1: enable current direction	0x0
9	DIR_MODE0_5	RW	DAC direction select (configure channel5,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offset 1: enable affect offset	0x0
8	DIR_MODE1_5	RW	DAC direction select (configure channel5,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offsef 1: enable affect offset	0x1
7:2	Reserved	RO	Reserved	0x0
1:0	VDAC_RANGE_5	RW	DAC calibration offset range (configure channel5,16 channels in total,the channel offset address is 0x20*channel +0x8) 0b00: ±0.540*VS/3 0b01: ±0.540*VS/4 0b10: ±0.540*VS/5 0b11: ±0.540*VS/6	0x0

DACH5DR: (Offset ACh)

Bit	Symbol	R/W	Description	Default
31:30	Reserved	RO	Reserved	0x0
29:16	AD_OS_5	RW	ADC OFFSET residual.directly save the Adc result,that is, the ADC code, and convert it to two's complement operation when used (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0
15:12	Reserved	RO	Reserved	0x0
11:0	DA_5	RW	D/A data register (configure channel5,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0

ADCH5DR: (Offset B0h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13:0	ADDR_5	RO	channel 5 value(configure channel5,16 channels in total,the channel offset address is 0x20*channel +0x10)	0x0

ADCH6CR0: (Offset C0h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:29	Reserved	RO	Reserved	0x0
28:24	SP_MUX_6	RW	Positive terminal of DC voltage channel.(configure channel6,16 channels in total,the channel offset address is 0x20) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
23:21	Reserved	RO	Reserved	0x0
20:16	SN_MUX_6	RW	negative terminal of DC voltage channel.(configure channel6,16 channels in total,the channel offset address is 0x20) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
15	RED_OS_6	RW	offset Residual cancellation enable signal (configure channel6, 16channels in total,the channel offset address is 0x20) 0: no elimination of residuals 1: elimination of residuals	0x0
14	DMOF_6	RW	differential input mode output format(configure channel6,16 channels in total,the channel offset address is 0x20) 0: original code of result 1: complement of result	0x0
13	PD_DOUBLE_VIN_6	RW	in ADC single-ended mode, turn off the double-ended input (configure channel6,16 channels in total,the channel offset address is 0x20) 0: double-ended input 1: single-ended input	0x1
12	EN_DIFF_6	RW	ADC input working mode (configure channel6,15 channels in total,the channel offset address is 0x20) 0: single-ended mode 1: differential mode	0x1
11:8	PD_SW_IN_6	RW	PA3-PA0 analog switch control (configure channel6,16 channels in total,the channel offset address is 0x20) 0: strobe vs 1: disable	0xF

7:4	PD_AINP_6	RW	CHx sensor positive input selection (configure channel6,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 positive 0b0001: sensor1 positive 0b0010: sensor2 positive 0b0011: sensor3 positive 0b0100: sensor4 positive 0b0101: sensor5 positive 0b0110: sensor6 positive 0b0111: sensor7 positive 0b1000: sensor8 positive 0b1001: sensor9 positive 0b1010: sensor10 positive 0b1011:sensor11 positive	0xF
3:0	PD_AINN_6	RW	CHx sensor negative input selection (configure channel6,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 negative 0b0001: sensor1 negative 0b0010: sensor2 negative 0b0011: sensor3 negative 0b0100: sensor4 negative 0b0101: sensor5 negative 0b0110: sensor6 negative 0b0111: sensor7 negative 0b1000: sensor8 negative 0b1001: sensor9 negative 0b1010: sensor10 negative 0b1011:sensor11 negative	0xF

ADCH6CR1: (Offset C4h)

Bit	Symbol	R/W	Description	Default
31	Reserved	RO	Reserved	0x0
30:28	PGA_IBIASE_6	RW	PGA module overall current selection(configure channel6,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1μA 0b001: 1.25μA 0b010: 1.5μA 0b011: 1.75μA 0b100: 2μA 0b101: 2.25μA 0b110: 2.5μA 0b111: 2.75μA	0x4
27	Reserved	RO	Reserved	0x0

26:24	BW_FILTER_6	RW	PGA RC filter output frequency selection(configure channel6,16channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 125kHz 0b001: 250kHz 0b010: 167kHz 0b011: 500kHz 0b100: 143kHz 0b101: 333kHz 0b110: 200kHz 0b111: 1000kHz	0x3
23:22	VREF_SEL_6	RW	VRP voltage selection(configure channel6,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b00: 2.4v 0b01: 2.8v 0b10: 3.0v 0b11: 3.1v	0x1
21	VREF_GEN_SEL_6	RW	ADC refrence voltage selection(configure channel6,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: AVDD 1: VRP	0x1
20	VCM_ADJ_6	RW	PGA output common mode voltage selection(configure channel6,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: 0.5*AVDD 1: 0.5*AVDD-0.1	0x0
19	Reserved	RO	Reserved	0x0
18:16	ADC_IBIAS_6	RW	ADC BIAS current control(configure channel6,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 2μA 0b001: 2.5μA 0b010: 3μA 0b011: 3.5μA 0b100: 4μA 0b101: 4.5μA 0b110: 5μA 0b111: 5.5μA	0x4
15:13	Reserved	RO	Reserved	0x0
12	INV_AD_6	RW	SAR ADC output flip enable (configure channel6,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: no flip 1: flip	0x0
11	EN_PGA_6	RW	PGA enable switch (configure channel6,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: disable 1: enable	0x0

10	PD_PGA1_6	RW	First level of PGA enable switch (configure channel6,16channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
9	PD_PGA2_6	RW	second level of PGA enable switch (configure channel6,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
8	PD_FILTER_6	RW	turn off the PGA2 filter (configure channel6,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: turn on 1: turn off	0x0
7	Reserved	RO	Reserved	0x0
6:4	GAIN_PGA1_6	RW	First level of PGA gain selection(configure channel6,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256 0b110: 256 0b111: 256	0x2
3	Reserved	RO	Reserved	0x0
2:0	GAIN_PGA2_6	RW	second level of PGA gain selection(configure channel6,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

DACH6CR: (Offset C8h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13	EN_DAC_CAL_6	RW	enable digital DAC calibration loop operation(configure channel6,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0

12	EN_DAC_6	RW	enable calibration offset DAC (configure channel6,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0
11	EN_DAC_VIN_6	RW	turn on DAC negative current input(configure channel6,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: turn off 1: turn on	0x1
10	DIR_DAC_6	RW	DAC direction select (configure channel6,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable current direction 1: enable current direction	0x0
9	DIR_MODE0_6	RW	DAC direction select (configure channel6,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offset 1: enable affect offset	0x0
8	DIR_MODE1_6	RW	DAC direction select (configure channel6,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offsef 1: enable affect offset	0x1
7:2	Reserved	RO	Reserved	0x0
1:0	VDAC_RANGE_6	RW	DAC calibration offset range (configure channel6,16 channels in total,the channel offset address is 0x20*channel +0x8) 0b00: ±0.540*VS/3 0b01: ±0.540*VS/4 0b10: ±0.540*VS/5 0b11: ±0.540*VS/6	0x0

DACH6DR: (Offset CCh)

Bit	Symbol	R/W	Description	Default
31:30	Reserved	RO	Reserved	0x0
29:16	AD_OS_6	RW	ADC OFFSET residual.directly save the Adc result,that is, the ADC code, and convert it to two's complement operation when used (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0
15:12	Reserved	RO	Reserved	0x0
11:0	DA_6	RW	D/A data register (configure channel6,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0

ADCH6DR: (Offset D0h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13:0	ADDR_6	RO	channel 6 value(configure channel6,16 channels in total,the channel offset address is 0x20*channel +0x10)	0x0

ADCH7CR0: (Offset E0h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:29	Reserved	RO	Reserved	0x0
28:24	SP_MUX_7	RW	Positive terminal of DC voltage channel.(configure channel7,16 channels in total,the channel offset address is 0x20) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
23:21	Reserved	RO	Reserved	0x0
20:16	SN_MUX_7	RW	negative terminal of DC voltage channel.(configure channel7,16 channels in total,the channel offset address is 0x20) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
15	RED_OS_7	RW	offset Residual cancellation enable signal (configure channel7, 16channels in total,the channel offset address is 0x20) 0: no elimination of residuals 1: elimination of residuals	0x0
14	DMOF_7	RW	differential input mode output format(configure channel7,16 channels in total,the channel offset address is 0x20) 0: original code of result 1: complement of result	0x0
13	PD_DOUBLE_VIN_7	RW	in ADC single-ended mode, turn off the double-ended input (configure channel7,16 channels in total,the channel offset address is 0x20) 0: double-ended input 1: single-ended input	0x1
12	EN_DIFF_7	RW	ADC input working mode (configure channel7,15 channels in total,the channel offset address is 0x20) 0: single-ended mode 1: differential mode	0x1
11:8	PD_SW_IN_7	RW	PA3-PA0 analog switch control (configure channel7,16 channels in total,the channel offset address is 0x20) 0: strobe vs 1: disable	0xF

7:4	PD_AINP_7	RW	CHx sensor positive input selection (configure channel7,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 positive 0b0001: sensor1 positive 0b0010: sensor2 positive 0b0011: sensor3 positive 0b0100: sensor4 positive 0b0101: sensor5 positive 0b0110: sensor6 positive 0b0111: sensor7 positive 0b1000: sensor8 positive 0b1001: sensor9 positive 0b1010: sensor10 positive 0b1011:sensor11 positive	0xF
3:0	PD_AINN_7	RW	CHx sensor negative input selection (configure channel7,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 negative 0b0001: sensor1 negative 0b0010: sensor2 negative 0b0011: sensor3 negative 0b0100: sensor4 negative 0b0101: sensor5 negative 0b0110: sensor6 negative 0b0111: sensor7 negative 0b1000: sensor8 negative 0b1001: sensor9 negative 0b1010: sensor10 negative 0b1011:sensor11 negative	0xF

ADCH7CR1: (Offset E4h)

Bit	Symbol	R/W	Description	Default
31	Reserved	RO	Reserved	0x0
30:28	PGA_IBIASE_7	RW	PGA module overall current selection(configure channel7,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1μA 0b001: 1.25μA 0b010: 1.5μA 0b011: 1.75μA 0b100: 2μA 0b101: 2.25μA 0b110: 2.5μA 0b111: 2.75μA	0x4
27	Reserved	RO	Reserved	0x0

26:24	BW_FILTER_7	RW	PGA RC filter output frequency selection(configure channel7,16channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 125kHz 0b001: 250kHz 0b010: 167kHz 0b011: 500kHz 0b100: 143kHz 0b101: 333kHz 0b110: 200kHz 0b111: 1000kHz	0x3
23:22	VREF_SEL_7	RW	VRP voltage selection(configure channel7,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b00: 2.4v 0b01: 2.8v 0b10: 3.0v 0b11: 3.1v	0x1
21	VREF_GEN_SEL_7	RW	ADC refrence voltage selection(configure channel7,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: AVDD 1: VRP	0x1
20	VCM_ADJ_7	RW	PGA output common mode voltage selection(configure channel7,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: 0.5*AVDD 1: 0.5*AVDD-0.1	0x0
19	Reserved	RO	Reserved	0x0
18:16	ADC_IBIAS_7	RW	ADC BIAS current control(configure channel7,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 2μA 0b001: 2.5μA 0b010: 3μA 0b011: 3.5μA 0b100: 4μA 0b101: 4.5μA 0b110: 5μA 0b111: 5.5μA	0x4
15:13	Reserved	RO	Reserved	0x0
12	INV_AD_7	RW	SAR ADC output flip enable (configure channel7,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: no flip 1: flip	0x0
11	EN_PGA_7	RW	PGA enable switch (configure channel7,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: disable 1: enable	0x0

10	PD_PGA1_7	RW	First level of PGA enable switch (configure channel7,16channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
9	PD_PGA2_7	RW	second level of PGA enable switch (configure channel7,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
8	PD_FILTER_7	RW	turn off the PGA2 filter (configure channel7,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: turn on 1: turn off	0x0
7	Reserved	RO	Reserved	0x0
6:4	GAIN_PGA1_7	RW	First level of PGA gain selection(configure channel7,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256 0b110: 256 0b111: 256	0x2
3	Reserved	RO	Reserved	0x0
2:0	GAIN_PGA2_7	RW	second level of PGA gain selection(configure channel7,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

DACH7CR: (Offset E8h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13	EN_DAC_CAL_7	RW	enable digital DAC calibration loop operation(configure channel7,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0

12	EN_DAC_7	RW	enable calibration offset DAC (configure channel7,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0
11	EN_DAC_VIN_7	RW	turn on DAC negative current input(configure channel7,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: turn off 1: turn on	0x1
10	DIR_DAC_7	RW	DAC direction select (configure channel7,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable current direction 1: enable current direction	0x0
9	DIR_MODE0_7	RW	DAC direction select (configure channel7,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offset 1: enable affect offset	0x0
8	DIR_MODE1_7	RW	DAC direction select (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offsef 1: enable affect offset	0x1
7:2	Reserved	RO	Reserved	0x0
1:0	VDAC_RANGE_7	RW	DAC calibration offset range (configure channel7,16 channels in total,the channel offset address is 0x20*channel +0x8) 0b00: ±0.540*VS/3 0b01: ±0.540*VS/4 0b10: ±0.540*VS/5 0b11: ±0.540*VS/6	0x0

DACH7DR: (Offset ECh)

Bit	Symbol	R/W	Description	Default
31:30	Reserved	RO	Reserved	0x0
29:16	AD_OS_7	RW	ADC OFFSET residual.directly save the Adc result,that is, the ADC code, and convert it to two's complement operation when used (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0
15:12	Reserved	RO	Reserved	0x0
11:0	DA_7	RW	D/A data register (configure channel7,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0

ADCH7DR: (Offset F0h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13:0	ADDR_7	RO	channel 7 value(configure channel7,16 channels in total,the channel offset address is 0x20*channel +0x10)	0x0

ADCH8CR0: (Offset 100h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:29	Reserved	RO	Reserved	0x0
28:24	SP_MUX_8	RW	Positive terminal of DC voltage channel.(configure channel8,16 channels in total,the channel offset address is 0x20) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
23:21	Reserved	RO	Reserved	0x0
20:16	SN_MUX_8	RW	negative terminal of DC voltage channel.(configure channel8,16 channels in total,the channel offset address is 0x20) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
15	RED_OS_8	RW	offset Residual cancellation enable signal (configure channel8, 16channels in total,the channel offset address is 0x20) 0: no elimination of residuals 1: elimination of residuals	0x0
14	DMOF_8	RW	differential input mode output format(configure channel8,16 channels in total,the channel offset address is 0x20) 0: original code of result 1: complement of result.	0x0
13	PD_DOUBLE_VIN_8	RW	in ADC single-ended mode, turn off the double-ended input (configure channel8,16 channels in total,the channel offset address is 0x20) 0: double-ended input 1: single-ended input	0x1
12	EN_DIFF_8	RW	ADC input working mode (configure channel8,15 channels in total,the channel offset address is 0x20) 0: single-ended mode 1: differential mode	0x1
11:8	PD_SW_IN_8	RW	PA3-PA0 analog switch control (configure channel8,16 channels in total,the channel offset address is 0x20) 0: strobe vs 1: disable	0xF

7:4	PD_AINP_8	RW	CHx sensor positive input selection (configure channel8,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 positive 0b0001: sensor1 positive 0b0010: sensor2 positive 0b0011: sensor3 positive 0b0100: sensor4 positive 0b0101: sensor5 positive 0b0110: sensor6 positive 0b0111: sensor7 positive 0b1000: sensor8 positive 0b1001: sensor9 positive 0b1010: sensor10 positive 0b1011:sensor11 positive	0xF
3:0	PD_AINN_8	RW	CHx sensor negative input selection (configure channel8,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 negative 0b0001: sensor1 negative 0b0010: sensor2 negative 0b0011: sensor3 negative 0b0100: sensor4 negative 0b0101: sensor5 negative 0b0110: sensor6 negative 0b0111: sensor7 negative 0b1000: sensor8 negative 0b1001: sensor9 negative 0b1010: sensor10 negative 0b1011:sensor11 negative	0xF

ADCH8CR1: (Offset 104h)

Bit	Symbol	R/W	Description	Default
31	Reserved	RO	Reserved	0x0
30:28	PGA_IBIASE_8	RW	PGA module overall current selection(configure channel8,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1μA 0b001: 1.25μA 0b010: 1.5μA 0b011: 1.75μA 0b100: 2μA 0b101: 2.25μA 0b110: 2.5μA 0b111: 2.75μA	0x4
27	Reserved	RO	Reserved	0x0

26:24	BW_FILTER_8	RW	PGA RC filter output frequency selection(configure channel8,16channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 125kHz 0b001: 250kHz 0b010: 167kHz 0b011: 500kHz 0b100: 143kHz 0b101: 333kHz 0b110: 200kHz 0b111: 1000kHz	0x3
23:22	VREF_SEL_8	RW	VRP voltage selection(configure channel8,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b00: 2.4v 0b01: 2.8v 0b10: 3.0v 0b11: 3.1v	0x1
21	VREF_GEN_SEL_8	RW	ADC refrence voltage selection(configure channel8,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: AVDD 1: VRP	0x1
20	VCM_ADJ_8	RW	PGA output common mode voltage selection(configure channel8,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: 0.5*AVDD 1: 0.5*AVDD-0.1	0x0
19	Reserved	RO	Reserved	0x0
18:16	ADC_IBIAS_8	RW	ADC BIAS current control(configure channel8,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 2μA 0b001: 2.5μA 0b010: 3μA 0b011: 3.5μA 0b100: 4μA 0b101: 4.5μA 0b110: 5μA 0b111: 5.5μA	0x4
15:13	Reserved	RO	Reserved	0x0
12	INV_AD_8	RW	SAR ADC output flip enable (configure channel8,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: no flip 1: flip	0x0
11	EN_PGA_8	RW	PGA enable switch (configure channel8,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: disable 1: enable	0x0

10	PD_PGA1_8	RW	First level of PGA enable switch (configure channel8,16channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
9	PD_PGA2_8	RW	second level of PGA enable switch (configure channel8,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
8	PD_FILTER_8	RW	turn off the PGA2 filter (configure channel8,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: turn on 1: turn off	0x0
7	Reserved	RO	Reserved	0x0
6:4	GAIN_PGA1_8	RW	First level of PGA gain selection(configure channel8,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256 0b110: 256 0b111: 256	0x2
3	Reserved	RO	Reserved	0x0
2:0	GAIN_PGA2_8	RW	second level of PGA gain selection(configure channel8,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

DACH8CR: (Offset 108h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13	EN_DAC_CAL_8	RW	enable digital DAC calibration loop operation(configure channel8,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0

12	EN_DAC_8	RW	enable calibration offset DAC (configure channel8,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0
11	EN_DAC_VIN_8	RW	turn on DAC negative current input(configure channel8,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: turn off 1: turn on	0x1
10	DIR_DAC_8	RW	DAC direction select (configure channel8,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable current direction 1: enable current direction	0x0
9	DIR_MODE0_8	RW	DAC direction select (configure channel8,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offset 1: enable affect offset	0x0
8	DIR_MODE1_8	RW	DAC direction select (configure channel8,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offsef 1: enable affect offset	0x1
7:2	Reserved	RO	Reserved	0x0
1:0	VDAC_RANGE_8	RW	DAC calibration offset range (configure channel8,16 channels in total,the channel offset address is 0x20*channel +0x8) 0b00: ±0.540*VS/3 0b01: ±0.540*VS/4 0b10: ±0.540*VS/5 0b11: ±0.540*VS/6	0x0

DACH8DR: (Offset 10Ch)

Bit	Symbol	R/W	Description	Default
31:30	Reserved	RO	Reserved	0x0
29:16	AD_OS_8	RW	ADC OFFSET residual.directly save the Adc result,that is, the ADC code, and convert it to two's complement operation when used (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0
15:12	Reserved	RO	Reserved	0x0
11:0	DA_8	RW	D/A data register (configure channel8,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0

ADCH8DR: (Offset 110h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13:0	ADDR_8	RO	channel 8 value(configure channel8,16 channels in total,the channel offset address is 0x20*channel +0x10)	0x0

ADCH9CR0: (Offset 120h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:29	Reserved	RO	Reserved	0x0
28:24	SP_MUX_9	RW	Positive terminal of DC voltage channel.(configure channel9,16 channels in total,the channel offset address is 0x20) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
23:21	Reserved	RO	Reserved	0x0
20:16	SN_MUX_9	RW	negative terminal of DC voltage channel.(configure channel9,16 channels in total,the channel offset address is 0x20) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
15	RED_OS_9	RW	offset Residual cancellation enable signal (configure channel9, 16channels in total,the channel offset address is 0x20) 0: no elimination of residuals 1: elimination of residuals	0x0
14	DMOF_9	RW	differential input mode output format(configure channel9,16 channels in total,the channel offset address is 0x20) 0: original code of result 1: complement of result	0x0
13	PD_DOUBLE_VIN_9	RW	in ADC single-ended mode, turn off the double-ended input (configure channel9,16 channels in total,the channel offset address is 0x20) 0: double-ended input 1: single-ended input	0x1
12	EN_DIFF_9	RW	ADC input working mode (configure channel9,15 channels in total,the channel offset address is 0x20) 0: single-ended mode 1: differential mode	0x1
11:8	PD_SW_IN_9	RW	PA3-PA0 analog switch control (configure channel9,16 channels in total,the channel offset address is 0x20) 0: strobe vs 1: disable	0xF

7:4	PD_AINP_9	RW	CHx sensor positive input selection (configure channel9,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 positive 0b0001: sensor1 positive 0b0010: sensor2 positive 0b0011: sensor3 positive 0b0100: sensor4 positive 0b0101: sensor5 positive 0b0110: sensor6 positive 0b0111: sensor7 positive 0b1000: sensor8 positive 0b1001: sensor9 positive 0b1010: sensor10 positive 0b1011:sensor11 positive	0xF
3:0	PD_AINN_9	RW	CHx sensor negative input selection (configure channel9,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 negative 0b0001: sensor1 negative 0b0010: sensor2 negative 0b0011: sensor3 negative 0b0100: sensor4 negative 0b0101: sensor5 negative 0b0110: sensor6 negative 0b0111: sensor7 negative 0b1000: sensor8 negative 0b1001: sensor9 negative 0b1010: sensor10 negative 0b1011:sensor11 negative	0xF

ADCH9CR1: (Offset 124h)

Bit	Symbol	R/W	Description	Default
31	Reserved	RO	Reserved	0x0
30:28	PGA_IBIASE_9	RW	PGA module overall current selection(configure channel9,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1μA 0b001: 1.25μA 0b010: 1.5μA 0b011: 1.75μA 0b100: 2μA 0b101: 2.25μA 0b110: 2.5μA 0b111: 2.75μA	0x4
27	Reserved	RO	Reserved	0x0

26:24	BW_FILTER_9	RW	PGA RC filter output frequency selection(configure channel9,16channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 125kHz 0b001: 250kHz 0b010: 167kHz 0b011: 500kHz 0b100: 143kHz 0b101: 333kHz 0b110: 200kHz 0b111: 1000kHz	0x3
23:22	VREF_SEL_9	RW	VRP voltage selection(configure channel9,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b00: 2.4v 0b01: 2.8v 0b10: 3.0v 0b11: 3.1v	0x1
21	VREF_GEN_SEL_9	RW	ADC refrence voltage selection(configure channel9,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: AVDD 1: VRP	0x1
20	VCM_ADJ_9	RW	PGA output common mode voltage selection(configure channel9,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: 0.5*AVDD 1: 0.5*AVDD-0.1	0x0
19	Reserved	RO	Reserved	0x0
18:16	ADC_IBIAS_9	RW	ADC BIAS current control(configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 2μA 0b001: 2.5μA 0b010: 3μA 0b011: 3.5μA 0b100: 4μA 0b101: 4.5μA 0b110: 5μA 0b111: 5.5μA	0x4
15:13	Reserved	RO	Reserved	0x0
12	INV_AD_9	RW	SAR ADC output flip enable (configure channel9,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: no flip 1: flip	0x0
11	EN_PGA_9	RW	PGA enable switch (configure channel9,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: disable 1: enable	0x0

10	PD_PGA1_9	RW	First level of PGA enable switch (configure channel9,16channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
9	PD_PGA2_9	RW	second level of PGA enable switch (configure channel9,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
8	PD_FILTER_9	RW	turn off the PGA2 filter (configure channel9,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: turn on 1: turn off	0x0
7	Reserved	RO	Reserved	0x0
6:4	GAIN_PGA1_9	RW	First level of PGA gain selection(configure channel9,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256 0b110: 256 0b111: 256	0x2
3	Reserved	RO	Reserved	0x0
2:0	GAIN_PGA2_9	RW	second level of PGA gain selection(configure channel9,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

DACH9CR: (Offset 128h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13	EN_DAC_CAL_9	RW	enable digital DAC calibration loop operation(configure channel9,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0

12	EN_DAC_9	RW	enable calibration offset DAC (configure channel9,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0
11	EN_DAC_VIN_9	RW	turn on DAC negative current input(configure channel9,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: turn off 1: turn on	0x1
10	DIR_DAC_9	RW	DAC direction select (configure channel9,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable current direction 1: enable current direction	0x0
9	DIR_MODE0_9	RW	DAC direction select (configure channel9,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offset 1: enable affect offset	0x0
8	DIR_MODE1_9	RW	DAC direction select (configure channel9,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offsef 1: enable affect offset	0x1
7:2	Reserved	RO	Reserved	0x0
1:0	VDAC_RANGE_9	RW	DAC calibration offset range (configure channel9,16 channels in total,the channel offset address is 0x20*channel +0x8) 0b00: ±0.540*VS/3 0b01: ±0.540*VS/4 0b10: ±0.540*VS/5 0b11: ±0.540*VS/6	0x0

DACH9DR: (Offset 12Ch)

Bit	Symbol	R/W	Description	Default
31:30	Reserved	RO	Reserved	0x0
29:16	AD_OS_9	RW	ADC OFFSET residual.directly save the Adc result,that is, the ADC code, and convert it to two's complement operation when used (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0
15:12	Reserved	RO	Reserved	0x0
11:0	DA_9	RW	D/A data register (configure channel9,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0

ADCH9DR: (Offset 130h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13:0	ADDR_9	RO	channel 9 value(configure channel9,16 channels in total,the channel offset address is 0x20*channel +0x10)	0x0

ADCH10CR0: (Offset 140h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:29	Reserved	RO	Reserved	0x0
28:24	SP_MUX_10	RW	Positive terminal of DC voltage channel.(configure channel10,16 channels in total,the channel offset address is 0x20) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
23:21	Reserved	RO	Reserved	0x0
20:16	SN_MUX_10	RW	negative terminal of DC voltage channel.(configure channel10,16 channels in total,the channel offset address is 0x20) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
15	RED_OS_10	RW	offset Residual cancellation enable signal (configure channel10, 16channels in total,the channel offset address is 0x20) 0: no elimination of residuals 1: elimination of residuals	0x0
14	DMOF_10	RW	differential input mode output format(configure channel10,16 channels in total,the channel offset address is 0x20) 0: original code of result 1: complement of result	0x0
13	PD_DOUBLE_VIN_10	RW	in ADC single-ended mode, turn off the double-ended input (configure channel10,16 channels in total,the channel offset address is 0x20) 0: double-ended input 1: single-ended input	0x1
12	EN_DIFF_10	RW	ADC input working mode (configure channel10,15 channels in total,the channel offset address is 0x20) 0: single-ended mode 1: differential mode	0x1
11:8	PD_SW_IN_10	RW	PA3-PA0 analog switch control (configure channel10,16 channels in total,the channel offset address is 0x20) 0: strobe vs 1: disable	0xF

7:4	PD_AINP_10	RW	CHx sensor positive input selection (configure channel10,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 positive 0b0001: sensor1 positive 0b0010: sensor2 positive 0b0011: sensor3 positive 0b0100: sensor4 positive 0b0101: sensor5 positive 0b0110: sensor6 positive 0b0111: sensor7 positive 0b1000: sensor8 positive 0b1001: sensor9 positive 0b1010: sensor10 positive 0b1011:sensor11 positive	0xF
3:0	PD_AINN_10	RW	CHx sensor negative input selection (configure channel10,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 negative 0b0001: sensor1 negative 0b0010: sensor2 negative 0b0011: sensor3 negative 0b0100: sensor4 negative 0b0101: sensor5 negative 0b0110: sensor6 negative 0b0111: sensor7 negative 0b1000: sensor8 negative 0b1001: sensor9 negative 0b1010: sensor10 negative 0b1011:sensor11 negative	0xF

ADCH10CR1: (Offset 144h)

Bit	Symbol	R/W	Description	Default
31	Reserved	RO	Reserved	0x0
30:28	PGA_IBIASE_10	RW	PGA module overall current selection(configure channel10,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1μA 0b001: 1.25μA 0b010: 1.5μA 0b011: 1.75μA 0b100: 2μA 0b101: 2.25μA 0b110: 2.5μA 0b111: 2.75μA	0x4
27	Reserved	RO	Reserved	0x0

26:24	BW_FILTER_10	RW	PGA RC filter output frequency selection(configure channel10,16channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 125kHz 0b001: 250kHz 0b010: 167kHz 0b011: 500kHz 0b100: 143kHz 0b101: 333kHz 0b110: 200kHz 0b111: 1000kHz	0x3
23:22	VREF_SEL_10	RW	VRP voltage selection(configure channel10,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b00: 2.4v 0b01: 2.8v 0b10: 3.0v 0b11: 3.1v	0x1
21	VREF_GEN_SEL_10	RW	ADC refrence voltage selection(configure channel10,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: AVDD 1: VRP	0x1
20	VCM_ADJ_10	RW	PGA output common mode voltage selection(configure channel10,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: 0.5*AVDD 1: 0.5*AVDD-0.1	0x0
19	Reserved	RO	Reserved	0x0
18:16	ADC_IBIAS_10	RW	ADC BIAS current control(configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 2μA 0b001: 2.5μA 0b010: 3μA 0b011: 3.5μA 0b100: 4μA 0b101: 4.5μA 0b110: 5μA 0b111: 5.5μA	0x4
15:13	Reserved	RO	Reserved	0x0
12	INV_AD_10	RW	SAR ADC output flip enable (configure channel10,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: no flip 1: flip	0x0
11	EN_PGA_10	RW	PGA enable switch (configure channel10,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: disable 1: enable	0x0

10	PD_PGA1_10	RW	First level of PGA enable switch (configure channel10,16channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
9	PD_PGA2_10	RW	second level of PGA enable switch (configure channel10,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
8	PD_FILTER_10	RW	turn off the PGA2 filter (configure channel10,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: turn on 1: turn off	0x0
7	Reserved	RO	Reserved	0x0
6:4	GAIN_PGA1_10	RW	First level of PGA gain selection(configure channel10,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256 0b110: 256 0b111: 256	0x2
3	Reserved	RO	Reserved	0x0
2:0	GAIN_PGA2_10	RW	second level of PGA gain selection(configure channel10,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

DACH10CR: (Offset 148h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13	EN_DAC_CAL_10	RW	enable digital DAC calibration loop operation(configure channel10,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0

12	EN_DAC_10	RW	enable calibration offset DAC (configure channel10,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0
11	EN_DAC_VIN_10	RW	turn on DAC negative current input(configure channel10,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: turn off 1: turn on	0x1
10	DIR_DAC_10	RW	DAC direction select (configure channel10,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable current direction 1: enable current direction	0x0
9	DIR_MODE0_10	RW	DAC direction select (configure channel10,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offset 1: enable affect offset	0x0
8	DIR_MODE1_10	RW	DAC direction select (configure channel10,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offsef 1: enable affect offset	0x1
7:2	Reserved	RO	Reserved	0x0
1:0	VDAC_RANGE_10	RW	DAC calibration offset range (configure channel10,16 channels in total,the channel offset address is 0x20*channel +0x8) 0b00: ±0.540*VS/3 0b01: ±0.540*VS/4 0b10: ±0.540*VS/5 0b11: ±0.540*VS/6	0x0

DACH10DR: (Offset 14Ch)

Bit	Symbol	R/W	Description	Default
31:30	Reserved	RO	Reserved	0x0
29:16	AD_OS_10	RW	ADC OFFSET residual.directly save the Adc result,that is, the ADC code, and convert it to two's complement operation when used (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0
15:12	Reserved	RO	Reserved	0x0
11:0	DA_10	RW	D/A data register (configure channel10,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0

ADCH10DR: (Offset 150h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13:0	ADDR_10	RO	channel 10 value(configure channel10,16 channels in total,the channel offset address is 0x20*channel +0x10)	0x0

ADCH11CR0: (Offset 160h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:29	Reserved	RO	Reserved	0x0
28:24	SP_MUX_11	RW	Positive terminal of DC voltage channel.(configure channel11,16 channels in total,the channel offset address is 0x20) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
23:21	Reserved	RO	Reserved	0x0
20:16	SN_MUX_11	RW	negative terminal of DC voltage channel.(configure channel11,16 channels in total,the channel offset address is 0x20) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
15	RED_OS_11	RW	offset Residual cancellation enable signal (configure channel11, 16channels in total,the channel offset address is 0x20) 0: no elimination of residuals 1: elimination of residuals	0x0
14	DMOF_11	RW	differential input mode output format(configure channel11,16 channels in total,the channel offset address is 0x20) 0: original code of result 1: complement of result	0x0
13	PD_DOUBLE_VIN_11	RW	in ADC single-ended mode, turn off the double-ended input (configure channel11,16 channels in total,the channel offset address is 0x20) 0: double-ended input 1: single-ended input	0x1
12	EN_DIFF_11	RW	ADC input working mode (configure channel11,15 channels in total,the channel offset address is 0x20) 0: single-ended mode 1: differential mode	0x1
11:8	PD_SW_IN_11	RW	PA3-PA0 analog switch control (configure channel11,16 channels in total,the channel offset address is 0x20) 0: strobe vs 1: disable	0xF

7:4	PD_AINP_11	RW	CHx sensor positive input selection (configure channel11,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 positive 0b0001: sensor1 positive 0b0010: sensor2 positive 0b0011: sensor3 positive 0b0100: sensor4 positive 0b0101: sensor5 positive 0b0110: sensor6 positive 0b0111: sensor7 positive 0b1000: sensor8 positive 0b1001: sensor9 positive 0b1010: sensor10 positive 0b1011:sensor11 positive	0xF
3:0	PD_AINN_11	RW	CHx sensor negative input selection (configure channel11,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 negative 0b0001: sensor1 negative 0b0010: sensor2 negative 0b0011: sensor3 negative 0b0100: sensor4 negative 0b0101: sensor5 negative 0b0110: sensor6 negative 0b0111: sensor7 negative 0b1000: sensor8 negative 0b1001: sensor9 negative 0b1010: sensor10 negative 0b1011:sensor11 negative	0xF

ADCH11CR1: (Offset 164h)

Bit	Symbol	R/W	Description	Default
31	Reserved	RO	Reserved	0x0
30:28	PGA_IBIASE_11	RW	PGA module overall current selection(configure channel11,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1μA 0b001: 1.25μA 0b010: 1.5μA 0b011: 1.75μA 0b100: 2μA 0b101: 2.25μA 0b110: 2.5μA 0b111: 2.75μA	0x4
27	Reserved	RO	Reserved	0x0

26:24	BW_FILTER_11	RW	PGA RC filter output frequency selection(configure channel11,16channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 125kHz 0b001: 250kHz 0b010: 167kHz 0b011: 500kHz 0b100: 143kHz 0b101: 333kHz 0b110: 200kHz 0b111: 1000kHz	0x3
23:22	VREF_SEL_11	RW	VRP voltage selection(configure channel11,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b00: 2.4v 0b01: 2.8v 0b10: 3.0v 0b11: 3.1v	0x1
21	VREF_GEN_SEL_11	RW	ADC refrence voltage selection(configure channel11,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: AVDD 1: VRP	0x1
20	VCM_ADJ_11	RW	PGA output common mode voltage selection(configure channel11,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: 0.5*AVDD 1: 0.5*AVDD-0.1	0x0
19	Reserved	RO	Reserved	0x0
18:16	ADC_IBIAS_11	RW	ADC BIAS current control(configure channel11,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 2μA 0b001: 2.5μA 0b010: 3μA 0b011: 3.5μA 0b100: 4μA 0b101: 4.5μA 0b110: 5μA 0b111: 5.5μA	0x4
15:13	Reserved	RO	Reserved	0x0
12	INV_AD_11	RW	SAR ADC output flip enable (configure channel11,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: no flip 1: flip	0x0
11	EN_PGA_11	RW	PGA enable switch (configure channel11,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: disable 1: enable	0x0

10	PD_PGA1_11	RW	First level of PGA enable switch (configure channel11,16channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
9	PD_PGA2_11	RW	second level of PGA enable switch (configure channel11,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
8	PD_FILTER_11	RW	turn off the PGA2 filter (configure channel11,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: turn on 1: turn off	0x0
7	Reserved	RO	Reserved	0x0
6:4	GAIN_PGA1_11	RW	First level of PGA gain selection(configure channel11,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256 0b110: 256 0b111: 256	0x2
3	Reserved	RO	Reserved	0x0
2:0	GAIN_PGA2_11	RW	second level of PGA gain selection(configure channel11,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

DACH11CR: (Offset 168h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13	EN_DAC_CAL_11	RW	enable digital DAC calibration loop operation(configure channel11,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0

12	EN_DAC_11	RW	enable calibration offset DAC (configure channel11,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0
11	EN_DAC_VIN_11	RW	turn on DAC negative current input(configure channel11,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: turn off 1: turn on	0x1
10	DIR_DAC_11	RW	DAC direction select (configure channel11,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable current direction 1: enable current direction	0x0
9	DIR_MODE0_11	RW	DAC direction select (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offset 1: enable affect offset	0x0
8	DIR_MODE1_11	RW	DAC direction select (configure channel11,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offsef 1: enable affect offset	0x1
7:2	Reserved	RO	Reserved	0x0
1:0	VDAC_RANGE_11	RW	DAC calibration offset range (configure channel11,16 channels in total,the channel offset address is 0x20*channel +0x8) 0b00: ±0.540*VS/3 0b01: ±0.540*VS/4 0b10: ±0.540*VS/5 0b11: ±0.540*VS/6	0x0

DACH11DR: (Offset 16Ch)

Bit	Symbol	R/W	Description	Default
31:30	Reserved	RO	Reserved	0x0
29:16	AD_OS_11	RW	ADC OFFSET residual.directly save the Adc result,that is, the ADC code, and convert it to two's complement operation when used (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0
15:12	Reserved	RO	Reserved	0x0
11:0	DA_11	RW	D/A data register (configure channel11,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0

ADCH11DR: (Offset 170h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13:0	ADDR_11	RO	channel 11 value(configure channel11,16 channels in total,the channel offset address is 0x20*channel +0x10)	0x0

ADCH12CR0: (Offset 180h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:29	Reserved	RO	Reserved	0x0
28:24	SP_MUX_12	RW	Positive terminal of DC voltage channel.(configure channel12,16 channels in total,the channel offset address is 0x20) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
23:21	Reserved	RO	Reserved	0x0
20:16	SN_MUX_12	RW	negative terminal of DC voltage channel.(configure channel12,16 channels in total,the channel offset address is 0x20) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
15	RED_OS_12	RW	offset Residual cancellation enable signal (configure channel12,16channels in total,the channel offset address is 0x20) 0: no elimination of residuals 1: elimination of residuals	0x0
14	DMOF_12	RW	differential input mode output format(configure channel12,16 channels in total,the channel offset address is 0x20) 0: original code of result 1: complement of result	0x0
13	PD_DOUBLE_VIN_12	RW	in ADC single-ended mode, turn off the double-ended input (configure channel12,16 channels in total,the channel offset address is 0x20) 0: double-ended input 1: single-ended input	0x1
12	EN_DIFF_12	RW	ADC input working mode (configure channel12,15 channels in total,the channel offset address is 0x20) 0: single-ended mode 1: differential mode	0x1
11:8	PD_SW_IN_12	RW	PA3-PA0 analog switch control (configure channel12,16 channels in total,the channel offset address is 0x20) 0: strobe vs 1: disable	0xF

7:4	PD_AINP_12	RW	CHx sensor positive input selection (configure channel12,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 positive 0b0001: sensor1 positive 0b0010: sensor2 positive 0b0011: sensor3 positive 0b0100: sensor4 positive 0b0101: sensor5 positive 0b0110: sensor6 positive 0b0111: sensor7 positive 0b1000: sensor8 positive 0b1001: sensor9 positive 0b1010: sensor10 positive 0b1011:sensor11 positive	0xF
3:0	PD_AINN_12	RW	CHx sensor negative input selection (configure channel12,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 negative 0b0001: sensor1 negative 0b0010: sensor2 negative 0b0011: sensor3 negative 0b0100: sensor4 negative 0b0101: sensor5 negative 0b0110: sensor6 negative 0b0111: sensor7 negative 0b1000: sensor8 negative 0b1001: sensor9 negative 0b1010: sensor10 negative 0b1011:sensor11 negative	0xF

ADCH12CR1: (Offset 184h)

Bit	Symbol	R/W	Description	Default
31	Reserved	RO	Reserved	0x0
30:28	PGA_IBIASE_12	RW	PGA module overall current selection(configure channel12,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1μA 0b001: 1.25μA 0b010: 1.5μA 0b011: 1.75μA 0b100: 2μA 0b101: 2.25μA 0b110: 2.5μA 0b111: 2.75μA	0x4
27	Reserved	RO	Reserved	0x0

26:24	BW_FILTER_12	RW	PGA RC filter output frequency selection(configure channel12,16channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 125kHz 0b001: 250kHz 0b010: 167kHz 0b011: 500kHz 0b100: 143kHz 0b101: 333kHz 0b110: 200kHz 0b111: 1000kHz	0x3
23:22	VREF_SEL_12	RW	VRP voltage selection(configure channel12,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b00: 2.4v 0b01: 2.8v 0b10: 3.0v 0b11: 3.1v	0x1
21	VREF_GEN_SEL_12	RW	ADC refrence voltage selection(configure channel12,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: AVDD 1: VRP	0x1
20	VCM_ADJ_12	RW	PGA output common mode voltage selection(configure channel12,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: 0.5*AVDD 1: 0.5*AVDD-0.1	0x0
19	Reserved	RO	Reserved	0x0
18:16	ADC_IBIAS_12	RW	ADC BIAS current control(configure channel12,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 2μA 0b001: 2.5μA 0b010: 3μA 0b011: 3.5μA 0b100: 4μA 0b101: 4.5μA 0b110: 5μA 0b111: 5.5μA	0x4
15:13	Reserved	RO	Reserved	0x0
12	INV_AD_12	RW	SAR ADC output flip enable (configure channel12,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: no flip 1: flip	0x0
11	EN_PGA_12	RW	PGA enable switch (configure channel12,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: disable 1: enable	0x0

10	PD_PGA1_12	RW	First level of PGA enable switch (configure channel12,16channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
9	PD_PGA2_12	RW	second level of PGA enable switch (configure channel12,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
8	PD_FILTER_12	RW	turn off the PGA2 filter (configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: turn on 1: turn off	0x0
7	Reserved	RO	Reserved	0x0
6:4	GAIN_PGA1_12	RW	First level of PGA gain selection(configure channel12,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256 0b110: 256 0b111: 256	0x2
3	Reserved	RO	Reserved	0x0
2:0	GAIN_PGA2_12	RW	second level of PGA gain selection(configure channel12,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

DACH12CR: (Offset 188h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13	EN_DAC_CAL_12	RW	enable digital DAC calibration loop operation(configure channel12,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0

12	EN_DAC_12	RW	enable calibration offset DAC (configure channel12,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0
11	EN_DAC_VIN_12	RW	turn on DAC negative current input(configure channel12,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: turn off 1: turn on	0x1
10	DIR_DAC_12	RW	DAC direction select (configure channel12,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable current direction 1: enable current direction	0x0
9	DIR_MODE0_12	RW	DAC direction select (configure channel12,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offset 1: enable affect offset	0x0
8	DIR_MODE1_12	RW	DAC direction select (configure channel12,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offsef 1: enable affect offset	0x1
7:2	Reserved	RO	Reserved	0x0
1:0	VDAC_RANGE_12	RW	DAC calibration offset range (configure channel12,16 channels in total,the channel offset address is 0x20*channel +0x8) 0b00: ±0.540*VS/3 0b01: ±0.540*VS/4 0b10: ±0.540*VS/5 0b11: ±0.540*VS/6	0x0

DACH12DR: (Offset 18Ch)

Bit	Symbol	R/W	Description	Default
31:30	Reserved	RO	Reserved	0x0
29:16	AD_OS_12	RW	ADC OFFSET residual.directly save the Adc result,that is, the ADC code, and convert it to two's complement operation when used (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0
15:12	Reserved	RO	Reserved	0x0
11:0	DA_12	RW	D/A data register (configure channel12,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0

ADCH12DR: (Offset 190h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13:0	ADDR_12	RO	channel 12 value(configure channel12,16 channels in total,the channel offset address is 0x20*channel +0x10)	0x0

ADCH13CR0: (Offset 1A0h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:29	Reserved	RO	Reserved	0x0
28:24	SP_MUX_13	RW	Positive terminal of DC voltage channel.(configure channel13,16 channels in total,the channel offset address is 0x20) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
23:21	Reserved	RO	Reserved	0x0
20:16	SN_MUX_13	RW	negative terminal of DC voltage channel.(configure channel13,16 channels in total,the channel offset address is 0x20) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
15	RED_OS_13	RW	offset Residual cancellation enable signal (configure channel13,16channels in total,the channel offset address is 0x20) 0: no elimination of residuals 1: elimination of residuals	0x0
14	DMOF_13	RW	differential input mode output format(configure channel13,16 channels in total,the channel offset address is 0x20) 0: original code of result 1: complement of result	0x0
13	PD_DOUBLE_VIN_13	RW	in ADC single-ended mode, turn off the double-ended input (configure channel13,16 channels in total,the channel offset address is 0x20) 0: double-ended input 1: single-ended input	0x1
12	EN_DIFF_13	RW	ADC input working mode (configure channel13,15 channels in total,the channel offset address is 0x20) 0: single-ended mode 1: differential mode	0x1
11:8	PD_SW_IN_13	RW	PA3-PA0 analog switch control (configure channel13,16 channels in total,the channel offset address is 0x20) 0: strobe vs 1: disable	0xF

7:4	PD_AINP_13	RW	CHx sensor positive input selection (configure channel13,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 positive 0b0001: sensor1 positive 0b0010: sensor2 positive 0b0011: sensor3 positive 0b0100: sensor4 positive 0b0101: sensor5 positive 0b0110: sensor6 positive 0b0111: sensor7 positive 0b1000: sensor8 positive 0b1001: sensor9 positive 0b1010: sensor10 positive 0b1011:sensor11 positive	0xF
3:0	PD_AINN_13	RW	CHx sensor negative input selection (configure channel13,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 negative 0b0001: sensor1 negative 0b0010: sensor2 negative 0b0011: sensor3 negative 0b0100: sensor4 negative 0b0101: sensor5 negative 0b0110: sensor6 negative 0b0111: sensor7 negative 0b1000: sensor8 negative 0b1001: sensor9 negative 0b1010: sensor10 negative 0b1011:sensor11 negative	0xF

ADCH13CR1: (Offset 1A4h)

Bit	Symbol	R/W	Description	Default
31	Reserved	RO	Reserved	0x0
30:28	PGA_IBIASE_13	RW	PGA module overall current selection(configure channel13,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1μA 0b001: 1.25μA 0b010: 1.5μA 0b011: 1.75μA 0b100: 2μA 0b101: 2.25μA 0b110: 2.5μA 0b111: 2.75μA	0x4
27	Reserved	RO	Reserved	0x0

26:24	BW_FILTER_13	RW	PGA RC filter output frequency selection(configure channel13,16channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 125kHz 0b001: 250kHz 0b010: 167kHz 0b011: 500kHz 0b100: 143kHz 0b101: 333kHz 0b110: 200kHz 0b111: 1000kHz	0x3
23:22	VREF_SEL_13	RW	VRP voltage selection(configure channel13,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b00: 2.4v 0b01: 2.8v 0b10: 3.0v 0b11: 3.1v	0x1
21	VREF_GEN_SEL_13	RW	ADC refrence voltage selection(configure channel13,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: AVDD 1: VRP	0x1
20	VCM_ADJ_13	RW	PGA output common mode voltage selection(configure channel13,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: 0.5*AVDD 1: 0.5*AVDD-0.1	0x0
19	Reserved	RO	Reserved	0x0
18:16	ADC_IBIAS_13	RW	ADC BIAS current control(configure channel13,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 2μA 0b001: 2.5μA 0b010: 3μA 0b011: 3.5μA 0b100: 4μA 0b101: 4.5μA 0b110: 5μA 0b111: 5.5μA	0x4
15:13	Reserved	RO	Reserved	0x0
12	INV_AD_13	RW	SAR ADC output flip enable (configure channel13,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: no flip 1: flip	0x0
11	EN_PGA_13	RW	PGA enable switch (configure channel13,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: disable 1: enable	0x0

10	PD_PGA1_13	RW	First level of PGA enable switch (configure channel13,16channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
9	PD_PGA2_13	RW	second level of PGA enable switch (configure channel13,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
8	PD_FILTER_13	RW	turn off the PGA2 filter (configure channel13,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: turn on 1: turn off	0x0
7	Reserved	RO	Reserved	0x0
6:4	GAIN_PGA1_13	RW	First level of PGA gain selection(configure channel13,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256 0b110: 256 0b111: 256	0x2
3	Reserved	RO	Reserved	0x0
2:0	GAIN_PGA2_13	RW	second level of PGA gain selection(configure channel13,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

DACH13CR: (Offset 1A8h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13	EN_DAC_CAL_13	RW	enable digital DAC calibration loop operation(configure channel13,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0

12	EN_DAC_13	RW	enable calibration offset DAC (configure channel13,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0
11	EN_DAC_VIN_13	RW	turn on DAC negative current input(configure channel13,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: turn off 1: turn on	0x1
10	DIR_DAC_13	RW	DAC direction select (configure channel13,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable current direction 1: enable current direction	0x0
9	DIR_MODE0_13	RW	DAC direction select (configure channel13,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offset 1: enable affect offset	0x0
8	DIR_MODE1_13	RW	DAC direction select (configure channel13,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offsef 1: enable affect offset	0x1
7:2	Reserved	RO	Reserved	0x0
1:0	VDAC_RANGE_13	RW	DAC calibration offset range (configure channel13,16 channels in total,the channel offset address is 0x20*channel +0x8) 0b00: ±0.540*VS/3 0b01: ±0.540*VS/4 0b10: ±0.540*VS/5 0b11: ±0.540*VS/6	0x0

DACH13DR: (Offset 1ACh)

Bit	Symbol	R/W	Description	Default
31:30	Reserved	RO	Reserved	0x0
29:16	AD_OS_13	RW	ADC OFFSET residual.directly save the Adc result,that is, the ADC code, and convert it to two's complement operation when used (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0
15:12	Reserved	RO	Reserved	0x0
11:0	DA_13	RW	D/A data register (configure channel13,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0

ADCH13DR: (Offset 1B0h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13:0	ADDR_13	RO	channel 13 value(configure channel13,16 channels in total,the channel offset address is 0x20*channel +0x10)	0x0

ADCH14CR0: (Offset 1C0h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:29	Reserved	RO	Reserved	0x0
28:24	SP_MUX_14	RW	Positive terminal of DC voltage channel.(configure channel14,16 channels in total,the channel offset address is 0x20) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
23:21	Reserved	RO	Reserved	0x0
20:16	SN_MUX_14	RW	negative terminal of DC voltage channel.(configure channel14,16 channels in total,the channel offset address is 0x20) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
15	RED_OS_14	RW	offset Residual cancellation enable signal (configure channel14, 16channels in total,the channel offset address is 0x20) 0: no elimination of residuals 1: elimination of residuals	0x0
14	DMOF_14	RW	differential input mode output format(configure channel14,16 channels in total,the channel offset address is 0x20) 0: original code of result 1: complement of result	0x0
13	PD_DOUBLE_VIN_14	RW	in ADC single-ended mode, turn off the double-ended input (configure channel14,16 channels in total,the channel offset address is 0x20) 0: double-ended input 1: single-ended input	0x1
12	EN_DIFF_14	RW	ADC input working mode (configure channel14,15 channels in total,the channel offset address is 0x20) 0: single-ended mode 1: differential mode	0x1
11:8	PD_SW_IN_14	RW	PA3-PA0 analog switch control (configure channel14,16 channels in total,the channel offset address is 0x20) 0: strobe vs 1: disable	0xF

7:4	PD_AINP_14	RW	CHx sensor positive input selection (configure channel14,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 positive 0b0001: sensor1 positive 0b0010: sensor2 positive 0b0011: sensor3 positive 0b0100: sensor4 positive 0b0101: sensor5 positive 0b0110: sensor6 positive 0b0111: sensor7 positive 0b1000: sensor8 positive 0b1001: sensor9 positive 0b1010: sensor10 positive 0b1011:sensor11 positive	0xF
3:0	PD_AINN_14	RW	CHx sensor negative input selection (configure channel14,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 negative 0b0001: sensor1 negative 0b0010: sensor2 negative 0b0011: sensor3 negative 0b0100: sensor4 negative 0b0101: sensor5 negative 0b0110: sensor6 negative 0b0111: sensor7 negative 0b1000: sensor8 negative 0b1001: sensor9 negative 0b1010: sensor10 negative 0b1011:sensor11 negative	0xF

ADCH14CR1: (Offset 1C4h)

Bit	Symbol	R/W	Description	Default
31	Reserved	RO	Reserved	0x0
30:28	PGA_IBIASE_14	RW	PGA module overall current selection(configure channel14,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1μA 0b001: 1.25μA 0b010: 1.5μA 0b011: 1.75μA 0b100: 2μA 0b101: 2.25μA 0b110: 2.5μA 0b111: 2.75μA	0x4
27	Reserved	RO	Reserved	0x0

26:24	BW_FILTER_14	RW	PGA RC filter output frequency selection(configure channel14,16channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 125kHz 0b001: 250kHz 0b010: 167kHz 0b011: 500kHz 0b100: 143kHz 0b101: 333kHz 0b110: 200kHz 0b111: 1000kHz	0x3
23:22	VREF_SEL_14	RW	VRP voltage selection(configure channel14,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b00: 2.4v 0b01: 2.8v 0b10: 3.0v 0b11: 3.1v	0x1
21	VREF_GEN_SEL_14	RW	ADC refrence voltage selection(configure channel14,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: AVDD 1: VRP	0x1
20	VCM_ADJ_14	RW	PGA output common mode voltage selection(configure channel14,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: 0.5*AVDD 1: 0.5*AVDD-0.1	0x0
19	Reserved	RO	Reserved	0x0
18:16	ADC_IBIAS_14	RW	ADC BIAS current control(configure channel14,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 2μA 0b001: 2.5μA 0b010: 3μA 0b011: 3.5μA 0b100: 4μA 0b101: 4.5μA 0b110: 5μA 0b111: 5.5μA	0x4
15:13	Reserved	RO	Reserved	0x0
12	INV_AD_14	RW	SAR ADC output flip enable (configure channel14,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: no flip 1: flip	0x0
11	EN_PGA_14	RW	PGA enable switch (configure channel14,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: disable 1: enable	0x0

10	PD_PGA1_14	RW	First level of PGA enable switch (configure channel14,16channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
9	PD_PGA2_14	RW	second level of PGA enable switch (configure channel14,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
8	PD_FILTER_14	RW	turn off the PGA2 filter (configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: turn on 1: turn off	0x0
7	Reserved	RO	Reserved	0x0
6:4	GAIN_PGA1_14	RW	First level of PGA gain selection(configure channel14,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256 0b110: 256 0b111: 256	0x2
3	Reserved	RO	Reserved	0x0
2:0	GAIN_PGA2_14	RW	second level of PGA gain selection(configure channel14,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

DACH14CR: (Offset 1C8h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13	EN_DAC_CAL_14	RW	enable digital DAC calibration loop operation(configure channel14,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0

12	EN_DAC_14	RW	enable calibration offset DAC (configure channel14,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0
11	EN_DAC_VIN_14	RW	turn on DAC negative current input(configure channel14,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: turn off 1: turn on	0x1
10	DIR_DAC_14	RW	DAC direction select (configure channel14,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable current direction 1: enable current direction	0x0
9	DIR_MODE0_14	RW	DAC direction select (configure channel14,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offset 1: enable affect offset	0x0
8	DIR_MODE1_14	RW	DAC direction select (configure channel14,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offsef 1: enable affect offset	0x1
7:2	Reserved	RO	Reserved	0x0
1:0	VDAC_RANGE_14	RW	DAC calibration offset range (configure channel14,16 channels in total,the channel offset address is 0x20*channel +0x8) 0b00: ±0.540*VS/3 0b01: ±0.540*VS/4 0b10: ±0.540*VS/5 0b11: ±0.540*VS/6	0x0

DACH14DR: (Offset 1CCh)

Bit	Symbol	R/W	Description	Default
31:30	Reserved	RO	Reserved	0x0
29:16	AD_OS_14	RW	ADC OFFSET residual.directly save the Adc result,that is, the ADC code, and convert it to two's complement operation when used (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0
15:12	Reserved	RO	Reserved	0x0
11:0	DA_14	RW	D/A data register (configure channel14,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0

ADCH14DR: (Offset 1D0h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13:0	ADDR_14	RO	channel 14 value(configure channel14,16 channels in total,the channel offset address is 0x20*channel +0x10)	0x0

ADCH15CR0: (Offset 1E0h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:29	Reserved	RO	Reserved	0x0
28:24	SP_MUX_15	RW	Positive terminal of DC voltage channel.(configure channel15,16 channels in total,the channel offset address is 0x20) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
23:21	Reserved	RO	Reserved	0x0
20:16	SN_MUX_15	RW	negative terminal of DC voltage channel.(configure channel15,16 channels in total,the channel offset address is 0x20) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vs/2	0x0
15	RED_OS_15	RW	offset Residual cancellation enable signal (configure channel15, 16channels in total,the channel offset address is 0x20) 0: no elimination of residuals 1: elimination of residuals	0x0
14	DMOF_15	RW	differential input mode output format(configure channel15,16 channels in total,the channel offset address is 0x20) 0: original code of result 1: complement of result	0x0
13	PD_DOUBLE_VIN_15	RW	in ADC single-ended mode, turn off the double-ended input (configure channel15,16 channels in total,the channel offset address is 0x20) 0: double-ended input 1: single-ended input	0x1
12	EN_DIFF_15	RW	ADC input working mode (configure channel15,15 channels in total,the channel offset address is 0x20) 0: single-ended mode 1: differential mode	0x1
11:8	PD_SW_IN_15	RW	PA3-PA0 analog switch control (configure channel15,16 channels in total,the channel offset address is 0x20) 0: strobe vs 1: disable	0xF

7:4	PD_AINP_15	RW	CHx sensor positive input selection (configure channel15,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 positive 0b0001: sensor1 positive 0b0010: sensor2 positive 0b0011: sensor3 positive 0b0100: sensor4 positive 0b0101: sensor5 positive 0b0110: sensor6 positive 0b0111: sensor7 positive 0b1000: sensor8 positive 0b1001: sensor9 positive 0b1010: sensor10 positive 0b1011:sensor11 positive	0xF
3:0	PD_AINN_15	RW	CHx sensor negative input selection (configure channel15,16 channels in total,the channel offset address is 0x20) 0b0000: sensor0 negative 0b0001: sensor1 negative 0b0010: sensor2 negative 0b0011: sensor3 negative 0b0100: sensor4 negative 0b0101: sensor5 negative 0b0110: sensor6 negative 0b0111: sensor7 negative 0b1000: sensor8 negative 0b1001: sensor9 negative 0b1010: sensor10 negative 0b1011:sensor11 negative	0xF

ADCH15CR1: (Offset 1E4h)

Bit	Symbol	R/W	Description	Default
31	Reserved	RO	Reserved	0x0
30:28	PGA_IBIASE_15	RW	PGA module overall current selection(configure channel15,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1μA 0b001: 1.25μA 0b010: 1.5μA 0b011: 1.75μA 0b100: 2μA 0b101: 2.25μA 0b110: 2.5μA 0b111: 2.75μA	0x4
27	Reserved	RO	Reserved	0x0

26:24	BW_FILTER_15	RW	PGA RC filter output frequency selection(configure channel15,16channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 125kHz 0b001: 250kHz 0b010: 167kHz 0b011: 500kHz 0b100: 143kHz 0b101: 333kHz 0b110: 200kHz 0b111: 1000kHz	0x3
23:22	VREF_SEL_15	RW	VRP voltage selection(configure channel15,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b00: 2.4v 0b01: 2.8v 0b10: 3.0v 0b11: 3.1v	0x1
21	VREF_GEN_SEL_15	RW	ADC refrence voltage selection(configure channel15,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: AVDD 1: VRP	0x1
20	VCM_ADJ_15	RW	PGA output common mode voltage selection(configure channel15,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: 0.5*AVDD 1: 0.5*AVDD-0.1	0x0
19	Reserved	RO	Reserved	0x0
18:16	ADC_IBIAS_15	RW	ADC BIAS current control(configure channel15,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 2μA 0b001: 2.5μA 0b010: 3μA 0b011: 3.5μA 0b100: 4μA 0b101: 4.5μA 0b110: 5μA 0b111: 5.5μA	0x4
15:13	Reserved	RO	Reserved	0x0
12	INV_AD_15	RW	SAR ADC output flip enable (configure channel15,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: no flip 1: flip	0x0
11	EN_PGA_15	RW	PGA enable switch (configure channel15,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: disable 1: enable	0x0

10	PD_PGA1_15	RW	First level of PGA enable switch (configure channel15,16channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
9	PD_PGA2_15	RW	second level of PGA enable switch (configure channel15,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: enable 1: disable	0x0
8	PD_FILTER_15	RW	turn off the PGA2 filter (configure channel0,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0: turn on 1: turn off	0x0
7	Reserved	RO	Reserved	0x0
6:4	GAIN_PGA1_15	RW	First level of PGA gain selection(configure channel15,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256 0b110: 256 0b111: 256	0x2
3	Reserved	RO	Reserved	0x0
2:0	GAIN_PGA2_15	RW	second level of PGA gain selection(configure channel15,16 channels in total,the channel offset address is 0x20 *channel +0x4) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

DACH15CR: (Offset 1E8h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13	EN_DAC_CAL_15	RW	enable digital DAC calibration loop operation(configure channel15,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0

12	EN_DAC_15	RW	enable calibration offset DAC (configure channel15,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable 1: enable	0x0
11	EN_DAC_VIN_15	RW	turn on DAC negative current input(configure channel15,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: turn off 1: turn on	0x1
10	DIR_DAC_15	RW	DAC direction select (configure channel15,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable current direction 1: enable current direction	0x0
9	DIR_MODE0_15	RW	DAC direction select (configure channel15,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offset 1: enable affect offset	0x0
8	DIR_MODE1_15	RW	DAC direction select (configure channel15,16 channels in total,the channel offset address is 0x20*channel +0x8) 0: disable affect offsef 1: enable affect offset	0x1
7:2	Reserved	RO	Reserved	0x0
1:0	VDAC_RANGE_15	RW	DAC calibration offset range (configure channel15,16 channels in total,the channel offset address is 0x20*channel +0x8) 0b00: ±0.540*VS/3 0b01: ±0.540*VS/4 0b10: ±0.540*VS/5 0b11: ±0.540*VS/6	0x0

DACH15DR: (Offset 1ECh)

Bit	Symbol	R/W	Description	Default
31:30	Reserved	RO	Reserved	0x0
29:16	AD_OS_15	RW	ADC OFFSET residual.directly save the Adc result,that is, the ADC code, and convert it to two's complement operation when used (configure channel0,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0
15:12	Reserved	RO	Reserved	0x0
11:0	DA_15	RW	D/A data register (configure channel15,16 channels in total,the channel offset address is 0x20*channel +0xC)	0x0

ADCH15DR: (Offset 1F0h)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	0x0
13:0	ADDR_15	RO	channel 15 value(configure channel15,16 channels in total,the channel offset address is 0x20*channel +0x10)	0x0

ADMCR: (Offset 400h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:24	Reserved	RO	Reserved	0x0
23:20	UNVLD_RS	RW	finite scan mode1 for invalid conversions 0b0000: 0 0b0001: 1 0b0010: 2 0b0011: 3 0b0100: 4 0b0101: 5 0b0110: 6 0b0111: 7 0b1000: 8 0b1001: 9 0b1010: 10 0b1011: 11 0b1100: 12 0b1101: 13 0b1110: 14 0b1111: 15	0x0
19	CAL_S	RW	Selection of operation mode in finite period scan mode 0: direc averaging 1: remove the maximum and minimum values before averaging	0x0
18:16	VALID_NS	RW	finite scan mode2 effective conversions 0b000: 2 0b001: 4 0b010: 8 0b011: 16 0b100: 32 0b101: 64 0b110: 128 0b111: 256 note: in finite period scanning 1 and 2 mode,the ADC data register value is the average of the number of valid conversions N	0x0
15:12	Reserved	RO	Reserved	0x0
11	ADST	RW	A/D conversion begins. ADST will be automatically cleared by hardware after conversion in Single conversion mode and single-cycle scan mode. A/D conversion will continue until the software writes 0 or the system resets in the wireless periodic scan mode. 0: end 1: start	0x0
10:6	Reserved	RO	Reserved	0x0
5	TRGS	RW	A/D conversion trigger source selection. 0: AD conversion is initiated by software ADST 1: AD conversion is initiated by timer	0x0

4:2	ADMD	RW	A/D conversion operation mode control. 0b000: single conversion 0b001: single cycle scan 0b010: finite scan mode1 0b011: finite scan mode2 0b100: infinite scan mode 0b101: burst mode note : software clears ADST bit before changing operation mode	0x0
1	ADIE	RW	A/D interrupt enable control. 0: disable 1: enable	0x0
0	EN_ADC	RW	A/D enable conrol. 0: disable 1: enable	0x0

ADTDR: (Offset 404h)

Bit	Symbol	R/W	Description	Default
31:25	Reserved	RO	Reserved	0x0
24:16	ADC_WAIT	RW	ADC startup wait time(unit is clock period,preferably greater than 1)	0x0
15:8	Reserved	RO	Reserved	0x0
7:0	ETRDT	RW	timer trigger delay time(delay ADC start conversion) T= 16 * ETRDT * PCLK	0x0

ADSR: (Offset 408h)

Bit	Symbol	R/W	Description	Default
31:9	Reserved	RO	Reserved	0x0
8:4	CHANNEL	RO	current conversion channel it indicates the channel being converted when BUSY=1 and indicates the channel to be converted next time when BUSY =1	0x0
3	BUSY	RO	busy/free 0: free 1: busy	0x0
2	CMPF1	RW	comparison flag1 0: no match 1: match	0x0
1	CMPF0	RW	comparison flag0 0: no match 1: match	0x0

0	ADF	RW	end of conversion flag it indicate the end of A/D conversion.write 1 to clear this flag. ADF is set under the following three conditions: 1,at the end of the single conversion mode 2,conversion ends for all specified channels in single scan mode and continuous scan mode 3,in burst mode, the FIFO stores more than 32 conversion result values 0: conversion 1: conversion finish	0x0

ADCMPCR0: (Offset 40Ch)

Bit	Symbol	R/W	Description	Default
31:30	Reserved	RO	Reserved	0x0
29:16	CMPD0	RW	Compare values this 14-bit value will be compared with the conversion result of the specified channel	0x0
15:14	Reserved	RO	Reserved	0x0
13:8	CMPMATCNT0	RW	Compare matches internal counter is incremented by 1 when the conversion value of the specified channel matches the comparision condition CMPCOND[2], the hardware will set the CMPFx when the counter reaches the set value	0x0

7:3	CMPCH0	RW	channel selection 0b00000: channel 0 0b00001: channel 1 0b00010: channel2 0b00011: channel3 0b00100: channel4 0b00101: channel5 0b00110: channel6 0b00111: channel7 0b01000: channel8 0b01001: channel9 0b01010: channel10 0b01011: channel11 0b01100: channel12 0b01101: channel13 0b01110: channel14 0b01111: channel15 0b10000: channel16 0b10001: channel17 0b10010: channel18 0b10011: channel19 0b10100: channel20 0b10101: channel21 0b10110: channel22 0b10111: channel23 0b11000: channel24 0b11001: channel25 0b11010: channel26 0b11011: channel27 0b11100: channel28 0b11101: channel29 0b11110: channel30 0b11111: channel 31	0x0
2	CMPCOND0	RW	Compare condition 0: less than 1: greater than or equal	0x0
1	CMPIE0	RW	Compare interrupt enable 0: disable comparator interrupt 1: enable comparator interrupt	0x0
0	CMPEN0	RW	Compare enable 0: disable comparator 1: enable comparator	0x0

ADCMPCR1: (Offset 410h)

Bit	Symbol	R/W	Description	Default
31:30	Reserved	RO	Reserved	0x0
29:16	CMPD1	RW	Compare values this 14-bit value will be compared with the conversion result of the specified channel	0x0
15:14	Reserved	RO	Reserved	0x0

13:8	CMPMATCNT1	RW	Compare matches internal counter is incremented by 1 when the conversion value of the specified channel matches the comparision condition CMPCOND[2], the hardware will set the CMPFx when the counter reaches the set value	0x0
7:3	CMPCH1	RW	channel selection 0b00000: channel 0 0b00001: channel 1 0b00010: channel2 0b00011: channel3 0b00100: channel4 0b00101: channel5 0b00110: channel6 0b00111: channel7 0b01000: channel8 0b01001: channel9 0b01010: channel10 0b01011: channel11 0b01100: channel12 0b01101: channel13 0b01110: channel14 0b01111: channel15 0b10000: channel16 0b10001: channel17 0b10010: channel18 0b10011: channel19 0b10100: channel20 0b10101: channel21 0b10110: channel22 0b10111: channel23 0b11000: channel24 0b11001: channel25 0b11010: channel26 0b11011: channel27 0b11100: channel28 0b11101: channel29 0b11110: channel30 0b11111: channel 31	0x0
2	CMPCOND1	RW	Compare condition 0: less than 1: greater than or equal	0x0
1	CMPIE1	RW	Compare interrupt enable 0: disable comparator interrupt 1: enable comparator interrupt	0x0
0	CMPEN1	RW	Compare enable 0: disable comparator 1: enable comparator	0x0

ADCHEN: (Offset 414h)

Bit	Symbol	R/W	Description	Default

31:0	ADCH_EN	RW	Channel enable 0: disable 1: enable	0x0

DAOSDR: (Offset 418h)

Bit	Symbol	R/W	Description	Default
31:18	AD_OS	RW	AD offset calibration residual	0x0
17	Reserved	RO	Reserved	0x0
16	DAOSUP	RW	DAC offset calibration update channel DACHDR register enable 0: disable 1: enable	0x0
15:12	Reserved	RO	Reserved	0x0
11:0	DAOS	RO	DAC offset calibration result	0x0

GPIO: (Base Addr 0x40009000)

GPIO_ODR: (Offset 00h)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0x0
15:0	ODR	RW	Values written to this register are output on the I/O signals for Port A if the corresponding data direction bits for Port A are set to Output mode and the corresponding control bit for Port A is set to Software mode. The value read back is equal to the last value written to this register.	0x0

GPIO_OER: (Offset 04h)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0x0
15	OER15	RW	0: Input 1: Output	0x0
14	OER 14	RW	0: Input 1: Output	0x0
13	OER 13	RW	0: Input 1: Output	0x0
12	OER 12	RW	0: Input 1: Output	0x0
11	OER 11	RW	0: Input 1: Output	0x0
10	OER 10	RW	0: Input 1: Output	0x0
9	OER 9	RW	0: Input 1: Output	0x0
8	OER 8	RW	0: Input 1: Output	0x0
7	OER 7	RW	0: Input 1: Output	0x0

6	OER 6	RW	0: Input 1: Output	0x0
5	OER 5	RW	0: Input 1: Output	0x0
4	OER 4	RW	0: Input 1: Output	0x0
3	OER 3	RW	0: Input 1: Output	0x0
2	OER 2	RW	0: Input 1: Output	0x0
1	OER 1	RW	0: Input 1: Output	0x0
0	OER 0	RW	0: Input 1: Output	0x0

GPIO_INTR: (Offset 30h)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0x0
15	INT_EN15	RW	0: GPIO 1: interrupt	0x0
14	INT_EN14	RW	0: GPIO 1: interrupt	0x0
13	INT_EN13	RW	0: GPIO 1: interrupt	0x0
12	INT_EN12	RW	0: GPIO 1: interrupt	0x0
11	INT_EN11	RW	0: GPIO 1: interrupt	0x0
10	INT_EN10	RW	0: GPIO 1: interrupt	0x0
9	INT_EN9	RW	0: GPIO 1: interrupt	0x0
8	INT_EN8	RW	0: GPIO 1: interrupt	0x0
7	INT_EN7	RW	0: GPIO 1: interrupt	0x0
6	INT_EN6	RW	0: GPIO 1: interrupt	0x0
5	INT_EN5	RW	0: GPIO 1: interrupt	0x0

4	INT_EN4	RW	0: GPIO 1: interrupt	0x0
3	INT_EN3	RW	0: GPIO 1: interrupt	0x0
2	INT_EN2	RW	0: GPIO 1: interrupt	0x0
1	INT_EN1	RW	0: GPIO 1: interrupt	0x0
0	INT_EN0	RW	0: GPIO 1: interrupt	0x0

GPIO_INTMR: (Offset 34h)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0x0
15	INTR_MASK15	RW	0: Unmasked 1: Mask	0x0
14	INTR_MASK14	RW	0: Unmasked 1: Mask	0x0
13	INTR_MASK13	RW	0: Unmasked 1: Mask	0x0
12	INTR_MASK12	RW	0: Unmasked 1: Mask	0x0
11	INTR_MASK11	RW	0: Unmasked 1: Mask	0x0
10	INTR_MASK10	RW	0: Unmasked 1: Mask	0x0
9	INTR_MASK9	RW	0: Unmasked 1: Mask	0x0
8	INTR_MASK8	RW	0: Unmasked 1: Mask	0x0
7	INTR_MASK7	RW	0: Unmasked 1: Mask	0x0
6	INTR_MASK6	RW	0: Unmasked 1: Mask	0x0
5	INTR_MASK5	RW	0: Unmasked 1: Mask	0x0
4	INTR_MASK4	RW	0: Unmasked 1: Mask	0x0
3	INTR_MASK3	RW	0: Unmasked 1: Mask	0x0
2	INTR_MASK2	RW	0: Unmasked 1: Mask	0x0
1	INTR_MASK1	RW	0: Unmasked 1: Mask	0x0
0	INTR_MASK0	RW	0: Unmasked 1: Mask	0x0

GPIO_INTLR: (Offset 38h)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0x0
15	INTR_LVL15	RW	0: Level-sensitive 1: Edge-sensitive	0x0
14	INTR_LVL14	RW	0: Level-sensitive 1: Edge-sensitive	0x0
13	INTR_LVL13	RW	0: Level-sensitive 1: Edge-sensitive	0x0
12	INTR_LVL12	RW	0: Level-sensitive 1: Edge-sensitive	0x0
11	INTR_LVL11	RW	0: Level-sensitive 1: Edge-sensitive	0x0
10	INTR_LVL10	RW	0: Level-sensitive 1: Edge-sensitive	0x0
9	INTR_LVL9	RW	0: Level-sensitive 1: Edge-sensitive	0x0
8	INTR_LVL8	RW	0: Level-sensitive 1: Edge-sensitive	0x0
7	INTR_LVL7	RW	0: Level-sensitive 1: Edge-sensitive	0x0
6	INTR_LVL6	RW	0: Level-sensitive 1: Edge-sensitive	0x0
5	INTR_LVL5	RW	0: Level-sensitive 1: Edge-sensitive	0x0
4	INTR_LVL4	RW	0: Level-sensitive 1: Edge-sensitive	0x0
3	INTR_LVL3	RW	0: Level-sensitive 1: Edge-sensitive	0x0
2	INTR_LVL2	RW	0: Level-sensitive 1: Edge-sensitive	0x0
1	INTR_LVL1	RW	0: Level-sensitive 1: Edge-sensitive	0x0
0	INTR_LVL0	RW	0: Level-sensitive 1: Edge-sensitive	0x0

GPIO_INTPR: (Offset 3Ch)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0x0
15	INTR_PLR15	RW	0: Active-low 1: Active-high	0x0
14	INTR_PLR14	RW	0: Active-low 1: Active-high	0x0
13	INTR_PLR13	RW	0: Active-low 1: Active-high	0x0
12	INTR_PLR12	RW	0: Active-low 1: Active-high	0x0
11	INTR_PLR11	RW	0: Active-low 1: Active-high	0x0

10	INTR_PLR10	RW	0: Active-low 1: Active-high	0x0
9	INTR_PLR9	RW	0: Active-low 1: Active-high	0x0
8	INTR_PLR8	RW	0: Active-low 1: Active-high	0x0
7	INTR_PLR7	RW	0: Active-low 1: Active-high	0x0
6	INTR_PLR6	RW	0: Active-low 1: Active-high	0x0
5	INTR_PLR5	RW	0: Active-low 1: Active-high	0x0
4	INTR_PLR4	RW	0: Active-low 1: Active-high	0x0
3	INTR_PLR3	RW	0: Active-low 1: Active-high	0x0
2	INTR_PLR2	RW	0: Active-low 1: Active-high	0x0
1	INTR_PLR1	RW	0: Active-low 1: Active-high	0x0
0	INTR_PLR0	RW	0: Active-low 1: Active-high	0x0

GPIO_INTSR: (Offset 40h)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0x0
15:0	INTR_STAT	RO	Interrupt status of Port A 0x0000: no interrupt 0xffff: interrupt	0x0

GPIO_INTRSR: (Offset 44h)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0x0
15:0	RAW_INTR_STAT	RO	Raw interrupt of status of Port A (premasking bits) 0x0000: no interrupt 0xffff: interrupt	0x0

GPIO_ICR: (Offset 4Ch)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0x0
15	CLEAR_INT15	WO	0: Unclear 1: Clear interrupt	0x0
14	CLEAR_INT14	WO	0: Unclear 1: Clear interrupt	0x0
13	CLEAR_INT13	WO	0: Unclear 1: Clear interrupt	0x0
12	CLEAR_INT12	WO	0: Unclear 1: Clear interrupt	0x0
11	CLEAR_INT11	WO	0: Unclear 1: Clear interrupt	0x0

10	CLEAR_INT10	WO	0: Unclear 1: Clear interrupt	0x0
9	CLEAR_INT9	WO	0: Unclear 1: Clear interrupt	0x0
8	CLEAR_INT8	WO	0: Unclear 1: Clear interrupt	0x0
7	CLEAR_INT7	WO	0: Unclear 1: Clear interrupt	0x0
6	CLEAR_INT6	WO	0: Unclear 1: Clear interrupt	0x0
5	CLEAR_INT5	WO	0: Unclear 1: Clear interrupt	0x0
4	CLEAR_INT4	WO	0: Unclear 1: Clear interrupt	0x0
3	CLEAR_INT3	WO	0: Unclear 1: Clear interrupt	0x0
2	CLEAR_INT2	WO	0: Unclear 1: Clear interrupt	0x0
1	CLEAR_INT1	WO	0: Unclear 1: Clear interrupt	0x0
0	CLEAR_INT0	WO	0: Unclear 1: Clear interrupt	0x0

EXT_IDR: (Offset 50h)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0x0
15:0	IDR	RO	When GPIO is configured as Input, this register indicate the level on GPIO pin, each bit indicate one GPIO pin	0x0

GPIO_INTBER: (Offset 68h)

Bit	Symbol	R/W	Description	Default
31:16	Reserved	RO	Reserved	0x0
15:0	BOTH_EDGE	RW	Control if a interrupt can occur on both rising edge and falling edge,each bit indicate one GPIO pin 0: Disable 1: Enable	0x0

NVIC: (Base Addr 0xE000E100)

NVIC_ISER: (Offset 00h)

Bit	Symbol	R/W	Description	Default
31:12	Reserved	RO	Reserved	0x0
11	SETENA11_WDT	RW	Enable number IRQ11 interrupts. 0: disable 1: enable	0x0

10	SETENA10_FMC	RW	Enable number IRQ10 interrupts. 0: disable 1: enable	0x0
9	SETENA9_RMC	RW	Enable number IRQ9 interrupts. 0: disable 1: enable	0x0
8	SETENA8_GPIO	RW	Enable number IRQ8 interrupts. 0: disable 1: enable	0x0
7	SETENA7_AFE_CMP1	RW	Enable number IRQ7 interrupts. 0: disable 1: enable	0x0
6	SETENA6_AFE_CMP0	RW	Enable number IRQ6 interrupts. 0: disable 1: enable	0x0
5	SETENA5_AFE	RW	Enable number IRQ5 interrupts. 0: disable 1: enable	0x0
4	SETENA4_I²C	RW	Enable number IRQ4 interrupts. 0: disable 1: enable	0x0
3	SETENA3_UART	RW	Enable number IRQ3 interrupts. 0: disable 1: enable	0x0
2	SETENA2_TMR1	RW	Enable number IRQ2 interrupts. 0: disable 1: enable	0x0
1	SETENA1_TMR0	RW	Enable number IRQ1 interrupts. 0: disable 1: enable	0x0
0	SETENA0_UVLO	RW	Enable number IRQ0 interrupts. 0: disable 1: enable	0x0

NVIC_ICER: (Offset 80h)

Bit	Symbol	R/W	Description	Default
31:12	Reserved	RO	Reserved	0x0
11	CLRENA11	RW	disable number IRQ11 interrupts. 0: no effect 1: disable interrupt	0x0
10	CLRENA10	RW	disable number IRQ10 interrupts. 0: no effect 1: disable interrupt	0x0
9	CLRENA9	RW	disable number IRQ9 interrupts. 0: no effect 1: disable interrupt	0x0
8	CLRENA8	RW	disable number IRQ8 interrupts. 0: no effect 1: disable interrupt	0x0

7	CLRENA7	RW	disable number IRQ7 interrupts. 0: no effect 1: disable interrupt	0x0
6	CLRENA6	RW	disable number IRQ6 interrupts. 0: no effect 1: disable interrupt	0x0
5	CLRENA5	RW	disable number IRQ5 interrupts. 0: no effect 1: disable interrupt	0x0
4	CLRENA4	RW	disable number IRQ4 interrupts. 0: no effect 1: disable interrupt	0x0
3	CLRENA3	RW	disable number IRQ3 interrupts. 0: no effect 1: disable interrupt	0x0
2	CLRENA2	RW	disable number IRQ2 interrupts. 0: no effect 1: disable interrupt	0x0
1	CLRENA1	RW	disable number IRQ1 interrupts. 0: no effect 1: disable interrupt	0x0
0	CLRENA0	RW	disable number IRQ0 interrupts. 0: no effect 1: disable interrupt	0x0

NVIC_ISPR: (Offset 100h)

Bit	Symbol	R/W	Description	Default
31:12	Reserved	RO	Reserved	0x0
11	ISPR_SETPEND11	RW	pend number IRQ11 interrupts. 0: no effect 1: pend interrupt	0x0
10	ISPR_SETPEND10	RW	pend number IRQ10 interrupts. 0: no effect 1: pend interrupt	0x0
9	ISPR_SETPEND9	RW	pend number IRQ9 interrupts. 0: no effect 1: pend interrupt	0x0
8	ISPR_SETPEND8	RW	pend number IRQ8 interrupts. 0: no effect 1: pend interrupt	0x0
7	ISPR_SETPEND7	RW	pend number IRQ7 interrupts. 0: no effect 1: pend interrupt	0x0
6	ISPR_SETPEND6	RW	pend number IRQ6 interrupts. 0: no effect 1: pend interrupt	0x0
5	ISPR_SETPEND5	RW	pend number IRQ5 interrupts. 0: no effect 1: pend interrupt	0x0

4	ISPR_SETPEND4	RW	pend number IRQ4 interrupts. 0: no effect 1: pend interrupt	0x0
3	ISPR_SETPEND3	RW	pend number IRQ3 interrupts. 0: no effect 1: pend interrupt	0x0
2	ISPR_SETPEND2	RW	pend number IRQ2 interrupts. 0: no effect 1: pend interrupt	0x0
1	ISPR_SETPEND1	RW	pend number IRQ1 interrupts. 0: no effect 1: pend interrupt	0x0
0	ISPR_SETPEND0	RW	pend number IRQ0 interrupts. 0: no effect 1: pend interrupt	0x0

NVIC_ICPR: (Offset 180h)

Bit	Symbol	R/W	Description	Default
31:12	Reserved	RO	Reserved	0x0
11	SETPEND11	RW	un-pend number IRQ11 interrupts. 0: no effect 1: un-pend interrupt	0x0
10	SETPEND10	RW	un-pend number IRQ10 interrupts. 0: no effect 1: un-pend interrupt	0x0
9	SETPEND9	RW	un-pend number IRQ9 interrupts. 0: no effect 1: un-pend interrupt	0x0
8	SETPEND8	RW	un-pend number IRQ8 interrupts. 0: no effect 1: un-pend interrupt	0x0
7	SETPEND7	RW	un-pend number IRQ7 interrupts. 0: no effect 1: un-pend interrupt	0x0
6	SETPEND6	RW	un-pend number IRQ6 interrupts. 0: no effect 1: un-pend interrupt	0x0
5	SETPEND5	RW	un-pend number IRQ5 interrupts. 0: no effect 1: un-pend interrupt	0x0
4	SETPEND4	RW	un-pend number IRQ4 interrupts. 0: no effect 1: un-pend interrupt	0x0
3	SETPEND3	RW	un-pend number IRQ3 interrupts. 0: no effect 1: un-pend interrupt	0x0
2	SETPEND2	RW	un-pend number IRQ2 interrupts. 0: no effect 1: un-pend interrupt	0x0

1	SETPEND1	RW	un-pend number IRQ1 interrupts. 0: no effect 1: un-pend interrupt	0x0
0	SETPEND0	RW	un-pend number IRQ0 interrupts. 0: no effect 1: un-pend interrupt	0x0

NVIC_IPR0: (Offset 300h)

Bit	Symbol	R/W	Description	Default
31:30	PRI_3	RW	Priority of IRQ3. 0b00: highest 0b01: high 0b10: low 0b11: lowest	0x0
29:24	Reserved	RO	Reserved	0x0
23:22	PRI_2	RW	Priority of IRQ2. 0b00: highest 0b01: high 0b10: low 0b11: lowest	0x0
21:16	Reserved	RO	Reserved	0x0
15:14	PRI_1	RW	Priority of IRQ1. 0b00: highest 0b01: high 0b10: low 0b11: lowest	0x0
13:8	Reserved	RO	Reserved	0x0
7:6	PRI_0	RW	Priority of IRQ0. 0b00: highest 0b01: high 0b10: low 0b11: lowest	0x0
5:0	Reserved	RO	Reserved	0x0

NVIC_IPR1: (Offset 304h)

Bit	Symbol	R/W	Description	Default
31:30	PRI_7	RW	Priority of IRQ7. 0b00: highest 0b01: high 0b10: low 0b11: lowest	0x0
29:24	Reserved	RO	Reserved	0x0
23:22	PRI_6	RW	Priority of IRQ6. 0b00: highest 0b01: high 0b10: low 0b11: lowest	0x0
21:16	Reserved	RO	Reserved	0x0

15:14	PRI_5	RW	Priority of IRQ5. 0b00: highest 0b01: high 0b10: low 0b11: lowest	0x0
13:8	Reserved	RO	Reserved	0x0
7:6	PRI_4	RW	Priority of IRQ4. 0b00: highest 0b01: high 0b10: low 0b11: lowest	0x0
5:0	Reserved	RO	Reserved	0x0

NVIC_IPR2: (Offset 308h)

Bit	Symbol	R/W	Description	Default
31:30	PRI_11	RW	Priority of IRQ11. 0b00: highest 0b01: high 0b10: low 0b11: lowest	0x0
29:24	Reserved	RO	Reserved	0x0
23:22	PRI_10	RW	Priority of IRQ10. 0b00: highest 0b01: high 0b10: low 0b11: lowest	0x0
21:16	Reserved	RO	Reserved	0x0
15:14	PRI_9	RW	Priority of IRQ9. 0b00: highest 0b01: high 0b10: low 0b11: lowest	0x0
13:8	Reserved	RO	Reserved	0x0
7:6	PRI_8	RW	Priority of IRQ8. 0b00: highest 0b01: high 0b10: low 0b11: lowest	0x0
5:0	Reserved	RO	Reserved	0x0

PCB Layout Consideration

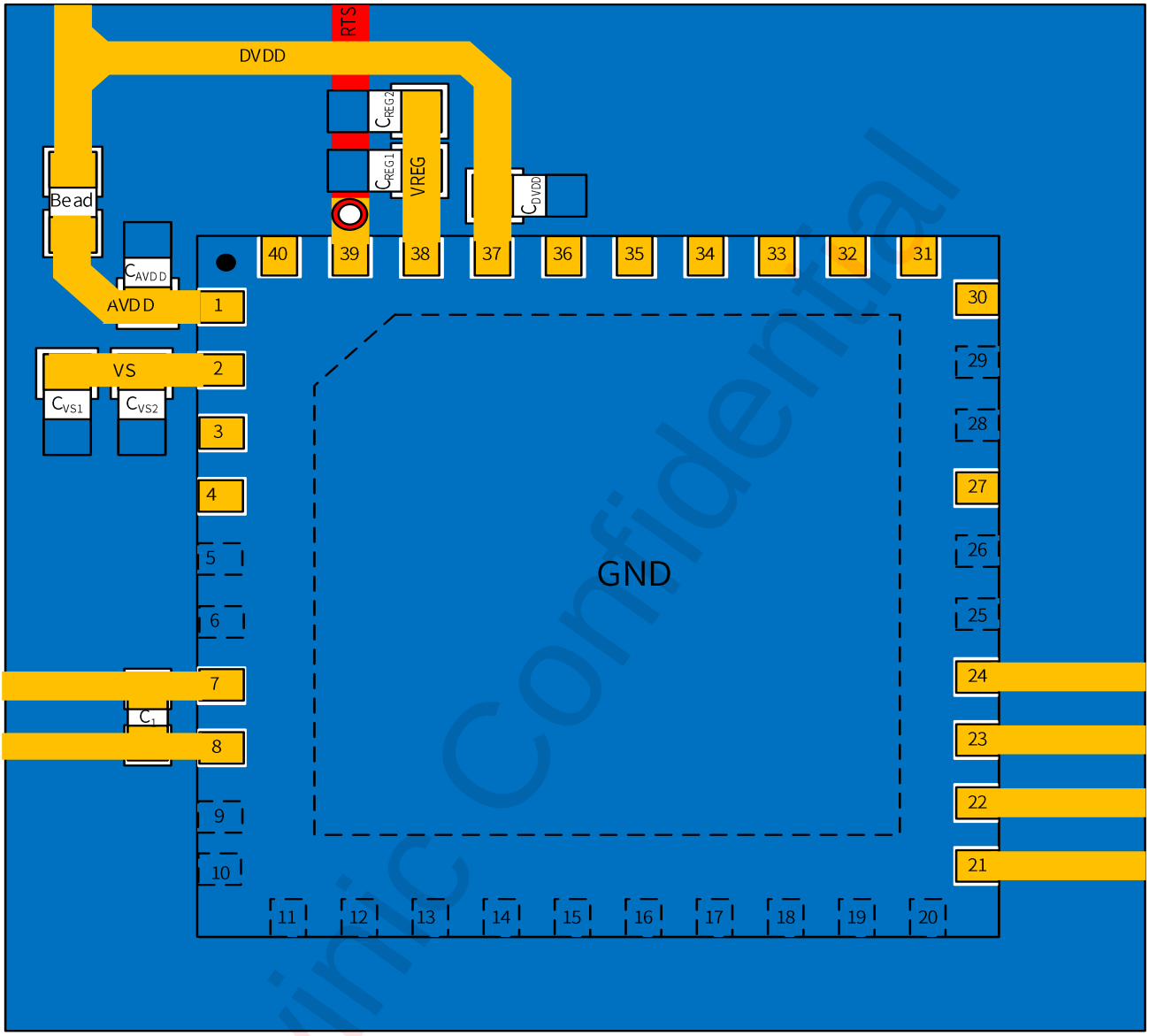


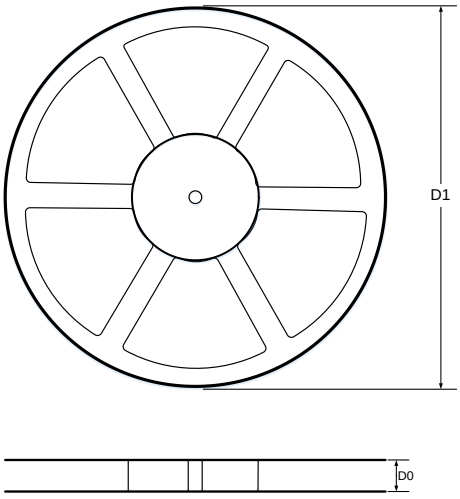
Figure 15 AW86803QNR-Q1 Typical Layout

PCB layout should be considered carefully. Here are some guidelines:

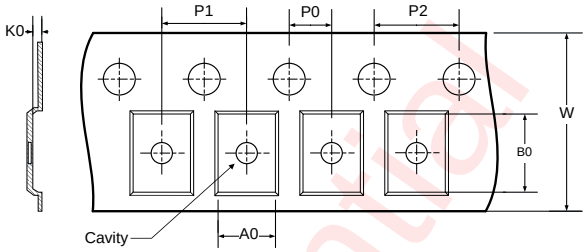
1. Capacitors C_{ADD}, C_{VDD}, C_{VS1} and C_{VS2} are as close to the chip pins as possible.
2. SAR ADC is used inside the chip, so the chip should be far away from the pressing area during layout.
3. SINPx/SINNx cable width is recommended to be 0.1mm. Follow the 3W cable routing rule.
4. The difference line SINPx/SINNx needs to be surrounded by a power ground.
5. Route SINPx/SINNx cables away from interference sources.
6. Keep the SINPx/SINNx cables away from heat sources.
7. The GND under the chip shall be connected with the GND of the next layer and ensure the integrity of the GND of the next layer.

Tape And Reel Information

REEL DIMENSIONS

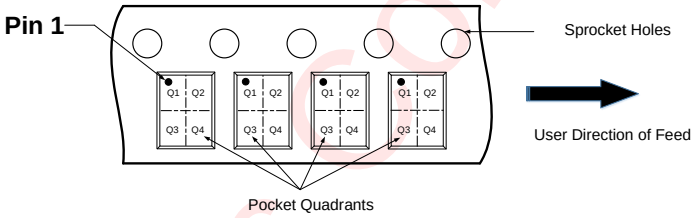


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



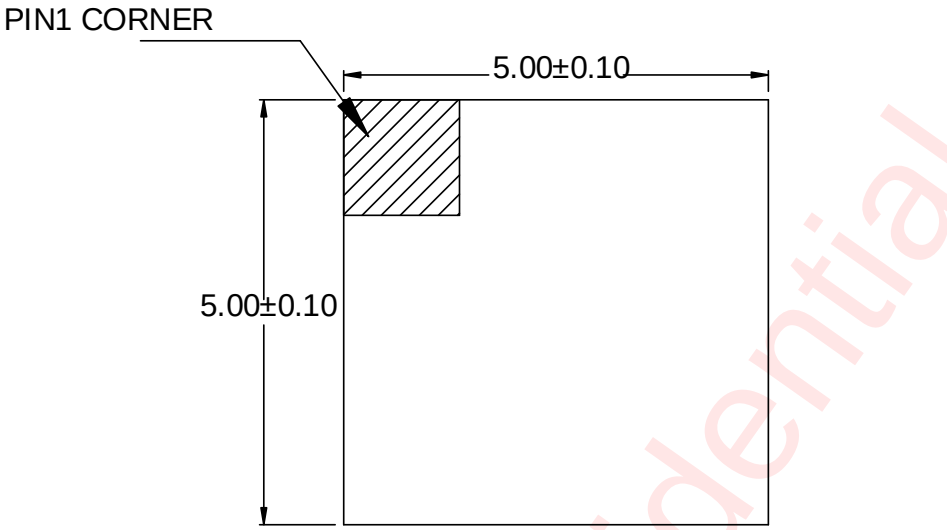
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

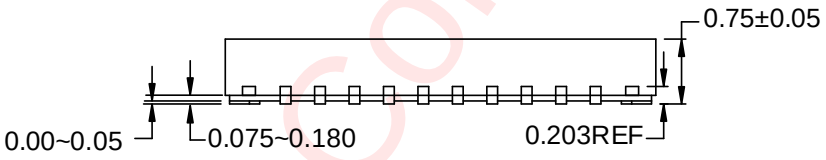
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	5.25	5.25	1.1	2	8	4	12	Q1

All dimensions are nominal

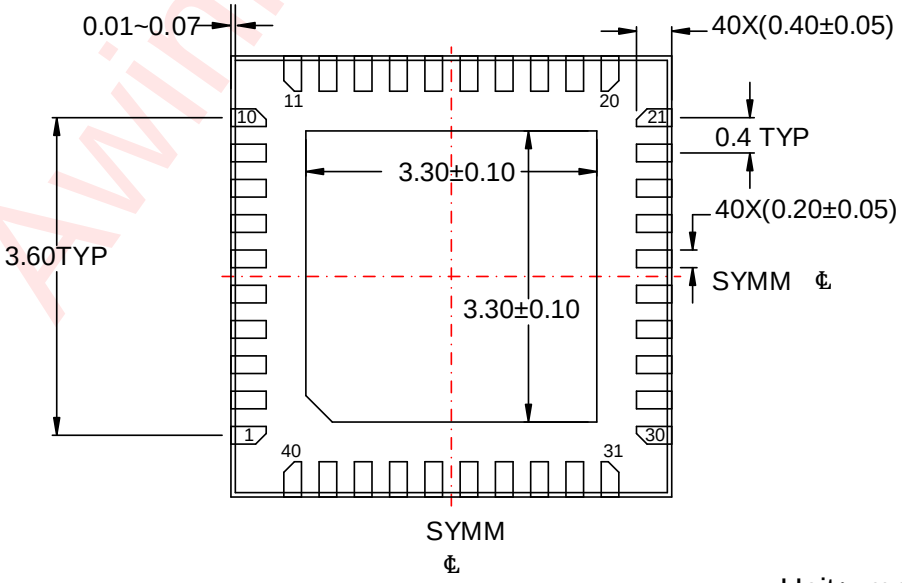
Package Description



TOP VIEW



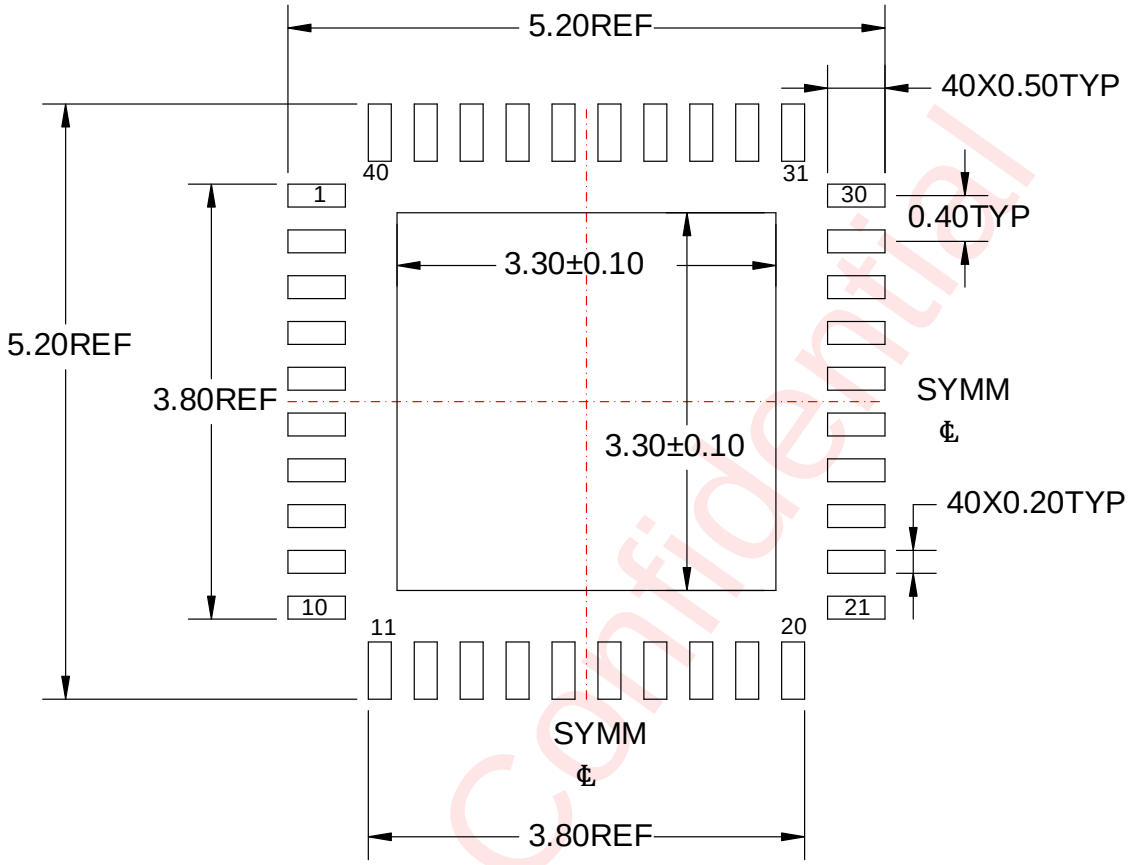
SIDE VIEW

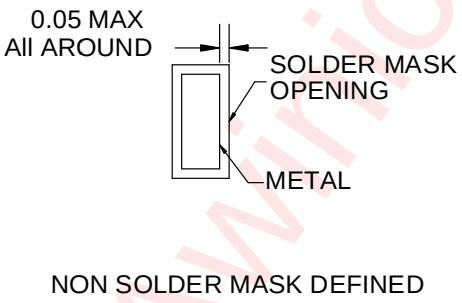


Unit：mm

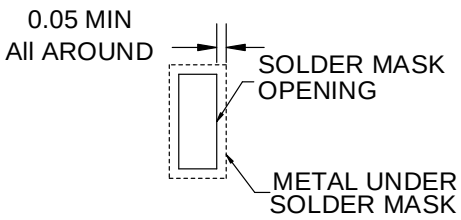
BOTTOM VIEW

Land Pattern Data





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Apr. 2023	Officially released.
V1.1	Aug. 2024	Add Light Synchronized with Sound
V1.2	Oct. 2025	Update the Power On and Power Down Sequence, modify the VIL, Isd and add design assurance explanation.

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