

## 1. General Description

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The EM74LVC00A is a quad 2-input NAND gate. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

## 2. Features and Benefits

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- Wide supply voltage range from 1.2 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- CMOS low power dissipation
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 3A exceeds 6000 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options

## EM74LVC00A

Quad 2-input NAND gate

### 3. Ordering Information

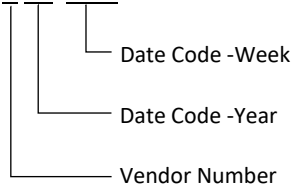
Table 1. Ordering information

| Type number  | Topside marking | Package   |                                                                           |          |
|--------------|-----------------|-----------|---------------------------------------------------------------------------|----------|
|              |                 | Name      | Description                                                               | Quantity |
| EM74LVC00AD  | LVC00A<br>XYYWW | SOP-14L   | plastic small outline package; 14 leads;<br>body width 3.9 mm             | 3000     |
| EM74LVC00APW | LVC00A<br>XYYWW | TSSOP-14L | plastic thin shrink small outline package; 14<br>leads; body width 4.4 mm | 3000     |

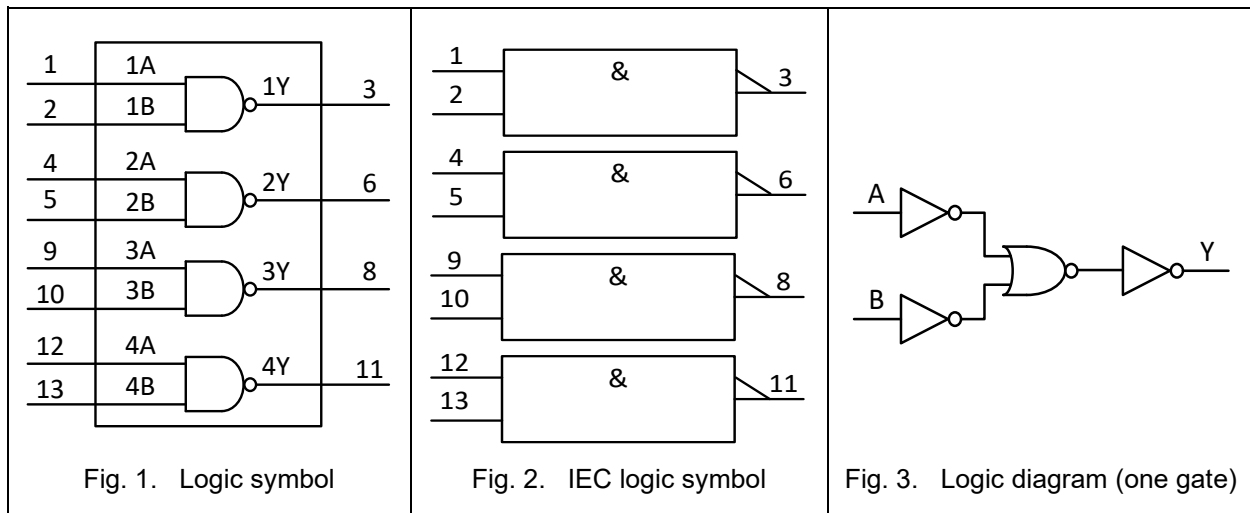
#### MARKING INFORMATION

NOTE: XYYWW = Vendor Code and Date Code.

X YY WW

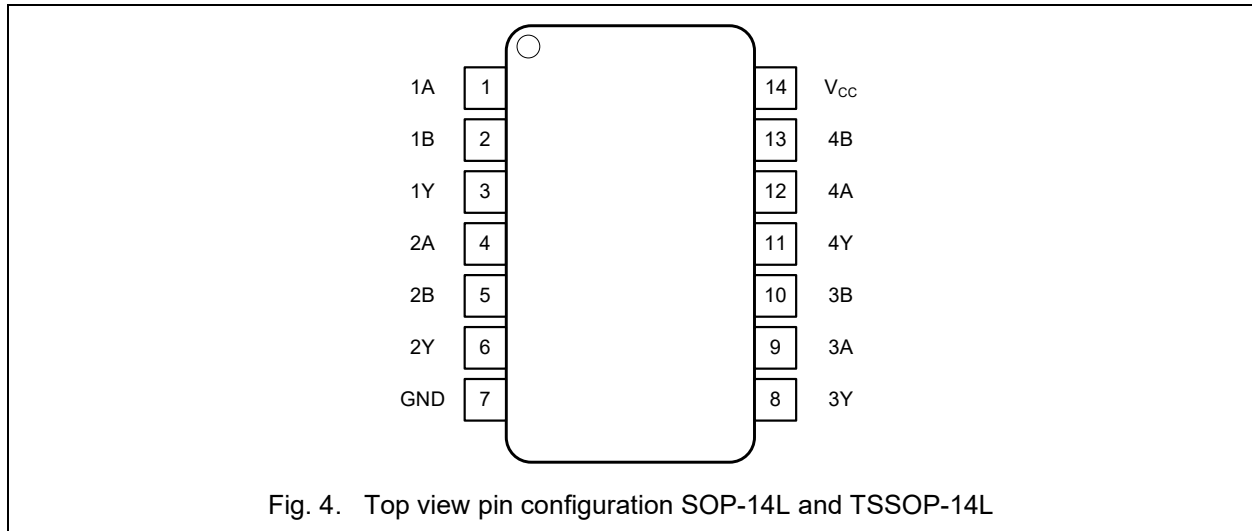


### 4. Function Diagram



## 5. Pinning Information

### 5.1. Pinning



### 5.2. Pin description

**Table 2. Pin description**

| Symbol          | Pin          | Description    |
|-----------------|--------------|----------------|
| 1A, 2A, 3A, 4A  | 1, 4, 9, 12  | Data input     |
| 1B, 2B, 3B, 4B  | 2, 5, 10, 13 | Data input     |
| 1Y, 2Y, 3Y, 4Y  | 3, 6, 8, 11  | Data output    |
| GND             | 7            | Ground (0V)    |
| V <sub>CC</sub> | 14           | Supply voltage |

## 6. Functional Description

**Table 3. Function table**

H = HIGH voltage level; L = LOW voltage level; X = don't care.

| Input nA | Input nB | Output nY |
|----------|----------|-----------|
| L        | X        | H         |
| X        | L        | H         |
| H        | H        | L         |

## 7. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

**Table 4. Absolute Maximum Ratings**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

| Symbol    | Parameter               | Conditions                          | Min  | Max            | Unit |
|-----------|-------------------------|-------------------------------------|------|----------------|------|
| $V_{CC}$  | supply voltage          |                                     | -0.5 | 6.5            | V    |
| $I_{IK}$  | input clamping current  | $V_I < 0$ V                         | -50  |                | mA   |
| $V_I$     | input voltage           | [1]                                 | -0.5 | 6.5            | V    |
| $I_{OK}$  | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V       |      | $\pm 50$       | mA   |
| $V_O$     | output voltage          | Active mode [1]                     | -0.5 | $V_{CC} + 0.5$ | V    |
|           |                         | Power-down mode; $V_{CC} = 0$ V [1] | -0.5 | 6.5            | V    |
| $I_O$     | output current          | $V_O = 0$ V to $V_{CC}$             |      | $\pm 50$       | mA   |
| $I_{CC}$  | supply current          |                                     |      | 100            | mA   |
| $I_{GND}$ | ground current          |                                     | -100 |                | mA   |
| $P_{tot}$ | total power dissipation | $T_{amb} = -40$ °C to $+125$ °C     |      | 500            | mW   |
| $T_{stg}$ | storage temperature     |                                     | -65  | 150            | °C   |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 8. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

**Table 5. Recommended Operating Conditions**

| Symbol              | Parameter                           | Conditions                      | Min  | Max      | Unit |
|---------------------|-------------------------------------|---------------------------------|------|----------|------|
| $V_{CC}$            | supply voltage                      |                                 | 1.65 | 5.5      | V    |
|                     |                                     | functional                      | 1.2  |          | V    |
| $V_I$               | input voltage                       |                                 | 0    | 5.5      | V    |
| $V_O$               | output voltage                      | Active mode                     | 0    | $V_{CC}$ | V    |
|                     |                                     | Power-down mode; $V_{CC} = 0$ V | 0    | 5.5      | V    |
| $T_{amb}$           | ambient temperature                 |                                 | -40  | 125      | °C   |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 1.65$ V to $2.7$ V    | 0    | 20       | ns/V |
|                     |                                     | $V_{CC} = 2.7$ V to $5.5$ V     | 0    | 10       | ns/V |

## 9.Static Characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol   | Parameter                 | Conditions                                                           | -40 °C to +85 °C |           |              | -40 °C to +125 °C |              | Unit          |
|----------|---------------------------|----------------------------------------------------------------------|------------------|-----------|--------------|-------------------|--------------|---------------|
|          |                           |                                                                      | Min              | Typ[1]    | Max          | Min               | Max          |               |
| $V_{IH}$ | HIGH-level input voltage  | $V_{CC} = 1.2 \text{ V}$                                             | 1.08             |           |              | 1.08              |              | V             |
|          |                           | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$                         | $0.65V_{CC}$     |           |              | $0.65V_{CC}$      |              | V             |
|          |                           | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$                           | 1.7              |           |              | 1.7               |              | V             |
|          |                           | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$                           | 2.0              |           |              | 2.0               |              | V             |
|          |                           | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$                           | $0.7V_{CC}$      |           |              | $0.7V_{CC}$       |              | V             |
| $V_{IL}$ | LOW-level input voltage   | $V_{CC} = 1.2 \text{ V}$                                             |                  |           | 0.12         |                   | 0.12         | V             |
|          |                           | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$                         |                  |           | $0.35V_{CC}$ |                   | $0.35V_{CC}$ | V             |
|          |                           | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$                           |                  |           | 0.7          |                   | 0.7          | V             |
|          |                           | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$                           |                  |           | 0.8          |                   | 0.8          | V             |
|          |                           | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$                           |                  |           | $0.3V_{CC}$  |                   | $0.3V_{CC}$  | V             |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH} \text{ or } V_{IL}$                                    |                  |           |              |                   |              |               |
|          |                           | $I_O = -100 \mu\text{A}; V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$  | $V_{CC} - 0.1$   |           |              | $V_{CC} - 0.1$    |              | V             |
|          |                           | $I_O = -4 \text{ mA}; V_{CC} = 1.65 \text{ V}$                       | 1.2              |           |              | 1.05              |              | V             |
|          |                           | $I_O = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$                        | 1.9              |           |              | 1.7               |              | V             |
|          |                           | $I_O = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$                       | 2.2              |           |              | 2.05              |              | V             |
|          |                           | $I_O = -24 \text{ mA}; V_{CC} = 3.0 \text{ V}$                       | 2.4              |           |              | 2.25              |              | V             |
|          |                           | $I_O = -32 \text{ mA}; V_{CC} = 4.5 \text{ V}$                       | 3.8              |           |              | 3.5               |              | V             |
| $V_{OL}$ | LOW-level output voltage  | $V_I = V_{IH} \text{ or } V_{IL}$                                    |                  |           |              |                   |              |               |
|          |                           | $I_O = 100 \mu\text{A}; V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$   |                  |           | 0.10         |                   | 0.10         | V             |
|          |                           | $I_O = 4 \text{ mA}; V_{CC} = 1.65 \text{ V}$                        |                  |           | 0.45         |                   | 0.65         | V             |
|          |                           | $I_O = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$                         |                  |           | 0.30         |                   | 0.45         | V             |
|          |                           | $I_O = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$                        |                  |           | 0.40         |                   | 0.60         | V             |
|          |                           | $I_O = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$                        |                  |           | 0.55         |                   | 0.80         | V             |
|          |                           | $I_O = 32 \text{ mA}; V_{CC} = 4.5 \text{ V}$                        |                  |           | 0.55         |                   | 0.80         | V             |
| $I_I$    | input leakage current     | $V_I = 5.5 \text{ V or GND}; V_{CC} = 0 \text{ V to } 5.5 \text{ V}$ |                  | $\pm 0.1$ | $\pm 5$      |                   | $\pm 20$     | $\mu\text{A}$ |

## EM74LVC00A

### Quad 2-input NAND gate

| Symbol          | Parameter                 | Conditions                                                                                                          | -40 °C to +85 °C |           |          | -40 °C to +125 °C |          | Unit          |
|-----------------|---------------------------|---------------------------------------------------------------------------------------------------------------------|------------------|-----------|----------|-------------------|----------|---------------|
|                 |                           |                                                                                                                     | Min              | Typ[1]    | Max      | Min               | Max      |               |
| $I_{OFF}$       | power-off leakage current | $V_{CC} = 0 \text{ V};$<br>$V_I \text{ or } V_O = 5.5 \text{ V}$                                                    |                  | $\pm 0.1$ | $\pm 10$ |                   | $\pm 20$ | $\mu\text{A}$ |
| $I_{CC}$        | supply current            | $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V};$<br>$V_I = 5.5 \text{ V or GND}; I_O = 0 \text{ A}$                     |                  | 0.01      | 10       |                   | 40       | $\mu\text{A}$ |
| $\Delta I_{CC}$ | additional supply current | per input pin ;<br>$V_{CC} = 2.3 \text{ V to } 5.5 \text{ V};$<br>$V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}$ |                  | 0.2       | 500      |                   | 5000     | $\mu\text{A}$ |
| $C_i$           | input capacitance         | $V_{CC} = 3.3 \text{ V};$<br>$V_I = \text{GND to } V_{CC}$                                                          |                  | 4         |          |                   |          | $\text{pF}$   |

[1] All typical values are measured at  $V_{CC} = 3.3 \text{ V}$  and  $T_{amb} = 25 \text{ }^\circ\text{C}$ .

## 10. Dynamic Characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

| Symbol      | Parameter                     | Conditions                                | -40 °C to +85 °C |        |      | -40 °C to +125 °C |      | Unit |
|-------------|-------------------------------|-------------------------------------------|------------------|--------|------|-------------------|------|------|
|             |                               |                                           | Min              | Typ[1] | Max  | Min               | Max  |      |
| $t_{pd}$    | propagation delay             | nA, nB to nY; see Fig. 5 [2]              |                  |        |      |                   |      |      |
|             |                               | $V_{CC} = 1.2V$                           |                  | 36     |      |                   |      | ns   |
|             |                               | $V_{CC} = 1.65 V$ to $1.95 V$             | 3.4              | 11.4   | 22   | 3.4               | 22.5 | ns   |
|             |                               | $V_{CC} = 2.3 V$ to $2.7 V$               | 2.7              | 6.3    | 10.5 | 2.7               | 11   | ns   |
|             |                               | $V_{CC} = 3.0 V$ to $3.6 V$               | 2.0              | 4.6    | 7.5  | 2.0               | 8.0  | ns   |
|             |                               | $V_{CC} = 4.5 V$ to $5.5 V$               | 1.5              | 3.3    | 5    | 1.5               | 5.5  | ns   |
| $t_{sk(o)}$ | output skew time              | $V_{CC} = 3.0 V$ to $3.6 V$ [3]           |                  |        | 1.0  |                   | 1.5  | ns   |
| $C_{PD}$    | power dissipation capacitance | per gate ;<br>$V_I = GND$ to $V_{CC}$ [4] |                  |        |      |                   |      |      |
|             |                               | $V_{CC} = 1.65 V$ to $1.95 V$             |                  | 12.7   |      |                   |      | pF   |
|             |                               | $V_{CC} = 2.3 V$ to $2.7 V$               |                  | 13.4   |      |                   |      | pF   |
|             |                               | $V_{CC} = 3.0 V$ to $3.6 V$               |                  | 14.3   |      |                   |      | pF   |
|             |                               | $V_{CC} = 4.5 V$ to $5.5 V$               |                  | 16.2   |      |                   |      | pF   |

[1] Typical values are measured at  $T_{amb} = 25\text{ °C}$  and  $V_{CC} = 1.2 V, 1.8 V, 2.5 V, 3.3 V$  and  $5.0 V$  respectively.

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

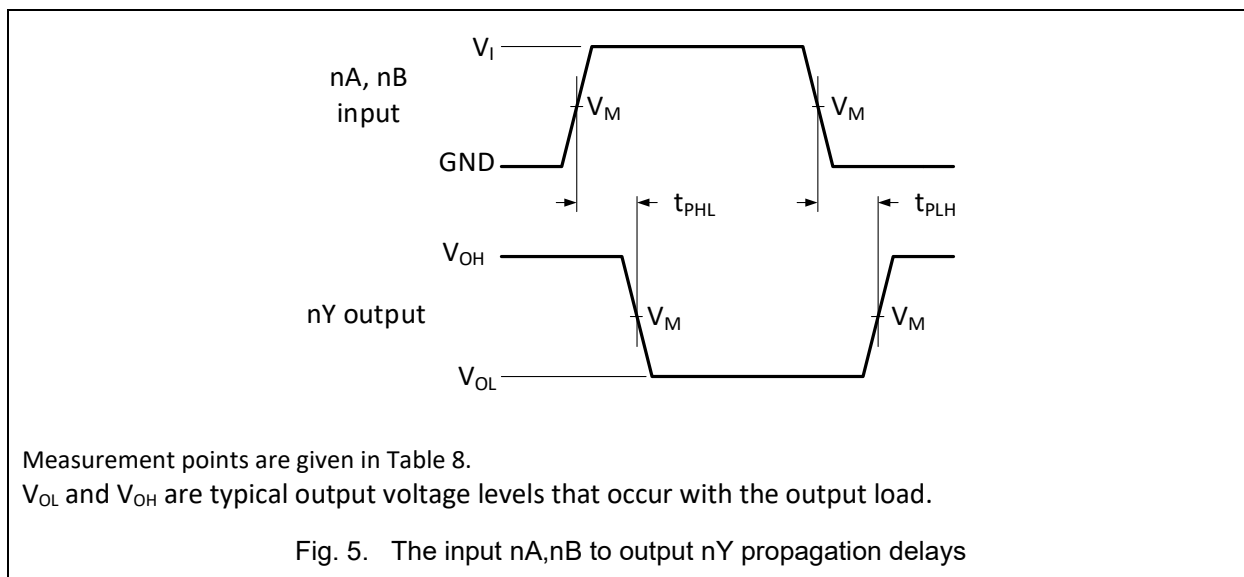
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

## 10.1. Waveforms and test circuit



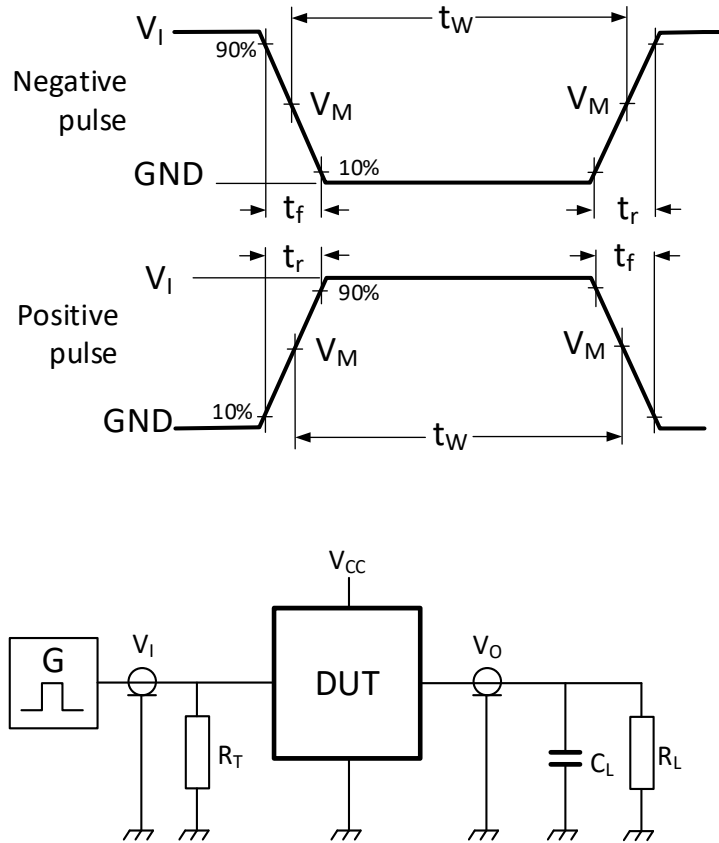
**Table 8. Measurement points**

| Supply voltage   | Input       | Output      |
|------------------|-------------|-------------|
| $V_{CC}$         | $V_M$       | $V_M$       |
| 1.2 V            | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 1.65 V to 1.95 V | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 2.3 V to 2.7 V   | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 3.0 V to 3.6 V   | 1.5 V       | 1.5 V       |
| 4.5 V to 5.5 V   | $0.5V_{CC}$ | $0.5V_{CC}$ |



# EM74LVC00A

## Quad 2-input NAND gate



Test data is given in Table 9.

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

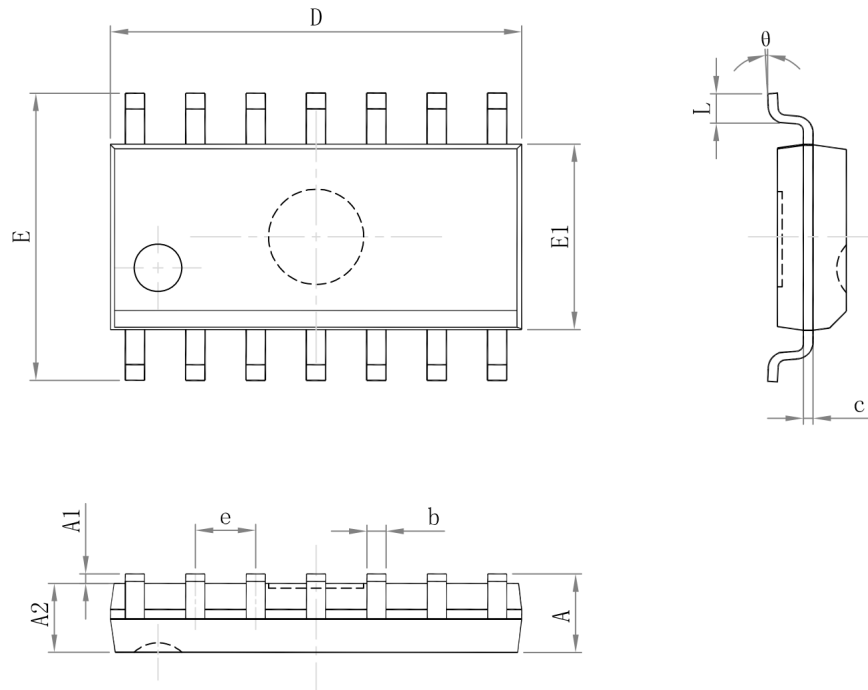
Fig. 6. Test circuit for measuring switching times

Table 9. Test data

| Supply voltage   | Input    |               | Load  |              |
|------------------|----------|---------------|-------|--------------|
| $V_{CC}$         | $V_I$    | $t_r = t_f$   | $C_L$ | $R_L$        |
| 1.2 V            | $V_{CC}$ | $\leq 2.0$ ns | 15 pF | 500 $\Omega$ |
| 1.65 V to 1.95 V | $V_{CC}$ | $\leq 2.0$ ns | 15 pF | 500 $\Omega$ |
| 2.3 V to 2.7 V   | $V_{CC}$ | $\leq 2.0$ ns | 15 pF | 500 $\Omega$ |
| 3.0 V to 3.6 V   | 3 V      | $\leq 2.0$ ns | 15 pF | 500 $\Omega$ |
| 4.5 V to 5.5 V   | $V_{CC}$ | $\leq 2.0$ ns | 15 pF | 500 $\Omega$ |

# 11. Package Outline

SOP-14L

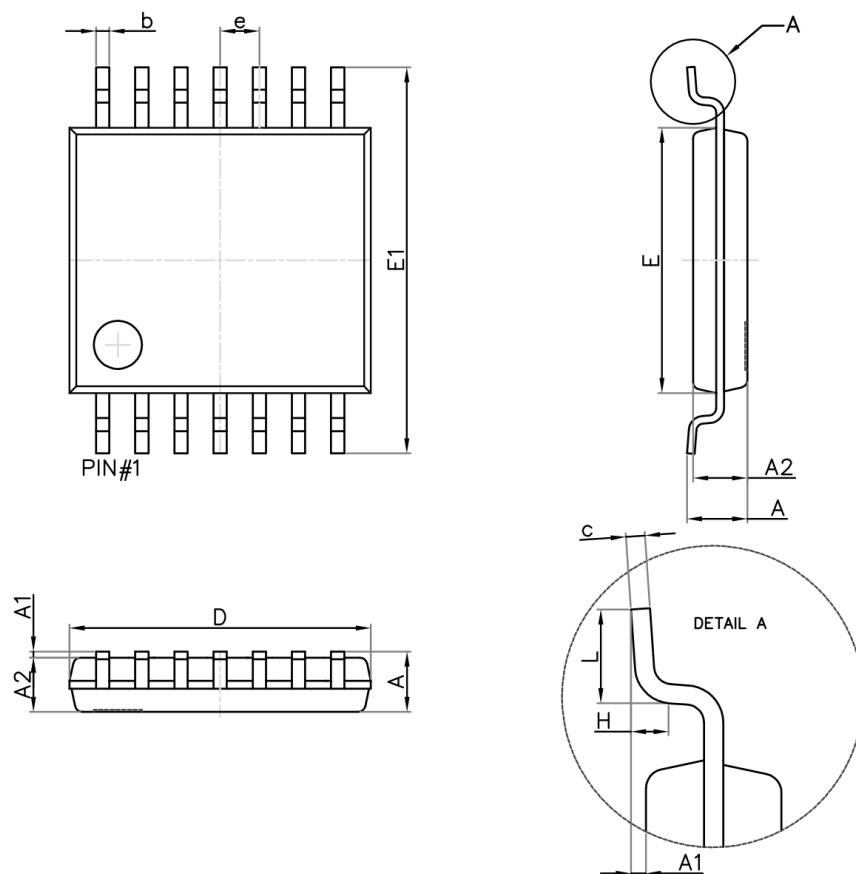


| Symbol | Dimensions In Millimeters |       | Dimensions In Inches |       |
|--------|---------------------------|-------|----------------------|-------|
|        | Min                       | Max   | Min                  | Max   |
| A      | —                         | 1.750 | —                    | 0.069 |
| A1     | 0.100                     | 0.250 | 0.004                | 0.010 |
| A2     | 1.250                     | —     | 0.049                | —     |
| b      | 0.310                     | 0.510 | 0.012                | 0.020 |
| c      | 0.100                     | 0.250 | 0.004                | 0.010 |
| D      | 8.450                     | 8.850 | 0.333                | 0.348 |
| E      | 5.800                     | 6.200 | 0.228                | 0.244 |
| E1     | 3.800                     | 4.000 | 0.150                | 0.157 |
| e      | 1.270(BSC)                |       | 0.050(BSC)           |       |
| L      | 0.400                     | 1.270 | 0.016                | 0.050 |
| θ      | 0°                        | 8°    | 0°                   | 8°    |

# EM74LVC00A

Quad 2-input NAND gate

## TSSOP-14L



| Symbol | Dimensions In Millimeters |       | Dimensions In Inches |       |
|--------|---------------------------|-------|----------------------|-------|
|        | Min.                      | Max.  | Min.                 | Max.  |
| D      | 4.900                     | 5.100 | 0.193                | 0.201 |
| E      | 4.300                     | 4.500 | 0.169                | 0.177 |
| b      | 0.190                     | 0.300 | 0.007                | 0.012 |
| c      | 0.090                     | 0.200 | 0.004                | 0.008 |
| E1     | 6.250                     | 6.550 | 0.246                | 0.258 |
| A      | —                         | 1.200 | —                    | 0.047 |
| A2     | 0.800                     | 1.000 | 0.031                | 0.039 |
| A1     | 0.050                     | 0.150 | 0.002                | 0.006 |
| e      | 0.65 (BSC)                |       | 0.026 (BSC)          |       |
| L      | 0.500                     | 0.700 | 0.020                | 0.028 |
| H      | 0.25(TYP)                 |       | 0.01(TYP)            |       |
| θ      | 1°                        | 7°    | 1°                   | 7°    |

## 12. Abbreviations

Table 10. Abbreviations

| Acronym | Description                             |
|---------|-----------------------------------------|
| CMOS    | Complementary Metal-Oxide Semiconductor |
| DUT     | Device Under Test                       |
| ESD     | ElectroStatic Discharge                 |
| HBM     | Human Body Model                        |
| CDM     | Charged Device Model                    |
| TTL     | Transistor-Transistor Logic             |

## 13. Revision History

Table 11. Revision history

| Document ID         | Release Date                                                                                                                                                                        | Data sheet status | Change notice | Supersedes          |
|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|---------------|---------------------|
| EM74LVC00A Rev. 1.2 | Dec 15, 2025                                                                                                                                                                        | Product datasheet |               | EM74LVC00A Rev. 1.1 |
| Modifications:      | Talbe 1: Added topside marking information.                                                                                                                                         |                   |               |                     |
| EM74LVC00A Rev. 1.1 | Aug 21, 2024                                                                                                                                                                        | Product datasheet |               | EM74LVC00A Rev. 1.0 |
| Modifications:      | <ul style="list-style-type: none"><li>Table 6: <math>V_{OH}</math> and <math>V_{OL}</math> updated.</li><li>Table 7: <math>t_{pd}</math> and <math>C_{pd}</math> updated.</li></ul> |                   |               |                     |
| EM74LVC00A Rev. 1.0 | May 20, 2024                                                                                                                                                                        | Product datasheet |               |                     |