PRELIMINARY

CYW20707

Embedded Bluetooth 4.1 SoC with MCU, Bluetooth Transceiver, and Baseband Processor

The Cypress CYW20707 is a monolithic, single-chip, Bluetooth 4.1 + HS compliant SOC, comprising a baseband processor, an ARM Cortex-M3 processor, and an integrated transceiver. It is designed for use in embedded applications, with on-chip support for an embedded stack. Manufactured using the industry's most advanced 40 nm CMOS low-power process, the CYW20707 employs the highest level of integration, eliminating all critical external components, and thereby minimizing the device's footprint and costs associated with the implementation of Bluetooth solutions.

The CYW20707 is the optimal solution for voice, data, home automation, accessories and other applications that require a Bluetooth SIG standards-compliant interface. The CYW20707 supports a host command interface (HCI) through USB or UART and also supports PCM audio.

The CYW20707 transceiver's enhanced radio performance meets the most stringent industrial temperature application requirements for compact integration into mobile handset and portable devices. The CYW20707 provides full radio compatibility, enabling it to operate simultaneously with GPS and cellular radios.

Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM20707	CYW20707
BCM20707UA1KFFB1G	CYW20707UA1KFFB1G

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Cypress documents, go to:
http://www.cypress.com/glossary

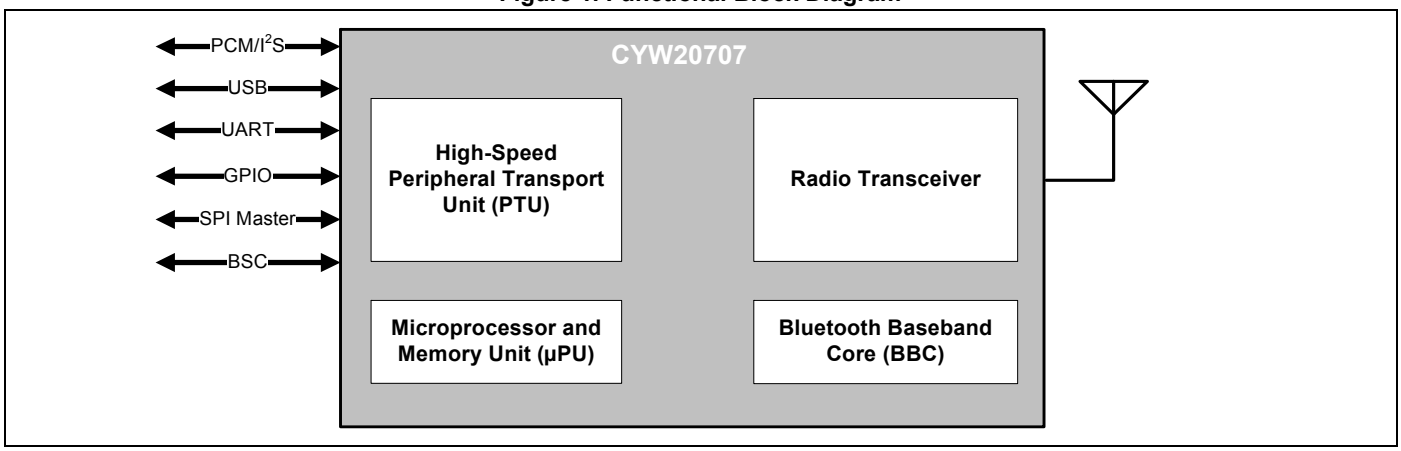
Features

- Complies with Bluetooth Core Specification Version 4.1+ HS with provisions for supporting future specifications
- Bluetooth Class 1 or Class 2 transmitter operation
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets
- Adaptive frequency hopping (AFH) for reducing radio frequency interference
- Interface support for USB or high-speed UART interface and PCM for audio data
- USB2.0 full-speed (12 Mbps)
- Supports Cypress proprietary 2 Mbps low energy mode.
- Ultra-low power consumption
- Supports serial flash interfaces
- Available in a 49-ball FcBGA package
- Supports mobile and PC applications without external memory
- 125-bump WLCSP available December 2014

Applications

- Home automation gateways, audio streaming, and other home automation use cases
- Bluetooth 4.1 embedded peripheral devices and accessories
- Personal digital assistants
- Automotive telematic systems

Figure 1. Functional Block Diagram



IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

Contents

1. Overview

The Cypress CYW20707 complies with Bluetooth Core Specification, version 4.1+ HS and is designed for use in embedded BT4.1 and UART/USB HCI applications. The combination of the Bluetooth Baseband Core (BBC), a Peripheral Transport Unit (PTU), and a Cortex-M3 based microprocessor with on-chip ROM provides a lower and upper layer Bluetooth stack, including Link Controller (LC), Link Manager (LM), and HCI.

1.1 Major Features

Major features of the CYW20707 include:

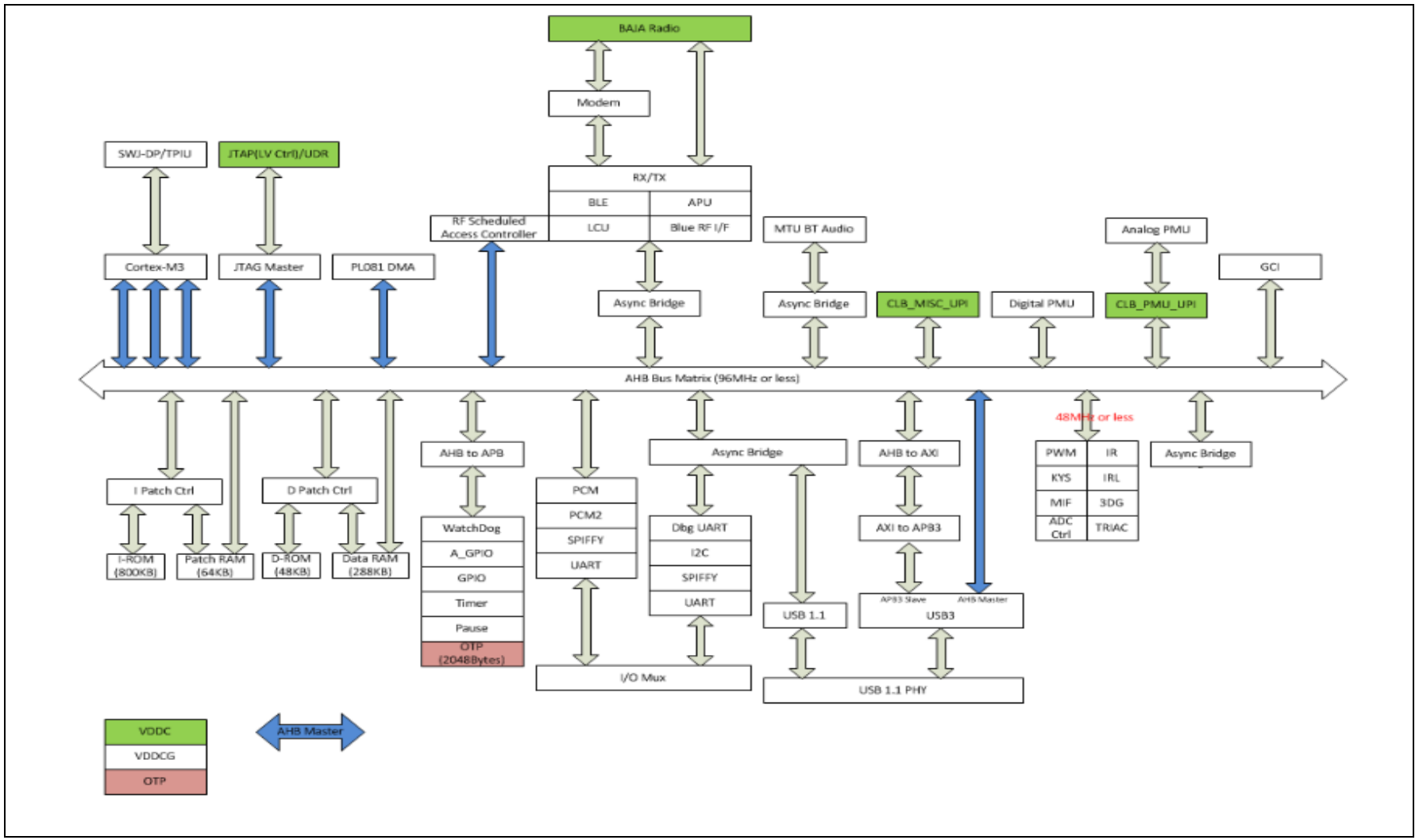
- Bluetooth v4.1 + EDR with integrated Class 1 PA
- BT host digital interface (can be used concurrently with below interfaces):
  - USB 2.0 full-speed (up to 12 Mbps)
  - UART (up to 4 Mbps)42
- Integrated RF section
  - Single-ended, 50Ω RF interface
  - Built-in TX/RX switch functionality
  - TX Class 1 output power capability
  - RX sensitivity basic rate of –93.5 dBm
  - RX sensitivity for Low Energy of –96.5 dBm
- GCI-enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives
- Supports maximum Bluetooth data rates over HCI UART, USB, and SPI interfaces
- I^2S/PCM for BT audio
- High-speed UART (H4, H4+) transport support
- Wideband speech support (16 bits linear data, MSB first, left-justified at 4K samples/s for transparent air coding, both through I^2S and PCM interface)
- Bluetooth SmartAudio® technology improves voice and music quality to headsets
- Bluetooth low-power inquiry and page scan
- Bluetooth low energy (BLE) support
- Supports Cypress proprietary 2 Mbps low energy mode
- Maximum of 100 LE Connections
- Supports TBFC (Triggered Cypress [Bluetooth] Fast Connect)
- Bluetooth packet loss concealment (PLC)
- Bluetooth wide band speech (WBS)
- High-speed UART transport support
  - H4 five-wire UART (four signal wires, one ground wire)
  - Maximum UART baud rates of 4 Mbps
  - Low-power out-of-band BT_WAKE and HOST_WAKE signaling
  - Proprietary compression scheme (allows more than two simultaneous A2DP packets and up to five devices at a time)

- HCI USB transport support
  - USB version 2.0 full-speed compliant interface
  - UHE (proprietary method for emulating a human interface device (HID) at system boot up)
- Standard Bluetooth test modes
- Extended radio and production test mode features
- Full support for power savings modes:
  - Bluetooth standard sniff
  - Deep sleep modes and regulator shutdown
- Built-in LPO clock
- Larger patch RAM space to support future enhancements
- Serial flash Interface with native support for devices from several manufacturers
- One-Time Programmable (OTP) memory

1.2 Block Diagram

Figure 2 shows the interconnect of the major CYW20707 physical blocks and associated external interfaces.

Figure 2. Functional Block Diagram



1.3 Usage Model

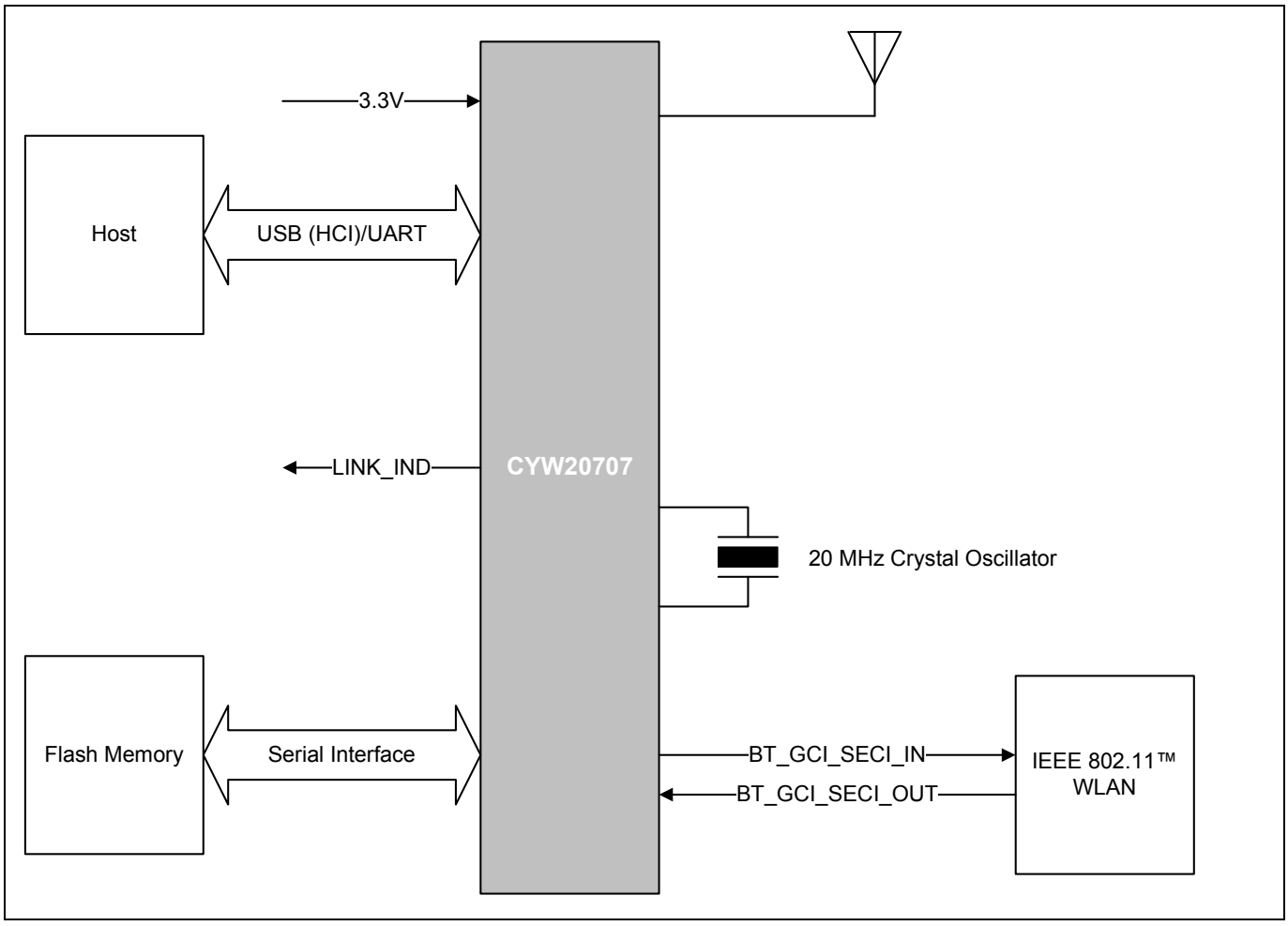
This section contains information on the Product Usage Model.

1.3.1 PC Product Usage Model

The CYW20707 can be directly interfaced using the UART interface, providing full support for embedded applications. The CYW20707 also supports applications such as external USB dongle peripheral devices.

Figure 3 shows an example of a typical PC product usage model.

Figure 3. A Typical Product Usage Model



2. Integrated Radio Transceiver

The CYW20707 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. The CYW20707 is fully compliant with the Bluetooth Radio Specification and enhanced data rate (EDR) specification and meets or exceeds the requirements to provide the highest communication link quality of service.

2.1 Transmit

The CYW20707 features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates p/4 – DQPSK for 2 Mbps and 8 – DPSK for 3 Mbps to support EDR. The transmitter section is compatible to the Bluetooth Low Energy specification. The transmitter PA bias can also be adjusted to provide Bluetooth class 1 or class 2 operation.

2.1.1 Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, pi/4 – DQPSK, and

8 – DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

2.1.2 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit-synchronization algorithm.

2.1.3 Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

2.2 Receiver

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology with built-in out-of-band attenuation enables the CYW20707 to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

2.2.1 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

2.2.2 Receiver Signal Strength Indicator

The radio portion of the CYW20707 provides a Receiver Signal Strength Indicator (RSSI) signal to the baseband, so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

2.3 Local Oscillator Generation

Local Oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The CYW20707 uses an internal RF and IF loop filter.

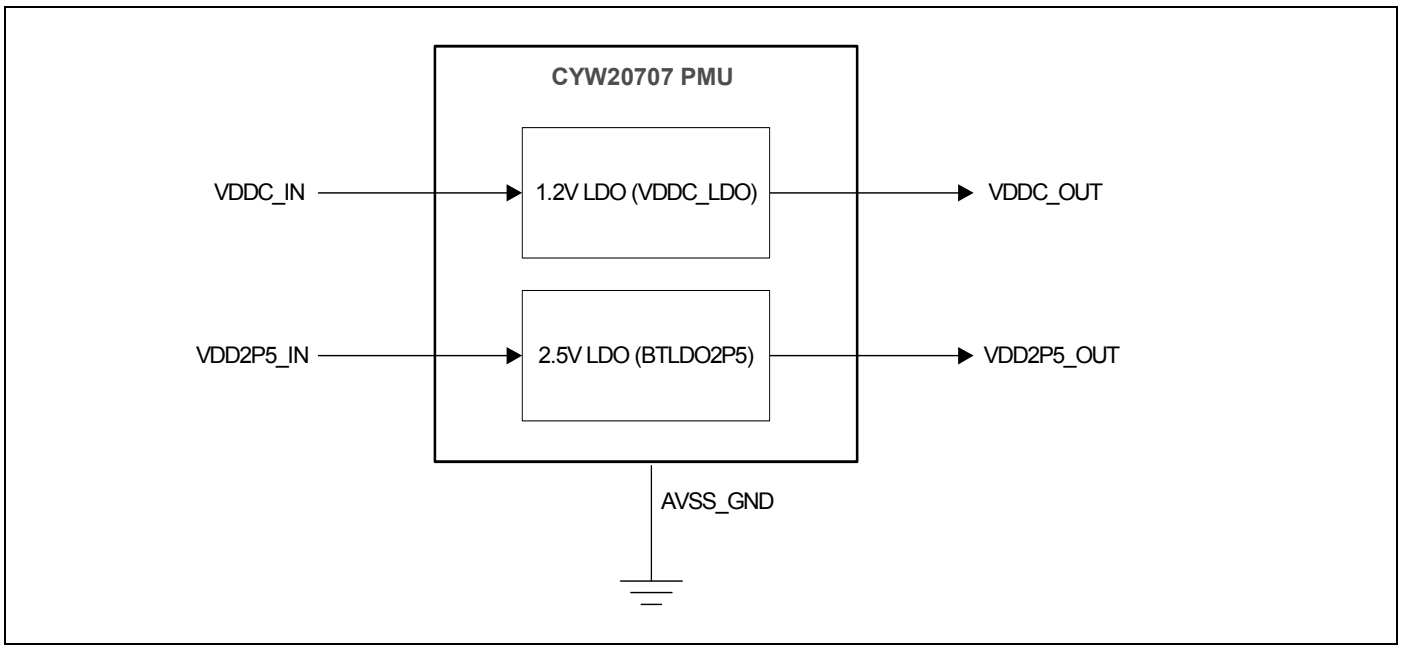
2.4 Calibration

The CYW20707 radio transceiver features an automated calibration scheme that is fully self contained in the radio. No user interaction is required during normal operation or during manufacturing to provide the optimal performance. Calibration optimizes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

2.5 Internal LDO

The CYW20707 uses two LDOs—one for 1.2V and the other for 2.5V. The 1.2V LDO is used to provide the power supply to the baseband and the radio while the 2.5V LDO is used for the PA power supply.

Figure 4. LDO Functional Block



3. Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.

Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

3.1 Bluetooth Low Energy

The CYW20707 supports dual-mode Bluetooth Low Energy (BT and BLE) operation.

3.2 Bluetooth 4.1 Features

The CYW20707 supports the new features expected in Bluetooth v4.1.

- Secure connections (LE/BR/EDR)
- Fast advertising interval
- Piconet clock adjust
- Clock nudging
- Connectionless Broadcast
- LE enhanced privacy
- Low duty cycle directed advertising
- LE dual mode topology

3.3 Bluetooth 4.0 Features

The CYW20707 supports all Bluetooth 4.0 features, with the following benefits:

- Extended Inquiry Response (EIR)
- Encryption Pause Resume (EPR)
- Sniff Subrating (SSR)
- Secure Simple Pairing (SSP)
- Link Supervision Time Out (LSTO)
- QoS enhancements

3.4 Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task performs a different state in the Bluetooth Link Controller.

- Major states:
  - Standby
  - Connection
- Substates:
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff

3.5 Test Mode Support

The CYW20707 fully supports Bluetooth Test mode as described in Specification of the Bluetooth Core v4.1, which includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence. In addition to the standard Bluetooth Test Mode, the CYW20707 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing, including:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern, PRBS-9, or PRBS-15
  - Enables modulated signal measurements with standard RF test equipment

3.6 Power Management Unit

The Power Management Unit (PMU) provides power management features that can be invoked through power management registers or packet handling in the baseband core. This section contains descriptions of the PMU features.

3.6.1 RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver. The transceiver then processes the power-down functions, accordingly.

3.6.2 SoC Power Management

The host can place the device in a sleep state, in which all nonessential blocks are powered off and all nonessential clocks are disabled. Power to the digital core is maintained so that the state of the registers and RAM is not lost. In addition, the CYW20707 internal LPO clock is applied to the internal sleep controller so that the chip can wake automatically at a specified time or based on signaling from the host. The goal is to limit the current consumption to a minimum, while maintaining the ability to wake up and resume a connection with minimal latency.

If a scan or sniff session is enabled while the device is in Sleep mode, the device automatically will wake up for the scan/sniff event, then go back to sleep when the event is done. In this case, the device uses its internal LPO-based timers to trigger the periodic wake up. While in Sleep mode, the transports are idle. However, the device can wake up at any time. If signaled to wake up while a scan or sniff session is in progress, the session continues but the device will not sleep between scan/sniff events. Once Sleep mode is enabled, the wake signaling mechanism can also be thought of as a sleep signaling mechanism, since removing the wake status will often cause the device to sleep.

In addition to a Bluetooth device wake signaling mechanism, there is a host wake signaling mechanism. This feature provides a way for the Bluetooth device to wake up a host that is in a reduced power state.

There are two mechanisms for the device and the host to signal wake status to each other:

USB	When running in USB mode the device supports the USB version 2.0 full-speed specification, suspend/resume signaling, as well as remote wake-up signaling for power control.
Bluetooth device WAKE (BT_DEV_WAKE) and Host WAKE (and BT_HOST_WAKE) signaling	The BT_DEV_WAKE signal allows the host to wake the BT device, and BT_HOST_WAKE is an output that allows the BT device to wake the host.

Table 2. Power Control Pin Summary

Pin	Direction	Description
BT_DEV_WAKE	Host output BT input	Bluetooth device wake-up: Signal from the host to the Bluetooth device that the host requires attention. ■ Asserted = Bluetooth device must wake up or remain awake. ■ Deasserted = Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low. By default, BT_DEV_WAKE is active-low (if BT-WAKE is low it requires the device to wake up or remain awake). For USB applications, this can be used for radio disable mode.
BT_HOST_WAKE	BT output Host input	Host wake-up. Signal from the Bluetooth device to the host indicating that Bluetooth device requires attention. ■ Asserted = Host device must wake up or remain awake. ■ Deasserted = Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
BT_CLK_REQ	BT output	Clock request ■ Asserted = External clock reference required ■ Deasserted = External clock reference may be powered down
RST_N	BT input	Used to place the chip in reset. RST_N is active-low.

3.6.3 Bluetooth Baseband Core Power Management

The following are low-power operations for the Bluetooth Baseband Core (BBC):

- Physical layer packet-handling turns the RF on and off dynamically within transmit/receive packets.
- Bluetooth-specified low-power connection modes: sniff, hold, and park. While in these modes, the CYW20707 runs on the low-power oscillator and wakes up after a predefined time period.

3.7 Adaptive Frequency Hopping

The CYW20707 supports host channel classification and dynamic channel classification Adaptive Frequency Hopping (AFH) schemes, as defined in the Bluetooth specification.

Host channel classification enables the host to set a predefined hopping map for the device to follow.

If dynamic channel classification is enabled, the device gathers link quality statistics on a channel-by-channel basis to facilitate channel assessment and channel map selection. To provide a more accurate frequency hop map, link quality is determined using both RF and baseband signal processing.

3.8 Collaborative Coexistence

The CYW20707 provides extensions and collaborative coexistence to the standard Bluetooth AFH for direct communication with WLAN devices. Collaborative coexistence enables WLAN and Bluetooth to operate simultaneously in a single device. The device supports industry-standard coexistence signaling, including 802.15.2, and supports Cypress and third-party WLAN solutions.

3.9 Global Coexistence Interface

The CYW20707 support the proprietary Cypress Global Coexistence Interface (GCI) which is a 2-wire interface.

The following key features are associated with the interface:

- Enhanced coexistence data can be exchanged over GCI_SECI_IN and GCI_SECI_OUT a two-wire interface, one serial input (GCI_SECI_IN), and one serial output (GCI_SECI_OUT). The pad configuration registers must be programmed to choose the digital I/O pins that serve the GCI_SECI_IN and GCI_SECI_OUT function.
- It supports generic UART communication between WLAN and Bluetooth devices.
- To conserve power, it is disabled when inactive.
- It supports automatic resynchronizaton upon waking from sleep mode.
- It supports a baud rate of up to 4 Mbps.

3.9.1 SECI I/O

The CYW20707 devices have dedicated GCI_SECI_IN and GCI_SECI_OUT pins. The two pin functions can be mapped to any of the Cypress Global Co-existence Interface (GCI) GPIO. Pin function mapping is controlled by the configuration file that is stored in either NVRAM or downloaded directly into on-chip RAM from the host.

4. Microprocessor Unit

4.1 Overview

The CYW20707 microprocessor unit runs software from the Link Control (LC) layer up to the stack and Application layer. In the HCI mode of operation the stack will be run on the external host. The microprocessor is based on the Cortex-M3 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. The microprocessor also includes 848 KB of ROM memory for program storage and boot ROM, 352 KB of RAM for data scratch-pad, and patch RAM code.

The internal boot ROM provides flexibility during power-on reset to enable the same device to be used in various configurations, including automatic host transport selection from UART and USB transports with or without external NVRAM. At power-up, the lower layer protocol stack is executed from the internal ROM.

External patches can be applied to the ROM-based firmware to provide flexibility for bug fixes and features additions. These patches can be downloaded from the host to the device through the SPI interface or UART and USB transports, or using external NVRAM. The device can also support the integration of user applications and profiles using an external serial flash memory.

4.2 NVRAM Configuration Data and Storage

4.2.1 Serial Interface

The CYW20707 includes an SPI master controller that can be used to access serial flash memory. The SPI master contains an AHB slave interface, transmit and receive FIFOs, and the SPI core PHY logic. Data is transferred to and from the module by the system CPU. DMA operation is not supported.

4.3 EEPROM

The CYW20707 includes a Broadcom Serial Control (BSC) master interface. The BSC interface supports low-speed and fast mode devices and is compatible with I^2C slave devices. Multiple I^2C master devices and flexible wait state insertion by the master interface or slave devices are not supported. The CYW20707 provides 400 kHz, full speed clock support.

The BSC interface is programmed by the CPU to generate the following BSC transfer types on the bus:

- Read-only
- Write-only
- Combined read/write
- Combined write-read

NVRAM may contain configuration information about the customer application, including the following:

- Fractional-N information
- BD_ADDR
- UART baud rate
- USB enumeration information
- SDP service record
- File system information used for code, code patches, or data

4.4 External Reset

The CYW20707 has an integrated power-on reset circuit which completely resets all circuits to a known power on state. This action can also be driven by an external reset signal, which can be used to externally control the device, forcing it into a power-on reset state. The RST_N signal is an active-low signal, which is an input to the CYW20707 chip. The CYW20707 does not require an external pull-up resistor on the RST_N input.

4.5 One-Time Programmable Memory

The CYW20707 includes a One-Time Programmable (OTP) memory, allowing manufacturing customization and avoiding the need for an on-board NVRAM.If customization is not required, then the OTP does not need to be programmed. Whether the OTP is programmed or not, it is disabled after the boot process completes to save power.

The OTP size is 2048 bytes.

The OTP is designed to store a minimal amount of information. Aside from OTP data, most user configuration information will be downloaded into RAM after the CYW20707 boots up and is ready for host transport communication. The OTP contents are limited to:

- Parameters required prior to downloading user configuration to RAM.
- Parameters unique to each part and each customer (i.e., the BD_ADDR, software license key, and USB PID/VID).

The OTP memory is particularly useful in a PC design with USB transport capability because:

- Some customer-specific information must be configured before enumerating the part on the USB transport.
- Part or customer unique information (BD_ADDR, software license key, and USB PID/VID) do not need to be stored on the host system.

4.5.1 Contents

The following are typical parameters programmed into the OTP memory:

- BD_ADDR
- Software license key
- USB PID/VID
- USB bus/self-powered status
- Output power calibration
- Frequency trimming
- Initial status LED drive configuration

The OTP contents also include a static error correction table to improve yield during the programming process as well as forward error correction codes to eliminate any long-term reliability problems. The OTP contents associated with error correction are not visible by customers.

4.5.2 Programming

OTP memory programming takes place through a combination of Cypress software integrated with the manufacturing test software and code embedded in CYW20707 firmware.

5. Peripheral Transport Unit

This section discusses the PCM, USB, UART, I^2S, and SPI peripheral interfaces. The CYW20707 has a 1040-byte transmit and receive FIFO, which is large enough to hold the entire payload of the largest EDR BT packet (3-DH5).

5.1 PCM Interface

The CYW20707 supports two independent PCM interfaces that share the pins with the I2S interfaces. The PCM Interface on the CYW20707 can connect to linear PCM codec devices in master or slave mode. In master mode, the CYW20707 generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the CYW20707.

The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

5.1.1 Slot Mapping

The CYW20707 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

5.1.2 Frame Synchronization

The CYW20707 supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

5.1.3 Data Formatting

The CYW20707 may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the CYW20707 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

5.1.4 Wideband Speech Support

When the host encodes Wideband Speech (WBS) packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 Kbps bit rate. The CYW20707 also supports slave transparent mode using a proprietary rate-matching scheme. In SBC-code mode, linear 16-bit data at 16 kHz (256 Kbps rate) is transferred over the PCM bus.

5.1.5 Burst PCM Mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24 MHz. This mode of operation is initiated with an HCI command from the host.

5.2 HCI Transport Detection Configuration

Note: HCI transport detection is only valid for the HCI operating mode.

The CYW20707 supports the following interface types for the HCI transport from the host:

- UART (H4)
- USB

Only one host interface can be active at a time. The firmware performs a transport detect function at boot-time to determine which host is the active transport. It can auto-detect UART and USB interfaces, but the SPI interface must be selected by strapping the SCL pin to 0.

The complete algorithm is summarized as follows:

1. Determine if any local NVRAM contains a valid configuration file. If it does and a transport configuration entry is present, select the active transport according to entry, and then exit the transport detection routine.
2. Look for start-of-frame (SOF) on the USB interface. If it is present, select USB.
3. Look for CTS_N = 0 on the UART interface. If it is present, select UART.
4. Repeat Step 2 and Step 3 until transport is determined.

5.3 USB Interface

5.3.1 Features

The following USB interface features are supported:

- USB Protocol, Revision 2.0, full-speed compliant (up to 12 Mbps)
- Global and selective suspend and resume with remote wake-up
- Optional Bluetooth HCI
- HID, DFU, UHE (proprietary method to emulate an HID device at system boot)
- Integrated detach resistor

Note: If the USB transport is not used, tie the CYW20707 USB pins and VDD_USB to groun

5.3.2 Operation

The CYW20707 can be configured to boot up as a single USB peripheral, and the host detects a single USB Bluetooth device. This configuration is typically used in a standalone mode. Other embedded mode applications may not be used at the same time as the UHE mode described below.

The CYW20707 can boot up showing the independent interfaces connected to logical USB devices internal to the CYW20707—a generic Bluetooth device, a mouse, and a keyboard. In this mode, the mouse and keyboard are emulated devices, since they connect to real HID devices via a Bluetooth link. The Bluetooth link to these HID devices is hidden from the USB host. To the host, the mouse and/or keyboard appear to be directly connected to the USB port. This Cypress proprietary architecture is called USB HID Emulation (UHE).

The USB device, configuration, and string descriptors are fully programmable, allowing manufacturers to customize the descriptors, including vendor and product IDs, the CYW20707 uses to identify itself on the USB port. To make custom USB descriptor information available at boot time, stored it in external NVRAM.

In the single USB peripheral operating mode, the Bluetooth device is configured to include the following interfaces:

Interface 0	Contains a Control endpoint (Endpoint 0x00) for HCI commands, a Bulk In Endpoint (Endpoint 0x82) for receiving ACL data, a Bulk Out Endpoint (Endpoint 0x02) for transmitting ACL data, and an Interrupt Endpoint (Endpoint 0x81) for HCI events.
Interface 1	Contains Isochronous In and Out endpoints (Endpoints 0x83 and 0x03) for SCO traffic. Several alternate Interface 1 settings are available for reserving the proper bandwidth of isochronous data (depending on the application).
Interface 2	Contains Bulk In and Bulk Out endpoints (Endpoints 0x84 and 0x04) used for proprietary testing and debugging purposes. These endpoints can be ignored during normal operation.

5.3.3 UHE Support

The CYW20707 supports the USB device model (USB 2.0-compatible, full-speed compliant). Optional mouse and keyboard interfaces utilize Cypress's proprietary USB HID Emulation (UHE) architecture, which allows these Bluetooth devices appear as standalone HID devices even though connected through a Bluetooth link.

The presence of UHE devices requires the CYW20707 to be configured as a composite device (Composite mode). In this mode, the Bluetooth mouse and keyboard interfaces are independently controlled and appear as standalone logical devices.

Cypress's standard composite configuration uses the following layout:

- Interface 0 – Keyboard
- Interface 1 – Mouse
- Interface 2/3/4 – Bluetooth (as described above)

When operating in Composite mode, every interface does not have to be enabled—each can be optionally enabled. The configuration record in NVRAM determines which devices are present.

5.4 UART Interface

The CYW20707 shares a single UART for Bluetooth. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 4.1 UART HCI specification: H4, and a custom Extended H4. The default baud rate is 115.2 Kbaud.

The CYW20707 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The CYW20707 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Table 3. Example of Common Baud Rates

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

5.5 Simultaneous UART Transport and Bridging

Note: Simultaneous UART transport and bridging is only valid for the HCI operating mode.

The CYW20707 supports UART or USB interfaces that can function as the host controller interface (HCI). Typically, a customer application would choose one of the two interfaces and the other would be idle. The CYW20707 allows the UART transport to operate simultaneously with the USB. To operate this way, the assumption is that the USB would function as the primary host transport, while the UART would function as a secondary communication channel that can operate at the same time. This can enable the following applications:

- Bridging primary HCI transport traffic to another device via the UART
- Generic communication to an external device for a vendor-supported application via the UART

Simultaneous UART transport and bridging is enabled by including:

- Two dedicated 64-byte FIFOs, one for the input and one for the output
- Additional DMA channels
- Additional vendor-supported commands over the HCI transport

6. Frequency References

The CYW20707 uses an external crystal for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference can be used.

6.1 Crystal Interface and Clock Generation

The CYW20707 uses a fractional-N synthesizer to generate the radio frequencies, clocks, and data/packet timing, enabling it to operate from any of a multitude of frequency sources. The source can be external, such as a crystal interfaced directly to the device or an external frequency reference can be used.

Typical crystal frequencies of 20 MHz and 40 MHz are supported using the XTAL_STRAP_1 pin on the CYW20707. The signal characteristics for the crystal interface are listed in Table 4 on page 20.

Table 4. Crystal Interface Signal Characteristics

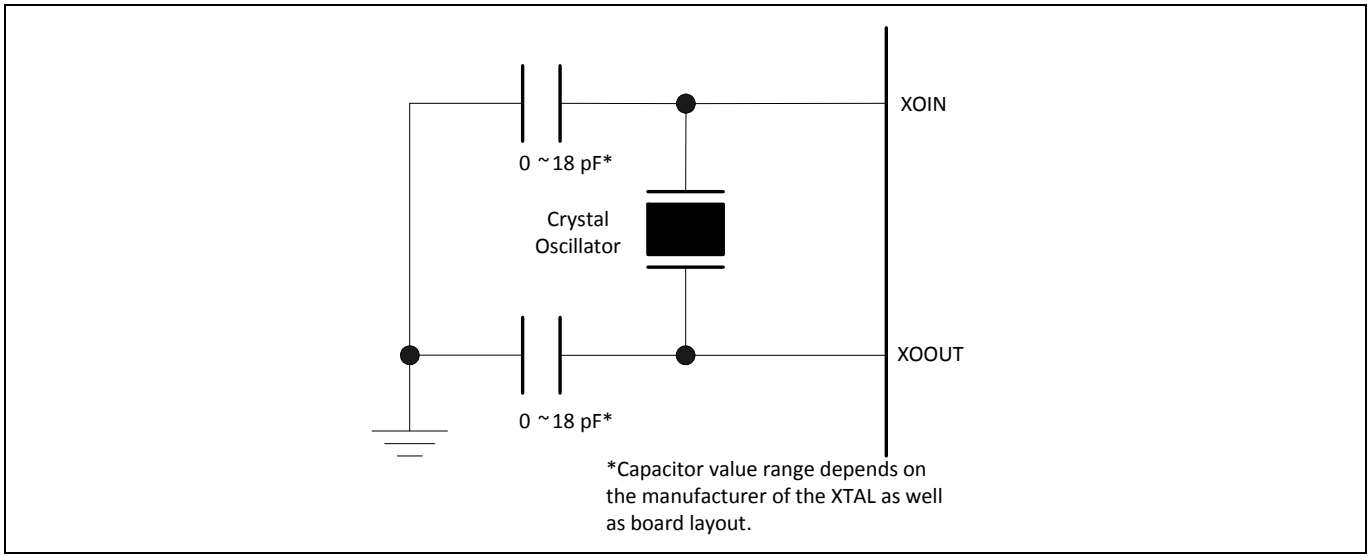
Parameter	Crystal	External Frequency Reference	Units
Acceptable frequencies	19.2–52 MHz in 2 ppm[a] steps	12–52 MHz in 2 ppm[a] steps	–
Crystal load capacitance	12 (typical)	N/A	pF
ESR	100 (max)	–	Ω
Power dissipation	200 (max)	–	µW
Input signal amplitude	N/A	400 to 1200 2000 to 3300 (requires a 10 pF DC blocking capacitor to attenuate the signal)	mVp-p
Signal type	N/A	Square-wave or sine-wave	–
Input impedance	N/A	≥1 ≤2	MΩ pF
Phase noise @ 1 kHz @ 10 kHz @ 100 kHz @ 1 MHz	N/A N/A N/A N/A N/A	– < –120 < –130 < –135 < –136	– dBc/Hz dBc/Hz dBc/Hz dBc/Hz
Tolerance without frequency trimming[b]	±20	±20	ppm
Initial frequency tolerance trimming range	±50	±50	ppm

a. The frequency step size is approximately 80 Hz resolution.
b. AT-Cut crystal or TXCO recommended.

6.2 Crystal Oscillator

The CYW20707 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator, including all external components, is shown in Figure 5.

Figure 5. Recommended Oscillator Configuration



6.3 Frequency Selection

Any frequency within the range specified for the crystal and frequency reference can be used. Since bit timing is derived from the reference frequency, the CYW20707 must have the reference frequency set correctly in order for any of the USB, UART, and PCM interfaces to function properly.

The CYW20707 reference frequency can be selected by using BT_XTAL_STRAP_1. The typical crystal frequencies of 20 MHz and 40 MHz are supported.

The GPIO_2 needs to be tied to ground.

Clock (MHz):	XTAL_Strap_1 (Pin-F2)
40:	Low
20:	High

If the application requires a frequencies other than these, the value can be stored in an external NVRAM. Programming the reference frequency in NVRAM provides the maximum flexibility in the selection of the reference frequency, since any frequency within the specified range for crystal and external frequency reference can be used. During power-on reset (POR), the device downloads the parameter settings stored in NVRAM, which can be programmed to include the reference frequency and frequency trim values. Typically, this is how a PC Bluetooth application is configured.

6.4 Frequency Trimming

The CYW20707 uses a fractional-N synthesizer to digitally fine-tune the frequency reference input to within ±2 ppm tuning accuracy. This trimming function can be applied to either the crystal or an reference frequency source. Unlike the typical crystal-trimming methods used, the CYW20707 changes the frequency using a fully digital implementation and is much more stable and unaffected by crystal characteristics or temperature. Input impedance and loading characteristics remain unchanged on the crystal during the trimming process and are unaffected by process and temperature variations.

The option to use or not use frequency trimming is based on the system designer's cost trade-off between bill-of-materials (BOM) cost of the crystal and the added manufacturing cost associated with frequency trimming. The frequency trimming value can either be stored in the host and written to the CYW20707 as a vendor-specific HCI command or stored in NVRAM and subsequently recalled during POR.

Frequency trimming is not a substitute for the poor use of tuning capacitors at an crystal oscillator (XTAL). Occasionally, trimming can help alleviate hardware changes.

7. Pin-out and Signal Descriptions

7.1 Pin Descriptions

Table 5. CYW20707 Signal Descriptions

Signal	FcBGA Pin (49-Ball)	I/O	Power Domain	Description
Radio				
RFOP	A2	I/O	VDD_RF	RF I/O antenna port
XO_IN	A4	I	VDD_RF	Crystal or reference input
XO_OUT	A5	O	VDD_RF	Crystal oscillator output
Voltage Regulators				
VBAT	D1	I	N/A	VBAT input pin
VDD2P5_IN	E1	I	N/A	2.5V LDO input
VDD2P5_OUT	E2	O	N/A	2.5V LDO output
VDDC_OUT	F1	O	N/A	1.2V LDO output
Straps				
BT_XTAL_STRAP_1	F2	I	VDDO	This pin is used as strap for choosing the XTAL frequencies.
RST_N	A6	I	VDDO	Active-low reset input
BT_TM1	G7	I	VDDO	Reserved: connect to ground.
Digital I/O				
BT_GPIO_0	F8	I	VDDO	BT_GPIO_0/BT_DEV_WAKE A signal from the host to the CYW20707 device that the host requires attention.
BT_GPIO_1	F7	O	VDDO	BT_GPIO_1/BT_HOST_WAKE A signal from the CYW20707 device to the host indicating that the Bluetooth device requires attention.
BT_GPIO_2	E4	I	VDDO	When high, this signal extends the XTAL warm-up time for external CLK requests. Otherwise, it is typically connected to ground.
BT_GPIO_3	C5	I/O	VDDO	General-purpose I/O.
BT_GPIO_4	D6	I/O	VDDO	General-purpose I/O. It can also be configured as a GCI pin.
BT_GPIO_5	B5	I/O	VDDO	General-purpose I/O. It can also be configured as a GCI pin.
BT_GPIO_6	B6	I/O	VDDO	General-purpose I/O. It can also be configured as a GCI pin.
BT_GPIO_7	C6	I/O	VDDO	General-purpose I/O. It can also be configured as a GCI pin.
BT_UART_RXD	F5	I/O	VDDO	UART receive data
BT_UART_TXD	F4	I/O	VDDO	UART transmit data
BT_UART_RTS_N	F3	I/O	VDDO	UART request to send output
BT_UART_CTS_N	G4	I/O	VDDO	UART clear to send input
BT_CLK_REQ	G8	O	VDDO	This pin is used for shared-clock application.
SPI2_MISO_I2S_SCL	D8	I/O	VDDO	BSC clock
SPI2_MOSI_I2S_SDA	E8	I/O	VDDO	BSC data
SPI2_CLK	E7	I/O	VDDO	Serial flash SPI clock
SPI2_CSN	D7	I/O	VDDO	Serial flash active-low chip select

Table 5. CYW20707 Signal Descriptions (Cont.)

Signal	FcBGA Pin (49-Ball)	I/O	Power Domain	Description
I2S_DI/PCM_IN	C7	I/O	VDDO	PCM/I2S data input
I2S_DO/PCM_OUT	A8	I/O	VDDO	PCM/I2S data output
I2S_CLK/PCM_CLK	B7	I/O	VDDO	PCM/I2S clock
I2S_WS/PCM_SYNC	C8	I/O	VDDO	PCM sync/I2S word select
USB				
BT_HUSB_DP	G2	I/O	VDD_USB	USB D+ signal. If not used, connect to GND.
BT_HUSB_DN	G3	I/O	VDD_USB	USB D- signal. If not used, connect to GND.
JTAG				
JTAG_SEL	D5	I/O	VDDO	Used for debugging
Supplies				
BT_VDD_USB	G1	I	N/A	3.3V USB transceiver supply voltage. If the USB transport is not needed, connect this pin to GND.
BT_IFVDD1P2	B4	I	N/A	Radio IF PLL supply
BT_PAVDD2P5	A1	I	N/A	Radio PA supply
BT_LNAVDD1P2	B1	I	N/A	Radio LNA supply
BT_VCOVDD1P2	C1	I	N/A	Radio VCO supply
BT_PLLVDD1P2	A3	I	N/A	Radio RF PLL supply
VDDC	B8, G6	I	N/A	Core logic supply
VDDO	G5	I	N/A	Digital I/O supply voltage
VSS	A7, B2, B3, C2, D2, F6	–	N/A	Ground

8. Ball Grid Arrays

Figure 6 shows the top view of the 49-ball 4.5 mm x 4 mm x 0.8 mm (FcBGA).

Figure 6. 4.5 mm x 4 mm x 0.8 mm (FcBGA) Array

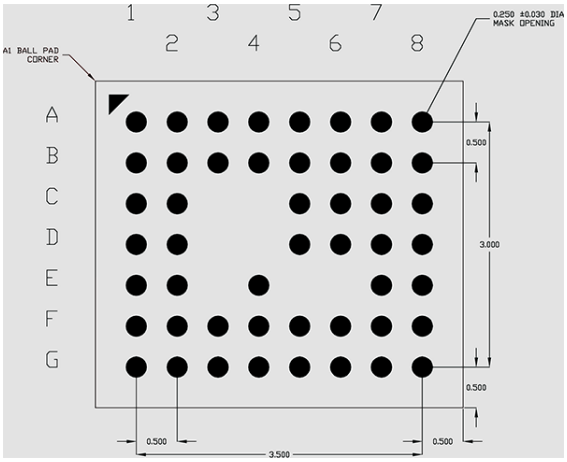


Figure 7. Ball-Out for the 49-Ball FcBGA

	1	2	3	4	5	6	7	8
A	BT_ PAVDD2P5	RFOP	BT_ PLLVDD1P2	XO_IN	XO_OUT	RST_N	VSSC	I2S_DO/ PCM_OUT
B	BT_LNAVDD1 P2	VSS	VSS	BT_ IFVDD1P2	BT_GPIO_5	BT_GPIO_6	I2S_CLK/ PCM_CLK	VDDC
C	BT_ VCOVDD1P2	VSS			BT_GPIO_3	BT_GPIO_7	I2S_DI/ PCM_IN	I2S_WS/ PCM_SYNC
D	VBAT	VSS			JTAG_SEL	BT_GPIO_4	SPI2_CSN	SPI2_MISO_ I2C_SCL
E	VDD2P5_IN	VDD2P5_ OUT		BT_GPIO_2			SPI2_CLK	SPI2_MOSI_ I2C_SDA
F	VDDC_OUT	BT_XTAL _STRAP_1	BT_UART _RST_N	BT_UART _TXD	BT_UART _RXD	VSS	BT_GPIO_1/ BT_HOST_ WAKE	BT_GPIO_0/ BT_DEV _WAKE
G	BT_VDD _USB	BT_HUSB _DP	BT_HUSB _DN	BT_UART _CTS_N	VDDO	VDDC	BT_TM1	BT_CLK _REQ

9. Electrical Characteristics

Note: All voltages listed in Table 6 are referenced to V_{DD}.

Table 6. Absolute Maximum Voltages

Requirement Parameter	Specification			Units
	Minimum	Nominal	Maximum	
Ambient Temperature of Operation	–30	25	85	°C
Storage temperature	–40	–	150	°C
ESD Tolerance HBM	–2000	–	2000	V
ESD Tolerance MM	–100	–	100	V
ESD Tolerance CDM	–500	–	500	V
Latch-up	TBD	TBD	TBD	TBD
VDD Core	1.14	1.2	1.26	V
VDD IO	3	3.3	3.6	V
VDD RF (excluding class 1 PA)	1.14	1.2	1.26	V
VDD PA (class 1 mode)	2.25	2.5	2.75	V

Table 7. Power Supply Specifications

Parameter	Conditions	Min.	Typ.	Max.	Units
VBAT input	–	1.62	3.3	3.6	V
2.5V LDO input	–	3.0	3.3	3.6	V

Table 8. VDDC LDO Electrical Specifications

Parameter	Conditions		Min.	Typ.	Max.	Units
Input Voltage	–		1.62	3.3	3.6	V
Nominal Output Voltage	–		–	1.2	–	V
DC Accuracy	Accuracy at any step, including bandgap reference.		–5	–	5	%
Output Voltage Programmability	Range		0.89	–	1.34	V
	Step Size		–	30	–	mV
Load Current	–		–	–	40	mA
Dropout Voltage	I_{load} = 40 mA		–	–	200	mV
Line Regulation	Vin from 1.62V to 3.6V, I_{load} = 40 mA		–	–	0.2	%Vo/V
Load Regulation	I_{load} = 1 mA to 40 mA, Vout = 1.2V, Package + PCB R = 0.3Ω		–	0.02	0.05	%Vo/mA
Quiescent Current	No load @Vin = 3.3V		–	18	23	µA
	Max load @Vin = 3.3V		–	–	0.56 0.65	mA
Power Down Current	Vin = 3.3V @25C		–	0.2	–	µA
PSRR	Vin = 3.3, Vout = 1.2V, I_{load} = 40 mA	1 kHz	65	–	–	dB
		10 kHz	60	–	–	dB
		100 kHz	55	–	–	dB
Over Current Limit	–		100	–	–	mA

Table 8. VDDC LDO Electrical Specifications (Cont.)

Parameter	Conditions	Min.	Typ.	Max.	Units
Turn-on Time	VBAT = 3.3V, BG already on, LDO OFF to ON, Co = 1 µF, 90% of Vout	–	–	100	µs
External Output Capacitor	Ceramic cap with ESR ≤0.5Ω	0.8	1	4.7	µF
External Input Capacitor	Ceramic, X5R, 0402, ±20%, 10V.	–	1	–	µF

Table 9. BTLDO_2P5 Electrical Specifications

Parameters	Conditions	Min	Typ	Max	Units
Input supply voltage, Vin	Min = Vo + 0.2V = 2.7V (for Vo = 2.5V) Dropout voltage requirement must be met under maximum load for performance specs.	3.0	3.3	3.6	V
Nominal output voltage, Vo	Default = 2.5V	–	2.5	–	V
Output voltage programmability	Range Accuracy at any step (including line/load regulation), load >0.1 mA	2.2 –5	–	2.8 5	V %
Dropout voltage	At max load	–	–	200	mV
Output current	–	0.1	–	70	mA
Quiescent current	No load; Vin = Vo + 0.2V Max load @ 70 mA; Vin = Vo + 0.2V	–	8 660	16 700	µA
Leakage current	Power-down mode. At junction temperature 85°C.	–	1.5	5	µA
Line regulation	Vin from (Vo + 0.2V) to 3.6V, max load	–	–	3.5	mV/V
Load regulation	Load from 1 mA to 70 mA, Vin = 3.6V	–	–	0.3	mV/mA
PSRR	Vin ≥ Vo + 0.2V, Vo = 2.5V, Co = 2.2 µF, max load, 100 Hz to 100 kHz	20	–	–	dB
LDO turn-on time	LDO turn-on time when rest of chip is up	–	–	150	µs
External output capacitor, Co	Ceramic, X5R, 0402, (ESR: 5m-240 mΩ), ±20%, 6.3V	0.7	2.2	2.64	µF
External input capacitor	Ceramic, X5R, 0402, ±20%, 10V	–	1	–	µF

Table 10. Digital I/O Characteristics

Characteristics	Symbol	Minimum	Typical	Maximum	Unit
Input low voltage (VDDO = 3.3V)	V_{IL}	–	–	0.8	V
Input high voltage (VDDO = 3.3V)	V_{IH}	2.0	–	–	V
Output low voltage	V_{OL}	–	–	0.4	V
Output high voltage	V_{OH}	VDDO – 0.4V	–	–	V
Input low current	I_{IL}	–	–	1.0	µA
Input high current	I_{IH}	–	–	1.0	µA
Output low current (VDDO = 3.3V, V_{OL} = 0.4V)	I_{OL}	–	–	2.0	mA
Output high current (VDDO = 3.3V, V_{OH} = 2.9V)	I_{OH}	–	–	4.0	mA
Input capacitance	C_{IN}	–	–	0.4	pF

Table 11. USB Interface Level

Parameter	Symbol	Minimum	Typical	Maximum	Unit
I/O supply voltage	VDD_USB	3.0	–	3.6	V
Supply current	Icchpf	–	–	500	mA
Input high voltage (driven)	Vih	2.0	–	–	V
Input high voltage (floating)	Vihz	2.7	–	3.6	V
Input low voltage	Vil	–	–	0.8	V
Differential input sensitivity	Vdi	0.2	–	–	V
Differential common-mode range	Vcm	0.8	–	2.5	V
Output low voltage	Vol	0.0	–	0.3	V
Output high voltage (driven)	Voh	2.8	–	3.6	V
Output signal crossover voltage	Vcrs	1.3	–	2.0	V

Table 12. Current Consumption—Common Use Cases

Condition	Current (mA)
Receive (1 Mbps) current level when receiving a basic rate packet (TBD mA).	12.5
Transmit (1 Mbps) current level when transmitting a basic rate packet.	26.5
Receive (EDR) current level when receiving a 2 or 3 Mbps rate packet.	12.5
Transmit (EDR) current level when transmitting a 2 or 3 Mbps rate packet.	20.0
DM1/DH1 average current during a basic rate maximum throughput connection that includes only this packet type.	14.5
DM3/DH3 average current during a basic rate maximum throughput connection that includes only this packet type.	17.0
DM5/DH5 average current during a maximum basic rate throughput connection that includes only this packet type.	17.5
HV1 average current during an SCO voice connection consisting of only this packet type. The ACL channel is in 500 ms Sniff.	14.0
HV2 average current during an SCO voice connection consisting of only this packet type. The ACL channel is in 500 ms Sniff.	9.0
HV3 average current during an SCO voice connection consisting of only this packet type. The ACL channel is in 500 ms Sniff.	7.0
Sleep UART transport active. External LPO clock available (TBD µA).	0.120
Inquiry Scan (1.28 sec.). Periodic scan rate is 1.28 sec.	0.188
Page Scan (R1) Periodic scan rate is R1 (1.28 sec).	0.188
Inquiry Scan + Page Scan (R1) Both inquiry and page scans are interlaced together at a 1.28 seconds periodic scan rate.	0.286
Sniff master (500 ms) attempt and timeout parameters set to 4. Quality connection that rarely requires more than a minimum packet exchange.	0.415
Sniff slave (500 ms) attempt and timeout parameters set to 4. Quality connection that rarely requires more than a minimum packet exchange.	0.408
Sniff (500 ms) + Inquiry or Page Scan (R1)	0.700
Sniff (500ms) + Inquiry Scan + Page Scan (R1)	0.800

Note: The values in this table were calculated for a 90% efficient DC-DC at 3V in HCI mode, and based on a Class I configuration bench-marked at Class II. Lower values are expected for a class II configuration using an external LPO and corresponding PA configuration.

9.1 RF Specifications

Table 13. Receiver RF Specifications[a, b]

Parameter	Conditions	Minimum	Typical [c]	Maximum	Unit
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity [d]	GFSK, 0.1% BER, 1 Mbps	–	–93.5	–	dBm
	p/4-DQPSK, 0.01% BER, 2 Mbps	–	–95.5	–	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–89.5	–	dBm
Maximum input	GFSK, 1 Mbps	–	–	–20	dBm
Maximum input	p/4-DQPSK, 8-DPSK, 2/3 Mbps	–	–	–20	dBm
Interference Performance					
■ GFSK Modulation[e]					
C/I cochannel	GFSK, 0.1% BER	–	9.5	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–5	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–40	–30.0	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER	–	–49	–40.0	dB
C/I image channel	GFSK, 0.1% BER	–	–27	–9.0	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	–	–37	–20.0	dB
■ QPSK Modulation[f]					
C/I cochannel	p/4-DQPSK, 0.1% BER	–	11	13	dB
C/I 1 MHz adjacent channel	p/4-DQPSK, 0.1% BER	–	–8	0	dB
C/I 2 MHz adjacent channel	p/4-DQPSK, 0.1% BER	–	–40	–30.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–50	–40.0	dB
C/I image channel	p/4-DQPSK, 0.1% BER	–	–27	–7.0	dB
C/I 1 MHz adjacent to image channel	p/4-DQPSK, 0.1% BER	–	–40	–20.0	dB
■ 8PSK Modulation[g]					
C/I cochannel	8-DPSK, 0.1% BER	–	17	21	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	–	–5	5	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	–	–40	–25.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–47	–33.0	dB
C/I Image channel	8-DPSK, 0.1% BER	–	–20	0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	–	–35	–13.0	dB
Out-of-Band Blocking Performance (CW) [h]					
30 MHz–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm

Table 13. Receiver RF Specifications[a, b] (Cont.)

Parameter	Conditions	Minimum	Typical [c]	Maximum	Unit
Out-of-Band Blocking Performance, Modulated Interferer					
776–764 MHz	CDMA	–	–10 [i]	–	dBm
824–849 MHz	CDMA	–	–10 [i]	–	dBm
1850–1910 MHz	CDMA	–	–23 [i]	–	dBm
824–849 MHz	EDGE/GSM	–	–10 [i]	–	dBm
880–915 MHz	EDGE/GSM	–	–10 [i]	–	dBm
1710–1785 MHz	EDGE/GSM	–	–23 [i]	–	dBm
1850–1910 MHz	EDGE/GSM	–	–23 [i]	–	dBm
1850–1910 MHz	WCDMA	–	–23 [i]	–	dBm
1920–1980 MHz	WCDMA	–	–23 [i]	–	dBm
Intermodulation Performance [j]					
BT, Df = 4 MHz	–	–39.0	–	–	dBm
Spurious Emissions [k]					
30 MHz to 1 GHz	–	–	–	–62	dBm
1–12.75 GHz	–	–	–	–47	dBm
65–108 MHz	FM RX	–	–147	–	dBm/Hz
746–764 MHz	CDMA	–	–147	–	dBm/Hz
851–894 MHz	CDMA	–	–147	–	dBm/Hz
925–960 MHz	EDGE/GSM	–	–147	–	dBm/Hz
1805–1880 MHz	EDGE/GSM	–	–147	–	dBm/Hz
1930–1990 MHz	PCS	–	–147	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–147	–	dBm/Hz

a. All specifications are single ended. Unused inputs are left open.
b. All specifications, except typical, are for industrial temperatures.
c. Typical operating conditions are 3.3V VBAT and 25°C ambient temperature.
d. The receiver sensitivity is measured at BER of 0.1% on the device interface.
e. Typical GFSK CI numbers at –7 MHz, –5 MHz, and –3 MHz are –45 dB, –42 dB, and –41 dB, respectively.
f. Typical QPSK CI numbers at –7 MHz, –5 MHz, and –3 MHz are –46 dB, –43 dB, and –42 dB, respectively.
g. Typical 8PSK CI numbers at –7 MHz, –5 MHz, and –3 MHz are –50 dB, –45 dB, and –45 dB, respectively.
h. Meets this specification using front-end band pass filter.
i. Numbers are referred to the pin output with an external BPF filter.
j. f0 = -64 dBm Bluetooth-modulated signal, f1 = –39 dBm sine wave, f2 = –39 dBm Bluetooth-modulated signal, f0 = 2f1 – f2, and |f2 – f1| = n*1 MHz, where n is 3, 4, or 5. For the typical case, n = 4.
k. Includes baseband radiated emissions.

Table 14. Transmitter RF Specifications [a b]

Parameter	Conditions	Minimum	Typical	Maximum	Unit
General					
Frequency range	–	2402	–	2480	MHz
Class1: GFSK TX power [c]	–	–	12	–	dBm
Class1: EDR TX power [d]	–	–	9	–	dBm
Class 2: GFSK TX power	–	–	2	–	dBm
Power control step	–	2	4	8	dB
Modulation Accuracy					
p/4-DQPSK Frequency Stability	–	–10	–	10	kHz
p/4-DQPSK RMS DEVM	–	–	–	20	%
p/4-QPSK Peak DEVM	–	–	–	35	%
p/4-DQPSK 99% DEVM	–	–	–	30	%
8-DPSK frequency stability	–	–10	–	10	kHz
8-DPSK RMS DEVM	–	–	–	13	%
8-DPSK Peak DEVM	–	–	–	25	%
8-DPSK 99% DEVM	–	–	–	20	%
In-Band Spurious Emissions					
1.0 MHz < |M – N| < 1.5 MHz	–	–	–	–26	dBc
1.5 MHz < |M – N| < 2.5 MHz	–	–	–	–20	dBm
|M – N| ≥ 2.5 MHz	–	–	–	–40	dBm
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–36.0 [e]	dBm
1–12.75 GHz	–	–	–	–30.0 [e, f]	dBm
1.8–1.9 GHz	–	–	–	–47.0	dBm
5.15–5.3 GHz	–	–	–	–47.0	dBm
GPS Band Noise Emission (without a front-end band pass filter)					
1572.92 MHz to 1577.92 MHz	–	–	–150	–127	dBm/Hz
Out-of-Band Noise Emissions (without a front-end band pass filter)					
65–108 MHz	FM RX	–	–145	–	dBm/Hz
746–764 MHz	CDMA	–	–145	–	dBm/Hz
869–960 MHz	CDMA	–	–145	–	dBm/Hz
925–960 MHz	EDGE/GSM	–	–145	–	dBm/Hz
1805–1880 MHz	EDGE/GSM	–	–145	–	dBm/Hz
1930–1990 MHz	PCS	–	–145	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–140	–	dBm/Hz

a. All specifications are for industrial temperatures.
b. All specifications are single-ended. Unused input are left open.
c. +12 dBm output for GFSK measured with PA VDD = 2.5V.
d. +9 dBm output for EDR measured with PA VDD = 2.5V.
e. Maximum value is the value required for Bluetooth qualification.
f. Meets this spec using a front-end bandpass filter.

Table 15. BLE RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Frequency Range	n/a	2402	–	2480	MHz
RX Sense[a]	GFSK, 0.1% BER, 1 Mbps	–	–96.5	–	dBm
TX Power[b]	n/a	–	9	–	dBm
Mod Char: Delta F1 average	n/a	225	255	275	kHz
Mod Char: Delta F2 max[c]	n/a	99.9	–	–	%
Mod Char: Ratio	n/a	0.8	0.95	–	%

a. Dirty TX is Off.
b. The BLE TX power can be increased to compensate for front-end losses such as BPF, diplexer, switch, etc. The output is capped at 12 dBm out. The BLE TX power at the antenna port cannot exceed the 10 dBm EIRP specification limit.
c. At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz.

9.2 Timing and AC Characteristics

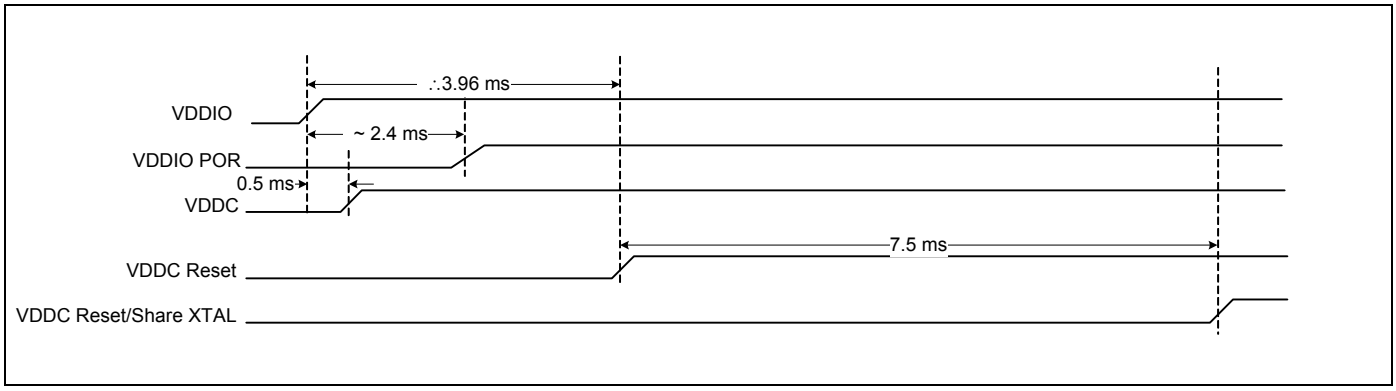
In this section, use the numbers listed in the reference column to interpret the timing diagrams.

9.2.1 Startup Timing

The global reset signal in the CYW20707 is a logical OR (actually a wired AND, since the signals are active low) of the RST_N input and the internal POR signals. The last signal to be released determines the time at which the chip is released from reset. The POR is typically asserted for 2.4 ms after the POR threshold is crossed.

The following two figures illustrate two startup timing scenarios.

Figure 8. Startup Timing



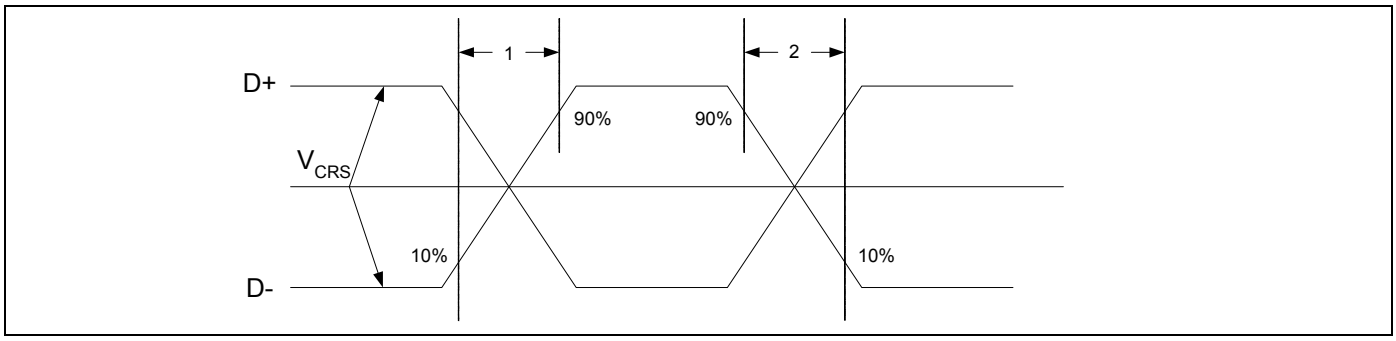
9.2.2 USB Full-Speed Timing

Table 16 through Figure 9 shows timing specifications for VDD_USB = 3.3V, V_{SS} = 0V, and T_A = 0°C to 85°C operating temperature range.

Table 16. USB Full-Speed Timing Specifications

Reference	Characteristics	Minimum	Maximum	Unit
1	Transition rise time	4	20	ns
2	Transition fall time	4	20	ns
3	Rise/fall timing matching	90	111	%
4	Full-speed data rate	12 – 0.25%	12 + 0.25%	Mb/s

Figure 9. USB Full-Speed Timing

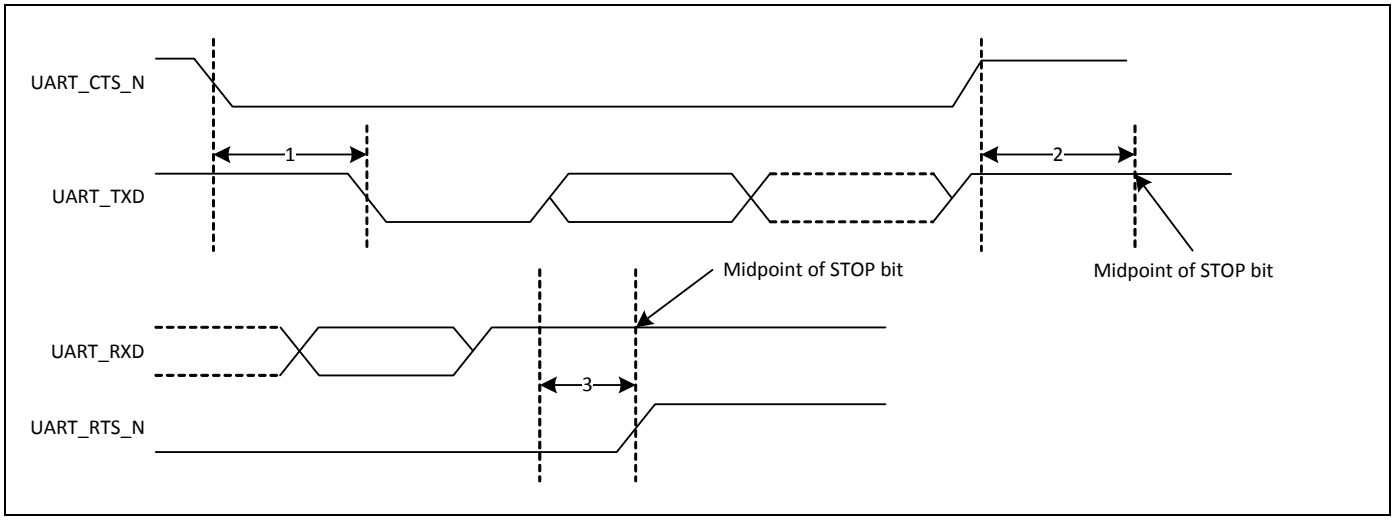


9.2.3 UART Timing

Table 17. UART Timing Specifications

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time UART_CTS_N low to UART TXD valid.	–	–	1.50	Bit periods
2	Setup time UART_CTS_N high before midpoint of stop bit.	–	–	0.67	Bit periods
3	Delay time Midpoint of stop bit to UART_RTS_N high.	–	–	1.33	Bit periods

Figure 10. UART Timing



9.2.4 PCM Interface Timing

Short Frame Sync, Master Mode

Figure 11. PCM Timing Diagram (Short Frame Sync, Master Mode)

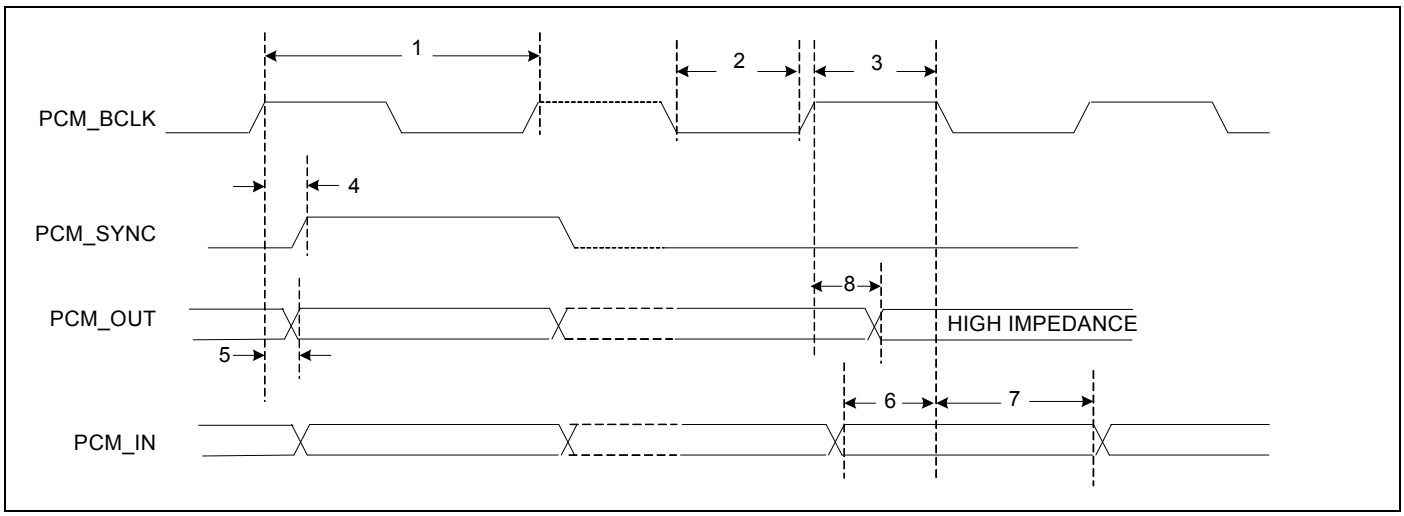


Table 18. PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	20.0	MHz
2	PCM bit clock LOW	20.0	–	–	ns
3	PCM bit clock HIGH	20.0	–	–	ns
4	PCM_SYNC delay	0.0	–	5.7	ns
5	PCM_OUT delay	–0.4	–	5.6	ns
6	PCM_IN setup	16.9	–	–	ns
7	PCM_IN hold	25.0	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	–0.4	–	5.6	ns

Short Frame Sync, Slave Mode

Figure 12. PCM Timing Diagram (Short Frame Sync, Slave Mode)

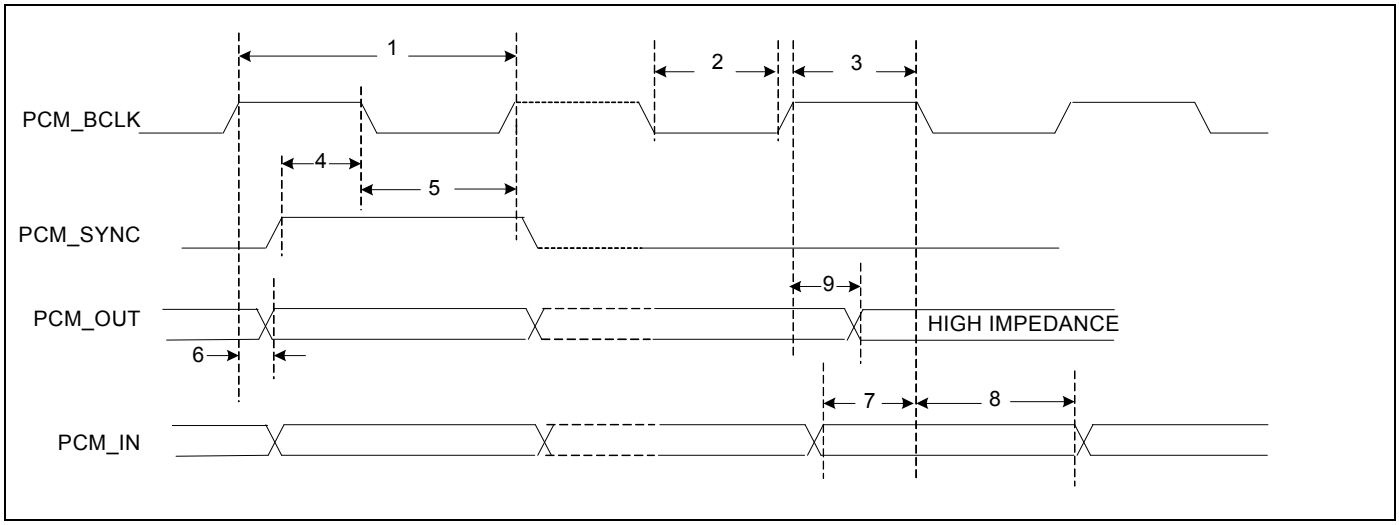


Table 19. PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24.0	MHz
2	PCM bit clock LOW	0.4	–	–	ns
3	PCM bit clock HIGH	18.5	–	–	ns
4	PCM_SYNC setup	17.0	–	–	ns
5	PCM_SYNC hold	–0.3	–	–	ns
6	PCM_OUT delay	3.6	–	9.5	ns
7	PCM_IN setup	18.5	–	–	ns
8	PCM_IN hold	0.4	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	3.6	–	9.5	ns

Long Frame Sync, Master Mode

Figure 13. PCM Timing Diagram (Long Frame Sync, Master Mode)

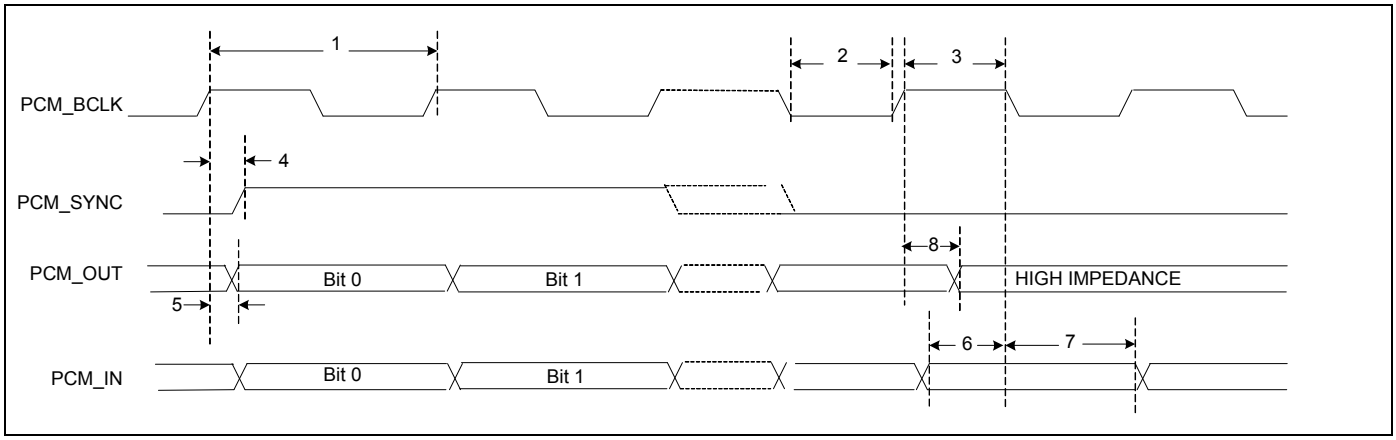


Table 20. PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	20.0	MHz
2	PCM bit clock LOW	20.0	–	–	ns
3	PCM bit clock HIGH	20.0	–	–	ns
4	PCM_SYNC delay	0.0	–	5.7	ns
5	PCM_OUT delay	–0.4	–	5.6	ns
6	PCM_IN setup	16.9	–	–	ns
7	PCM_IN hold	25.0	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	–0.4	–	5.6	ns

Long Frame Sync, Slave Mode

Figure 14. PCM Timing Diagram (Long Frame Sync, Slave Mode)

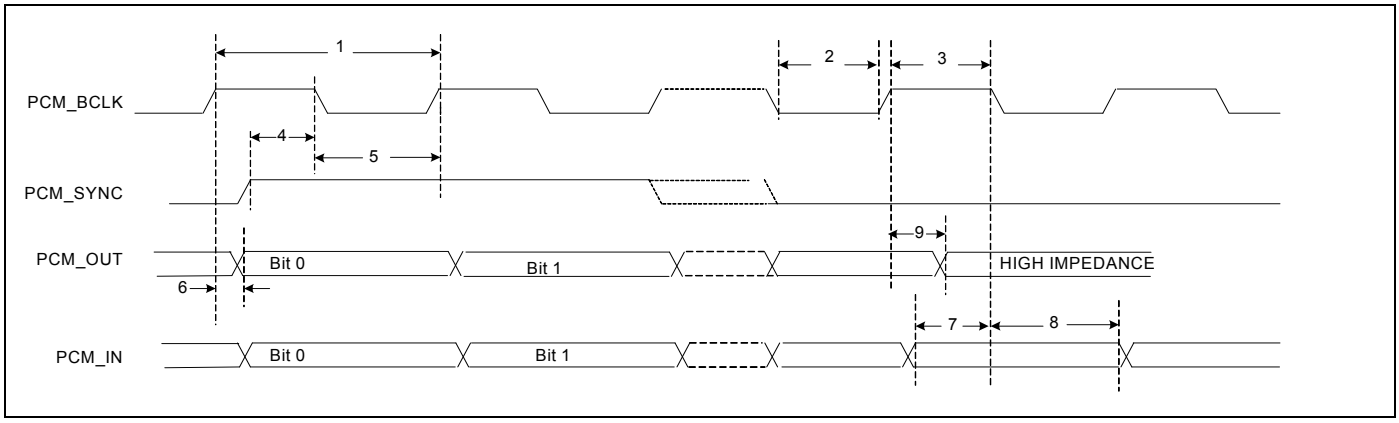


Table 21. PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24.0	MHz
2	PCM bit clock LOW	0.4	–	–	ns
3	PCM bit clock HIGH	18.5	–	–	ns
4	PCM_SYNC setup	17.0	–	–	ns
5	PCM_SYNC hold	Don’t care	–	–	ns
6	PCM_OUT delay	3.6	–	9.5	ns
7	PCM_IN setup	18.5	–	–	ns
8	PCM_IN hold	0.4	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	3.6	–	9.5	ns

Short Frame Sync, Burst Mode

Figure 15. PCM Burst Mode Timing (Receive Only, Short Frame Sync)

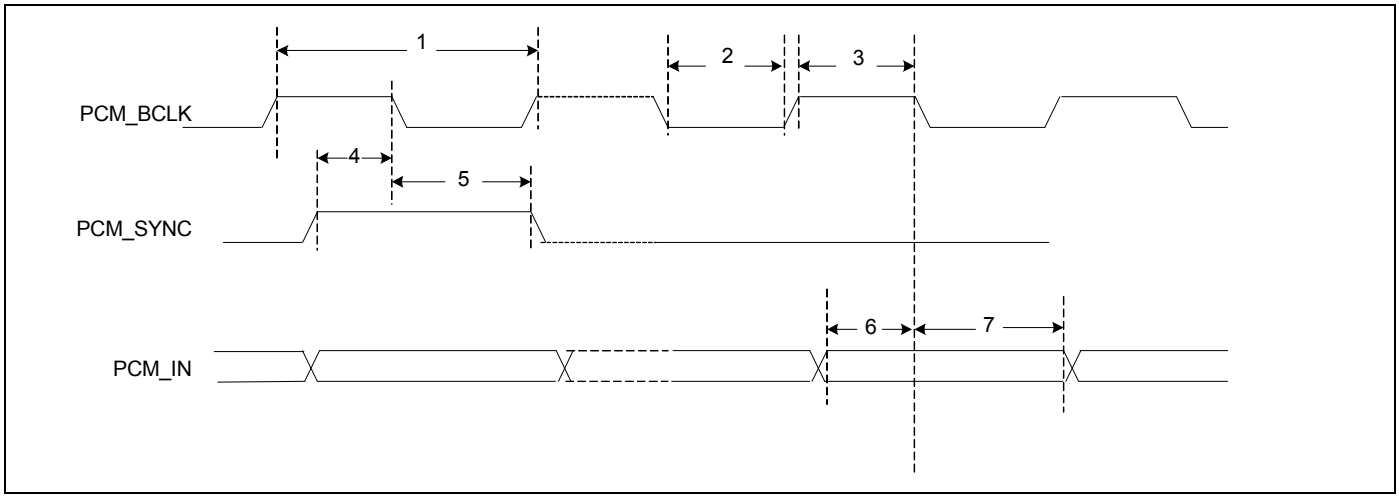


Table 22. PCM Burst Mode (Receive Only, Short Frame Sync)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24.0	MHz
2	PCM bit clock LOW	0.4	–	–	ns
3	PCM bit clock HIGH	18.5	–	–	ns
4	PCM_SYNC setup	17.0	–	–	ns
5	PCM_SYNC hold	–0.3	–	–	ns
6	PCM_IN setup	18.5	–	–	ns
7	PCM_IN hold	25.0	–	–	ns

Long Frame Sync, Burst Mode

Figure 16. PCM Burst Mode Timing (Receive Only, Long Frame Sync)

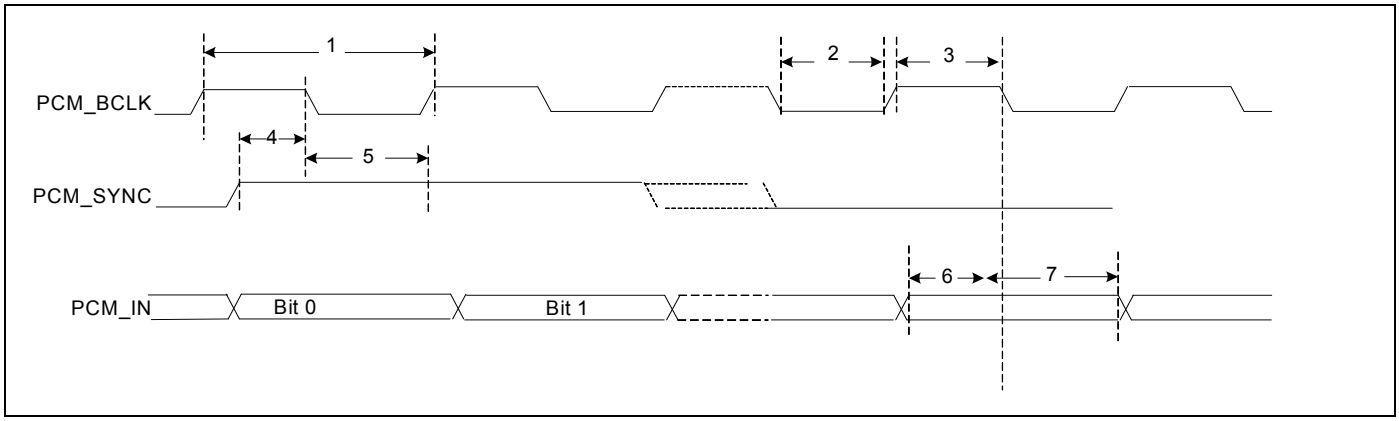


Table 23. PCM Burst Mode (Receive Only, Long Frame Sync)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24.0	MHz
2	PCM bit clock LOW	0.4	–	–	ns
3	PCM bit clock HIGH	18.5	–	–	ns
4	PCM_SYNC setup	17.0	–	–	ns
5	PCM_SYNC hold	Don't care	–	–	ns
6	PCM_IN setup	18.5	–	–	ns
7	PCM_IN hold	25.0	–	–	ns

9.3 I²S Interface

The CYW20707 supports two independent I²S digital audio ports. The I²S interface supports both master and slave modes. The I²S signals are:

- I²S clock: I²S SCK
- I²S Word Select: I²S WS
- I²S Data Out: I²S SDO
- I²S Data In: I²S SDI

I²S SCK and I²S WS become outputs in master mode and inputs in slave mode, while I²S SDO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I²S bus, per the I²S specification. The MSB of each data word is transmitted one bit clock cycle after the I²S WS transition, synchronous with the falling edge of bit clock. Left-channel data is transmitted when I²S WS is low, and right-channel data is transmitted when I²S WS is high. Data bits sent by the CYW20707 are synchronized with the falling edge of I2S_SCK and should be sampled by the receiver on the rising edge of I2S_SSCK.

The clock rate in master mode is either of the following:

48 kHz x 32 bits per frame = 1.536 MHz

48 kHz x 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider.

In the slave mode, any clock rate is supported to a maximum of 3.072 MHz.

9.3.1 I^2S Timing

Note: Timing values specified in Table 24 are relative to high and low threshold levels.

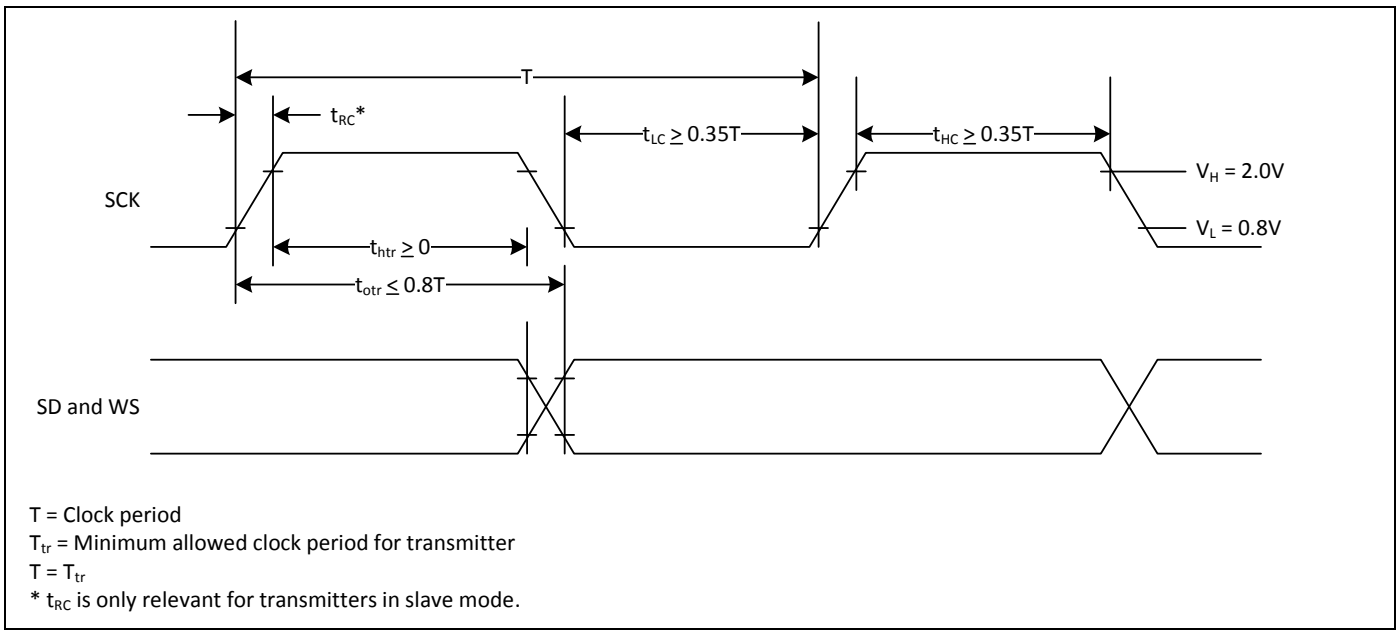
Table 24. Timing for I^2S Transmitters and Receivers

	Transmitter				Receiver				
	Lower LImit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	Notes
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	a
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	b
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	b
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	c
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	c
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–	–	–	d
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	e
Hold time t_{htr}	0	–	–	–	–	–	–	–	d
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2T_r$	–	–	f
Hold time t_{hr}	–	–	–	–	–	0	–	–	f

a. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
b. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
c. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
d. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
e. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
f. The data setup and hold time must not be less than the specified receiver setup and hold time.

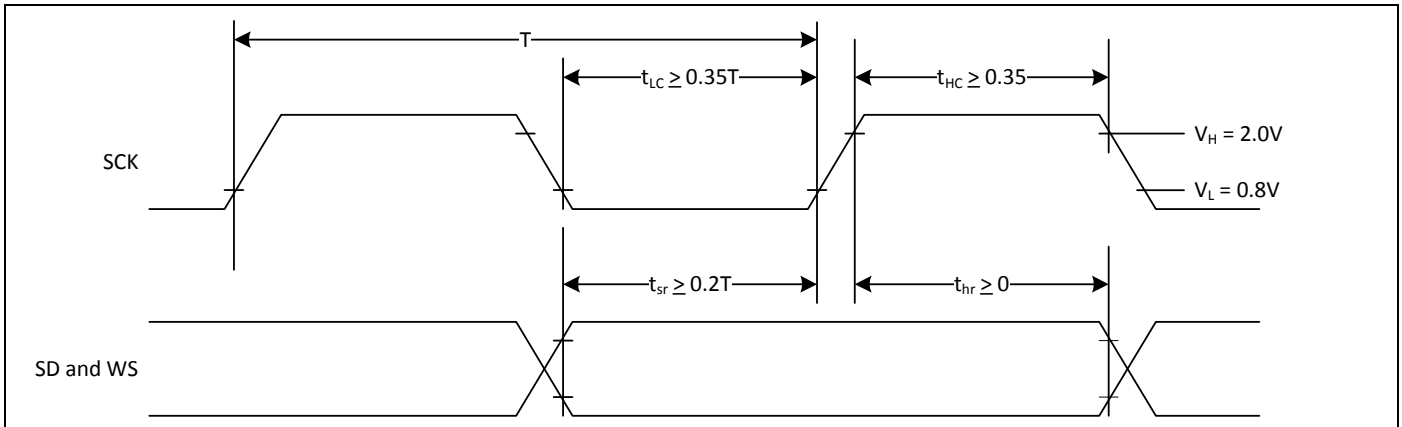
Note: The time periods specified in Figure 17 and Figure 18 are defined by the transmitter speed. The receiver specifications must match transmitter performance.

Figure 17. I²S Transmitter Timing



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
T = T_{tr}
* t_{RC} is only relevant for transmitters in slave mode.

Figure 18. I²S Receiver Timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
T > T_r

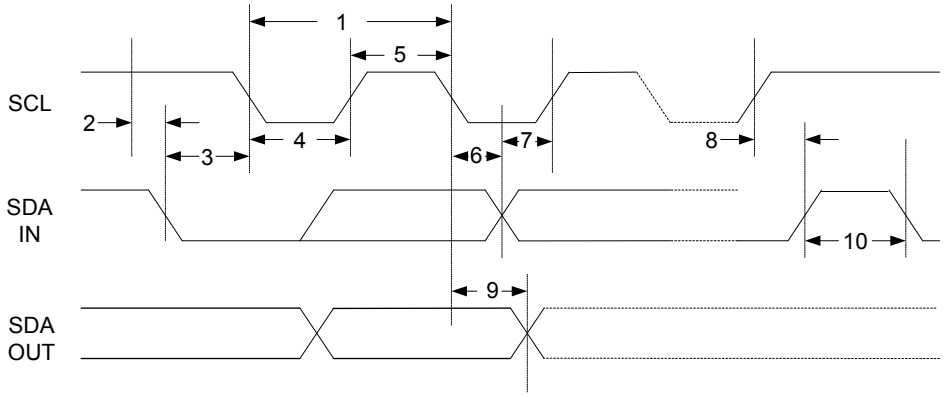
9.3.2 BSC Interface Timing

Table 25. BSC Interface Timing Specifications

Reference	Characteristics	Minimum	Maximum	Unit
1	Clock frequency	–	100 400 800 1000	kHz
2	START condition setup time	650	–	ns
3	START condition hold time	280	–	ns
4	Clock low time	650	–	ns
5	Clock high time	280	–	ns
6	Data input hold time[a]	0	–	ns
7	Data input setup time	100	–	ns
8	STOP condition setup time	280	–	ns
9	Output valid from clock	–	400	ns
10	Bus free time[b]	650	–	ns

a. As a transmitter, 300 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions
b. Time that the cbus must be free before a new transaction can start.

Figure 19. BSC Interface Timing Diagram



9.3.3 SPI Timing

The SPI interface can be clocked up to 12 MHz.

Table 26 and Figure 20 show the timing requirements when operating in SPI Mode 0 and 2.

Table 26. SPI Mode 0 and 2

Reference	Characteristics	Minimum	Maximum	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Hold time for MOSI data lines	12	½ SCK	ns
3	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
4	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	–	ns
5	Idle time between subsequent SPI transactions	1 SCK	–	ns

Figure 20. SPI Timing, Mode 0 and 2

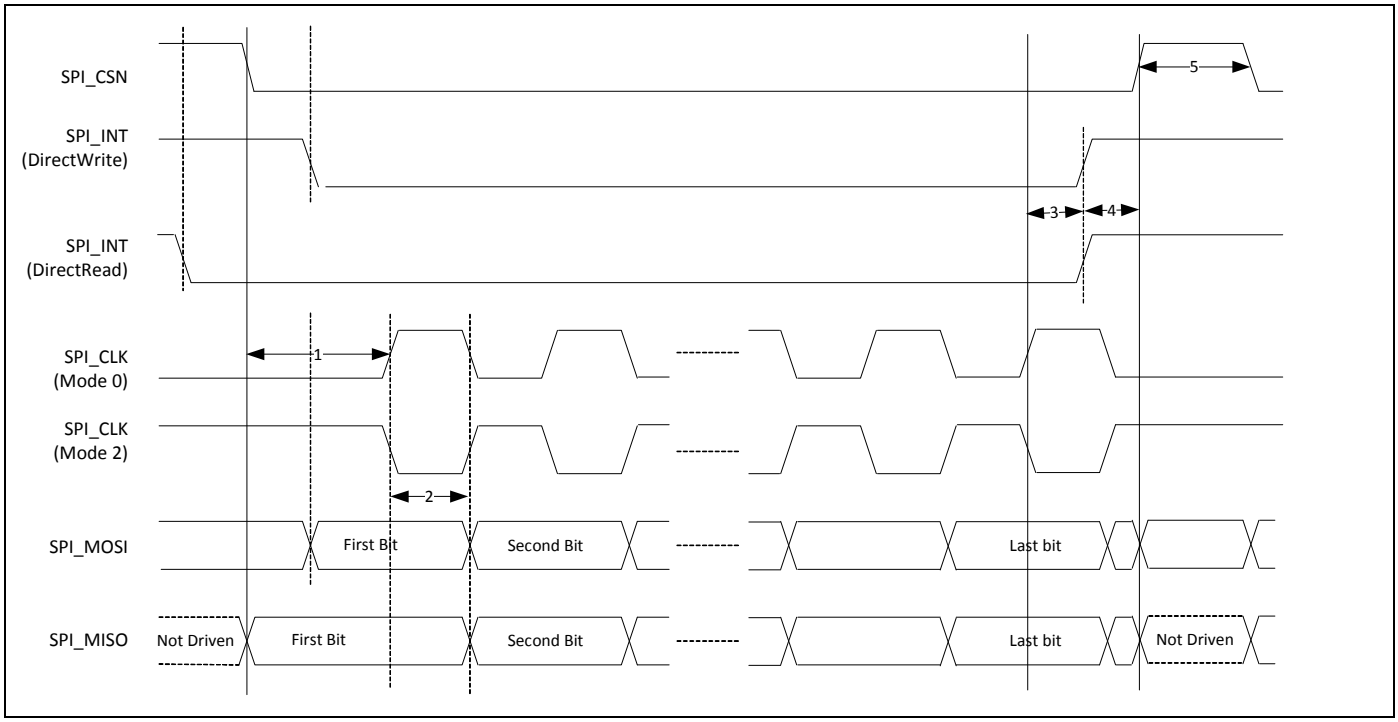
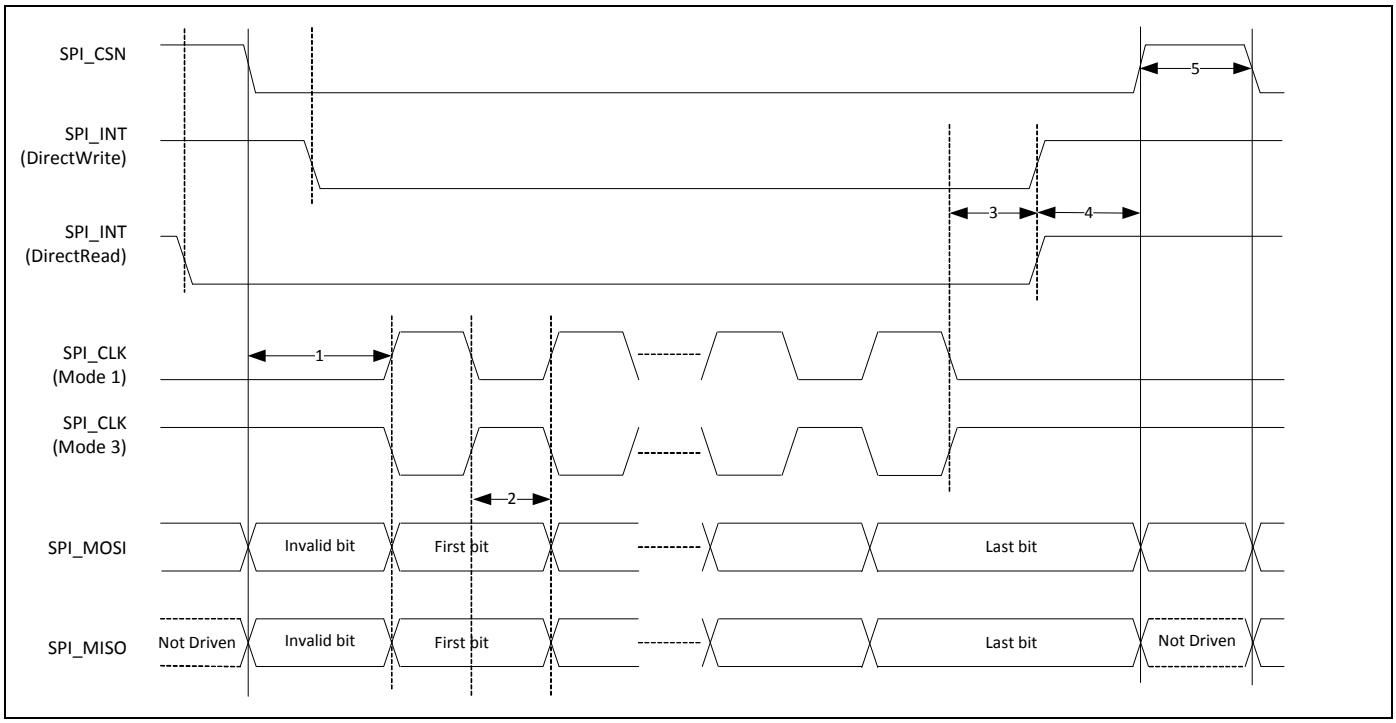


Table 27 and Figure 21 show the timing requirements when operating in SPI Mode 0 and 2.

Table 27. SPI Mode 1 and 3

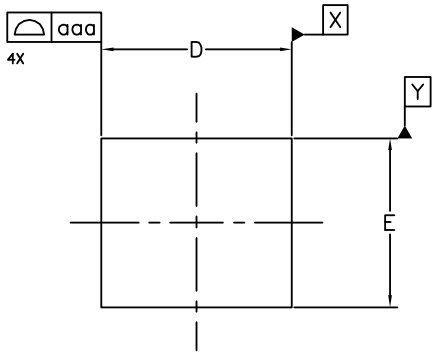
Reference	Characteristics	Minimum	Maximum	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Hold time for MOSI data lines	12	½ SCK	ns
3	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
4	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	–	ns
5	Idle time between subsequent SPI transactions	1 SCK	–	ns

Figure 21. SPI Timing, Mode 1 and 3

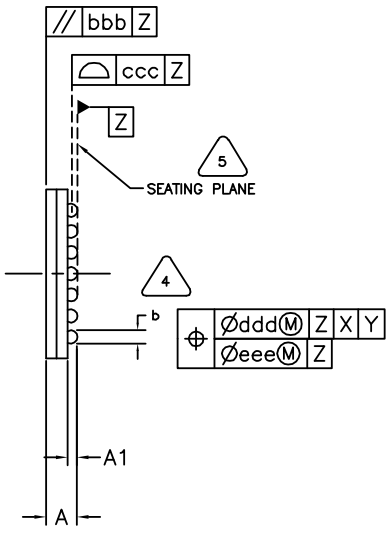


10. Mechanical Information

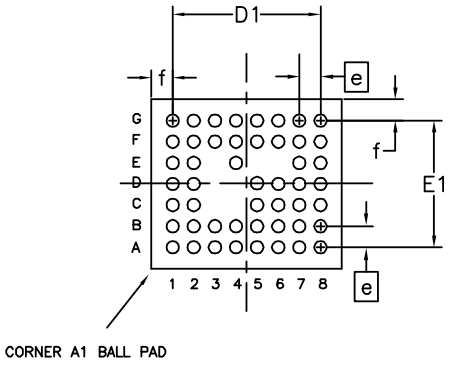
Figure 22. 49-Ball FcBGA Mechanical Drawing



TOP VIEW



SIDE VIEW



BOTTOM VIEW
(49 SOLDER BALLS)

DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	-	-	1.00
A1	0.13	0.16	0.19
D	4.40	4.60	4.80
D1		3.60 BSC	
E	3.90	4.00	4.10
E1		3.00 BSC	
b	0.20	0.25	0.30
e		0.50 BSC	
f	-	0.5	-
aaa	-	-	0.10
bbb	-	-	0.10
ccc	-	-	0.08
ddd	-	-	0.15
eee	-	-	0.05

Filename: MOD-000-0000-000

5. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BALL GRID PITCH IS 0.50mm

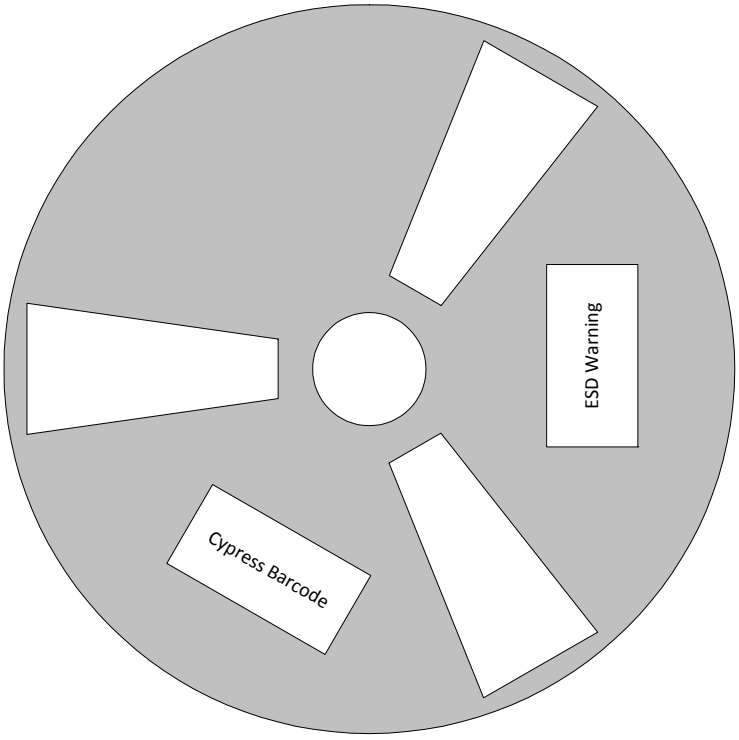
2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO-207.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

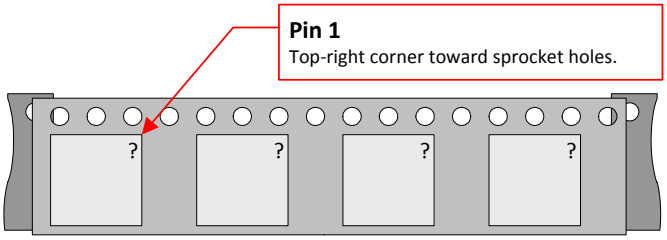
10.1 Tape, Reel, and Packing Specification

Figure 23. Reel, Labeling, and Packing Specification



Device Orientation/Mix Lot Number

Each reel may contain up to three lot numbers, independent of the date code.
Individual lots must be labeled on the box, moisture barrier bag, and the reel.



Moisture Barrier Bag Contents/Label

Desiccant pouch (minimum 1)
Humidity indicator (minimum 1)
Reel (maximum 1)

11. Ordering Information

Table 28 provides the available part number and its ordering information. This package is rated from –30°C to +85°C.

Table 28. Ordering Information

Part Number	Package Type
CYW20707UA1KFFB1G	Commercial 49-ball FcBGA, 4.5 mm x 4.0 mm x 0.8 mm.

Document History

Document Title: CYW20707 Embedded Bluetooth 4.1 SoC with MCU, Bluetooth Transceiver, and Baseband Processor Document Number: 002-15270				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	10/17/14	20707-DS100-R Initial release
*A	5478624	UTSV	10/17/16	Updated to Cypress Template
*B	5963539	AESATMP9	11/10/2017	Updated logo and copyright.

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