74HC192 High-speed CMOS logic presettable synchronous BCD decade up/down counter

1. General Description

1.1 Description

The 74HC192 is a synchronous BCD up/down counter. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CP_U clock is pulsed while CP_D is held HIGH, the device will count up. If the CP_D clock is pulsed while CP_U is held HIGH, the device will count down. Only one clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input ($\overline{PL}$).

The terminal count up ($\overline{TC_U}$) and terminal count down ($\overline{TC_D}$) outputs are normally HIGH. When the circuit has reached the maximum count state of 9, the next HIGH to-LOW transition of CP_U will cause $\overline{TC_U}$ to go LOW. $\overline{TC_U}$ will stay LOW until CP_U goes HIGH again, duplicating the count up clock.

Likewise, the $\overline{TC_D}$ output will go LOW when the circuit is in the zero state and the CP_D goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D0 to D3) is loaded into the counter and appears on the outputs (Q0 to Q3) regardless of the conditions of the clock inputs when the parallel load ($\overline{PL}$)input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs (Q0 to Q3) LOW.

1.2 Features

- Synchronous reversible counting
- Asynchronous parallel load
- Expandable without external logic
- Asynchronous reset
- Output capability: standard
- 2V to 6V operation

1.3 Ordering Information

PART NUMBER	PACKAGE
74HC192	DIP
	SOP
	TSSOP

2. Connection Diagrams and Pin Description

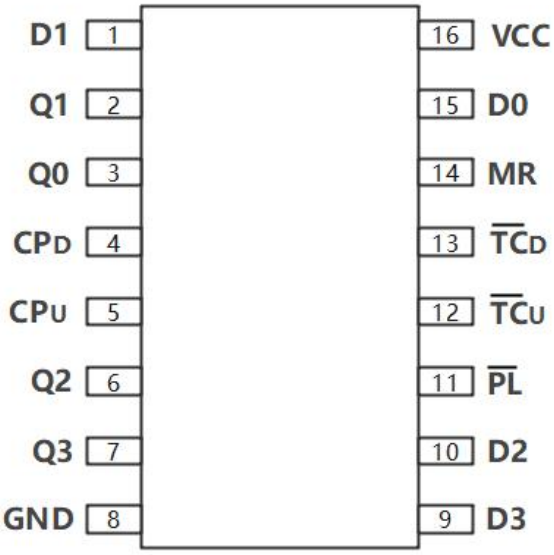


Figure 2.1 Top View

PIN No.	NAME	I/O	FUNCTION
1,9,10,15	D0 to D3	I	data inputs
2,3,6,7	Q0 to Q3	O	flip-flop outputs
4	CP_D	I	count down clock input
5	CP_U	I	count up clock input
8	GND	-	ground
11	$\overline{PL}$	I	asynchronous parallel load input (active LOW)
12	$\overline{TC_U}$	O	terminal count up (carry) output (active LOW)
13	$\overline{TC_D}$	O	terminal count down (borrow) output (active LOW)
14	MR	I	asynchronous master reset input (active HIGH)
16	Vcc	-	positive supply voltage

3. System Diagram

3.1 Logic Diagram

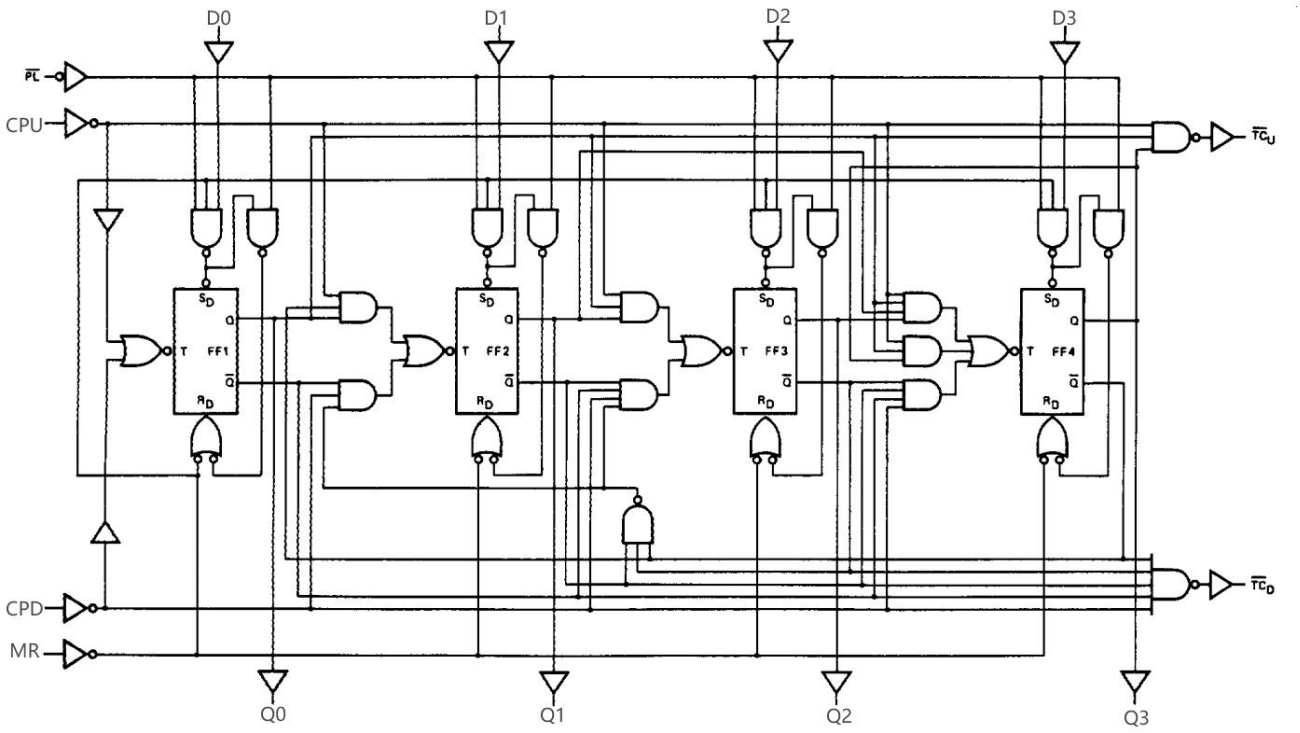


Figure 3.1：74HC192 Logic Diagram

3.2 Function Table

Operating Mode	Inputs								Outputs					
	MR	$\overline{PL}$	CP_U	CP_D	D0	D1	D2	D3	Q0	Q1	Q2	Q3	$\overline{TC_U}$	$\overline{TC_D}$
reset (clear)	1	X	X	0	X	X	X	X	0	0	0	0	1	0
	1	X	X	1	X	X	X	X	0	0	0	0	1	1
parallel load	0	0	X	0	0	0	0	0	0	0	0	0	1	0
	0	0	X	1	0	0	0	0	0	0	0	0	1	1
	0	0	0	X	1	X	X	1	Qn=Dn				0	1
	0	0	1	X	1	X	X	1	Qn=Dn				1	1
count up	0	1	↑	1	x	x	x	x	count up				1(2)	1
count down	0	1	1	↑	x	x	x	x	count down				1	1(3)

1. 1 = HIGH voltage level
   0 = LOW voltage level
   X = don't care
   ↑=LOW-to-HIGH clock transition
2. $\overline{TCU}$ = CP_U at terminal count up (1001)
3. $\overline{TCD}$ = CP_D at terminal count down (0000)

3.3 Typical Sequence

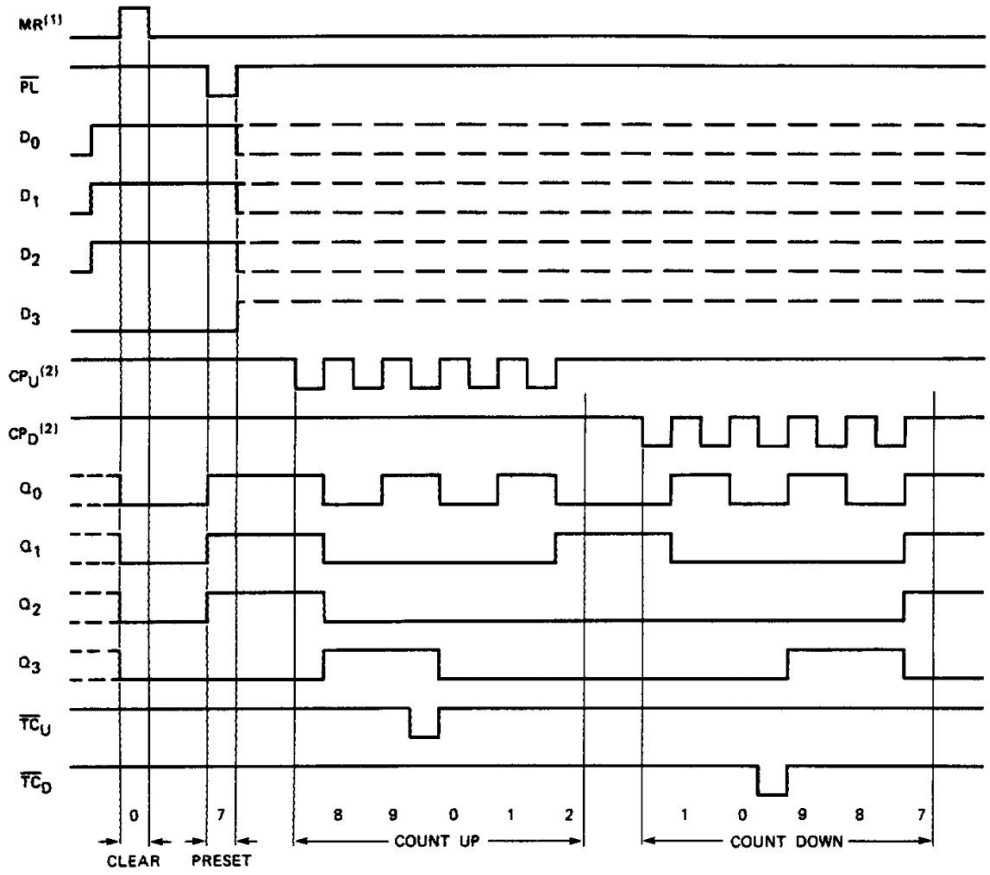


Figure 3.3：Typical clear, load and count sequence

(1) Clear overrides load, data and count inputs.

(2) When counting up the count down clock input (CP_D) must be HIGH, when counting down the count up clock input (CP_U) must be HIGH.

4. Specifications

4.1 Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Unit
V_{CC}	Supply Voltage	-0.5	7	V
V_{in}	Input Voltage (Referenced to GND)	-0.5	V_{CC}+0.5	V
V_{out}	Output Voltage (Referenced to GND)	-0.5	V_{CC}+0.5	V
P_D	Power Dissipation in Still Air, Plastic or Ceramic		500	mW
T_J	Junction Temperature		125	℃
T_{OP}	Operating Temperature	-40	85	℃
T_{stg}	Storage Temperature	-65	150	℃

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied.Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4.2 Recommended Operating Conditions

Symbol	Parameter	Test Condition	MIN	MAX	Unit
V_{CC}	Supply Voltage		2	6	V
V_{In},V_{OUT}	DC Input Voltage Output voltage		0	V_{CC}	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
V_{IH}	High Level Input Voltage	V_{CC}=2V	1.5		V
		V_{CC}=4.5V	3.15		V
		V_{CC}=6V	4.2		V
V_{IL}	Low Level Input Voltage	V_{CC}=2V		0.5	V
		V_{CC}=4.5V		1.35	V
		V_{CC}=6V		1.8	V

4.3 Electrical Characteristics

(T_a=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified)

Symbol	Parameter	Test Condition	MIN	TYP	MAX	Unit
DC Specifications						
V_{OH}	High Level Output Voltage	V_{CC}=2V,I_O=-20uA	1.9	--	--	V
		V_{CC}=4.5V,I_O=-20uA	4.4	--	--	V
		V_{CC}=6V,I_O=-20uA	5.9	--	--	V
		V_{CC}=4.5V,I_O=-4mA	4	--	--	V
		V_{CC}=6V,I_O=-5.2mA	5.5	--	--	V
V_{OL}	Low Level Output Voltage	V_{CC}=2V,I_O=20uA	--	--	0.1	V
		V_{CC}=4.5V,I_O=20uA	--	--	0.1	V
		V_{CC}=6V,I_O=20uA	--	--	0.1	V
		V_{CC}=4.5V,I_O=4mA	--	--	0.3	V
		V_{CC}=6V,I_O=5.2mA	--	--	0.3	V
I_I	Input Leakage Current	V_{CC}=6V,V_I=V_{CC} or GND	--	±0.1	±1	uA
I_{CC}	Quiescent Supply Current	V_{CC}=6V,V_I=V_{CC}/GND,I_O=0	--	--	10	uA

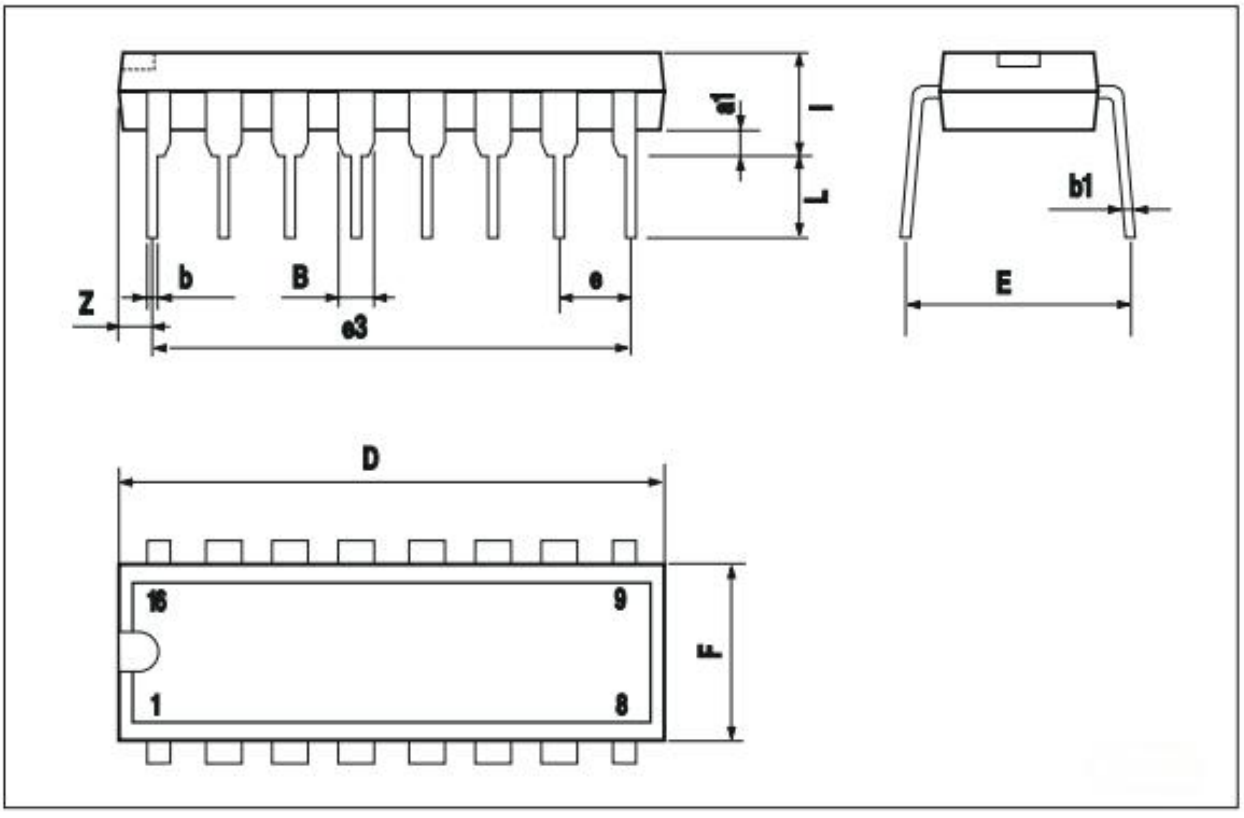
5. Ordering Information

Orderable Device	Package Type	Pins	Packing	Package Qty
74HC192ND16ATBE	DIP	16	Tube	25
74HC192NS16ARDQ	SOP	16	Tape & Reel	4000
74HC192TS16ARDQ	TSSOP	16	Tape & Reel	4000

6. Package Information

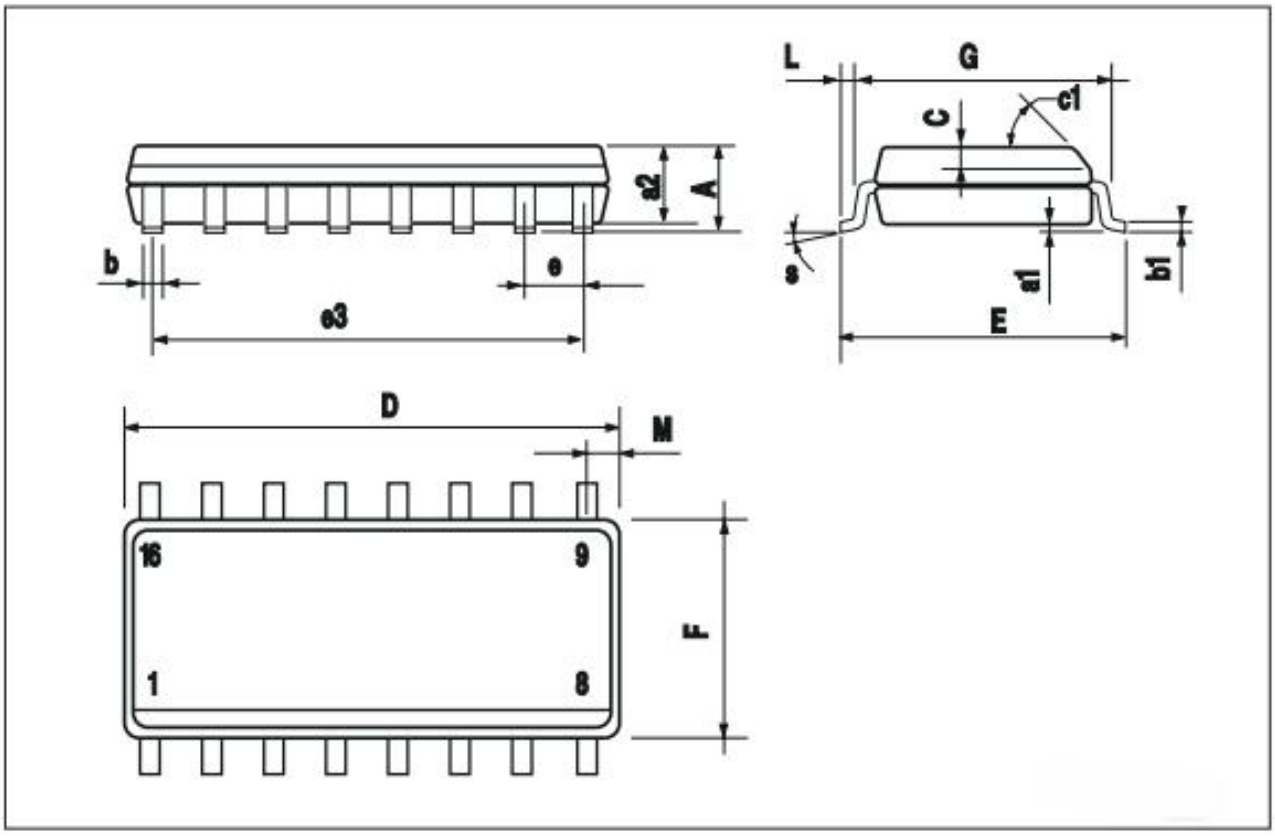
6.1 DIP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



6.2 SOP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.25	0.004		0.010
a2			1.64			0.063
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



6.3 TSSOP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030