钍地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65HVD20/HVD21/HVD22/HVD23/HVD24

SN65HVD2x Extended Common-Mode RS-485 Transceiver

网址 www.sztdbdt.com

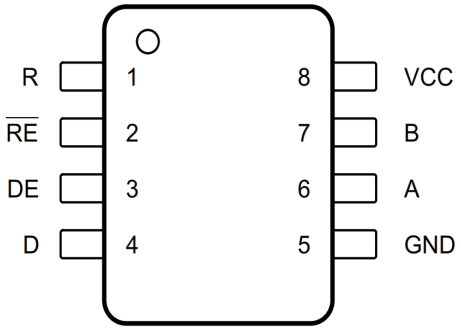
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- Common-mode voltage range (-20V to 25V), more than twice the range required by the TIA/E-485 standard
- Receiver equalization technology supports longer cables and higher signal transmission rates (SN65HVD2 [3,4])
- Unit load for up to256 nodes
- Bus I/O protection exceeds 16kV HBM
- Fail-safe receiver suitable for open-circuit, short-circuit, and bus conditions
- Low standby supply current: 1 μ A (max)
- Receiver hysteresis greater than 100mV



D or P Package, 8-Pin SOIC or PDIP
(Top View)

Applications

- Long cable solutions
  - Factory automation
  - Security networks
  - Building HVAC
- Harsh electrical environments
  - Power inverters
  - Industrial drivesAvionics

Description

The SN65HVD2x series transceivers provide performance far exceeding typical RS-485 devices. In addition all requirements of the TIA/EIA-485-A standard, the SN65HVD2x series operates over an extended common-mode voltage range and high ESD protection, wide receiver hysteresis, and fail-safe mode operation. This series of devices is suitable for long-cable networks and other applications where environments are too harsh for standard transivers.
These devices are designed for bidirectional data transmission over multi-point twisted-pair cables. Example applications include digital motor controllers, remote sensors and terminals, industrial process control, checkpoints, and environmental control systems.
These devices combine a three-state differential driver with a differential receiver, both powered bya single 5V supply. The driver's outputs and the receiver's differential inputs are internally connected to form a differential bus port that provides a minimum load to the bus. This port features an extended common-mode voltage range making these devices suitable for multi-point applications on long cables.

Description (Continued)

The SN65HVD20 device provides high signal transmission rates (up to 25Mbps for an interconnected network consisting of up to 64 nodes.
The SN65HVD21 device can connect up to 256 nodes at medium data ratesup to 5Mbps). By controlling the driver output slew rate, it provides reliable switching, achieves waveform shaping, and reduces high-frequency noise emissions.
The SN65VD22 device features a controlled driver output slew rate, which can achieve low radiated noise in emission-sensitive applications and improve signal quality through long stubs. Up to 25 SN65HVD22 nodes can be connected at signal transmission rates up to 500kbps.
The SN65HVD23 device uses receiver technology to improve jitter performance in differential bus applications, with data rates up to 25Mbps over cable lengths up to 160 meters.
The SN65H24 device uses receiver equalization technology to improve jitter performance in differential bus applications, with data rates from 1Mbps to 10Mbps over cable lengths up to 100 meters.
The receiver includes a fail-safe circuit that provides a high-level output within 250 microseconds after the input signal is lost. Common causes of signal loss include disconnection, line short circuits, or no transmitters operating on the bus. This function prevents noise from being received as valid data in these fault conditions and can be used for "wiredOR" bus signal transmission.
The SN65HVD2x devices have a rated operating temperature range of –40 ° C to 85 ° C

表 7-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	6	Bus input and output	Driver output or receiver input (complementary to B)
B	7	Bus input and output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low
VCC	8	Supply	4.5-V to 5.5-V supply

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Supply voltage(2)			- 0.5	7	V
Voltage at any bus I/O terminal			- 27	27	V
Voltage input, transient pulse	A, B	(through 100 Ω, see 图 9-16)	- 60	60	V
Voltage input	D, DE, $\overline{RE}$		- 0.5	V_{CC} + 0.5	V
Receiver output current			- 10	10	mA
Continuous total power dissipation			See *Power Dissipation Ratings*		
Junction temperature, T_J				150	°C
Storage temperature, T_{stg}				150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except 5, 6, and 7	±5000	V
			Pins 5, 6, and 7	±16000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1500	
		Machine Model (MM) (3)		±200	

(1) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(2) Tested in accordance with JEDEC Standard 22, Test Method C101.
(3) Tested in accordance with JEDEC Standard 22, Test Method A115-A

8.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
	Voltage at any bus I/O terminal	A, B	- 20		25	V
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{ID}	Differential input voltage	A with respect to B	- 25		25	V
	Output current	Driver	- 110		110	mA
		Receiver	- 8		8	

8.3 Recommended Operating Conditions (continued)

				MIN	NOM	MAX	UNIT
I_{CC}	Supply current	Driver enabled (DE at V_{CC}), Receiver enabled (RE at 0 V), No load, V_I = 0 V or V_{CC}	SN65HVD20		6	9	mA
			SN65HVD21		8	12	
			SN65HVD22		6	9	
			SN65HVD23		7	11	
			SN65HVD24		10	14	
		Driver enabled (DE at V_{CC}), Receiver disabled (RE at V_{CC}), No load, V_I = 0 V or V_{CC}	SN65HVD20		5	8	
			SN65HVD21		7	11	
			SN65HVD22		5	8	
			SN65HVD23		5	9	
			SN65HVD24		8	12	
		Driver disabled (DE at 0 V), Receiver enabled (RE at 0 V), No load	SN65HVD20		4	7	
			SN65HVD21		5	8	
			SN65HVD22		4	7	
			SN65HVD23		4.5	9	
			SN65HVD24		5.5	10	
		Driver disabled (DE at 0 V), Receiver disabled (RE at V_{CC}) D open	All SN65HVD2x			1	µA
T_A	Operating free-air temperature(1)			-40		85	°C
T_J	Junction temperature			-40		130	°C

(1) Maximum free-air temperature operation is allowed as long as the device recommended junction temperature is not exceeded.

8.4 Thermal Information

THERMAL METRIC(1)		SN65HVD2x		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.7	52.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	49.9	57.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.7	38.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.0	19.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.9	31.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Driver Electrical Characteristics

over recommended operating conditions (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = − 18 mA		− 1.5	0.75		V
V_O	Open-circuit output voltage	A or B, No load		0		V_{CC}	V
$\lvert V_{OD(SS)}\rvert$	Steady-state differential output voltage	No load (open circuit)		3.3	4.2	V_{CC}	V
		R_L = 54 Ω, See 图 9-1		1.8	2.5		
		With common-mode loading, See 图 9-2		1.8			
$\Delta\lvert V_{OD(SS)}\rvert$	Change in steady-state differential output voltage between logic states	See 图 9-1 and 图 9-3		− 0.1		0.1	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See 图 9-1		2.1	2.5	2.9	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage, $V_{OC(H)}$ − $V_{OC(L)}$	See 图 9-1 and 图 9-4		− 0.1		0.1	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage, $V_{OC(MAX)}$ − $V_{OC(MIN)}$	R_L = 54 Ω, C_L = 50 pF, See 图 9-1 and 图 9-4		0.35			V
$V_{OD(RING)}$	Differential output voltage over and under shoot	R_L = 54 Ω, C_L = 50 pF, See 图 9-5				10%	
I_I	Input current	D, DE		− 100		100	µA
I_O	Output current with power off. High impedance state output current.	V_O = − 7 V to 12 V, Other input = 0 V	SN65HVD2[0,3]	− 400		500	µA
			SN65HVD2[1,2,4]	− 100		125	
		V_O = − 20 V to 25 V, Other input = 0 V	SN65HVD2[0,3]	− 800		1000	
			SN65HVD2[1,2,4]	− 200		250	
I_{OS}	Short-circuit output current	V_O = − 20 V to 25 V, See 图 9-9		− 250		250	mA
C_{OD}	Differential output capacitance					20	pF

(1) All typical values are at V_{CC} = 5 V and 25°C.

8.6 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IT(+)}$	Positive-going differential input voltage threshold	See 图 9-10	V_O = 2.4 V, I_O = – 8 mA		60	200	mV
$V_{IT(-)}$	Negative-going differential input voltage threshold		V_O = 0.4 V, I_O = 8 mA	– 200	– 60		
V_{HYS}	Hysteresis voltage (V_{IT+} – V_{IT-})			100	130		mV
$V_{IT(F+)}$	Positive-going differential input failsafe voltage threshold	See 图 9-15	VCM = – 7 V to 12 V	40	120	200	mV
			VCM = – 20 V to 25 V		120	250	
$V_{IT(F-)}$	Negative-going differential input failsafe voltage threshold	See 图 9-15	VCM = – 7 V to 12 V	– 200	– 120	– 40	mV
			VCM = – 20 V to 25 V	– 250	– 120		
V_{IK}	Input clamp voltage	I_I = – 18 mA		– 1.5			V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = – 8 mA, See 图 9-11		4			V
V_{OL}	Low-level output voltage	V_{ID} = – 200 mV, I_{OL} = 8 mA, See 图 9-11				0.4	V
$I_{I(BUS)}$	Bus input current (power on or power off)	V_I = – 7 to 12 V, Other input = 0 V	SN65HVD2[0,3]	– 400		500	μA
			SN65HVD2[1,2,4]	– 100		125	
		V_I = – 20 to 25 V, Other input = 0 V	SN65HVD2[0,3]	– 800		1000	
			SN65HVD2[1,2,4]	– 200		250	
I_I	Input current	$\overline{RE}$		– 100		100	μA
R_I	Input resistance	SN65HVD2[0,3]		24			kΩ
		SN65HVD2[1,2,4]		96			
C_{ID}	Differential input capacitance	V_{ID} = 0.5 + 0.4 sine (2π × 1.5 × 10^6t)			20		pF

(1) All typical values are at V_{CC} = 5 V and 25°C.

8.7 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Differential output propagation delay, low-to-high and high-to-low	R_L = 54 Ω, C_L = 50 pF, See 图 9-3	SN65HVD2[0,3]	6	10	20	ns
			SN65HVD2[1,4]	20	32	60	
			SN65HVD22	160	280	500	
t_r, t_f	Differential output rise time and fall time	R_L = 54 Ω, C_L = 50 pF, See 图 9-3	SN65HVD2[0,3]	2	6	12	ns
			SN65HVD2[1,4]	20	40	60	
			SN65HVD22	175	400	600	
t_{PZH}, t_{PHZ}	Propagation delay time, high-impedance-to-high-level output and high-level output-to-high-impedance	$\overline{RE}$ at 0 V, See 图 9-6	SN65HVD2[0,3]			40	ns
			SN65HVD2[1,4]			100	
			SN65HVD22			300	
t_{PZL}, t_{PLZ}	Propagation delay time, high-impedance-to-high-level output and high-level output-to-high-impedance	$\overline{RE}$ at 0 V, See 图 9-7	SN65HVD2[0,3]			40	ns
			SN65HVD2[1,4]			100	
			SN65HVD22			300	
$t_{d(standby)}$	Time from an active differential output to standby	$\overline{RE}$ at V_{CC}, See 图 9-8				2	μs
$t_{d(wake)}$	Wake-up time from standby to an active differential output					8	μs
$t_{sk(p)}$	Pulse skew | t_{PLH} – t_{PHL} |	SN65HVD2[0,3]				2	ns
		SN65HVD2[1,4]				6	
		SN65HVD22				50	

(1) All typical values are at V_{CC} = 5 V and 25°C

8.8 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time, low-to-high level output and high-to low level output	See 图 9-11	SN65HVD2[0,3]		16	35	ns
			SN65HVD2[1,2,4]		25	50	
t_r t_f	Receiver output rise time Receiver output fall time	See 图 9-11			2	4	ns
t_{PZH} t_{PHZ}	Receiver output enable time to high level and disable time from high level	See 图 9-12			90	120	ns
					16	35	
t_{PZL} t_{PLZ}	Receiver output enable time to low level and disable time from low level	See 图 9-13			90	120	ns
					16	35	
$t_{r(standby)}$	Time from an active receiver output to standby	See 图 9-14, DE at 0 V				2	µs
$t_{r(wake)}$	Wake-up time from standby to an active receiver output	See 图 9-14, DE at 0 V				8	µs
$t_{sk(p)}$	Pulse skew $\lvert t_{PLH} - t_{PHL} \rvert$					5	ns
$t_{p(set)}$	Delay time, bus fail to failsafe set	See 图 9-15, pulse rate = 1 kHz			250	350	µs
$t_{p(reset)}$	Delay time, bus recovery to failsafe reset	See 图 9-15, pulse rate = 1 kHz			50		ns

8.9 Receiver Equalization Characteristics

over recommended operating conditions (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS				TYP	UNIT
$t_{j(pp)}$	Peak-to-peak eye-pattern jitter	Peudo-random NRZ code with a bit pattern length of $2^{16} - 1$, Beldon 3105A cable, See 图 10-2	25 Mbps	0 m	SN65HVD23	2	ns
				100 m	SN65HVD20	6	ns
					SN65HVD23	3	
				150 m	SN65HVD20	15	ns
					SN65HVD23	4	
				200 m	SN65HVD20	27	ns
					SN65HVD23	8	
			10 Mbps	200 m	SN65HVD20	22	ns
					SN65HVD23	8	
				250 m	SN65HVD20	34	ns
					SN65HVD23	15	
				300 m	SN65HVD20	49	ns
					SN65HVD23	27	
			5 Mbps	500 m	SN65HVD21	128	ns
					SN65HVD24	18	
			3 Mbps	500 m	SN65HVD20	93	ns
					SN65HVD21	103	
					SN65HVD23	90	
					SN65HVD24	16	
			1 Mbps	1000 m	SN65HVD21	216	ns
					SN65HVD24	62	

(1) The SN65HVD20 and SN65HVD21 do not have receiver equalization, but are specified for comparison.
(2) All typical values are at V_{CC} = 5 V, and temperature = 25°C.

8.10 Power Dissipation

PARAMETERS		TEST CONDITIONS			VALUE	UNIT
P_D	Device power dissipation	Typical	V_{CC} = 5 V, T_J = 25°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver), 50% Duty cycle square-wave signal, Driver and receiver enabled	SN65HVD20: 25 Mbps	295	mW
				SN65HVD21: 5 Mbps	260	
				SN65HVD22: 500 kbps	233	
				SN65HVD23: 25 Mbps	302	
				SN65HVD24: 5 Mbps	267	
		Worst case	V_{CC} = 5.5 V, T_J = 125°C, R_L = 54 Ω, C_L = 50 pF, C_L = 15 pF (receiver), 50% Duty cycle square-wave signal, Driver and receiver enabled	SN65HVD20: 25 Mbps	408	mW
				SN65HVD21: 5 Mbps	342	
				SN65HVD22: 500 kbps	300	
				SN65HVD23: 25 Mbps	417	
				SN65HVD24: 5 Mbps	352	
T_{SD}	Thermal shut down junction temperature				170	°C

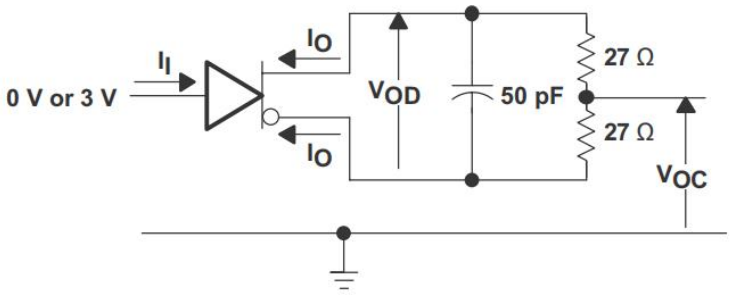


图 9-1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

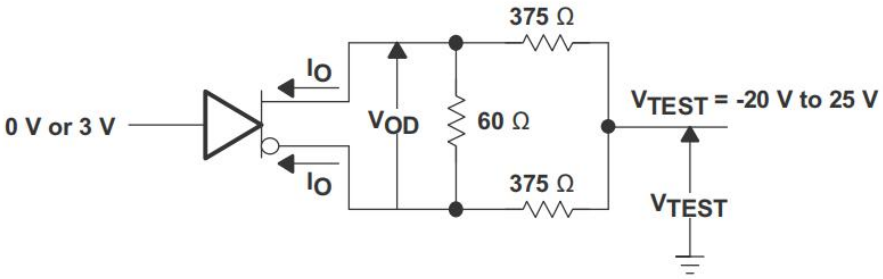


图 9-2. Driver Test Circuit, V_{OD} With Common-Mode Loading

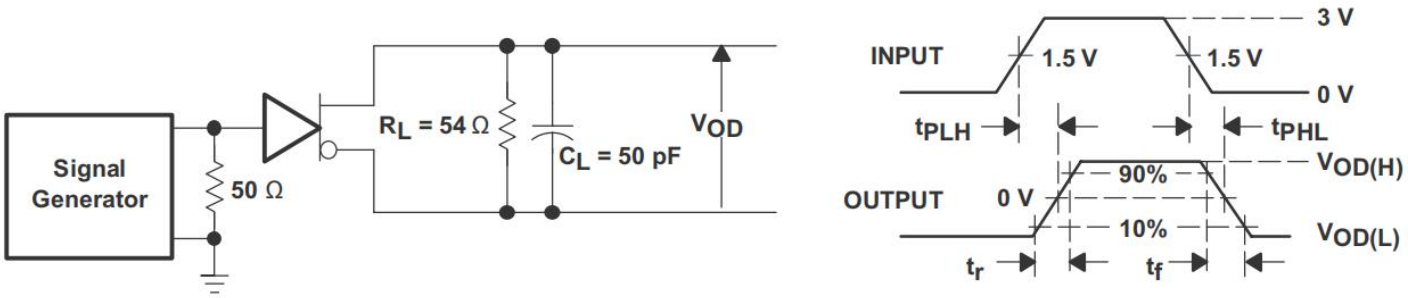


图 9-3. Driver Switching Test Circuit and Waveforms

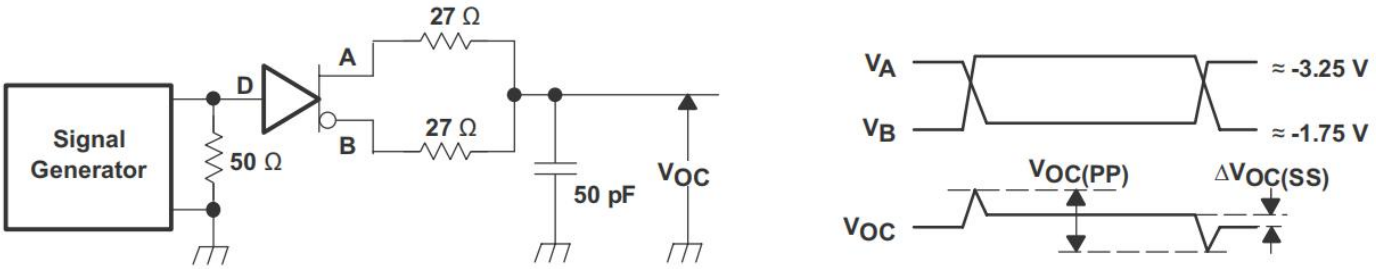
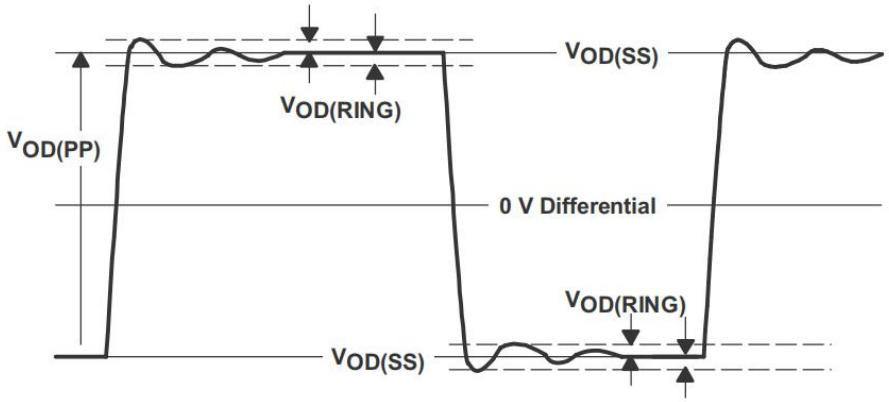


图 9-4. Driver V_{OC} Test Circuit and Waveforms



$V_{OD(RING)}$ is measured at four points on the output waveform, corresponding to overshoot and undershoot from the $V_{OD(H)}$ and $V_{OD(L)}$ steady state values.

图 9-5. $V_{OD(RING)}$ Waveform and Definitions

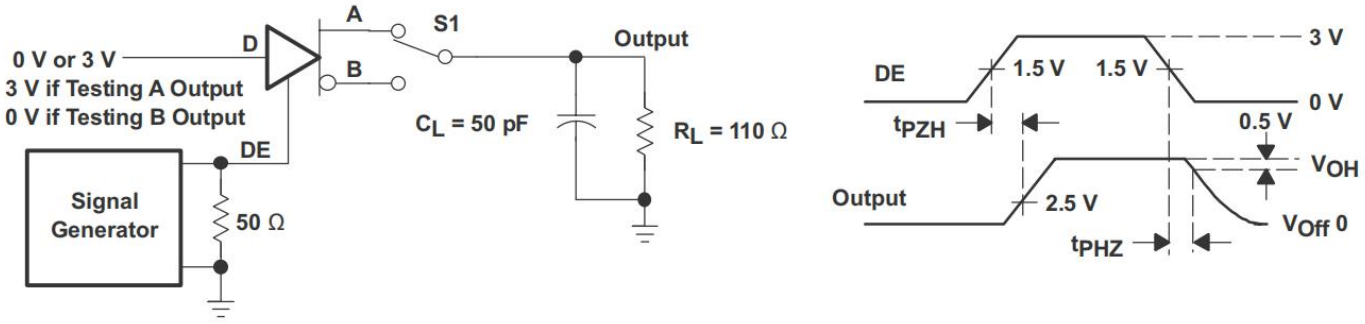


图 9-6. Driver Enable and Disable Test, High Output

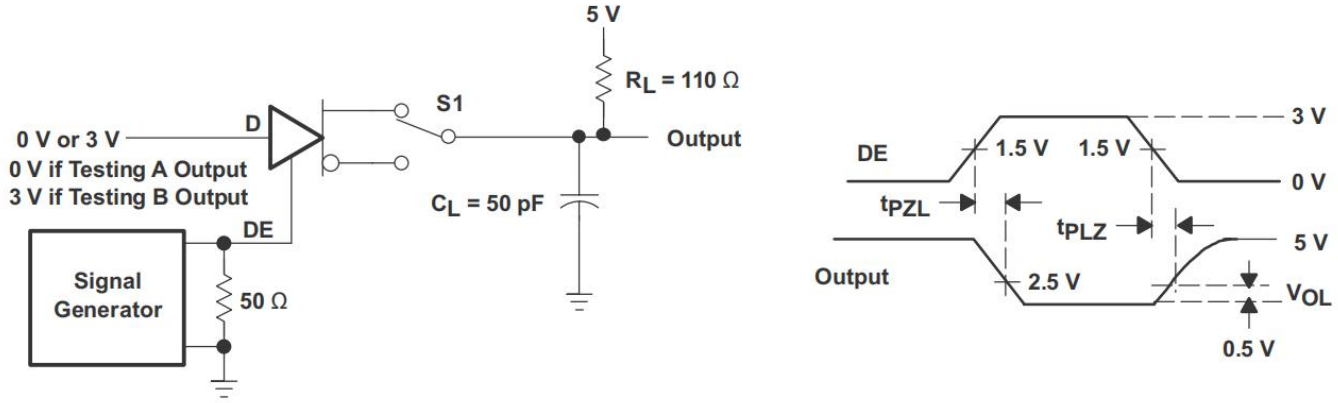


图 9-7. Driver Enable and Disable Test, Low Output

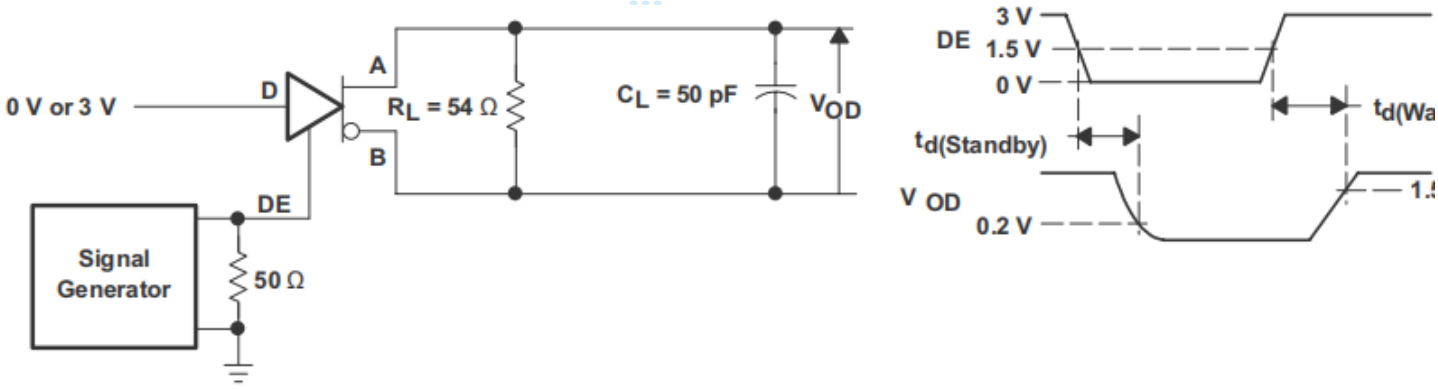


图 9-8. Driver Standby and Wake Test Circuit and Waveforms

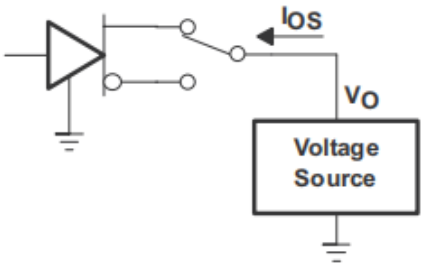


图 9-9. Driver Short-Circuit Test

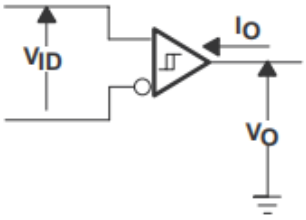


图 9-10. Receiver DC Parameter Definitions

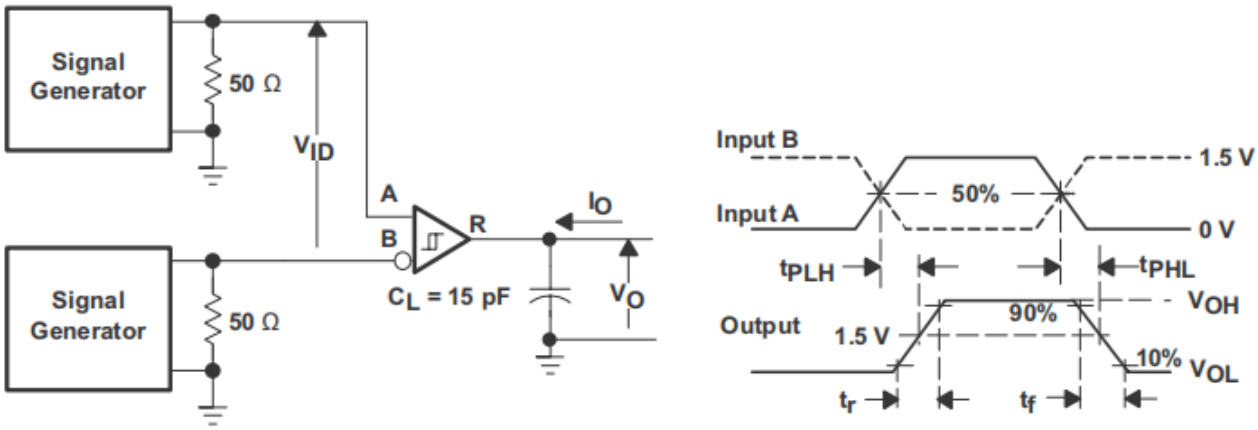


图 9-11. Receiver Switching Test Circuit and Waveforms

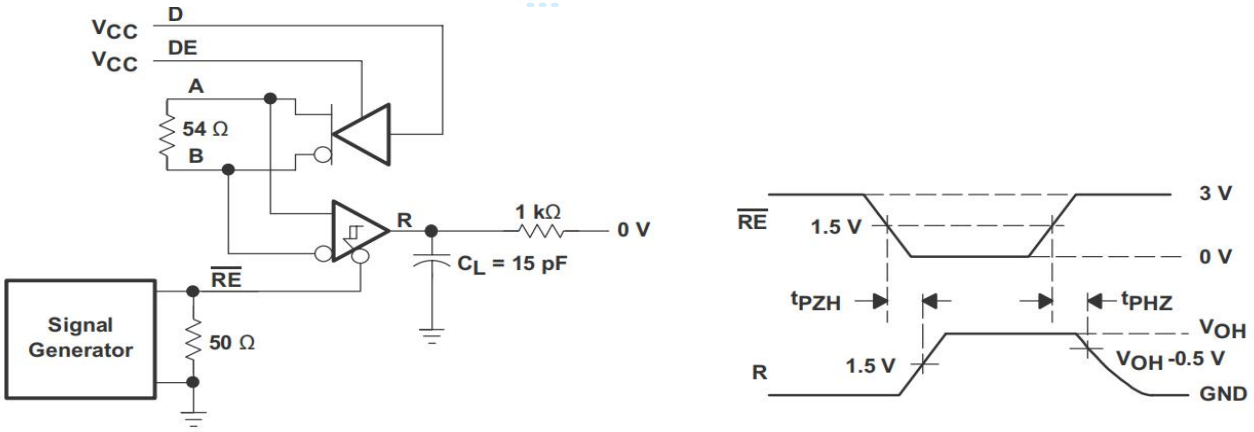


图 9-12. Receiver Enable Test Circuit and Waveforms, Data Output High

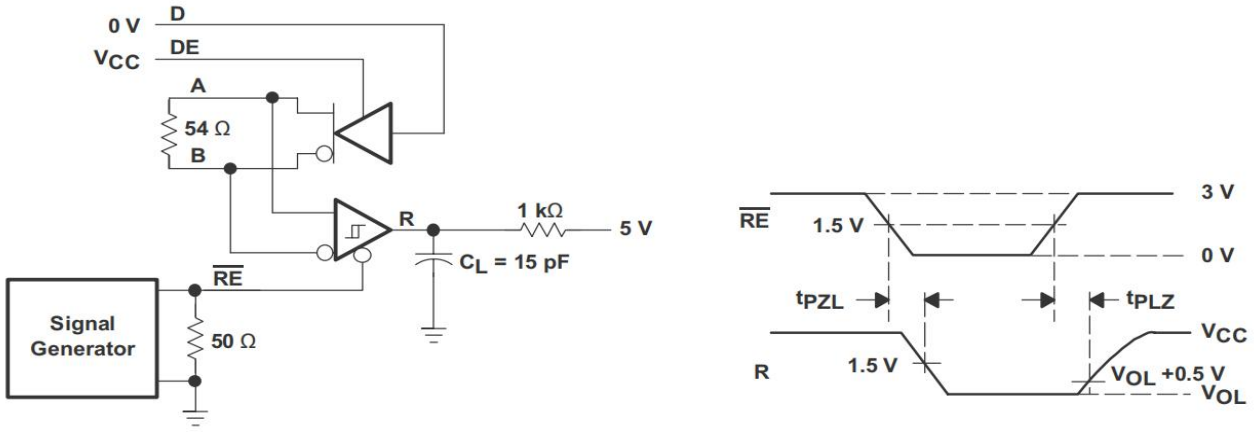


图 9-13. Receiver Enable Test Circuit and Waveforms, Data Output Low

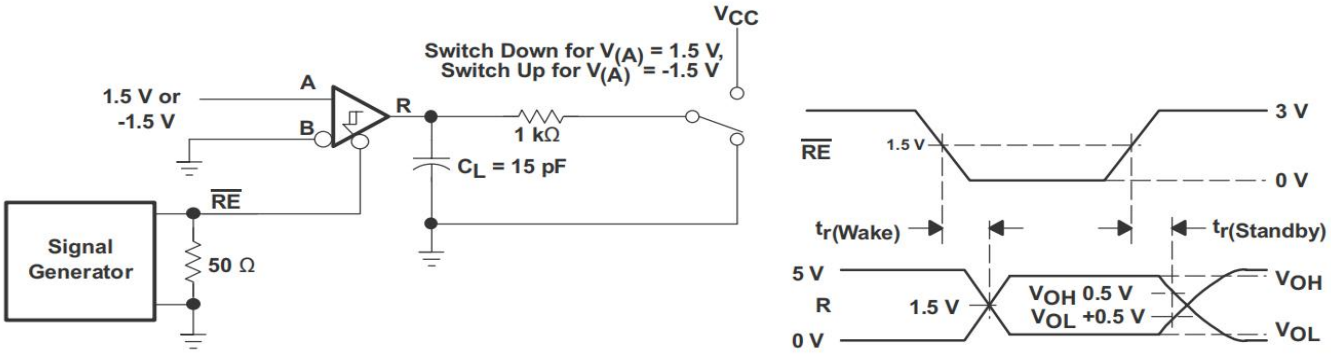


图 9-14. Receiver Standby and Wake Test Circuit and Waveforms

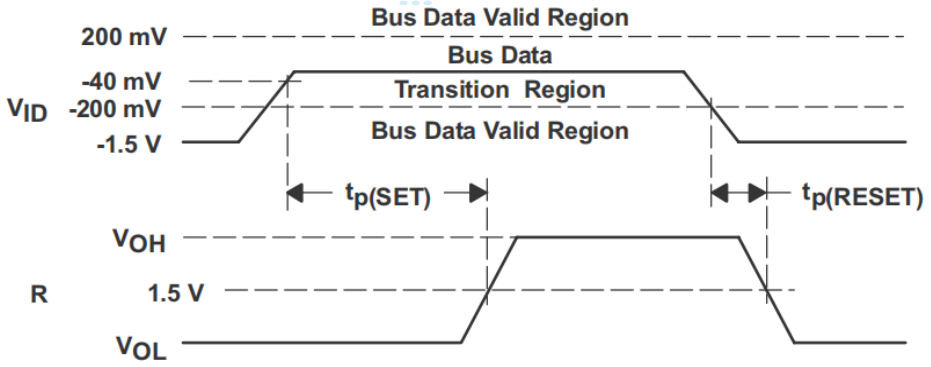


图 9-15. Receiver Active Failsafe Definitions and Waveforms

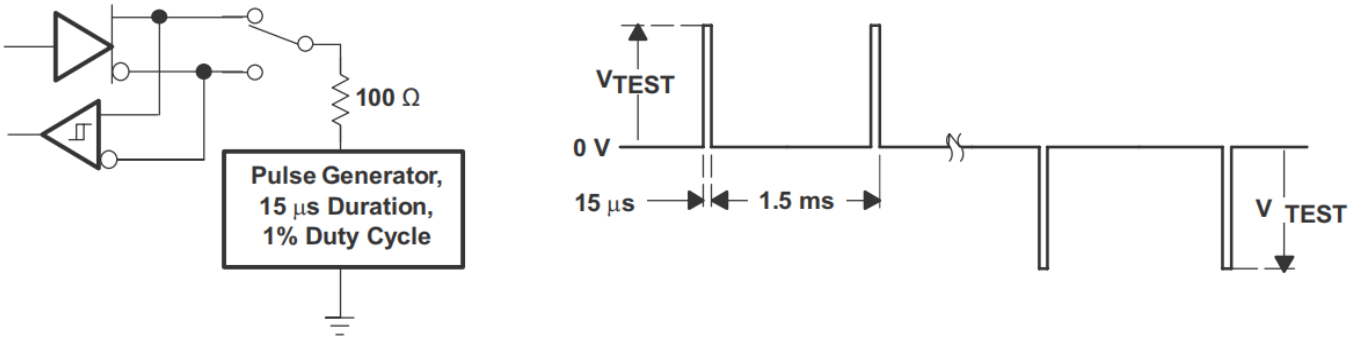


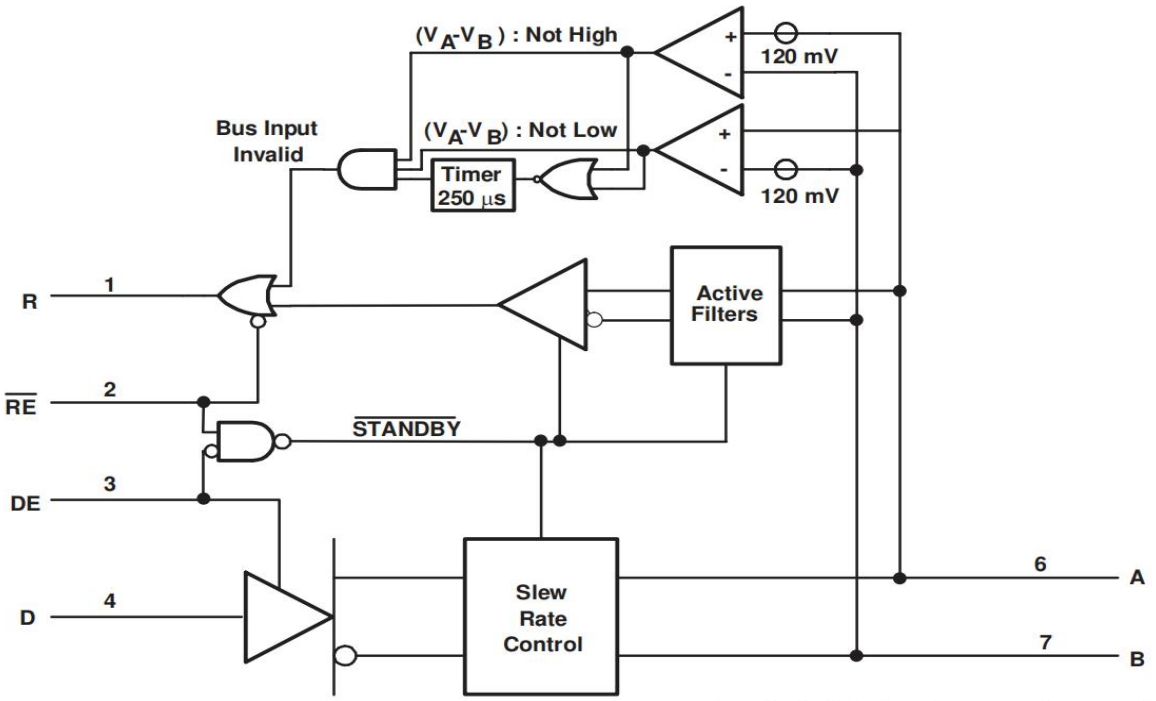
图 9-16. Test Circuit and Waveforms, Transient Overvoltage Test

10 Detailed Description

10.1 Overview

The SN65HVD2x family of devices are RS-485 compliant half-duplex transceivers designed for communication rates up to 500 kbps (SN65HVD22), 3 Mbps (SN65HVD24), 5 Mbps (SN65HVD21), or 25 Mpbs (SN65HVD20 and SN65HVD23). The devices feature extended common-mode range support, which provides immunity to larger ground potential differences that can occur between nodes that communicate over longer distances. The SN65HVD23 and the SN65HVD24 devices feature receiver equalization, which reduces the amount of data-dependent jitter that is introduced by the high-frequency losses associated with long cables.

10.2 Functional Block Diagram



10.3 Feature Description

The SN65HVD2x family of devices integrates a differential receiver and differential driver with additional features for improved performance in electrically-noisy, long-cable, or other fault-intolerant applications.

The receiver hysteresis (typically 130 mV) is much larger than found in typical RS-485 transceivers. This helps reject spurious noise signals which would otherwise cause false changes in the receiver output state.

Slew rate limiting on the driver outputs (SN65HVD2[1,2,4]) reduces the high-frequency content of signal edges. This decreases reflections from bus discontinuities, and allows longer stub lengths between nodes and the main bus line. Designers must consider the maximum signaling rate and cable length required for a specific application, and choose the transceiver best matching those requirements.

When DE is low, the differential driver is disabled, and the A and B outputs are in high-impedance states. When DE is high, the differential driver is enabled, and drives the A and B outputs according to the state of the D inputs.

When $\overline{RE}$ is high, the differential receiver output buffer is disabled, and the R output is in a high-impedance state. When $\overline{RE}$ is low, the differential receiver is enabled, and the R output reflects the state of the differential bus inputs on the A and B pins.

If both the driver and receiver are disabled, (DE low and $\overline{RE}$ high) then all nonessential circuitry, including auxiliary functions such as failsafe and receiver equalization is placed in a low-power standby state. This reduces power consumption to less than 5 μW. When either enable input is asserted, the circuitry again becomes active.

In addition to the primary differential receiver, these devices incorporate a set of comparators and logic to implement an active receiver failsafe feature. These components determine whether the differential bus signal is valid. Whenever the differential signal is close to zero volts (neither high nor low), a timer initiates, If the differential input remains within the transition range for more than 250 μs, the timer expires and set the receiver output to the high state. If a valid bus input (high or low) is received at any time, the receiver output reflects the valid bus state, and the timer is reset.

10.4 Device Functional Modes

The driver and receiver behavior for different input conditions are shown in 表 10-1 and 表 10-2, respectively.

表 **10-1. Driver Function Table**(1)

DEVICE	INPUT	ENABLE	OUTPUTS	
	D	DE	A	B
SN65HVD2[0,1,2]	H	H	H	L
	L	H	L	H
	X	L	Z	Z
	X	OPEN	Z	Z
	OPEN	H	H	L
SN65HVD2[3,4]	H	H	H	L
	L	H	L	H
	X	L	Z	Z
	X	OPEN	Z	Z
	OPEN	H	L	H

(1) Legend: H = high level, L = low level, X = don’t care, Z = high impedance (off), ? = indeterminate

表 **10-2. Receiver Function Table**(1)

DIFFERENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE $\overline{RE}$	OUTPUT R
0.2 V ≤ V_{ID}	L	H
− 0.2 V < V_{ID} < 0.2 V	L	H(2)
V_{ID} ≤ − 0.2 V	L	L
X	H	Z
X	OPEN	Z
Open circuit	L	H
Short Circuit	L	H
Idle (terminated) bus	L	H

(1) H = high level, L = low level, Z = high impedance (off)
(2) If the differential input V_{ID} remains within the transition range for more than 250 μs, the integrated failsafe circuitry detects a bus fault, and set the receiver output to a high state. See 图 9-15.

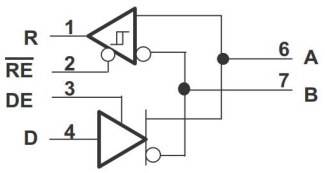


图 **10-3. Logic Diagram**

10.4.2 Equivalent Input and Output Schematic Diagrams

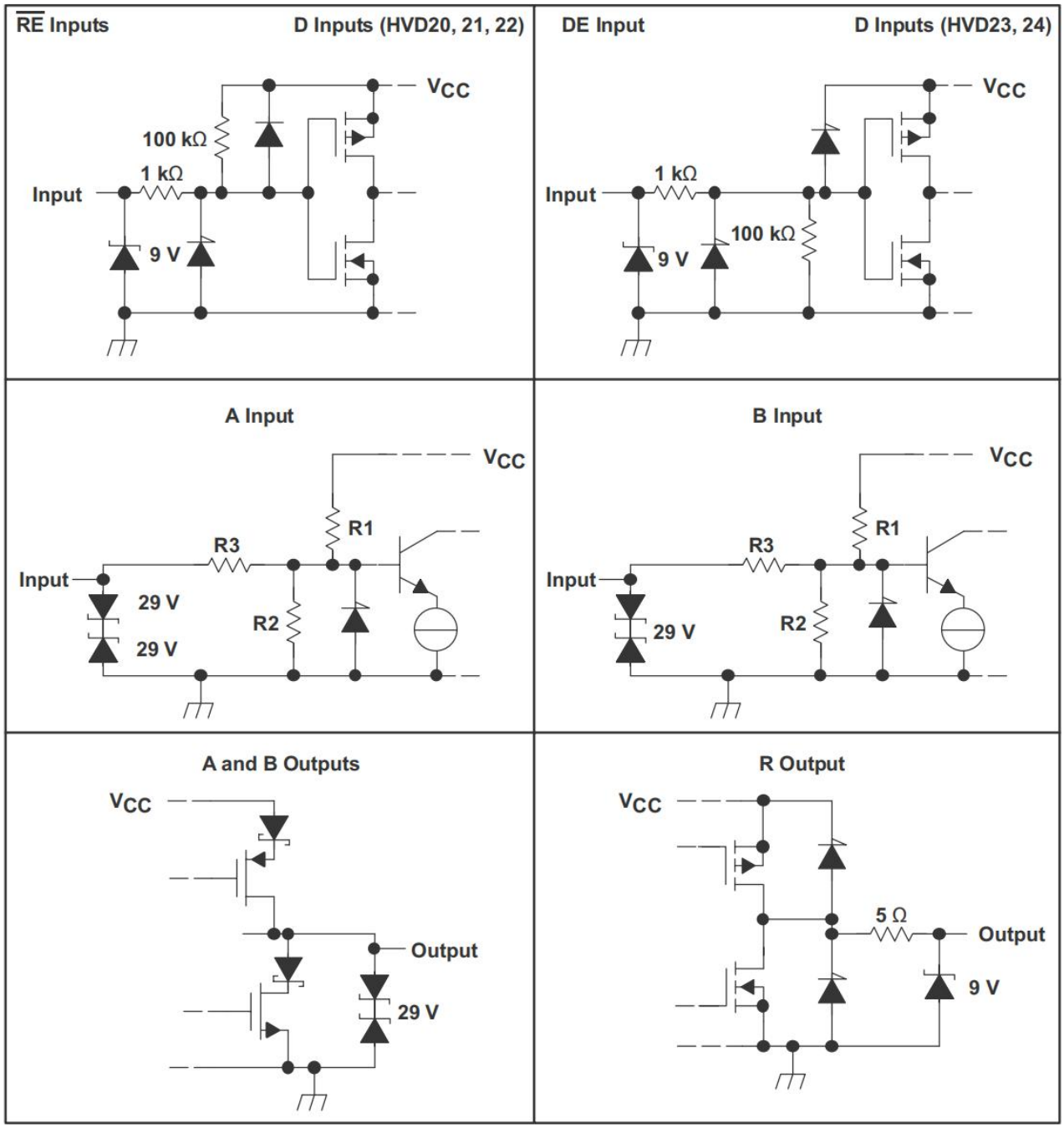


图 10-4. Equivalent Input and Output Schematic Diagrams

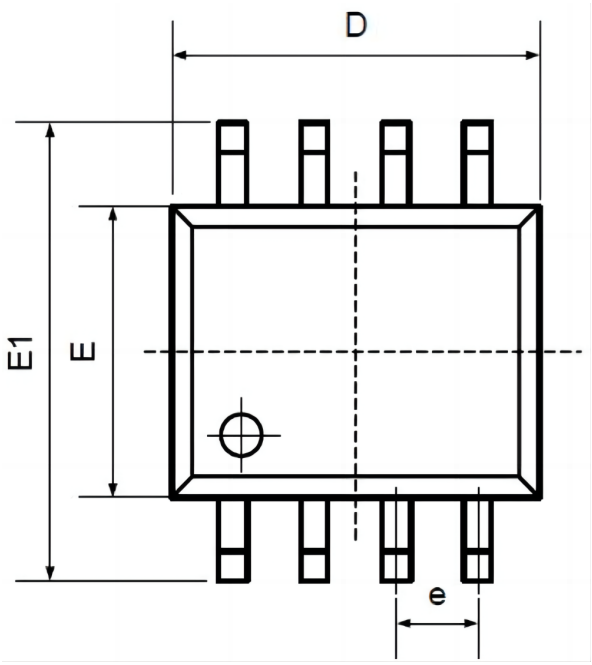
表 10-3. Input and Output Resistor Values

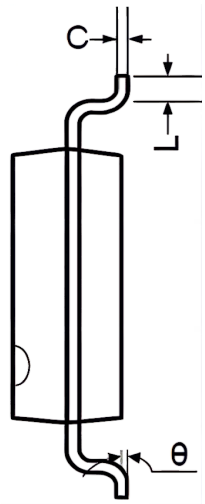
DEVICE	R1, R2	R3
SN65HVD2[0,3]	9 kΩ	45 kΩ
SN65HVD2[1,2,4]	36 kΩ	180 kΩ

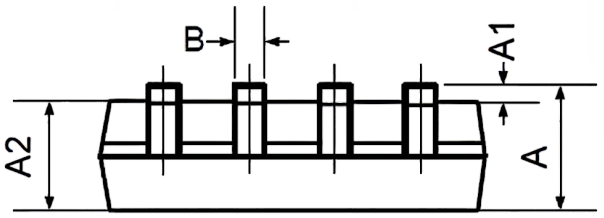
Order information

Order Number	Package	Package Quantity	Marking On The park
SN65HVD20DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD20DR
SN65HVD21DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD21DR
SN65HVD22DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD22DR
SN65HVD23DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD23DR
SN65HVD24DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD24DR

Package SOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Important statement:

●TUDI Semiconductor reserves the right to modify the product manual without prior notice! Before placing an order, customers need to confirm whether the obtained information is the latest version and verify the completeness of the relevant information.

●Any semi-guide product is subject to failure or malfunction under specified conditions. It is the buyer's responsibility to comply with safety standards when using TUDI Semiconductor products for system design and whole machine manufacturing.And take the appropriate safety measures to avoid the potential in the risk of loss of personal injury or loss of property situation!

●TUDI Semiconductor products have not been licensed for life support, military, and aerospace applications,and therefore TUDI Semiconductor is not responsible for any consequences arising from the use of this product in these areas.

●If any or all TUDI Semiconductor products (including technical data, services) described or contained in this document are subject to any applicable local export control laws and regulations, they may not be exported without an export license from the relevant authorities in accordance with such laws.

●The specifications of any and all TUDI Semiconductor products described or contained in this document specify the performance, characteristics, and functionality of said products in their standalone state, but do not guarantee the performance, characteristics, and functionality of said products installed in Customer's products or equipment. In order to verify symptoms and conditions that cannot be evaluated in a standalone device, the Customer should ultimately evaluate and test the device installed in the Customer's product device.

●TUDI Semiconductor documentation is only allowed to be copied without any alteration of the content and with the relevant authorization.TUDI Semiconductor assumes no responsibility or liability for altered documents.

●TUDI Semiconductor is committed to becoming the preferred semiconductor brand for customers, and TUDI Semiconductor will strive to provide customers with better performance and better quallity products.