Low Noise Amplifier with Bypass Switch for LTE Low Band

FEATURES

- Operating frequency 728MHz to 960MHz
- Noise figure(NF) =0.7dB
- High power gain =15.5dB
- Insertion Loss in bypass mode =3dB
- Gain mode IIP3inb=+3.2dBm
- Gain mode input 1dB compression point=-3dBm
- Bypass mode input 1dB compression point= +5dBm
- Supply voltage: 1.5V to 3.1V
- Gain mode current 7.6mA
- Bypass mode current <1uA
- Input and output DC decoupled
- Requires only one input matching inductor
- Integrated matching for the output
- FCDFN 1.1mmX0.7mmX0.37mm -6L package
- 2kV HBM ESD protection (including RFIN and RFOUT pin)

APPLICATIONS

- Cell phones
- Tablets
- Other RF front-end modules

GENERAL DESCRIPTION

The AW5008L2FDR is a Low Noise Amplifier with bypass designed for LTE receiver applications. The AW5008L2FDR requires only one external input matching inductor, reduces assembly complexity and the PCB area, enabling a cost-effective solution.

The AW5008L2FDR achieves low noise figure, high linearity, high gain, over a wide range of supply voltages from 1.5V up to 3.1V. All these features make AW5008L2FDR an excellent choice for LTE LNA as it improves sensitivity with low noise figure and high gain, provides better immunity against jammer signals with high linearity, reduces filtering requirement of preceding stage and hence reduces the overall cost.

The AW5008L2FDR is available in a small lead-free, RoHS-Compliant, FCDFN 1.1mmX0.7mmX0.37 mm -6L package.

TYPICAL APPLICATION CIRCUIT

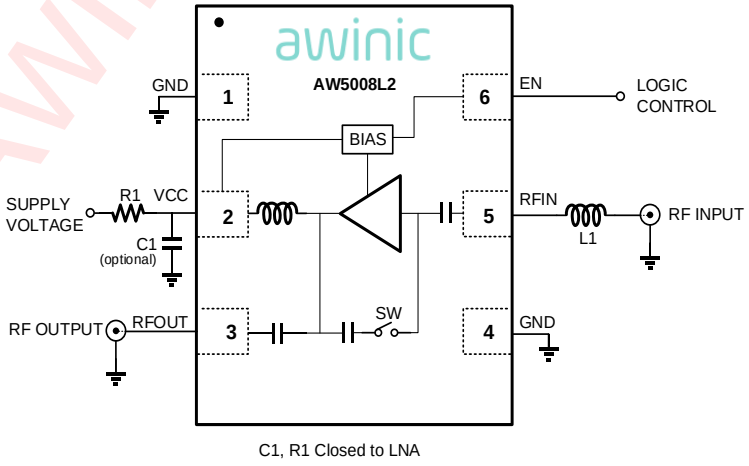

Figure 1 Typical Application Circuit of AW5008L2FDR

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PIN CONFIGURATION AND TOP MARK

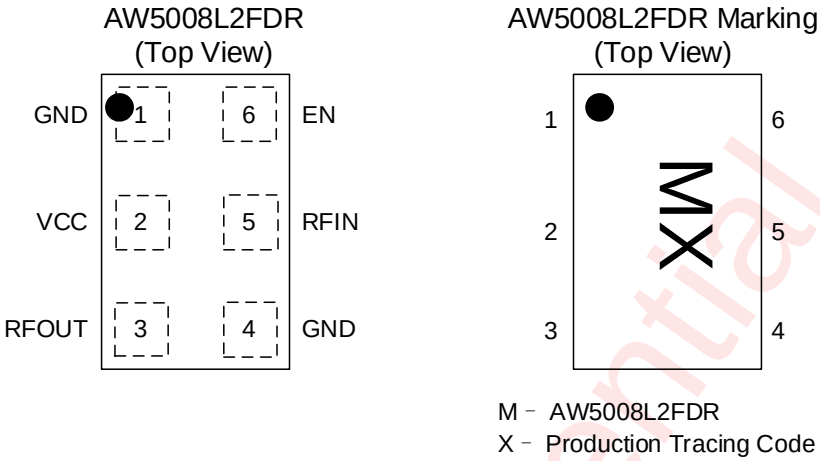

Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
1	GND	Ground.
2	VCC	Supply connection.
3	RFOUT	RF output
4	GND	Ground
5	RFIN	RF input
6	EN	EN (high level) supports 1.8V/2.8V IO with internal 150kohm pull-down resistor.

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FUNCTIONAL BLOCK DIAGRAM

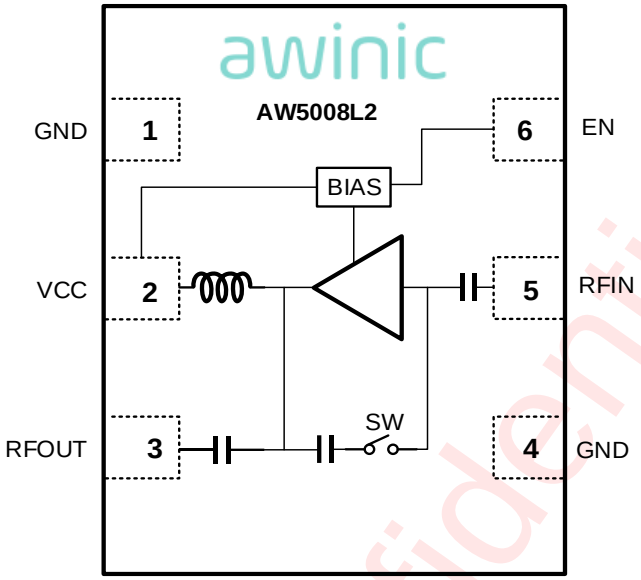

Figure 3 Functional Block Diagram

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW5008L2FDR	-40℃ ~ 85℃	FCDFN 1.1mmX 0.7mm -6L	M	MSL1	ROHS+HF	9000 units/Tape & Reel

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ABSOLUTE MAXIMUM RATINGS[1]

PARAMETERS	RANGE
Supply voltage VCC	-0.3V to 3.6V
EN pin voltage	-0.3V to 3.6V
Supply maximum current ICC	30mA
RF input power Pin	10dBm
Maximum Junction temperature T_{JMAX}	150℃
Storage temperature T_{STG}	-65℃ to 150℃
Operating free-air temperature range	-40℃ to 85℃
Lead temperature (Soldering 10 Seconds)	260℃
ESD[2]	
HBM	±2kV
CDM	±1kV
Latch-up	
Standard: JEDEC STANDARD NO.78D NOVEMBER 2011	+IT: +200mA -IT: -200mA

[1] Conditions out of those ranges listed in “absolute maximum ratings” may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in “recommended operating conditions”. Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

[2] The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883J Method 3015.9. The CDM test method: JEDEC EIA/JESD22-C101F.

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ELECTRICAL CHARACTERISTICS

DC Characteristic

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
VCC	Supply Voltage		1.5	-	3.1	V
VEN	Digital Input-Logic High		0.8			V
	Digital Input-Logic Low				0.45	V

TA=+25°C , V_{CC}=2.8V, EN=2.8V, frequency=728MHz to 960MHz. Input matched to 50Ω using a 18nH[3] inductor in series. (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Gain Mode						
ICC	Supply Current			8.6		mA
Gp	Power Gain	f=740MHz [4]		15.0		dB
		f=882MHz [5]		15.5		
		f=943MHz [6]		15.0		
Rlin	Input Return Loss	f=740MHz [4]		-6		dB
		f=882MHz [5]		-12		
		f=943MHz [6]		-12		
Rlout	Output Return Loss	f=740MHz [4]		-8.5		dB
		f=882MHz [5]		-19.0		
		f=943MHz [6]		-20.0		
ISL	Reverse Isolation	f=740MHz [4]		-27.5		dB
		f=882MHz [5]		-24.0		
		f=943MHz [6]		-24.0		
NF	Noise Figure	f=740MHz [4][7]		0.7		dB
		f=882MHz [5][7]		0.7		
		f=943MHz [6][7]		0.75		
IP1dB	In-band input 1dB-compression point	f=740MHz [4]		-3		dBm
		f=882MHz [5]		-3.8		
		f=943MHz [6]		-3.6		
IIP3ib	In-band input 3rd-order intercept point	f=740MHz [4]		1.6		dBm
		f=882MHz [5]		3		
		f=943MHz [6]		3.2		
ton	turn-on time	time from V_{EN} ON to 90% of the gain		2.2		μs
toff	turn-off time	time from V_{EN} OFF to 10% of the gain		0.5		μs
Bypass Mode						

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Symbol	Parameter	Test Condition	Min	Typ	Max	Units
ICC	Supply Current	VEN<0.45V			1	uA
Gp	Power Gain	f=740MHz [4]		-4.0		dB
		f=882MHz [5]		-3.0		
		f=943MHz [6]		-3.0		
RLin	Input Return Loss	f=740MHz [4]		-12.0		dB
		f=882MHz [5]		-10.0		
		f=943MHz [6]		-9.0		
RLout	Output Return Loss	f=740MHz [4]		-8.0		dB
		f=882MHz [5]		-18.0		
		f=943MHz [6]		-23.0		
IP1dB	In-band input 1dB-compression point	f=740MHz [4]		5		dBm
		f=882MHz [5]		4		
		f=943MHz [6]		4		

[3] High quality-factor 18nH inductor.
[4] E-UTRA operating band 17(734MHz to 746MHz) , input power is -25dBm.
[5] E-UTRA operating band 5(869MHz to 894MHz) , input power is -25dBm.
[6] E-UTRA operating band 8(925MHz to 960MHz) , input power is -25dBm.
[7] PCB losses are subtracted.

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TA=+25°C , V_{CC}=1.8V, EN=1.8V, frequency=728MHz to 960MHz. Input matched to 50Ω using a 18nH[3] inductor in series. (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Gain Mode						
ICC	Supply Current			7.6		mA
Gp	Power Gain	f=740MHz [4]		14.5		dB
		f=882MHz [5]		15.0		
		f=943MHz [6]		14.5		
RLin	Input Return Loss	f=740MHz [4]		-6		dB
		f=882MHz [5]		-11.0		
		f=943MHz [6]		-11.0		
RLout	Output Return Loss	f=740MHz [4]		-8.0		dB
		f=882MHz [5]		-20.0		
		f=943MHz [6]		-22.0		
ISL	Reverse Isolation	f=740MHz [4]		-27.5		dB
		f=882MHz [5]		-24.5		
		f=943MHz [6]		-24.0		

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Symbol	Parameter	Test Condition	Min	Typ	Max	Units
NF	Noise Figure	f=740MHz [4][7]		0.75		dB
		f=882MHz [5][7]		0.75		
		f=943MHz [6][7]		0.8		
IP1dB	In-band input 1dB-compression point	f=740MHz [4]		-7.5		dBm
		f=882MHz [5]		-8.0		
		f=943MHz [6]		-7.5		
IIP3ib	In-band input 3rd-order intercept point	f=740MHz [4]		1.1		dBm
		f=882MHz [5]		2.1		
		f=943MHz [6]		2.8		
ton	turn-on time	time from V_{EN} ON to 90% of the gain		1		μs
toff	turn-off time	time from V_{EN} OFF to 10% of the gain		0.5		μs
Bypass Mode						
ICC	Supply Current	VEN<0.45V			1	uA
Gp	Power Gain	f=740MHz [4]		-4.0		dB
		f=882MHz [5]		-3.0		
		f=943MHz [6]		-3.0		
RLin	Input Return Loss	f=740MHz [4]		-13.0		dB
		f=882MHz [5]		-11.0		
		f=943MHz [6]		-9.5		
RLout	Output Return Loss	f=740MHz [4]		-8.0		dB
		f=882MHz [5]		-18.0		
		f=943MHz [6]		-23.0		
IP1dB	In-band input 1dB-compression point	f=740MHz [4]		5.0		dBm
		f=882MHz [5]		4.0		
		f=943MHz [6]		4.0		

[3] High quality-factor 18nH inductor.
[4] E-UTRA operating band 17(734MHz to 746MHz) , input power is -25dBm.
[5] E-UTRA operating band 5(869MHz to 894MHz) , input power is -25dBm.
[6] E-UTRA operating band 8(925MHz to 960MHz) , input power is -25dBm.
[7] PCB losses are subtracted.

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AW5008L2FDR APPLICATION BOARD

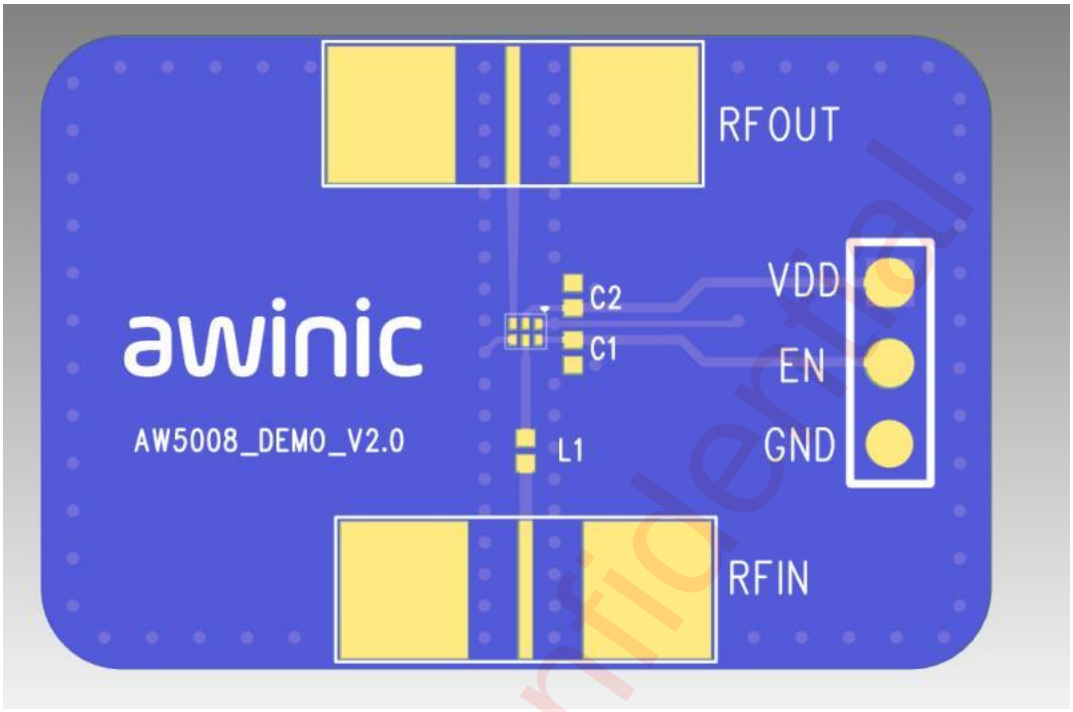

Figure 4 AW5008L2FDR EVB

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MEASUREMENT DIAGRAM

Test DC Characteristics(Current & Power Consumption)

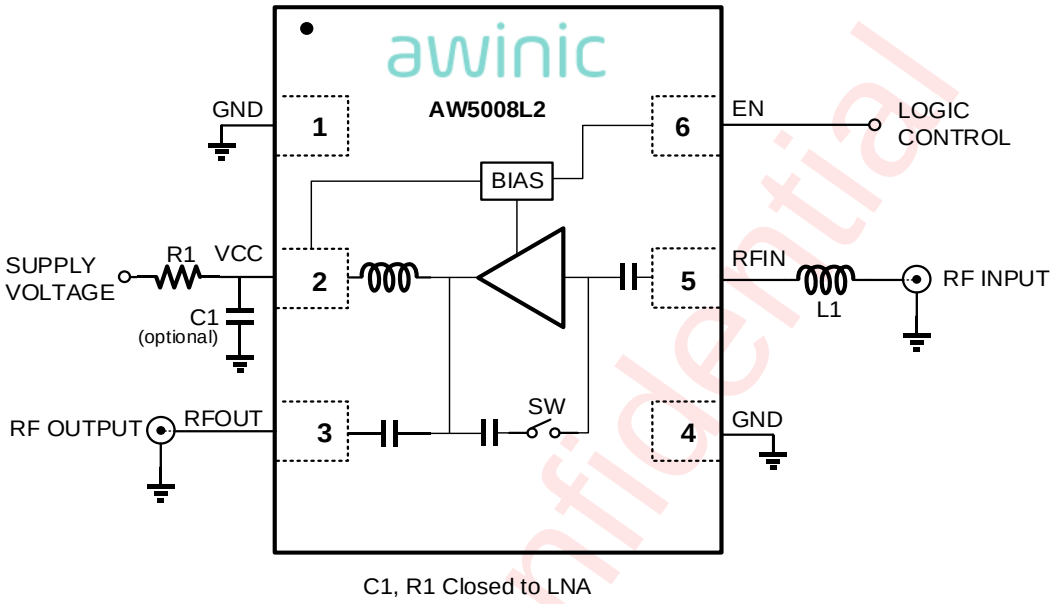

Figure 5 AW5008L2FDR DC Test Diagram

Test S-Parameter

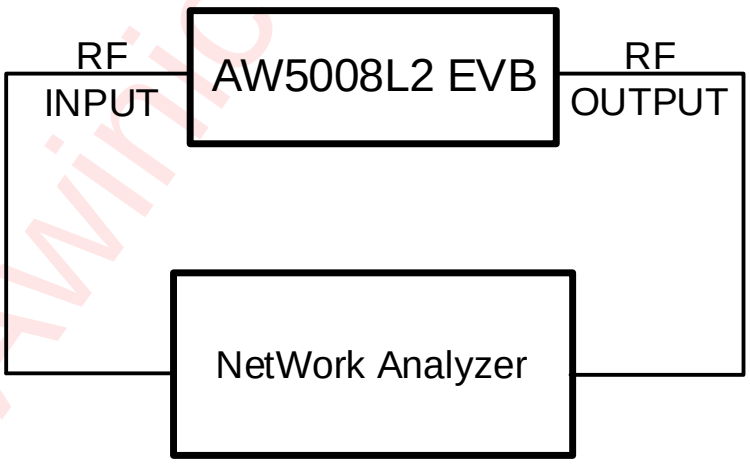

Figure 6 AW5008L2FDR S-parameter Measurement Diagram

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Test Noise Figure

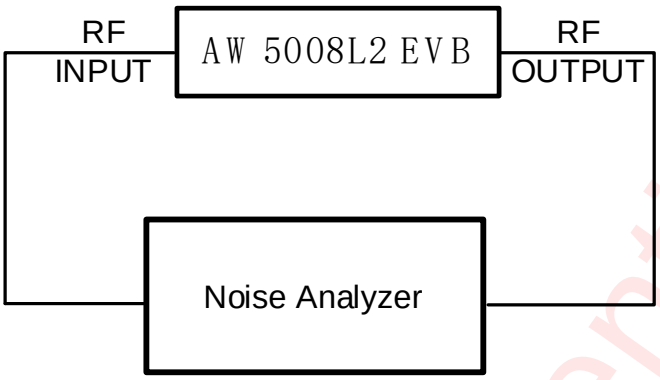

Figure 7 AW5008L2FDR Noise Figure Measurement Diagram

Test IIP3

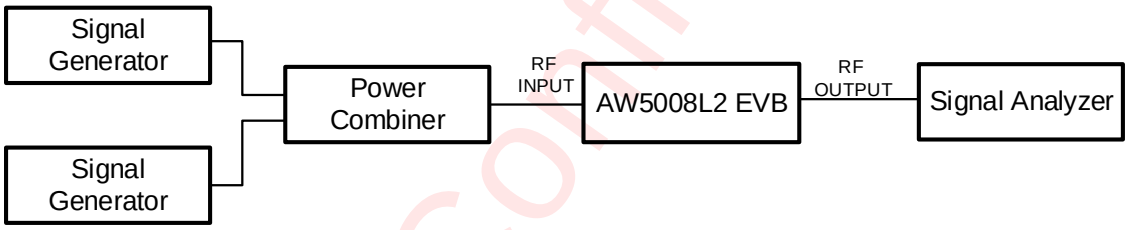

Figure 8 AW5008L2FDR IIP3 Measurement Diagram

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APPLICATION INFORMATION

Choice of components

1. The AW5008L2FDR requires only one external inductor for input matching. If the device/phone manufacturers implement very good power supply filtering on their boards, the bypass capacitor mentioned in this application circuit may be optional. With the power supply decoupling capacitor, better performance would be received, like a little higher gain, etc. The value is optimized for the key performance, such as higher power gain, lower noise figure, and better return loss. Typical value of inductor is 18nH with high quality factor, and capacitor is 1nF. The typical application circuit can refer to Figure1.

2. The output of AW5008L2FDR is internally matched to 50 ohm and a DC blocking capacitor is integrated on-chip, thus no external component is required at the output.

3. The AW5008L2FDR should be placed close to the diversity antenna with the input-matching inductor. Use 50 ohm micro-strip lines to connect RF INPUT and RF OUTPUT. Bypass capacitor need be located close to the device. For long V_{CC} lines, it may be necessary to add more decoupling capacitors. Proper grounding of the GND pins is very important.

Following tables show recommended inductor and capacitor values.

Inductor Selection Table

Part	Typical(nH)	Q(min)	Frequency(MHz)	MFR	Size
LQW15A	18	25	250	Murata	0402

Capacitor Selection Table

Part	Typical(pF)	Voltage(V)	MFR	Size
GRM155	1000	50	Murata	0402

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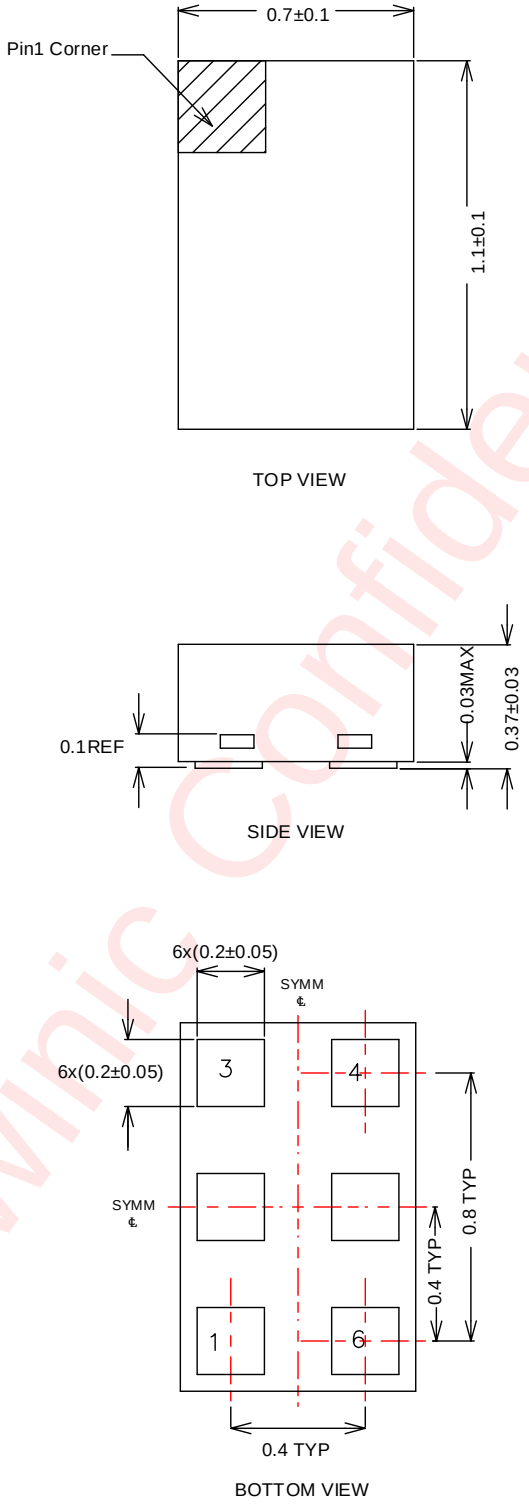
PACKAGE DESCRIPTION



Unit: mm

Figure 9 Package Outline

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LAND PATTERN

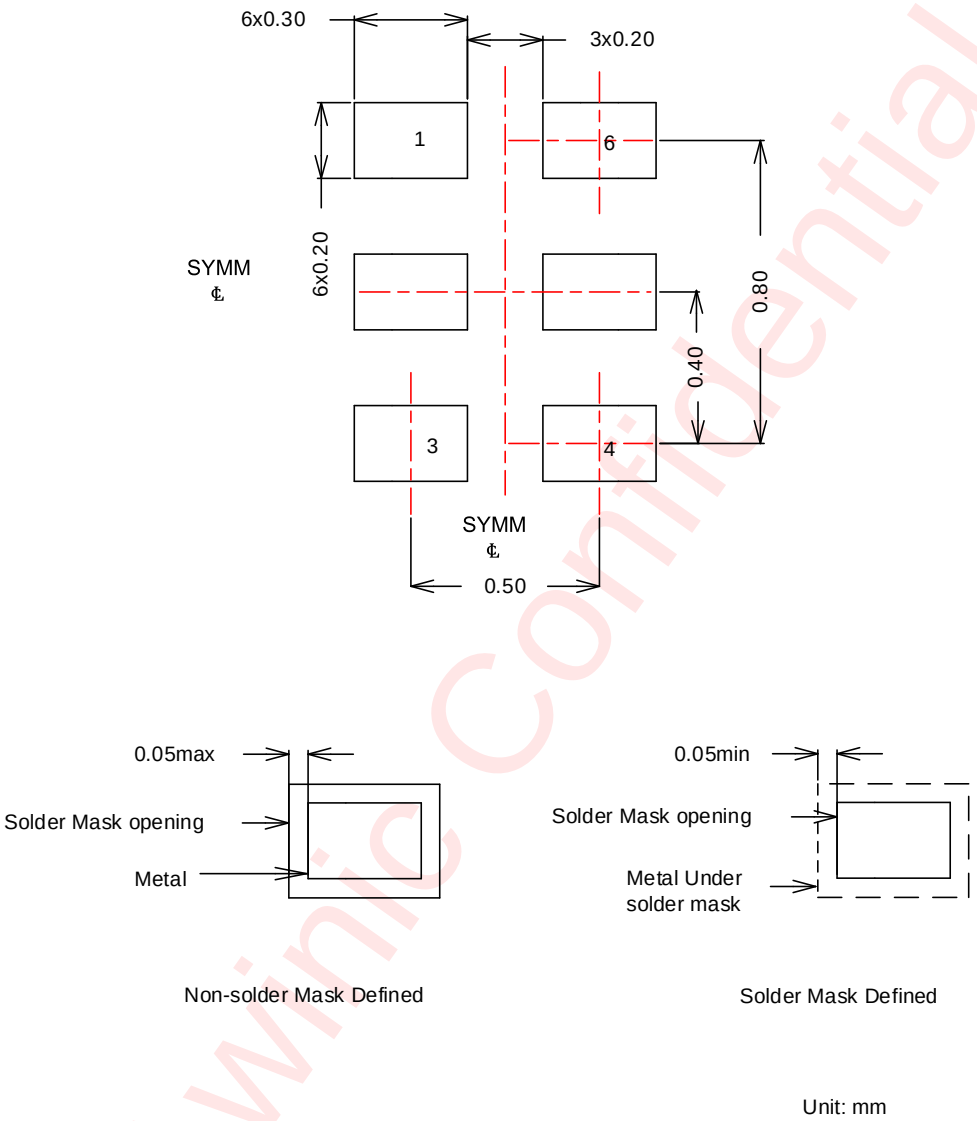

Figure 10 Land Pattern

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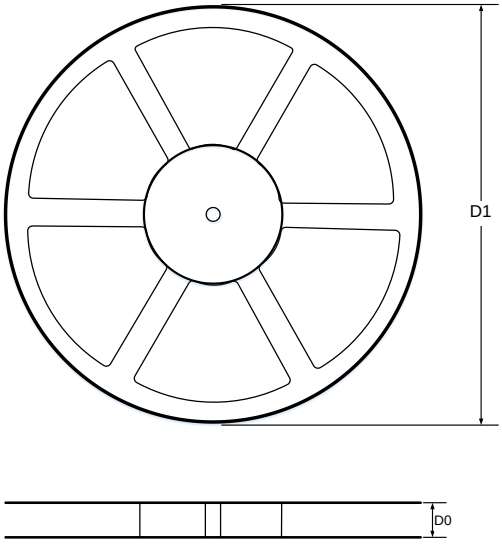
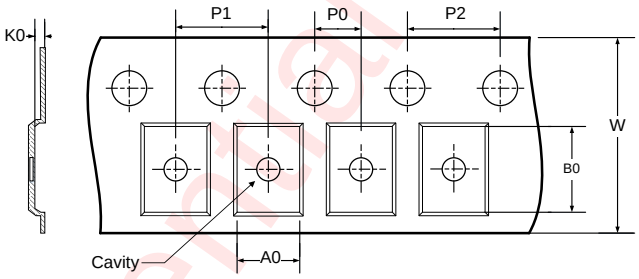
TAPE & REEL DESCRIPTION

REEL DIMENSIONS

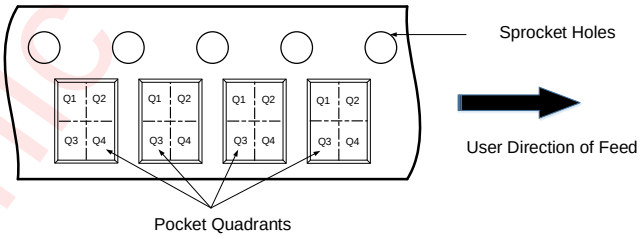


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D0：Reel width
D1：Reel diameter

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

All dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	0.8	1.2	0.55	2	2	4	8	Q1

Figure 11 Tape & Reel Description

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REVISION HISTORY

Version	Date	Change Record
V1.0	Sept. 2018	Officially Released
V1.1	Jan. 2019	Update FCDFN
V1.2	Dec. 2024	Update MPQ

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