Ultra-Low Noise, High PSRR, 500 mA Low-Dropout Linear Regulator

Features

- Input voltage range: 2.2V to 5.5V
- Available in fixed voltage option: 1.2V,3.3V
- Rated output current: 500mA
- Quiescent current: typical 22μA
- Typical 0.1μA shutdown current
- Typical 550mV dropout voltage (I_{OUT}=500mA, 1.2V output)
- Power supply rejection ratio: typical 87dB (I_{OUT}=50mA, Freq=1kHz, 1.2V output)
- Noise: typical 12μVrms (I_{OUT}=50mA, BW=10Hz to 100kHz, 1.2V output)
- Built-in output short protection: typical 150mA when output short to ground
- DFN 1mmX1mmX0.37mm-4L package and SOT 23-5L package

Applications

Battery-powered equipment

Smart phone

Digital camera

Other portable electronic device

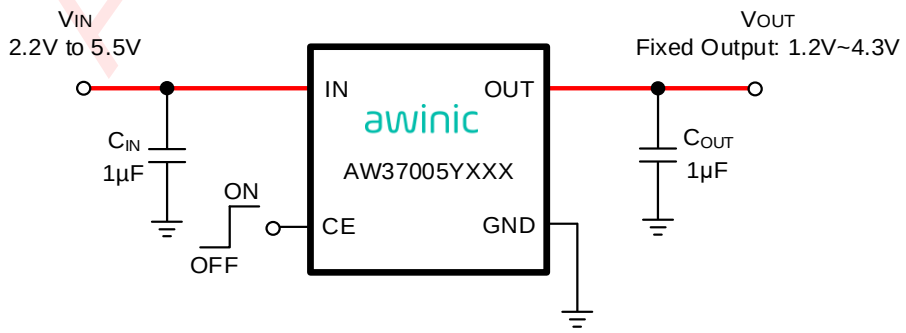
General Description

AW37005YXXX is a low dropout voltage regulator featuring low ON resistance, high PSRR, low Noise, good load/line transient response and smooth soft-start.

AW37005YXXX integrates current limit, short circuit protection, thermal shutdown, sufficiently protecting IC from being damaged.

AW37005YXXX is designed to work with a 1μF or more input ceramic capacitor and a 1μF or more output ceramic capacitor. The low power dissipation and good dynamic response make AW37005YXXX very suitable for hand-held communication equipment. Tiny package makes high density mounting of the IC on boards possible.

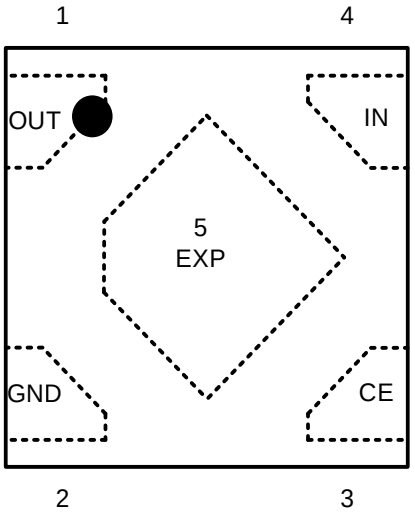
Typical Application Circuit



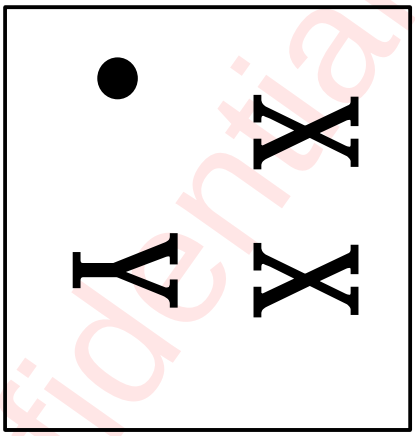
Pin Configuration And Top Mark

DFN 1X1-4L

AW37005YXXXDNR
(Top View)



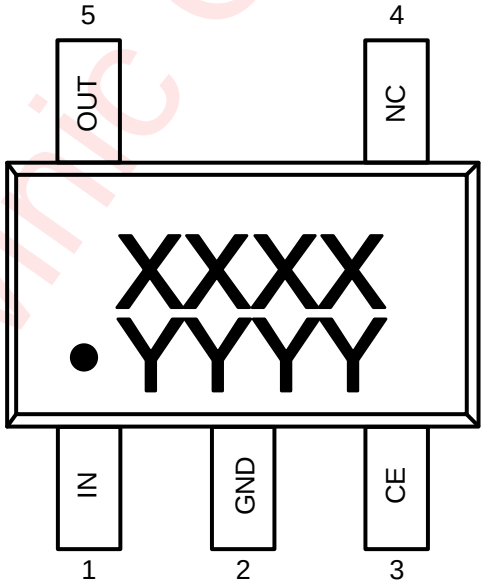
AW37005YXXXDNR Marking
(Top View)



XX –AW37005YXXXDNR
Y –Production Tracing Code

SOT 23-5L

AW37005YXXXSTR Marking
(Top View)



XXXX – AW37005YXXXSTR
YYYY – Production Tracing Code

Pin Definition

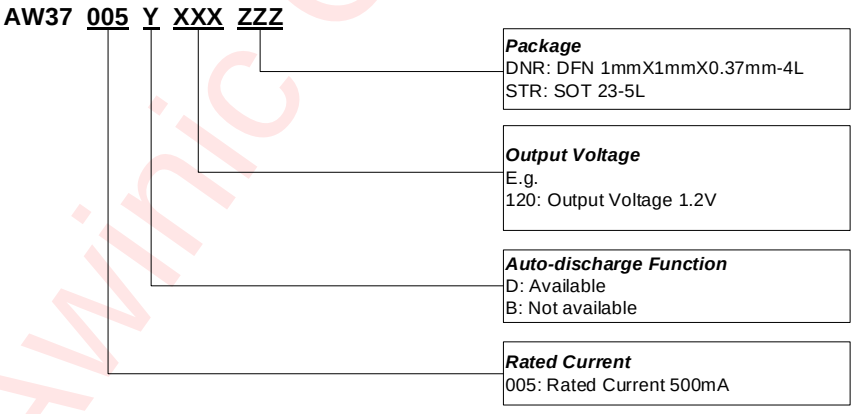
DFN 1X1-4L

No.	NAME	DESCRIPTION
1	OUT	Regulated output voltage pin. Put a 1μF or more ceramic capacitor at the output pin.
2	GND	Ground.
3	CE	Chip enable pin. Built-in 420nA pull-down current. (High Active)
4	IN	Input supply pin. Put a 1μF or more bypass capacitor at the power supply.
5	EXP	Expose pad should be tied to ground plane for better power dissipation.

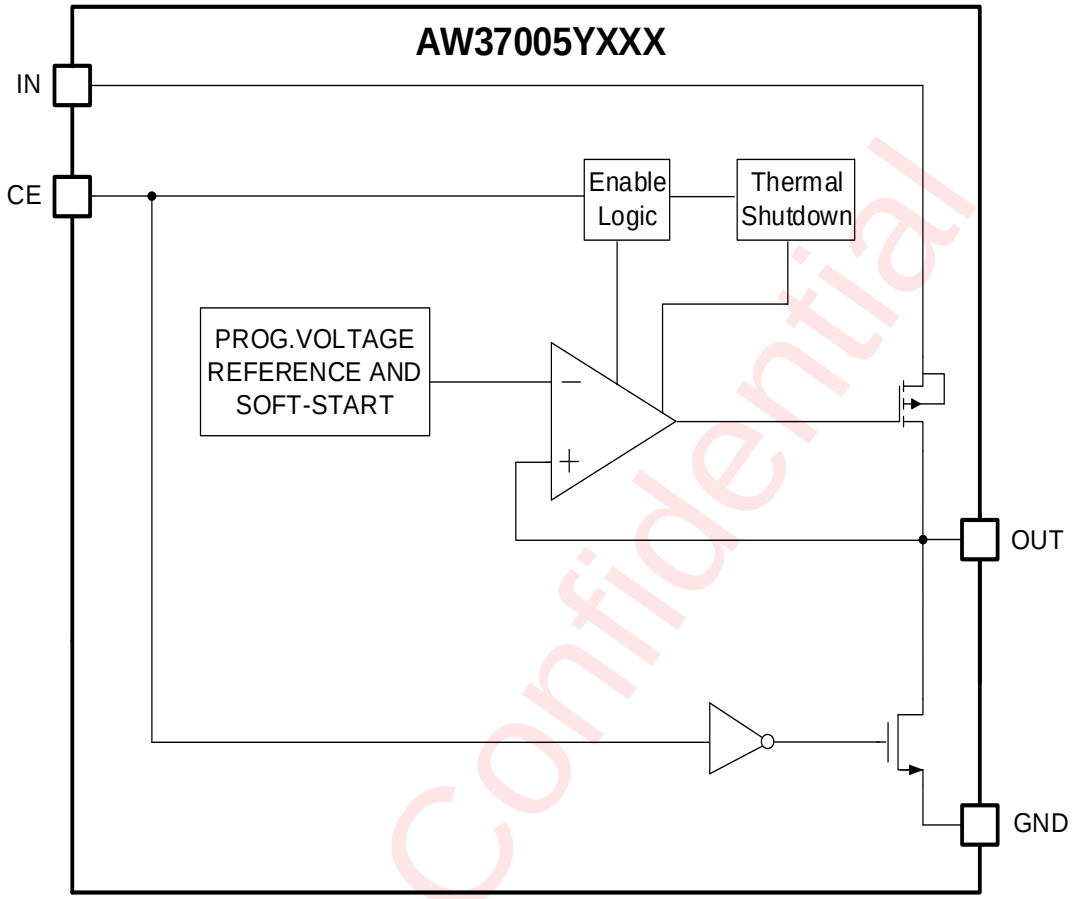
SOT 23-5L

No.	NAME	DESCRIPTION
1	IN	Input supply pin. Put a 1μF or more bypass capacitor at the power supply.
2	GND	Ground.
3	CE	Chip enable pin. Built-in 420nA pull-down current. (High Active)
4	NC	Not connected.
5	OUT	Regulated output voltage pin. Put a 1μF or more ceramic capacitor at the output pin.

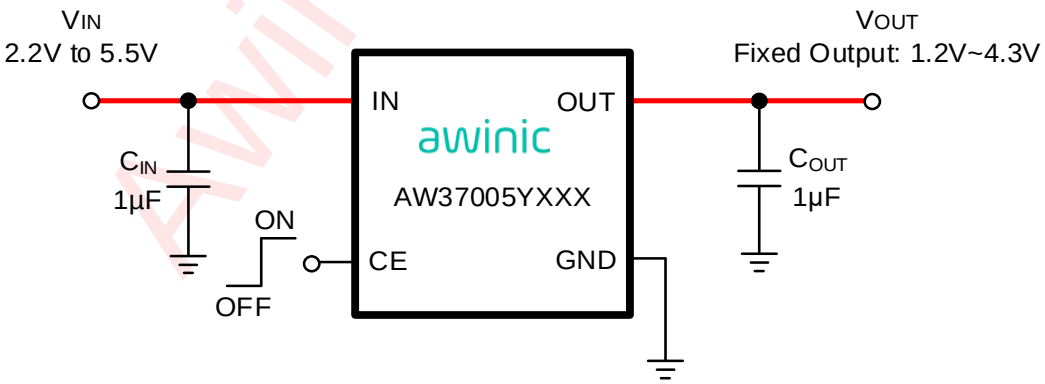
Name Rule



Functional Block Diagram



Typical Application Circuit



AW37005YXXX Application Circuit

Notice for typical application circuits:

Capacitance of C_{IN} and C_{OUT} should be 1μF or more.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW37005D120DNR	-40°C～85°C	DFN 1X1-4L	BA	MSL1	ROHS+HF	9000 units/ Tape and Reel
AW37005D330STR	-40°C～85°C	SOT 23-5L	8L30	MSL3	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Input voltage range		-0.3V to 6.5V
Enable control voltage range		-0.3V to 6.5V
Output voltage range		-0.3V to VIN+0.3V, max. 6.5V
Maximum operating junction temperature T_{J_MAX}		150°C
Recommended operating junction temperature T_{J_REC}		-40°C to 125°C
Operating free-air temperature range		-40°C to 85°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
Junction-to-ambient thermal resistance $R_{\theta JA}$(NOTE2)	DFN 1X1-4L	215.4°C/W
	SOT 23-5L	177.4°C/W
ESD	HBM (Human body model)(NOTE3)	±2kV
	CDM(Charged device model) (NOTE4)	±1.5kV
Latch-Up(NOTE5)		+IT：200mA - IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Thermal resistances follow JEDEC 2S2P standards, and is usually highly dependent on PCB layout. Exceptionally, $R_{\theta JC(top)}$ of DFN 1mmX1mm-4L Package follows SEMI standard G43-87.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS-001: 2017.

NOTE4: All pins. Test Condition: ESDA/JEDEC JS-002: 2022.

NOTE5: Test Condition: JEDEC Standard No.78F.01.

Electrical Characteristics

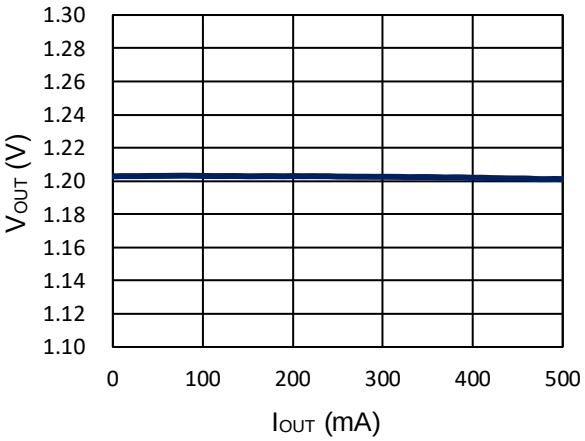
V_{IN}=$V_{OUT(SET)}$+1V, V_{CE}>1V, I_{OUT}=1mA, C_{IN}=C_{OUT}=1μF, T_A=25°C (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range			2.2		5.5	V
V_{OUT_ACC}	Output Voltage Accuracy	DFN 1X1-4L	T_A=25°C	-1		1	%
			-40°C ≤T_A≤85°C	-2		2	
		SOT 23-5L	T_A=25°C	-1.5		1.5	
			-40°C ≤T_A≤85°C	-2.5		2.5	
V_{OUT}	Output Voltage Range			1.2		4.3	V
$LOAD_{Reg}$	Load Regulation	1mA≤I_{OUT}≤500mA			5	20	mV
$LINE_{Reg}$	Line Regulation	2.2V≤V_{IN} ≤5.5V			0.1		mV
$V_{dropout}$	Dropout Voltage	I_{OUT}=500mA, When V_{OUT} falls 100mV below $V_{OUT(SET)}$	$V_{OUT(SET)}$=1.2V		550		mV
			$V_{OUT(SET)}$=3.3V		174		
I_{SD}	Shutdown Current	V_{CE}<0.4V			0.1	1	μA
I_Q	Quiescent Current	I_{OUT}=0mA			22		μA
V_{CEH}	CE Input Voltage “H”	-40°C ≤T_A≤85°C		0.84			V
V_{CEL}	CE Input Voltage “L”	-40°C ≤T_A≤85°C				0.36	V
PSRR	Power Supply Ripple Rejection	V_{IN}=2.3V I_{OUT}=50mA, $V_{OUT(SET)}$=1.2V	f=1kHz		87		dB
			f=10kHz		90		
			f=100kHz		72		
			f=1MHz		42		
V_N	Output Voltage Noise	I_{OUT}=50mA, BW=10Hz to 100kHz	$V_{OUT(SET)}$=1.2V		12		μVrms
			$V_{OUT(SET)}$=3.3V		20		
I_{CL}	Output Current Limit	V_{OUT}=90%*$V_{OUT(SET)}$		500			mA
I_{SC}	Short Current Limit	V_{OUT}<10%*$V_{OUT(SET)}$			150		mA
R_{DISC}	Auto Discharge Resistance	V_{CE}<0.36V			200		Ω
I_{CE}	CE Pull Down Current	V_{CE}=5V			420		nA
T_{SDH}	Thermal Shutdown Threshold	Temperature Rising			160		°C
T_{SDL}	Thermal Shutdown Reset Threshold	Temperature Falling			135		°C

Typical Characteristics

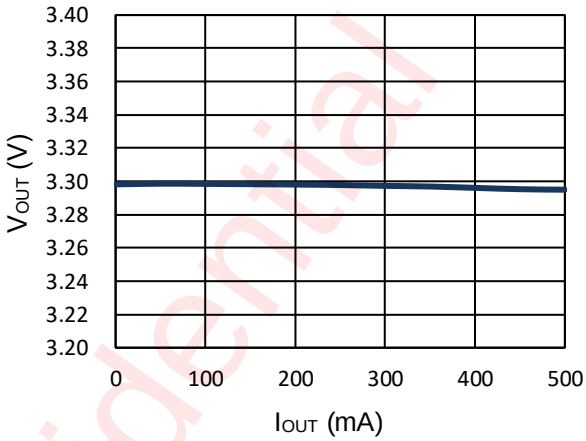
V_{IN}=$V_{OUT(SET)}$+1V, V_{CE}>1V, I_{OUT}=1mA, C_{IN}=C_{OUT}=1μF, T_A=25°C, In Typical Application Circuit, unless otherwise noted.

AW37005D120



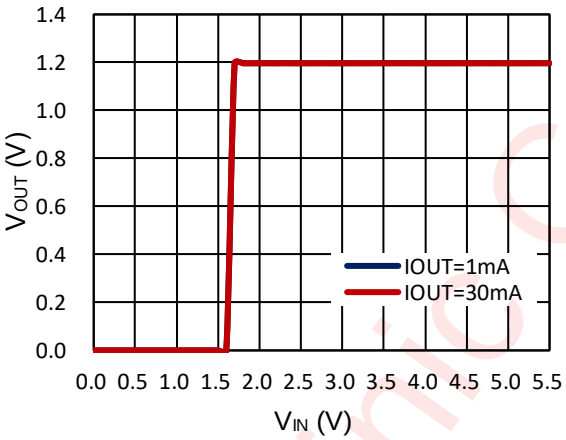
Output Voltage vs Output Current

AW37005D330



Output Voltage vs Output Current

AW37005D120



Output Voltage vs Input Voltage

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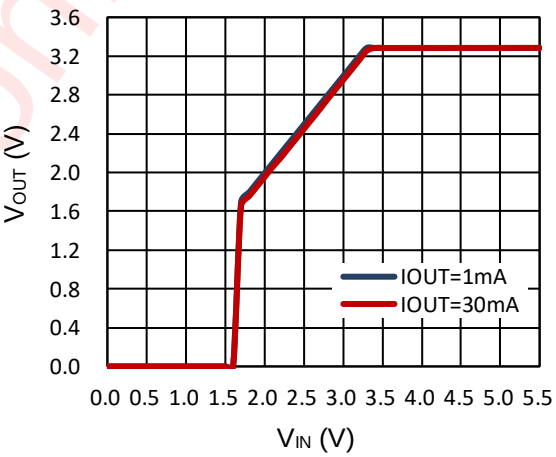

Output Voltage vs Input Voltage

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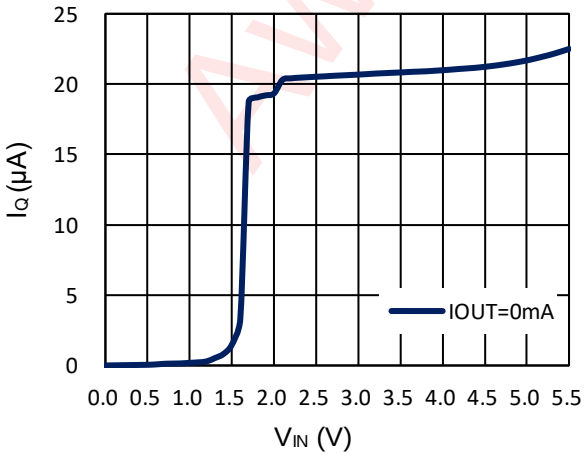
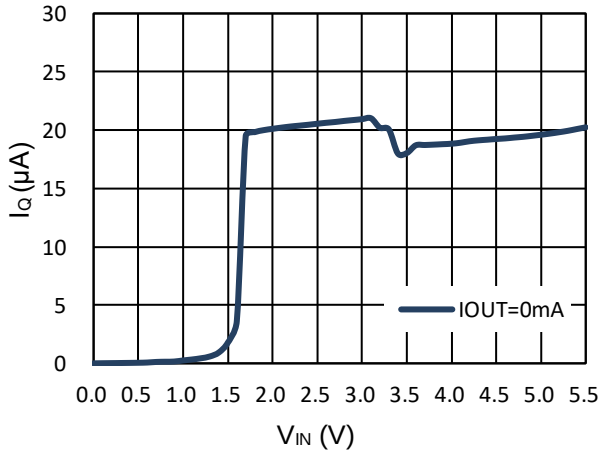


Quiescent Current vs Input Voltage

AW37005D330



Quiescent Current vs Input Voltage

Typical Characteristics (Continued)

V_{IN}=$V_{OUT(SET)}$+1V, V_{CE}>1V, I_{OUT}=1mA, C_{IN}=C_{OUT}=1μF, T_A=25°C, In Typical Application Circuit, unless otherwise noted.

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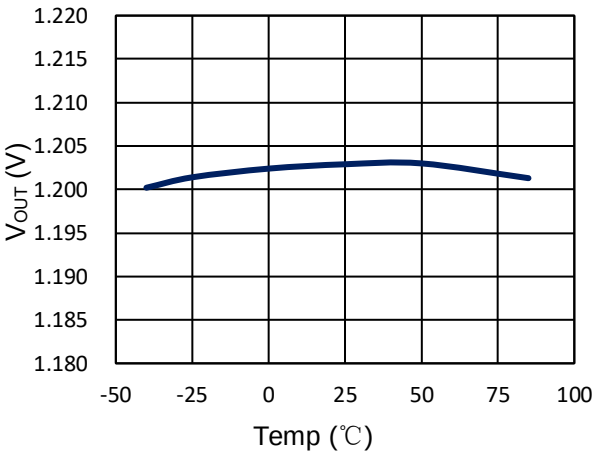
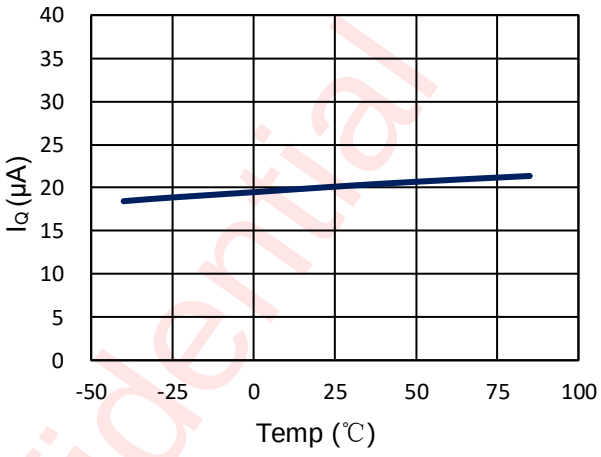


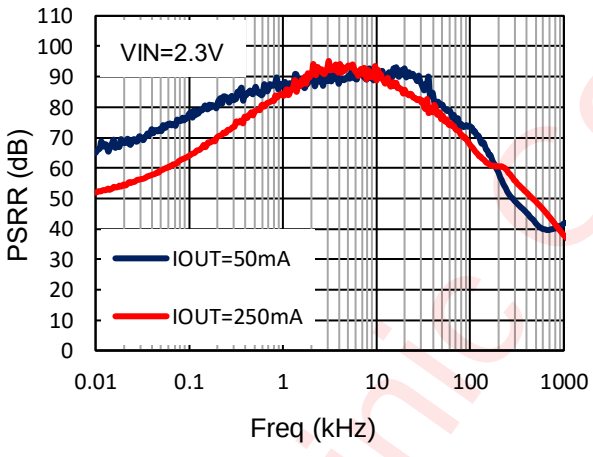
Output Voltage vs Temperature

AW37005D120



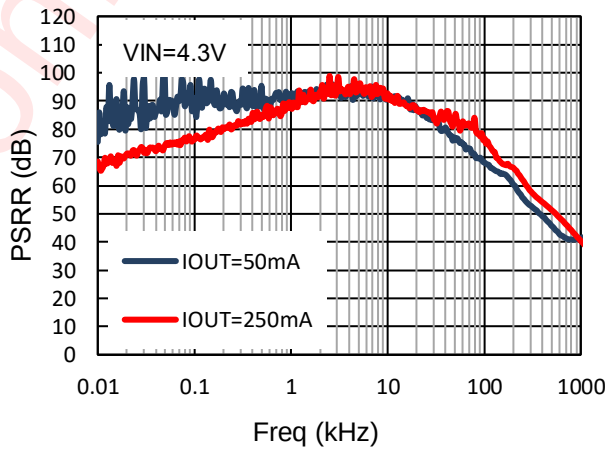
Quiescent Current vs Temperature

AW37005D120



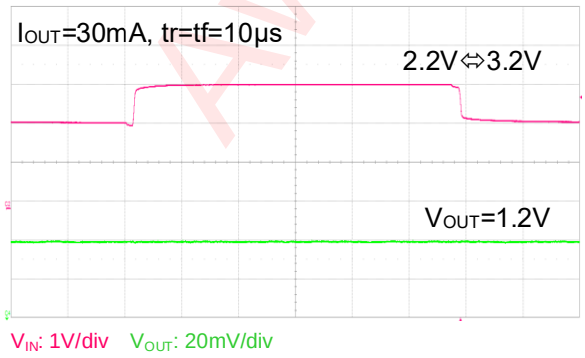
PSRR vs Frequency

AW37005D330



PSRR vs Frequency

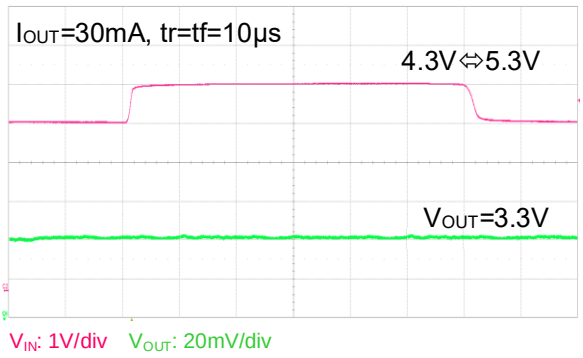
AW37005D120



Time(200μs/div)

Input Transient Response

AW37005D330



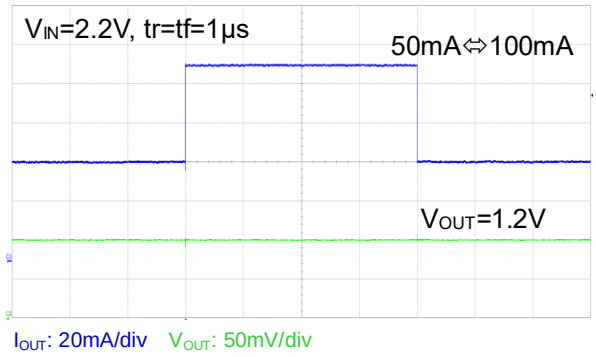
Time(200μs/div)

Input Transient Response

Typical Characteristics (Continued)

$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25°C$, In Typical Application Circuit, unless otherwise noted.

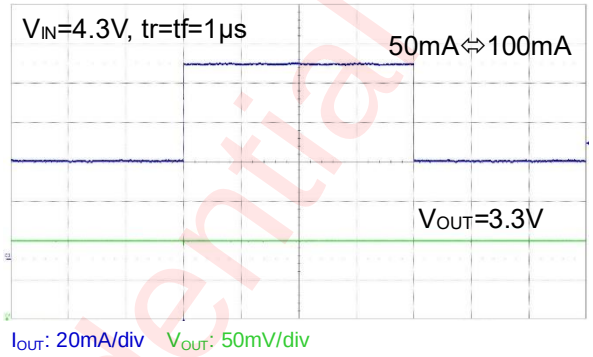
AW37005D120



Time(500μs/div)

Load Transient Response

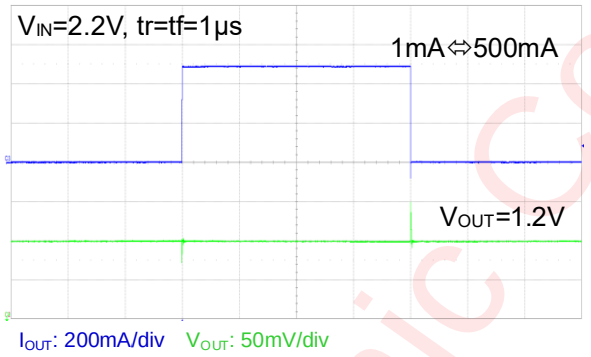
AW37005D330



Time(500μs/div)

Load Transient Response

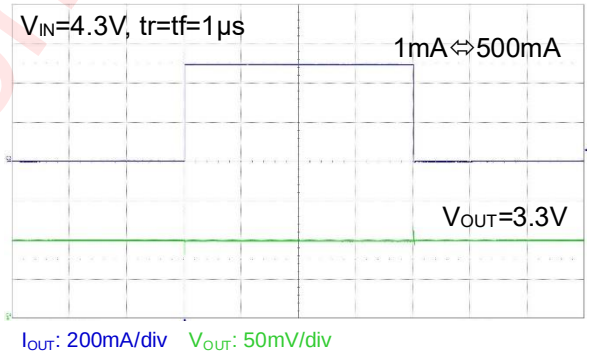
AW37005D120



Time(500μs/div)

Load Transient Response

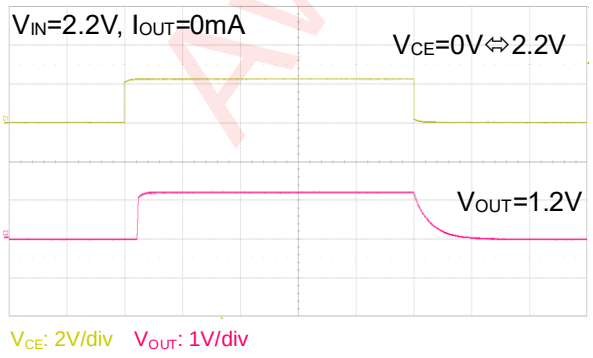
AW37005D330



Time(500μs/div)

Load Transient Response

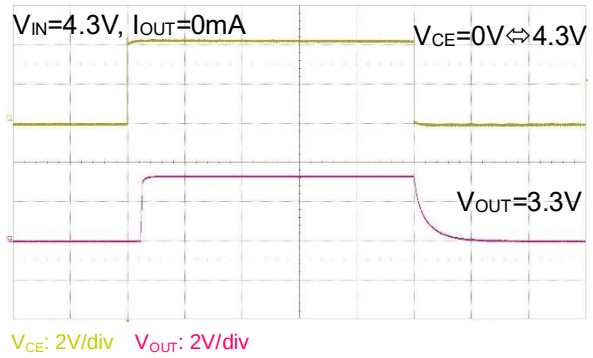
AW37005D120



Time(1ms/div)

Turn On&Off Speed with CE pin

AW37005D330



Time(1ms/div)

Turn On&Off Speed with CE pin

Typical Characteristics (Continued)

V_{IN}=$V_{OUT(SET)}$+1V, V_{CE}>1V, I_{OUT}=1mA, C_{IN}=C_{OUT}=1μF, T_A=25°C, In Typical Application Circuit, unless otherwise noted.

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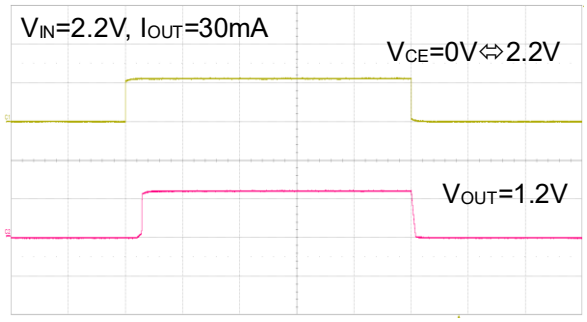
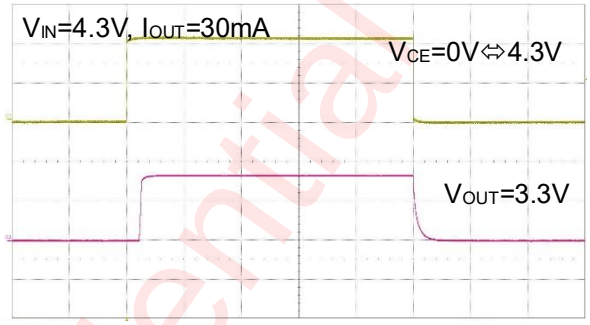


Time(1ms/div)

Turn On&Off Speed with CE pin

AW37005D330



Time(1ms/div)

Turn On&Off Speed with CE pin

Detailed Functional Description

AW37005YXXX is a low dropout voltage regulator. After powered on, with CE pin assertion, feedback voltage signal from the integrated resistor network and a voltage related to the voltage reference are transmit to positive input terminal and negative input terminal of an error amplifier (EA) respectively. The output signal of EA is used to control the open-state of power MOSFET. After soft-start, feedback voltage signal compares with the established reference voltage, making output voltage stable and accurate. AW37005YXXX integrates function of load transient accelerating, making LDO obtain excellent dynamic load transient response performance.

Enable Operation

AW37005YXXX uses CE pin to realize enable operation. Applying proper value of voltage to CE pin can make IC enable/disable.

If the voltage of CE pin is less than 0.36V, AW37005YXXX is guaranteed to be disabled. In this state, function modules of IC and power MOSFET are turned off. And the auto discharge function is enabled making output discharge through an on-state NMOSFET to Ground. In disable state, AW37005YXXX only consumes a typical 100nA current.

If the voltage of CE pin is more than 0.84V, AW37005YXXX is guaranteed to be enabled. In this state, the auto discharge function is disabled, and AW37005YXXX regulates output voltage to the designed value of voltage.

A 420nA pull down current to Ground is built-in at CE pin, making sure that the IC is disabled when CE pin floats. If Enable function is not required, CE pin should be connected directly to IN pin.

Output Current Limit

AW37005YXXX integrates output current limit function, protecting IC from excessive current.

When the load is excessively heavy, AW37005YXXX limits the current flowing through the IC to a typical 650mA current. This value is specially designed, so that IC is protected properly and the output capability of 500mA is not influenced either.

Meanwhile, AW37005YXXX integrates a 150mA fold-back current limit function, lowering the system dissipation when output overload or short to Ground.

Thermal Shutdown

AW37005YXXX integrates thermal shutdown function, protect IC from excessively high temperature.

When the chip temperature exceeds 160°C, AW37005YXXX detects it as an over-temperature event, triggering thermal shutdown, which will turn off the main function module, including power MOSFET. This inhibits increase of chip's temperature. IC would keep the protection-state on until the chip's temperature falls below to 135°C. At this moment, the over-temperature protection-state is released, IC resumes to work again. The hysteresis avoids IC's turning off and on frequently around the Thermal Shutdown threshold.

Auto Discharge

AW37005YXXX makes output voltage discharge quickly when in CE disable state or thermal shutdown state, benefit from integrating auto discharge function. Auto discharge function is implemented by integrated a NMOSFET of typical 200Ω Rdson route from Output to Ground, and the route is get through in CE disable state or thermal shutdown state. This feature prevents residual charge voltage on the output capacitor, which may impact proper power up of the system connected to the converter. It should be noted that auto discharge function is optional according to different specs.

Application Information

Power Dissipation and Device Operation

The permissible power dissipation is dependent on the ambient temperature T_A and the junction-to-ambient thermal resistance $R_{\theta JA}$.

The absolute maximum allowable power dissipation for the device in a given package can be calculated using Equation below, where T_{J_MAX} = 150°C :

$$PD_{MAX\_ABS} = (T_{J\_MAX} - T_A) / R_{\theta JA}$$

The recommended maximum allowable power dissipation for the device in a given package can be calculated using Equation below, where T_{J_REC} = 125°C :

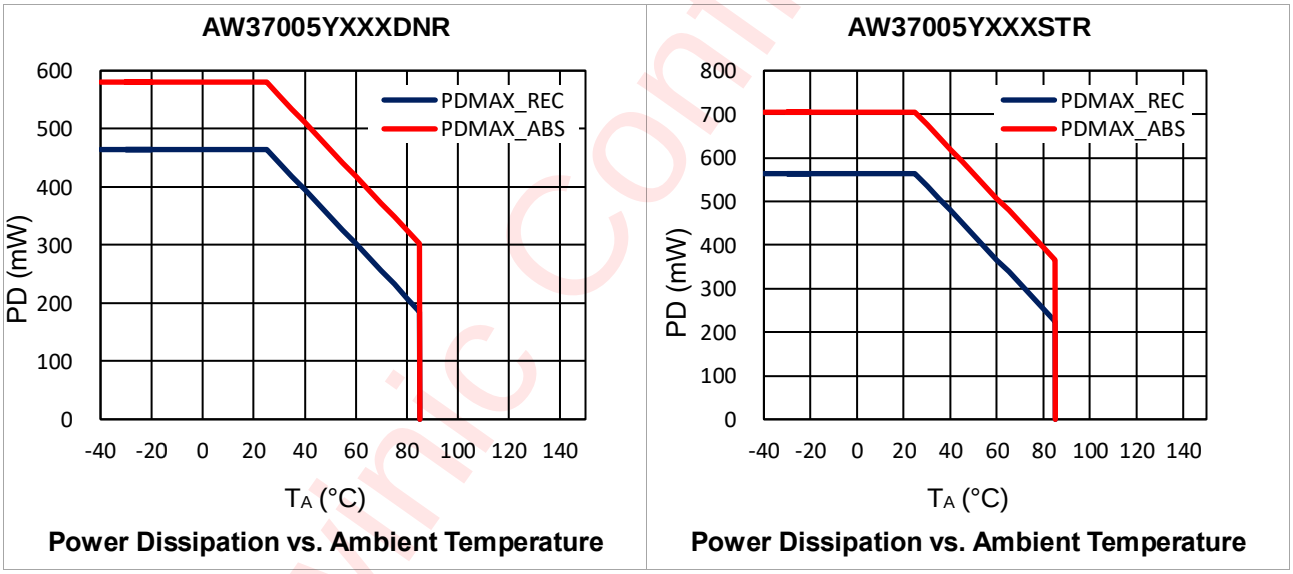
$$PD_{MAX\_REC} = (T_{J\_REC} - T_A) / R_{\theta JA}$$

The actual power being dissipated in the device can be represented by Equation below:

$$PD_{ACT} = (V_{IN} - V_{OUT}) \times I_{OUT}$$

These equations above establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device.

The graphs of Power Dissipation vs. Ambient Temperature are showed below :



Power Dissipation vs. Ambient Temperature **Power Dissipation vs. Ambient Temperature**

The above graphs show the maximum power dissipation of the respective package at T_{J_REC} = 125°C and T_{J_MAX} = 150°C. Operating the device in the region between PD_{MAX_REC} and PD_{MAX_ABS} might have a negative influence on its lifetime.

Capacitors Selection

IN pin: Input Capacitor C_{IN}

AW37005YXXX advises to use a 1μF or more X5R or X7R ceramic capacitor at IN pin as shown in Typical Application Circuit.

OUT pin: Output Capacitor C_{OUT}

AW37005YXXX advises to use a 1μF or more X5R or X7R ceramic capacitor at OUT pin as shown in Typical Application Circuit.

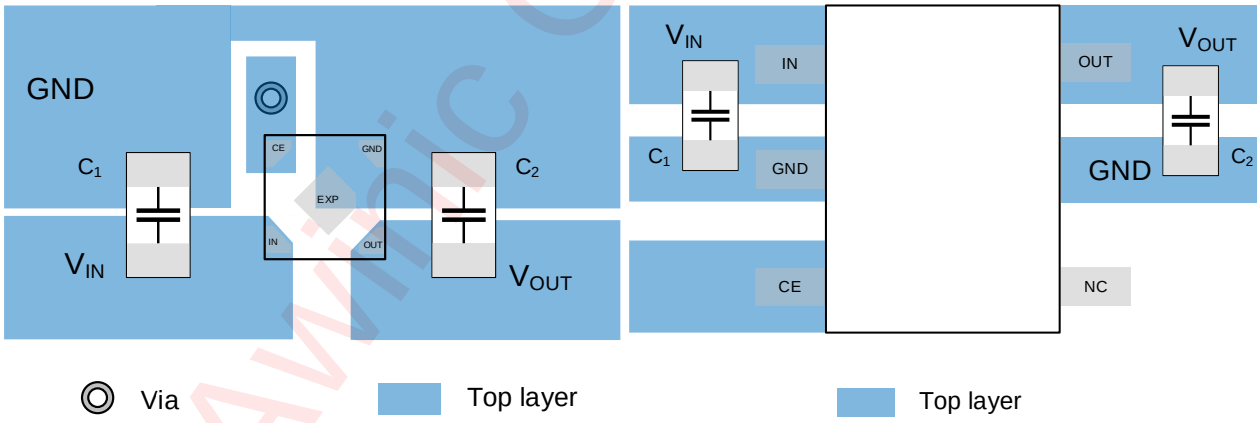
Recommended Components List

Component	PART No.	DESCRIPTION	MFR	TYP.	UNIT
C_{IN}	GRM155R61A105KE15	10V, X5R, 0402	MURATA	1	μF
C_{OUT}	GRM155R61A105KE15	10V, X5R, 0402	MURATA	1	μF

PCB Layout Consideration

The performance of a power source circuit using this device is highly dependent on a peripheral circuit. To obtain the optimal performance, a peripheral component or the device mounted on PCB should not exceed its rated voltage, rated current or rated power. When designing a peripheral circuit, guidelines below for PCB layout of AW37005YXXX should be obeyed:

1. All peripheral components should be placed as close to the chip as possible. C_{IN} and C_{OUT} should be close to IN and OUT pins respectively. Avoid connecting device and chip pins with two different layers of copper, use the same layer of copper instead.
2. IN and OUT pin are the large current input and output of the chip, make IN, OUT, and meanwhile GND lines sufficient.
3. The connection lines between the planes of C_{IN} or C_{OUT} and respective chip pin should be as short and wide as possible, to reduce noise and EMI interference, or it may cause noise pickup or unstable operation.
4. The exposed plane of chip and GND pins must be connected to the large-area ground layer of PCB directly, meanwhile place sufficient vias below the exposed plane. Thus we can decrease the thermal resistor on the board to optimize heat-diffusion performance.

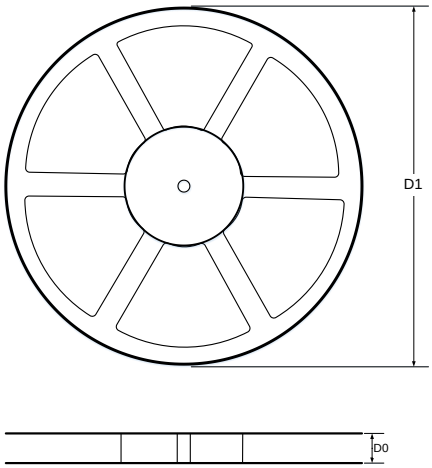


AW37005YXXX PCB LAYOUT

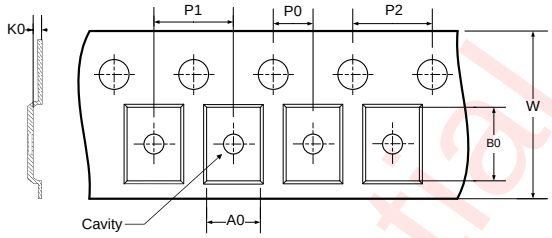
Tape And Reel Information

DFN 1X1-4L

REEL DIMENSIONS

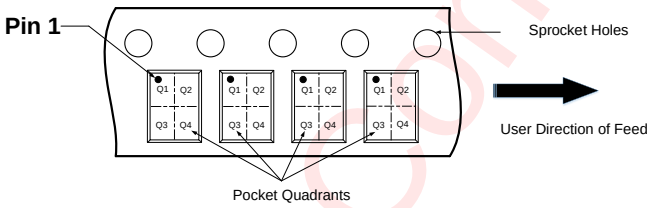


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

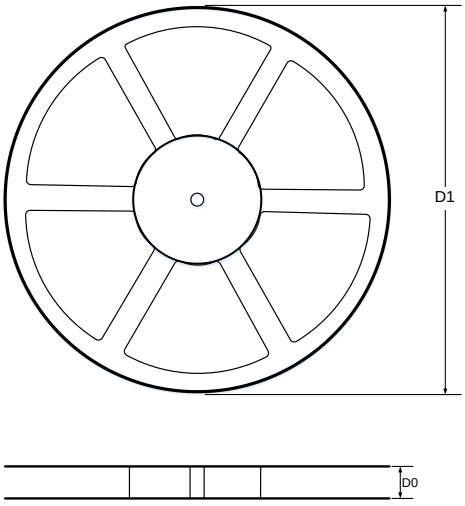
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178.00	8.40	1.16	1.16	0.50	2.00	2.00	4.00	8.00	Q1

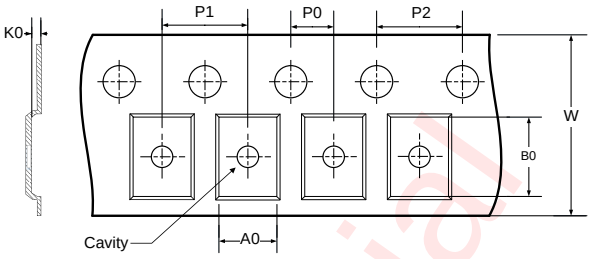
All dimensions are nominal

SOT 23-5L

REEL DIMENSIONS

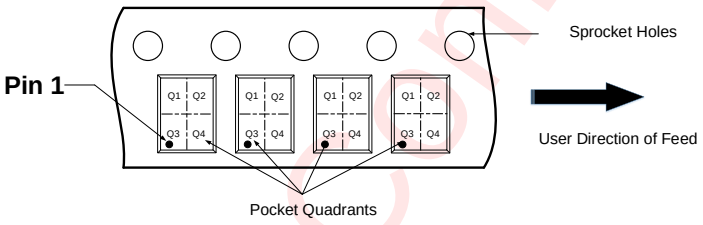


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

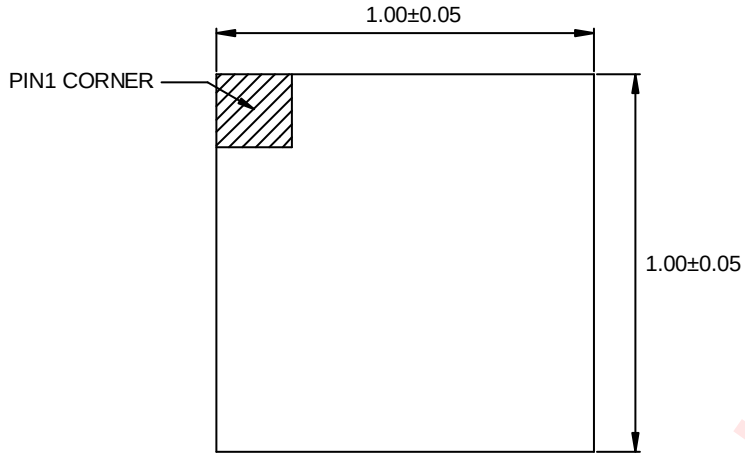
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178.00	8.40	3.30	3.20	1.40	2.00	4.00	4.00	8.00	Q3

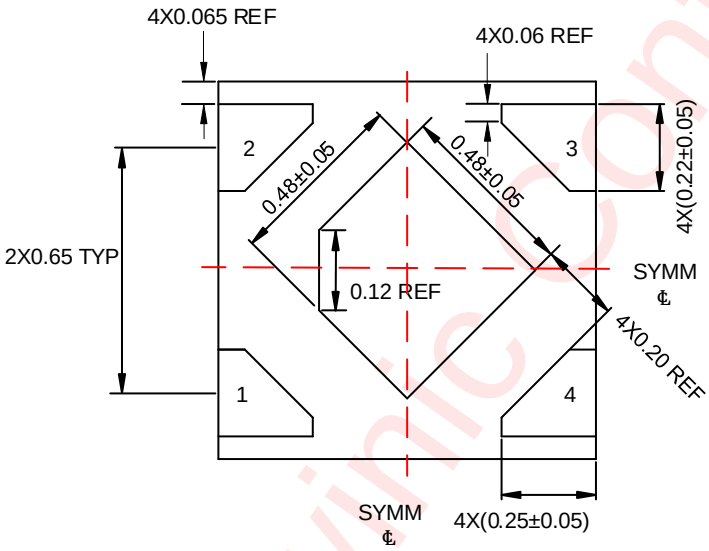
All dimensions are nominal

Package Description

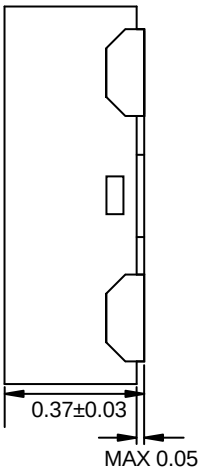
DFN 1X1-4L



Top View



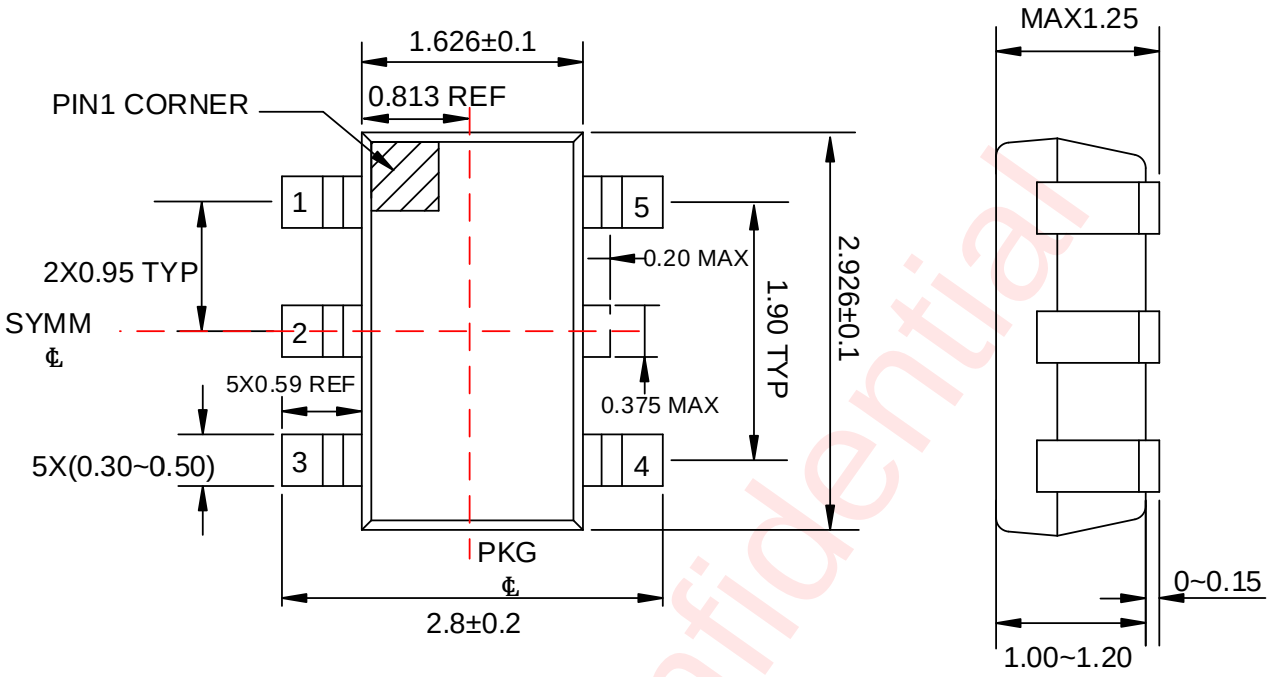
Bottom View



Side View

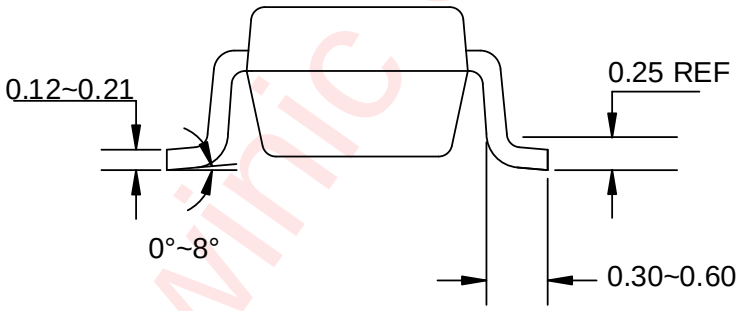
Unit:mm

SOT 23-5L



Top View

Side View

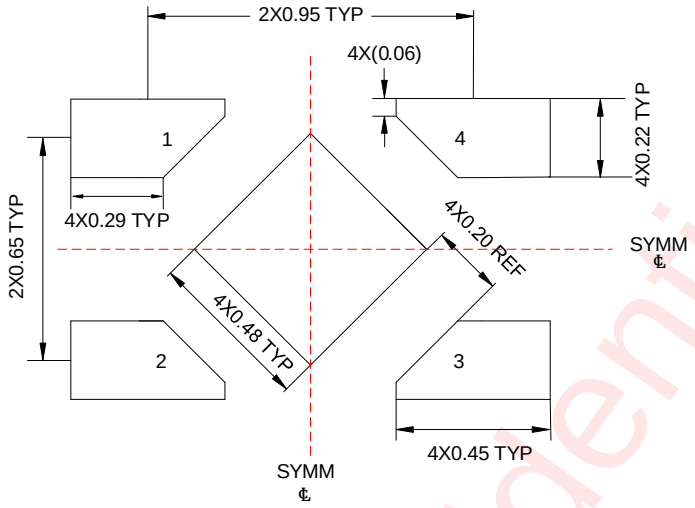


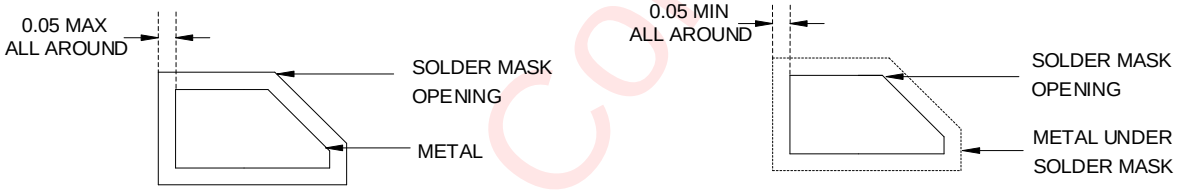
Side View

Unit: mm

Land Pattern Data

DFN 1X1-4L



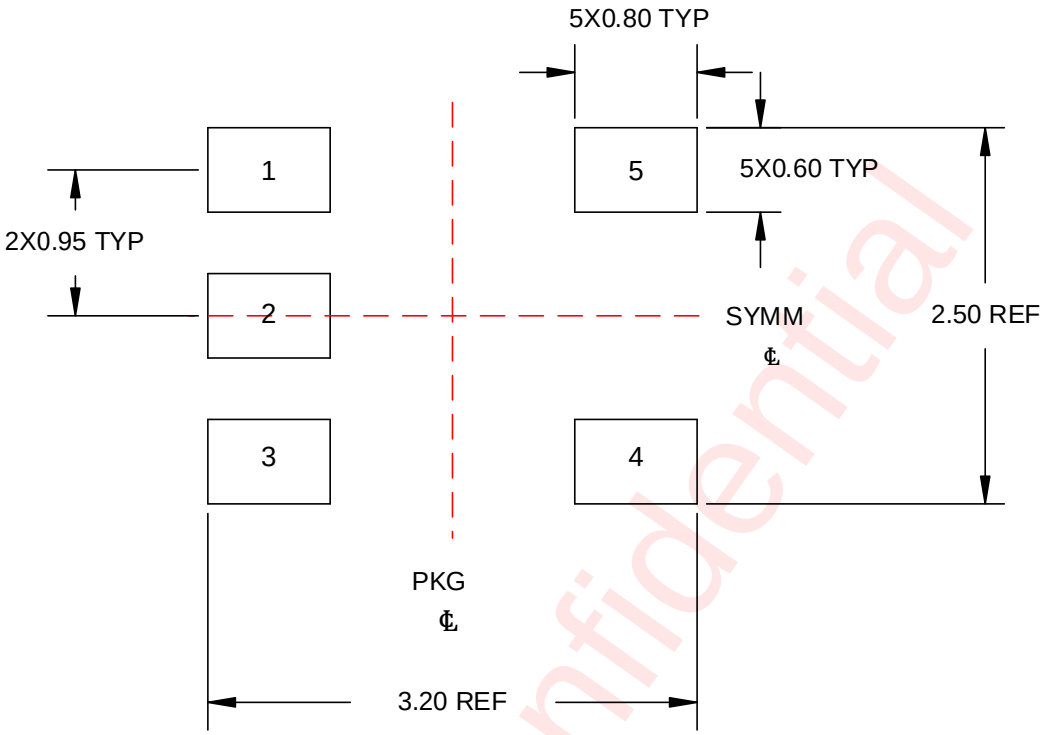


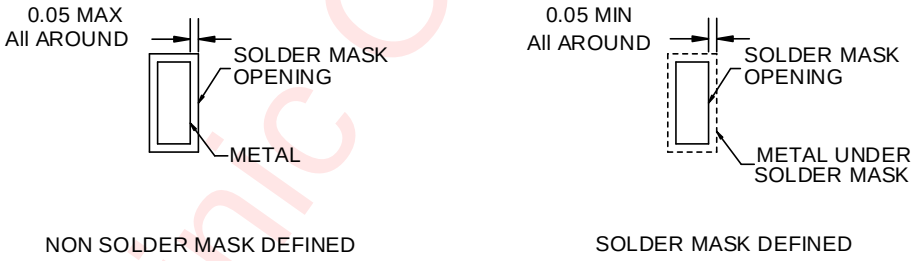
NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

UNIT : mm

SOT 23-5L



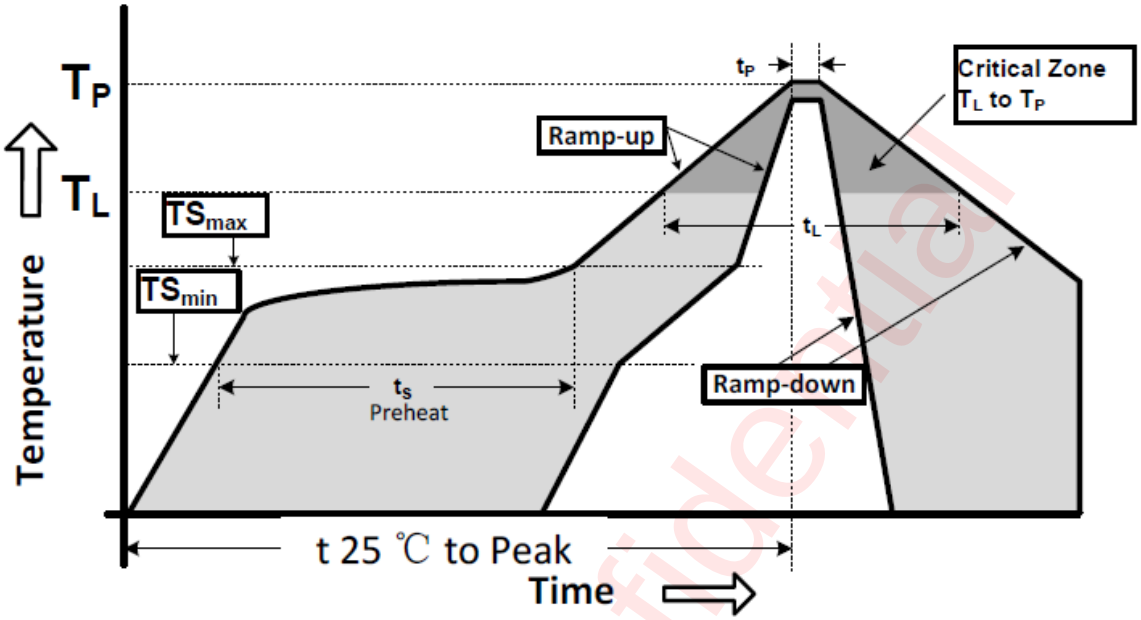


NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit: mm

Reflow



Reflow Note	Spec
Ramp-up rate（TSmax to T_P）	3°C/second max.
Preheat temperature（TSmin to TSmax）	150°C to 200°C
Preheat time（t_s）	60 - 180 seconds
Time above T_L , 217°C（t_L）	60 - 150 seconds
Peak temperature（T_P）	260°C
Time within 5°C of peak temperature(t_P)	20 - 40 seconds
Ramp-down rate	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

Revision History

Version	Date	Change Record
V1.0	Jul. 2023	Officially released
V1.1	Dec. 2025	Add V_{OUT} of 3.3V.

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