USB Type-C Port Protector: OVP And IEC ESD Protection IC

FEATURES

- Short-to-VBUS Over-Voltage protection
  - $32V_{DC}$ tolerance on CC1/2, SBU1/2
  - Fast 70ns OVP response Time
- IEC 61000-4-2 ESD protection
  - ±8kV contact discharge on CC1/2
  - ±15kV air gap discharge on CC1/2
  - ±6kV contact discharge on SBU1/2
  - ±15kV air gap discharge on SBU1/2
- IEC 61000-4-5 Surge protection
  - ±40V surge tolerance on CC1/2
  - ±25V surge tolerance on SBU1/2
- CC1/2 with 600mA current capability for V_{CONN}
- Dead battery support without power supplied
- QFN 3.0mm × 3.0mm x 0.75mm-20L package

APPLICATIONS

- Desktop PC
- Notebook PC
- Monitors or TVs with Type-C
- HUB or Docking station
- Port/Cable adapters and dongles
- Smartphones

GENERAL DESCRIPTION

The AW35622 is a single-chip USB Type-C port protection device that provides Short-to-V_{BUS} $32V_{DC}$ tolerance and IEC ESD protection.

The AW35622 protects the CC and SBU pins without interfering with normal operation by providing over-voltage protection on the CC and SBU pins. The device integrated high voltage FETs in series with the SBU and CC lines. These channels will shut off if a voltage above OVP threshold is detected, isolating the rest of the system from the risk of high voltage.

Besides, the AW35622 integrates IEC 61000-4-2 ESD protection for the external pins in Type-C connector as CC1, CC2, SBU1, SBU2, D+ and D-, eliminating the necessity of the external TVS on the connector.

Typical Application Circuit

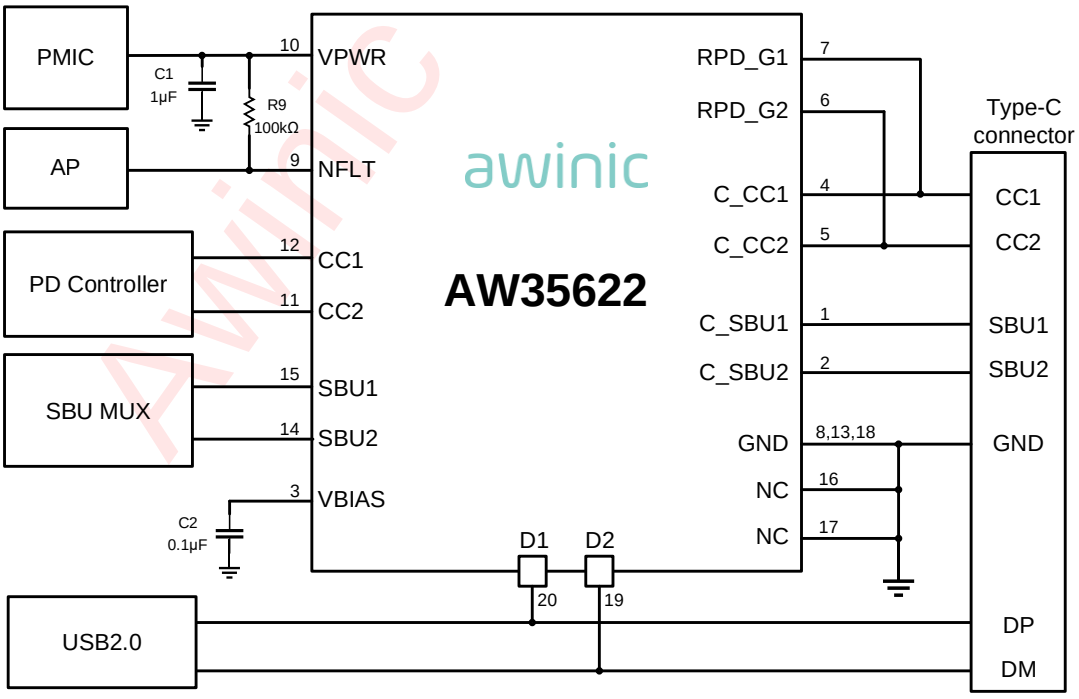


Figure 1 AW35622 typical application circuit

Pin Configuration And Top Mark

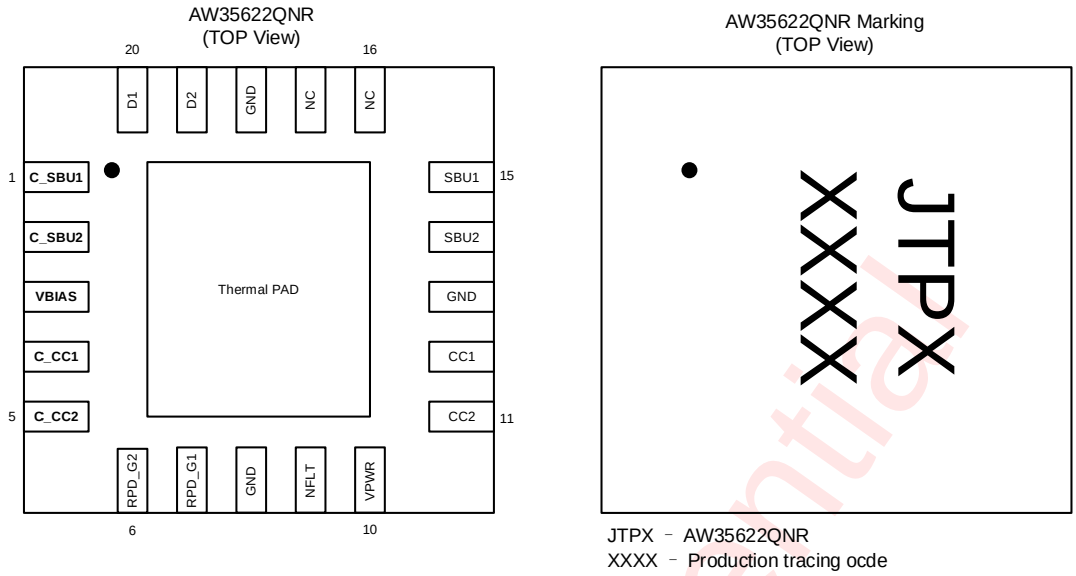


Figure 2 Pin Configuration

Pin Definition

NO.	NAME	DESCRIPTION
1	C_SBU1	Connector side of the SBU1 OVP FET. Connect to either SBU pin of the USB Type-C connector. Alternatively, connect to either USB2.0 pin of the USB Type-C connector to protect the USB2.0 pins instead of the SBU pins
2	C_SBU2	Connector side of the SBU2 OVP FET. Connect to either SBU pin of the USB Type-Connector. Alternatively, connect to either USB2.0 pin of the USB Type-C connector to protect the USB2.0 pins instead of the SBU pins
3	VBIAS	Pin for ESD support capacitor. Place a 0.1-μF capacitor on this pin to ground
4	C_CC1	Connector side of the CC1 OVP FET. Connect to either CC pin of the USB Type-C connector
5	C_CC2	Connector side of the CC2 OVP FET. Connect to either CC2 pin of the USB Type-C connector
6	RPD_G2	Short to C_CC2 if dead battery resistors are needed. If dead battery resistors are not needed, short pin to GND.
7	RPD_G1	Short to C_CC1 if dead battery resistors are needed. If dead battery resistors are not needed, short pin to GND.
8	GND	Ground
9	NFLT	Open drain for fault reporting
10	VPWR	2.7V to 5.5V power supply.
11	CC2	System side of the CC2 OVP FET.
12	CC1	System side of the CC1 OVP FET.
13	GND	Ground
14	SBU2	System side of the SBU2 OVP FET.
15	SBU1	System side of the SBU1 OVP FET.
16	NC	Unused pin. Connect to Ground
17	NC	Unused pin. Connect to Ground
18	GND	Ground
19	D2	Connect to any of the USB2.0 pins of the USB Type-C connector
20	D1	Connect to any of the USB2.0 pins of the USB Type-C connector

Functional Block Diagram

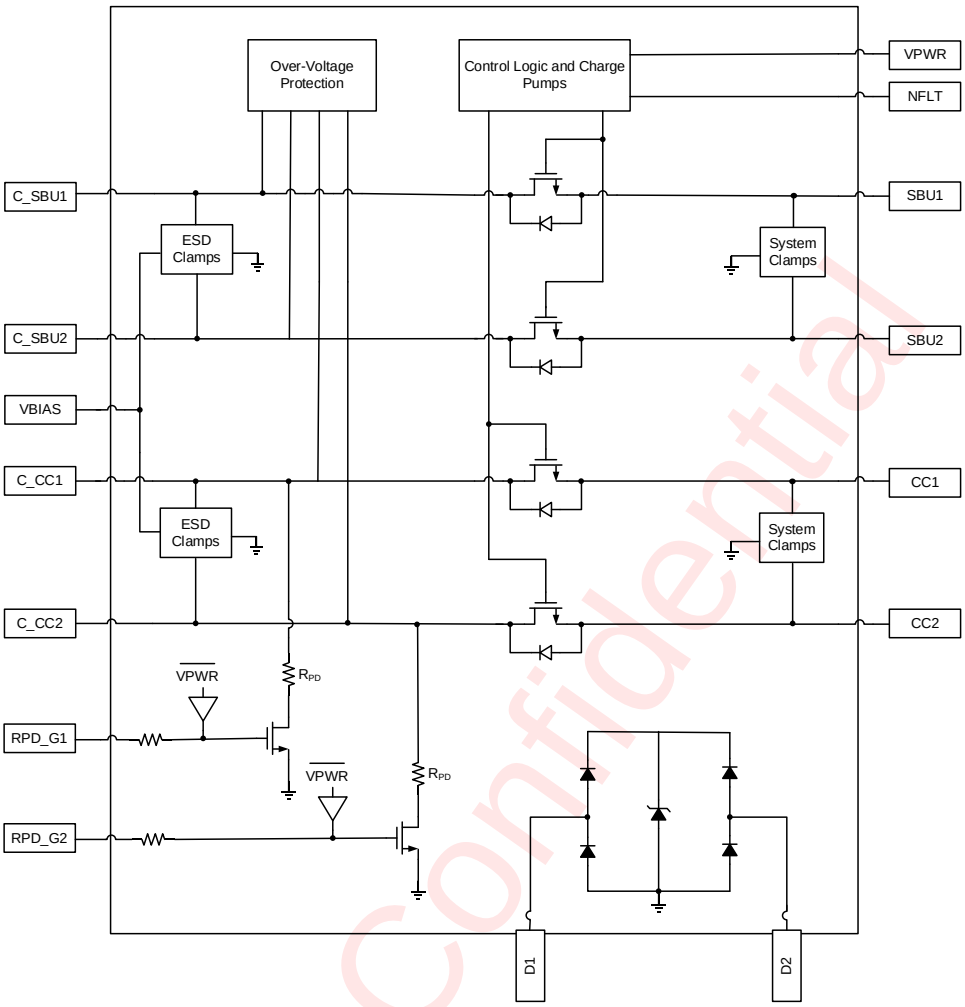


Figure 3 Functional Block Diagram

Typical Application Circuit

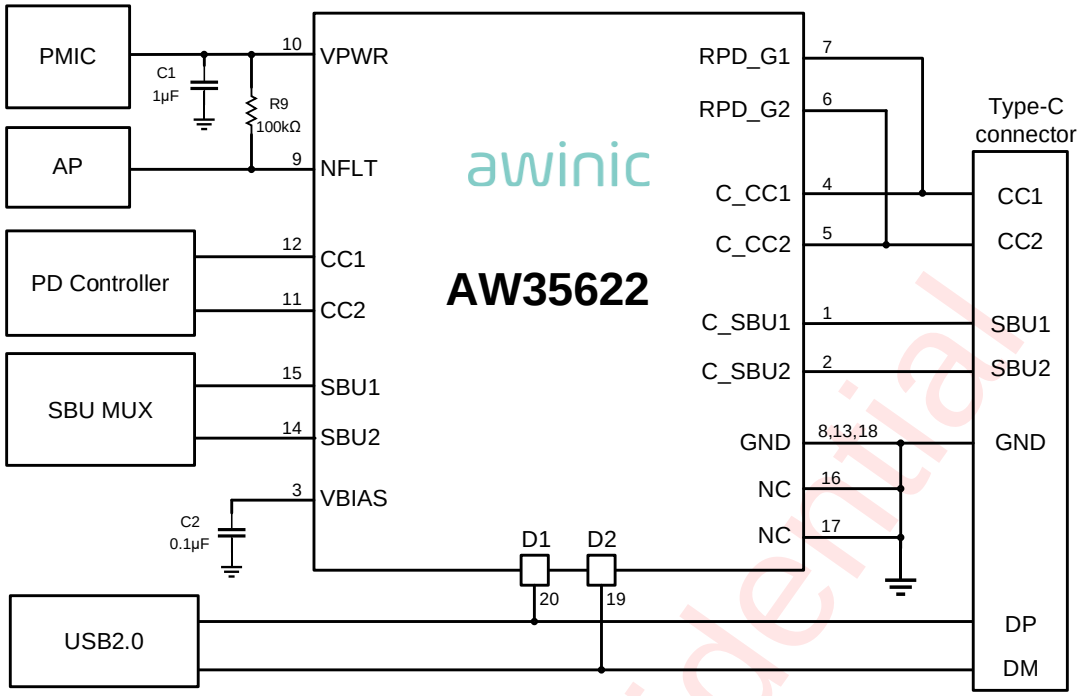


Figure 4 AW35622 typical application circuit

Notice for typical application circuits.

1. If RPD_Gx pins or Dx pins are unused in design, they must be connected to GND, and so are NC pins.
2. NFLT is an open drain output pin, so a 100kΩ pullup resistor is needed connected to VPWR. If not used, it can be left floating.
3. A 1μF ceramic bypass capacitors are necessary between VPWR and ground, placed close to the device, but far away from signal trace.
4. VBIAS capacitor is used for ESD protection support. A 0.1μF/50V X5R or X7R capacitor is recommended for this application. Note that this capacitor should be placed as close as possible to the VBIAS pin.
5. CC1, CC2 channels can support up to 600mA current, so the traces on PCB layout should be wide enough for that.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environment Information	Delivery Form
AW35622QNR	-40°C~85°C	QFN 3.0mm×3.0mm-20L	JTPX	MSL1	ROHS+HF	6000 units/Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage range V_{PWR}		-0.3V to 6V
Input voltage range	V_{C_CC}, V_{C_SBU}, V_{RPD},	-0.3V to 32V
	V_{D1}, V_{D2}	-0.3V to 6V
output voltage range	V_{CC}, V_{SBU}, V_{NFLT}	-0.3V to 6V
	VBIAS	-0.3V to 32V
Input current range	I_{C_CC}	-0.6 to 0.6A
	I_{C_SBU}	-100 to 100mA
Junction-to ambient thermal resistance θ_{JA}		65.9
Maximum operating junction temperature T_{JMAX}		150°C
Storage temperature T_{STG}		-65 to 150°C
Soldering temperature (soldering 10 seconds)		260°C
ESD(Including CDM HBM MM)		
Human body model(All pins,per ESDA/JEDEC JS-001) (NOTE2)		±2000V
Charged device model(All pins,per ESDA/JEDEC JS -002) (NOTE3)		±500V
ESD IEC61000-4-2		
Contact discharge	C_CC1, C_CC2, D1, D2	±8000V
	C_SBU1, C_SBU2	±6000V
Air-gap discharge	C_CC1, C_CC2, D1, D2	±15000V
	C_SBU1, C_SBU2	±15000V
Latch-up		
Test condition:JESD78E		±200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017

NOTE3: Test method: ESDA/JEDEC JS -002-2018

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{PWR}	Input DC voltage	2.7	3.3	4.5	V
V_{RPD}	RPD_G1, RPD_G2	0		5.5	V
V_{NFLT}	NFLT output voltage	2.7		5.5	V
V_{C_CC}, V_{CC}	C_CC1, C_CC2, CC1, CC2 voltage	0		5.5	V
V_{C_SBU}, V_{SBU}	C_SBU1, C_SBU2, SBU1, SBU2 voltage	0		4.3	V
V_{D1}, V_{D2}	D1, D2 voltage	-0.3		5.5	V
I_{VCONN}	Current flowing into CC1/2 and out of C_CC1/2			0.6	A
T_A	Operating free-air temperature range	-40		85	°C

Electrical Characteristics

VPWR=3.3V, T_A=25°C for typical values (unless otherwise noted).

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Power supply and leakage current						
V_{UVLO}	VPWR under voltage lockout	Place 1 V on VPWR and raise voltage until SBU or CC FETs turn on.	2.1	2.3	2.5	V
V_{UVLO_HYS}	VPWR UVLO hysteresis	Place 3 V on VPWR and lower voltage until SBU or CC FETs turnoff; measure difference between rising and falling UVLO to calculate hysteresis.	100	150	200	mV
I_{VPWR}	VPWR supply current	VPWR = 3.3 V (typical), VPWR = 4.5 V (maximum). –40°C ≤ TJ ≤ +85°C.		80		μA
I_{CC_LEAK}	Leakage current for CC pins when device is powered	VPWR = 3.3 V, VC_CCx = 3.6 V, CCx pins are floating, measure leakage into C_CCx pins. Result must be same if CCx side is biased and C_CCx is left floating.		1	3	μA
I_{SBU_LEAK}	Leakage current for CC pins when device is powered	VPWR = 3.3 V, VC_SBUx = 3.6 V, SBUx pins are floating, measure leakage into C_SBUx pins. Result must be same if SBUx side is biased and C_SBUx is left floating.		1	3	μA
$I_{C\_CC\_LEAK\_OVP}$	Leakage current for CC pins when device is in OVP	VPWR = 0 V or 3.3 V, VC_CCx = 28 V, CCx pins are set to 0 V, measure leakage into C_CCx pins		5.4		mA
$I_{C\_SBU\_LEAK\_OVP}$	Leakage current for SBU pins when device is in OVP	VPWR = 0 V or 3.3 V, VC_SBUx = 28 V, SBUx pins are set to 0 V, measure leakage into C_SBUx pins		400		μA
$I_{CC\_LEAK\_OVP}$	Leakage current for CC pins when device is in OVP	VPWR = 0 V or 3.3 V, VC_CCx = 28 V, CCx pins are set to 0 V, measure leakage out of CCx pins		0.1		μA
$I_{SBU\_LEAK\_OVP}$	Leakage current for SBU pins when device is in OVP	VPWR = 0 V or 3.3 V, VC_SBUx = 28 V, SBUx pins are set to 0 V, measure leakage out of SBUx pins		0.1		μA
I_{Dx_LEAK}	Leakage current for Dx pins	V_Dx = 3.6 V, measure leakage into Dx pins			1	μA
CC switches						
R_{ON}	On resistance of CC OVP FETs	V_{CCx}=5.5V		280	420	mΩ
R_{ON_FLAT}	On resistance flatness	Sweep CCx voltage between 0 V and 1.2 V			5	mΩ
C_{ON_CC}	Equivalent on capacitance on CCx	Capacitance from C_CCx or CCx to GND when device is powered. VC_CCx/VCCx = 0 V to 1.2 V, f = 400 kHz		45		pF

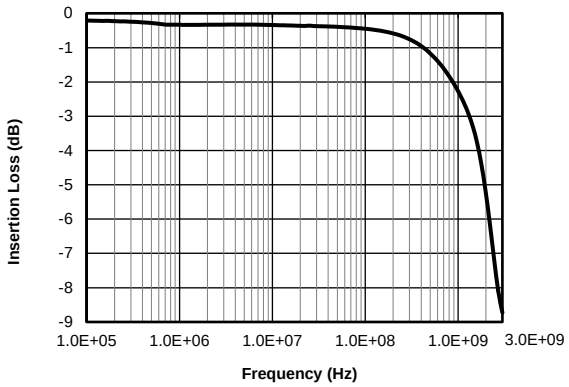
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
RD	Dead battery pull-down resistance (only present when device is unpowered). Effective resistance of RD and FET in series	V_C_CCx = 2.6 V	4.1	5.1	6.1	kΩ
VTH_DB	Threshold voltage of the pulldown FET in series with RD during dead battery	I_CC = 80 μA	0.5	0.75	1.1	V
V_{OVPCC}	OVP threshold on CC pins	VC_CCx rising from 5.5V until NFLT pin is asserted	5.75	6	6.2	V
V_{OVPCC_HYS}	Hysteresis on CC OVP	VC_CCx falling from 6.5V until NFLT pin is deasserted		100		mV
BW_{ON}	On bandwidth single ended (-3dB)	Measure the -3dB bandwidth from C_CCx to CCx. Single ended measurement, 50-Ω system.		160		MHz
V_{STBUS_CC}	Short-to-VBUS tolerance on the CC pins	Hot-Plug C_CCx with a 1-meter USB Type C Cable. Place a 30-Ω load on CCx			28	V
$V_{STBUS\_CC\_CLAMP}$	Short-to-VBUS system-side clamping voltage on the CC pins (CCx)	Hot-Plug C_CCx with a 1-meter USB Type C Cable. Hot-Plug voltage C_CCx = 28 V. Place a 30-Ω load on CCx		8		V
SBU Switches						
R_{ON}	On resistance of SBU OVP FETs	V_{SBUx}=3.6V		4	6.5	Ω
R_{ON_FLAT}	On resistance flatness	Sweep SBUx voltage between 0 V and 3.6 V		0.3		Ω
C_{ON_SBU}	Equivalent on capacitance on SBUx	Capacitance from C_SBUx or SBUx to GND when device is powered. VC_SBUx/VSBUx = 0.3V to 3.6 V		5		pF
V_{OVPSBU}	OVP threshold on SBU pins	VC_SBUx rising from 3.6V until NFLT pin is asserted	4.35	4.5	4.7	V
V_{OVPSBU_HYS}	Hysteresis on SBU OVP	VC_SBUx falling from 5V until NFLT pin is deasserted		100		mV
BW_{ON}	On bandwidth single ended (-3dB)	Measure the -3dB bandwidth from C_SBUx to SBUx. Single ended measurement, 50-Ω system		1.1		GHz
X_{TALK}	Crosstalk	Measure crosstalk at f = 1 MHz from SBU1 to C_SBU2 or SBU2 to C_SBU1. Be sure to terminate open sides to 50Ω		-70		dB
V_{STBUS_SBU}	Short-to-VBUS tolerance on the SBU pins	Hot-Plug C_SBUx with a 1-meter USB Type C Cable. Place a 40-Ω load on SBUx			28	V
$V_{STBUS\_SBU\_CLAMP}$	Short-to-VBUS system-side clamping voltage on the SBU pins (SBUx)	Hot-Plug C_SBUx with a 1-meter USB Type C Cable. Hot-Plug voltage C_SBUx = 28 V. Place a 150-nF capacitor in series with a 40-Ω load on SBUx		8		V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
NFLT pin						
V_{OL}	Low-level output voltage	I_{OL} = 3 mA. Measure the voltage at the NFLT pin			0.4	V
Thermal shutdown						
T_{SD_RISING}	The rising over-temperature protection shutdown threshold			150		°C
$T_{SD\_FALLING}$	The falling over-temperature shutdown threshold			130		°C
T_{SDN_HYST}	The over-temperature protection hysteresis			20		°C
Dx ESD Protection						
V_{RWM_POS}	Reverse stand-off voltage from Dx to GND	Dx to GND. IDX ≤ 1 μA			5.5	V
V_{RWM_NEG}	Reverse stand-off voltage from GND to Dx	GND to Dx			0	V
V_{BR_POS}	Break-down voltage from Dx to GND	Dx to GND. IBR = 1 mA	7			V
V_{BR_NEG}	Break-down voltage from GND to Dx	GND to Dx. IBR = 8 mA	0.6			V
C_{IO}	Dx to GND or GND to Dx			3		pF
ΔC_{IO}	Differential capacitance between two Dx pins			0.02		pF
R_{DYN}	Dynamic on-resistance Dx IEC clamps	Dx to GND or GND to Dx		0.3		Ω
Timings requirements						
t_{ON_FET}	Time from crossing rising VPWR UVLO until CC and SBU OVP FETs are on			1.3		ms
$t_{ON\_FET\_DB}$	Time from crossing rising VPWR UVLO until CC and SBU OVP FETs are on and the dead battery resistors are turned off			5		ms
$t_{OVP\_RESPONSE\_CC}$	OVP response time on the CC pins. Time from OVP asserted until OVP FETs turnoff			70		ns
$t_{OVP\_RESPONSE\_SBU}$	OVP response time on the SBU pins. Time from OVP asserted until OVP FETs turnoff			70		ns
$t_{OVP\_RECOVERY\_CC\_1\_FET}$	OVP recovery time on the CC pins. Once an OVP has occurred, the minimum time duration until the CC FETs turn back on. OVP must be removed for CC FETs to turn back on			0.9		ms
$t_{OVP\_RECOVERY\_CC\_1\_DB}$	OVP recovery time on the CC pins. Once an OVP has occurred, the minimum time duration until the CC FETs turn back on and the dead battery resistors turn off. OVP must be removed for CC FETs to turn back on			4.5		ms

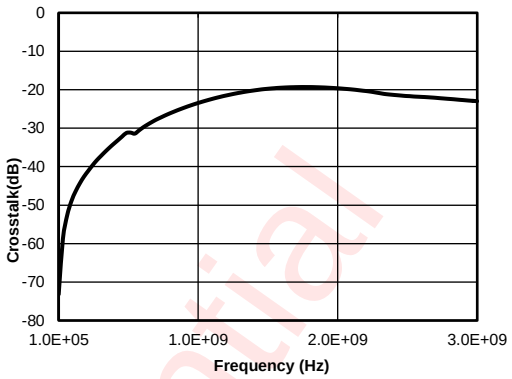
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{OVP\_RECOVERY\_SBU\_1}$	OVP recovery time on the SBU pins. Once an OVP has occurred, the minimum time duration until the SBU FETs turn back on. OVP must be removed for SBU FETs to turn back on			0.51		ms
$t_{OVP\_RECOVERY\_CC\_2\_FET}$	OVP recovery time on the CC pins. Time from OVP removal until CC FETs turn back on, if device has been in OVP > 0.6 ms			0.6		ms
$t_{OVP\_RECOVERY\_CC\_2\_DB}$	OVP recovery time on the CC pins. Time from OVP removal until CC FETs turn back on and dead battery			4.3		ms
$t_{OVP\_RECOVERY\_SBU\_2}$	OVP recovery time on the SBU pins. Time from OVP removal until SBU FETs turn back on, if device has been in OVP > 0.6 ms			0.3		ms
$t_{OVP\_NFLT\_ASSERTION}$	Time from OVP asserted to FLT assertion			20		μs
$t_{OVP\_NFLT\_DEASSERTION}$	Time from CC FET turn on after an OVP to FLT deassertion			4.1		ms

Typical Characteristics

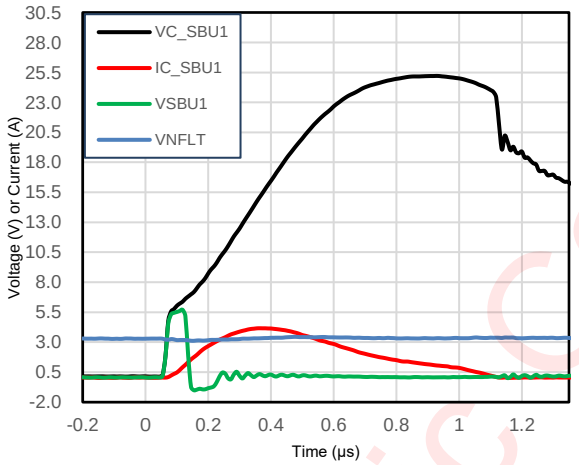
VPWR=3.3V, T_A=25°C for typical values (unless otherwise noted).



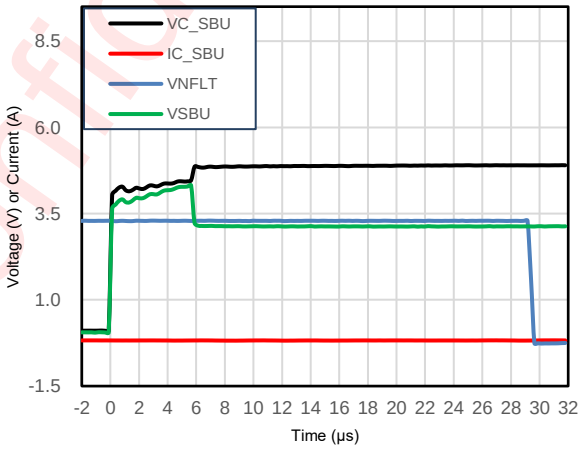
SBU S21 BW



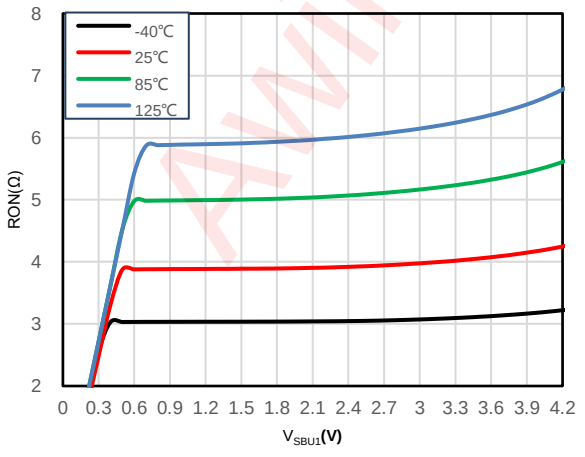
SBU Crosstalk



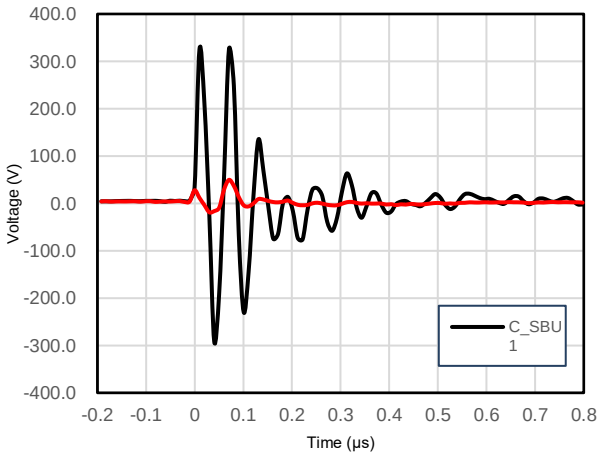
SBU Short-to-V_{BUS} 20V



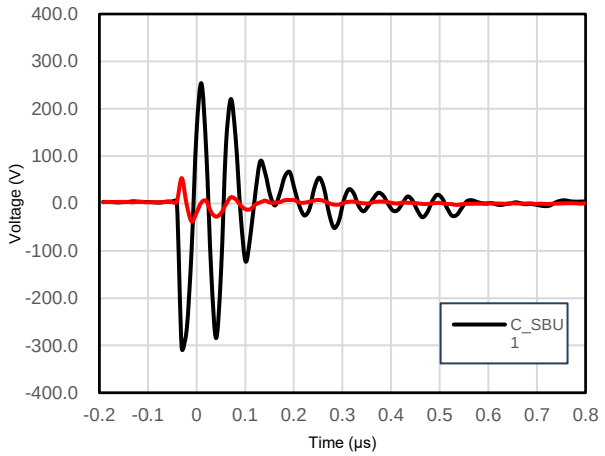
SBU Short-to-V_{BUS} 5V



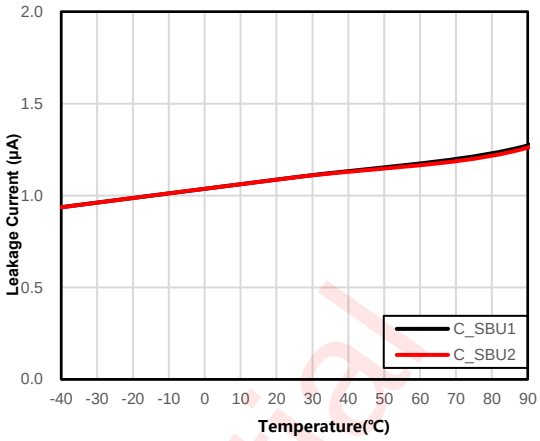
SBU R_{ON} Flatness



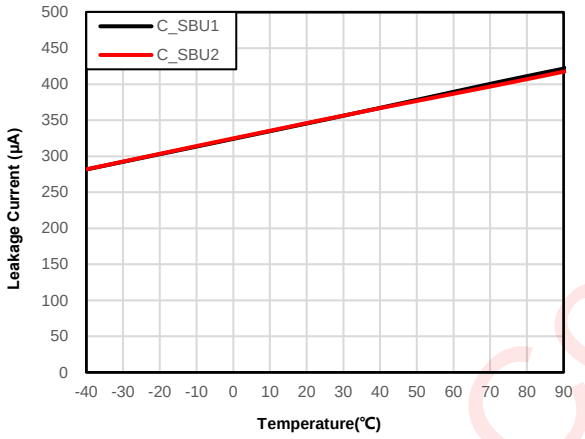
SBU IEC 61000-4-2 4-kV Response Waveform



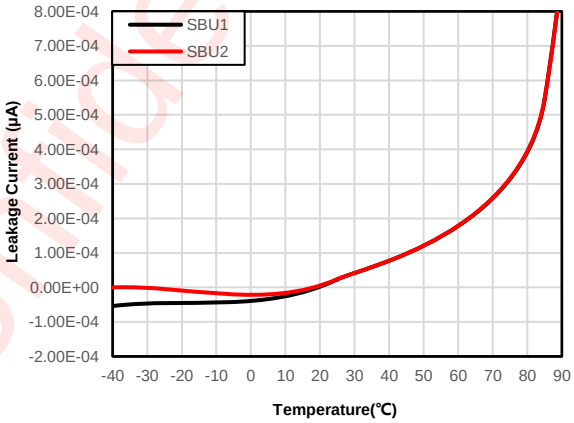
SBU IEC 61000-4-2 -4-kV Response Waveform



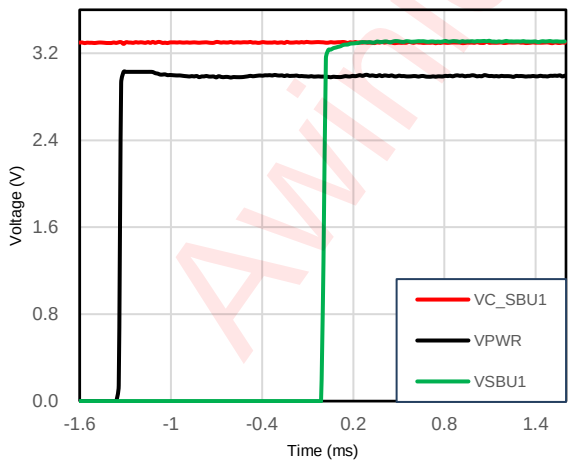
SBU Path Leakage Current vs Ambient Temperature at 3.6V



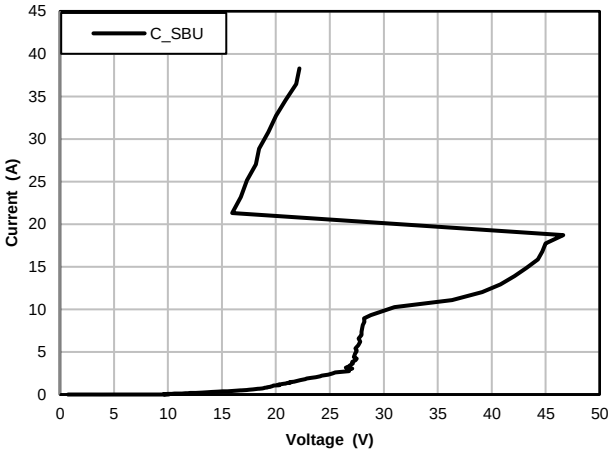
C_SBU OVP Leakage Current vs Ambient Temperature at 28V



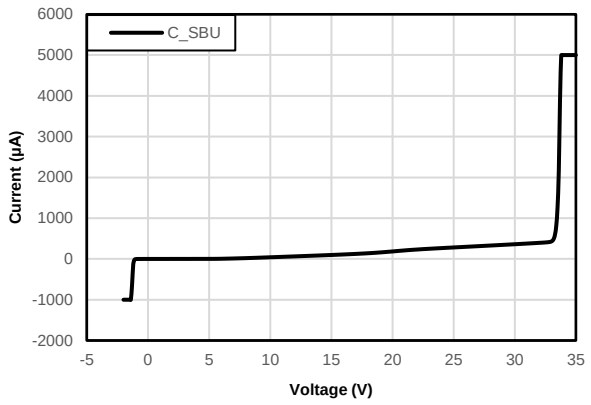
SBU OVP Leakage Current vs Ambient Temperature at 28V



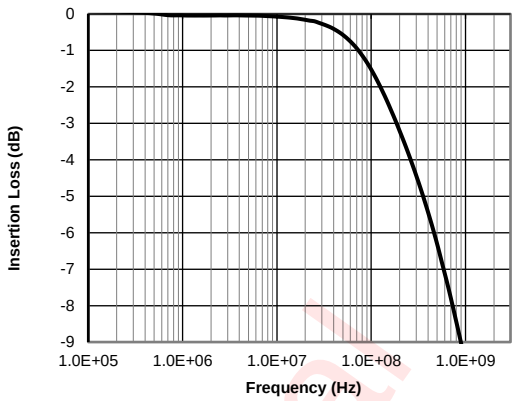
SBU FET Turnon Timing



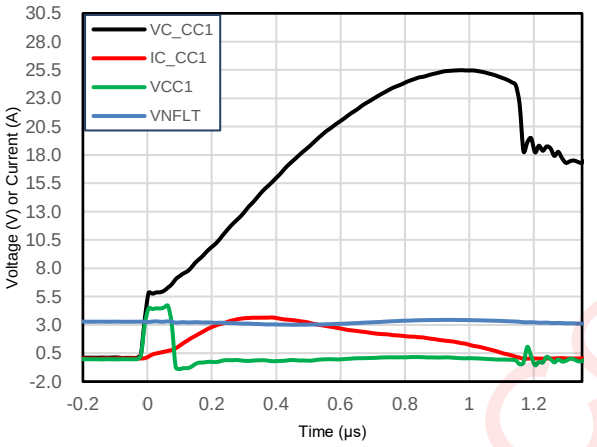
C_SBU TLP Curve Unpowered



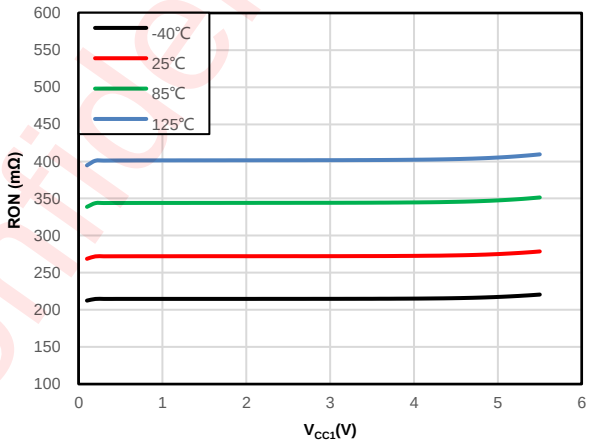
SBU IV Curve



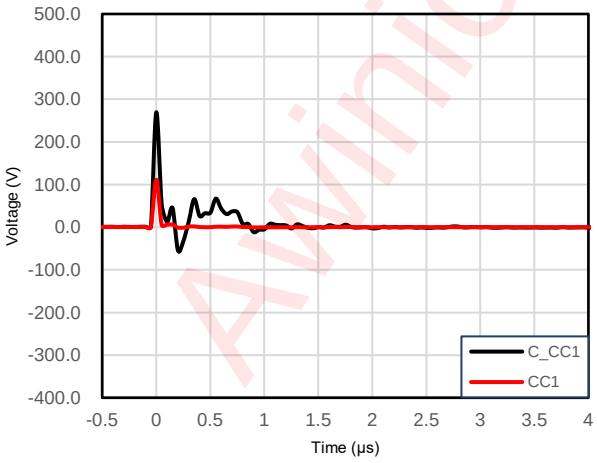
CC S21 BW



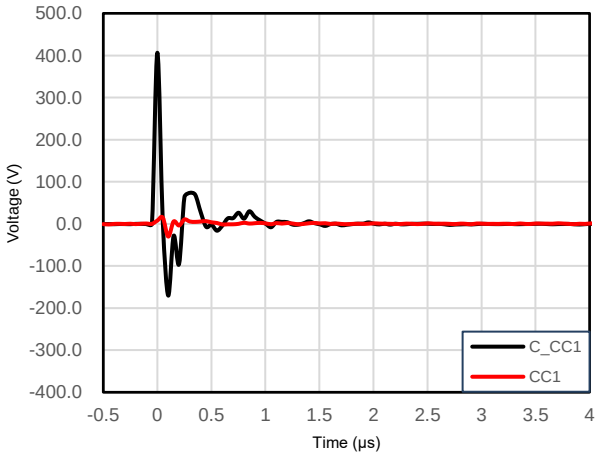
CC Short-to-V_{BUS} 20V



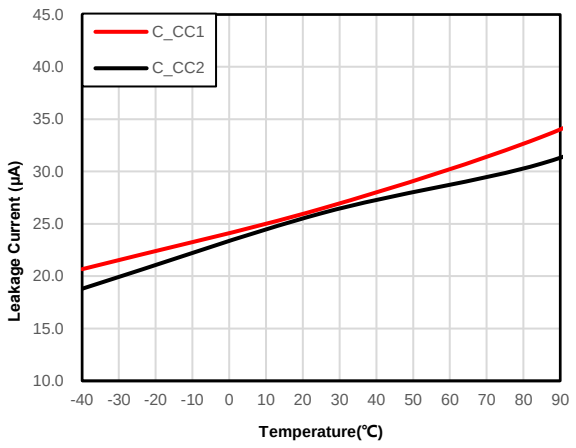
CC R_{ON} Flatness



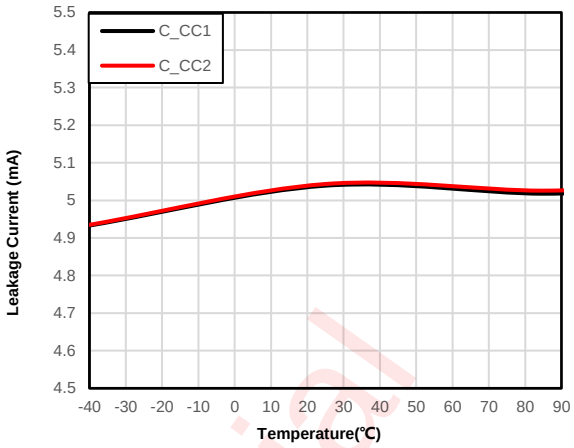
CC IEC 61000-4-2 8-kV Response Waveform



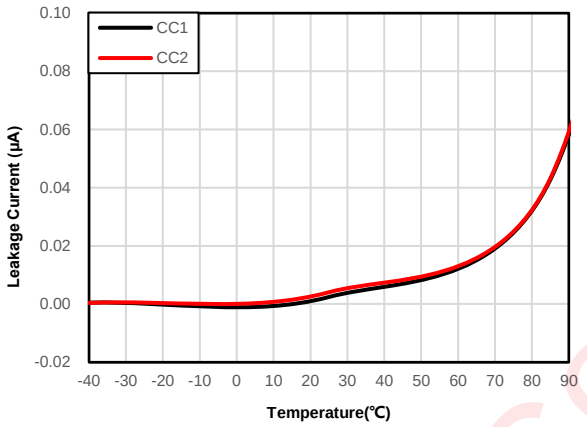
CC IEC 61000-4-2 -8-kV Response Waveform



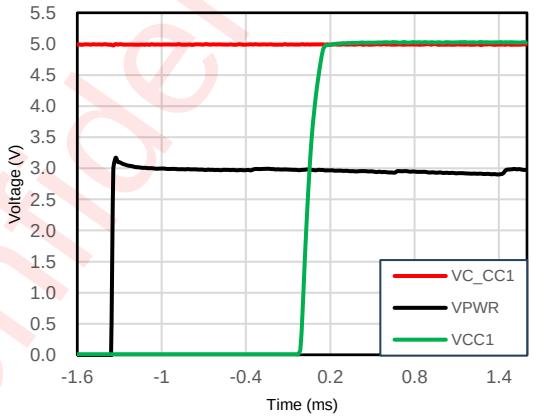
CC Path Leakage Current vs Ambient Temperature at 5.5V



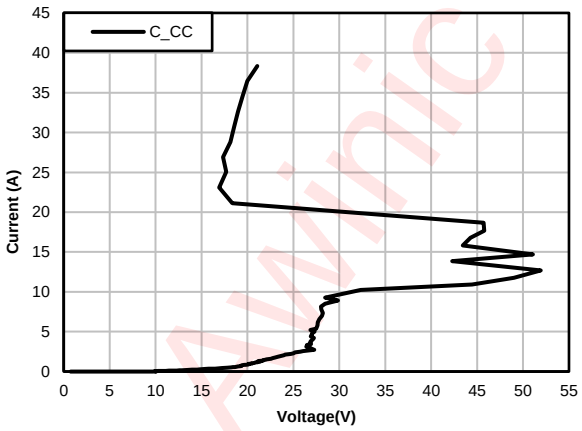
C_CC OVP Leakage Current vs Ambient Temperature at 28V



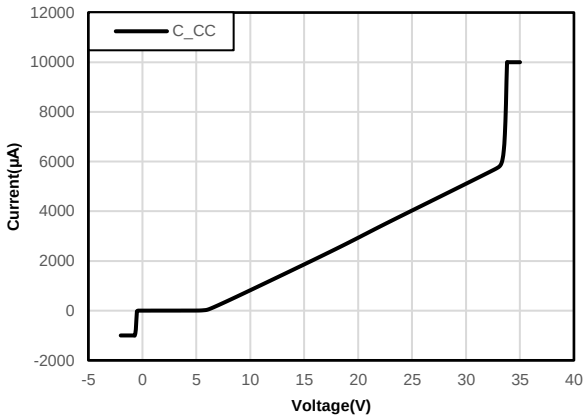
CC OVP Leakage Current vs Ambient Temperature at 28V



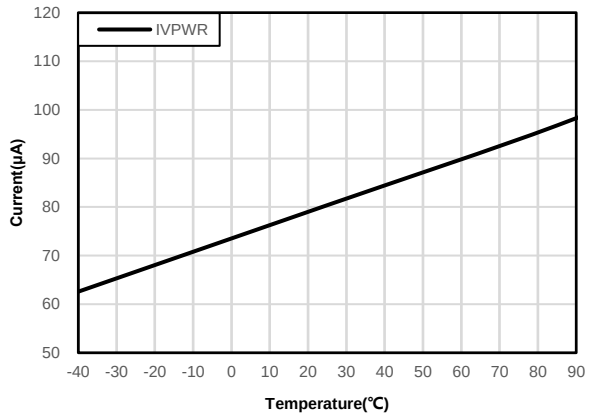
CC FET Turnon Timing



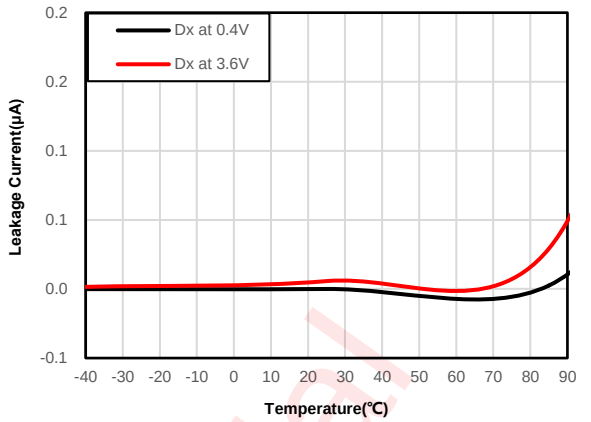
C_CC TLP Curve Unpowered



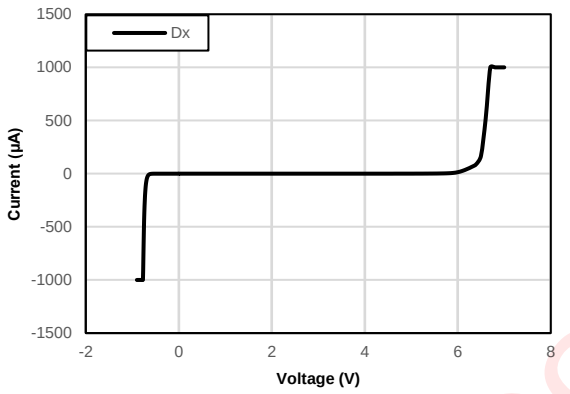
C_CC IV Curve



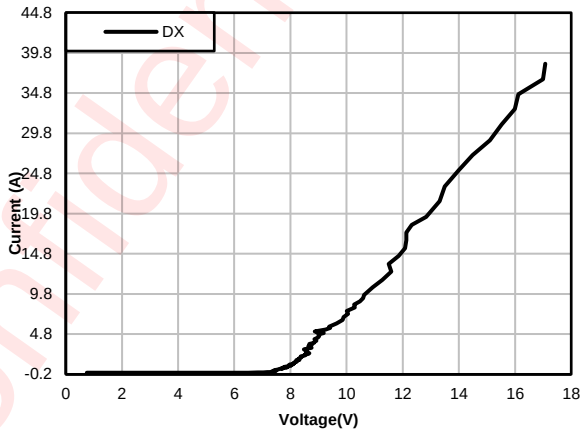
VPWR Supply Leakage vs Ambient Temperature at 3.3V



Dx Leakage Current vs Ambient Temperature at 0.4 V and 3.6 V



Dx IV Curve



Dx TLP Curve

Detailed Functional Description

The AW35622 is a single chip USB Type-C port protection solution. It integrates 4 channel switches with over-voltage protection function that protect low voltage pins CC1, CC2, SBU1 and SBU2. In order to support the protection in USB PD 3.0 specification, the C_CC1, C_CC2, C_SBU1 and C_SBU2 pins are $32V_{DC}$ tolerant, so they can be well protected in case of being shorted to VBUS pin by accident or moisture. Additionally, The AW35622 integrates 6 channels of IEC61000-4-2 ESD protection for the CC1, CC2, SBU1, SBU2, D+ and D- pins of the USB Type-C connector. The AW35622 combines ESD protection and short-to-VBUS protection to replace discrete protection devices for cost and space saving.

Over-Voltage Protection

The AW35622 integrates 4-Channels of Short-to-VBUS Over-Voltage protection with $32V_{DC}$ tolerance for CC1, CC2, SBU1 and SBU2. When over-voltage event is detected on any of C_CC1, C_CC2, C_SBU1 or C_SBU2, the device will shut off all the channels within 70ns (typical), as well as pull down the NFLT pin to indicate an over-voltage event to system. The typical OVP threshold voltage is 6V for C_CC1 and C_CC2 pins, and 4.5V for C_SBU1 and C_SBU2 pins.

Over-Temperature Protection

The AW35622 support over-temperature protection to avoid the abnormal overheating in the application, which will shut off all channels and pull down the NFLT pin to indicate the fault event.

IEC 61000-4-2 ESD Protection

The AW35622 integrates 6-Channels of IEC 61000-4-2 system level ESD protection for the CC1, CC2, SBU1, SBU2, D1 and D2 pins. So external TVS devices are never needed on these pins, which helps space saving and cost down.

During the ESD event, AW35622 will avoid the possibility of Type-C disconnection for a sink. When an OVP happened due to ESD strike, AW35622 will shut off the CC channels within 70ns and turn on its dead battery resistor, which makes the connected SRC port always see an Rd resistor to avoid the disconnection. After the ESD strike have passed, AW35622 will turn the CC channels back on within 1ms, much faster than a sinks minimum disconnect time, which is 10ms in USB Type-C specification.

It should be noted that the RPD_G1/2 pins are not individually rated for IEC_ESD protection, when they are shorted to the C_CC1/2 pins, the C_CC1/2 pins will provide protection for either the C_CC1/2 pins or the RPD_G1/2 pins.

CC Dead Battery Resistors

AW35622 integrates dead battery pull-down resistor RD on RPD_G1 and RPD_G2 pins to allow for USB Type-C power supply charging in dead battery condition.

If dead battery support is required, short the RPD_G1 pin to the C_CC1 pin, and short the RPD_G2 pin to the C_CC2 pin. In dead battery condition, the AW35622 is unpowered, the pull-up resistor from an adaptor will activate the pull-down resistor in AW35622 and power delivery will be established on VBUS from adaptor to the system.

Once the AW35622 is supplied on its VPWR pin, it will turn on CC channels in 1.3ms and removes its dead battery pull-down resistor R_{PD} in another 3.7ms after the CC channels are fully on. It ensures the USB Type-C power supply remains attached because a USB Type-C sink must have an R_{PD} present on the CC channel at all times to stay connection according to the USB Type-C specification.

During the over-voltage event, the AW35622 will turn on its dead battery resistors on CC channels as soon as they are shut off. But during over-temperature condition, the dead battery resistors will not be presented until OTP is over, and will be removed when CC channels are fully on again.

If dead battery function is not required, connects the RPD_G1 and RPD_G2 pins to ground.

CC Switch Power Delivery

The typical on-resistance of the integrated switches of CC1 and CC2 is 270Mω, the two switches are both able to deliver 600Ma current, which is compliant with the USB Type-C specification.

High Bandwidth SBU Switch

The SBU1 and SBU2 switches have typically 1.1GHz -3Db bandwidth, which can be used to transmit SBU signal or other high-speed signal, e.g. USB 2.0 D+/D- data.

NFLT Fault Report

NFLT pin is the fault reporting pin, which is recommended to be pulled up by 100Kω resistor to an I/O voltage. During normal operation, NFLT is pulled up to logic high by pull-up resistor. When over-voltage event happens, NFLT will output logic low.

Device Functional Logic Modes

Table 1 shows all of the AW35622 functional logic modes.

VPWR	Conditions	Outputs			
		CC1/2	SBU1/2	RD	NFLT
>UVLO	Normal	ON	ON	OFF	High-Z
	CC1/2 OVP	OFF	OFF	ON	Active Low
	SBU1/2 OVP	OFF	OFF	ON	Active Low
	OTP	OFF	OFF	ON	Active Low
< UVLO	UVLO	OFF	OFF	ON	High-Z

Application Information

VBIAS Capacitance Selection

AW35622 uses an ESD support capacitor for ESD protection. The VBIAS capacitor should be placed between the VBIAS pin and GND. A 50V rated capacitor is recommend for 20V VBUS application, as the greater than 2x ringing voltage may occur in the short-to-VBUS RLC circuit. Therefore, A 0.1Mf/50V X5R or X7R capacitor is recommended for this application.

VPWR Capacitance Selection

Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground. So low-ESR, 1Mf/10V ceramic bypass capacitors are necessary between VPWR and ground, placed close to the device, but far away signal trace.

CC Line Capacitance

USB PD specification limited the total amount of capacitance for proper USB PD BMC operation on the CC lines. The specification of CC Line capacitance is given blow:

Name	Description	Min	Nom	Max	Unit	Comment
cReceiver	CC receiver capacitance	200		600	Pf	The DFP or UFP system Shall have capacitance within this range when not transmitting on the line.

Therefore, the sum of the capacitance including AW35622 with any other external capacitor or parasitic capacitance on the CC lines must be kept between 200 Pf and 600 Pf when USB PD is being used.

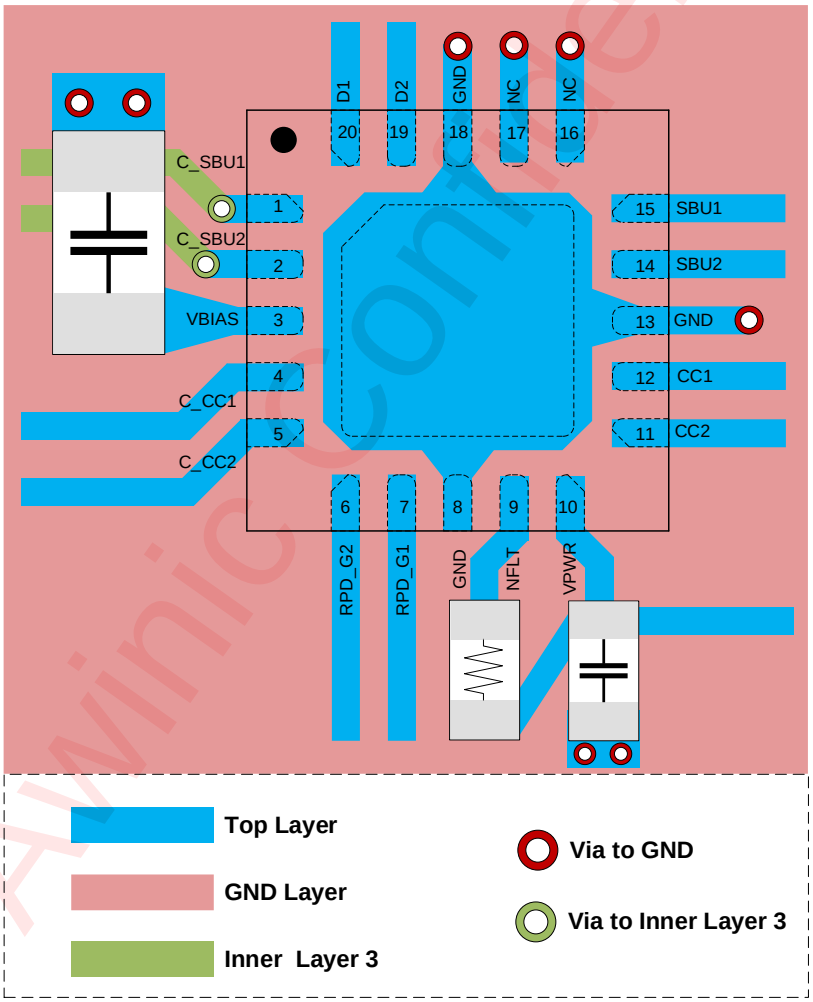
Unused pins

If RPD_Gx pins or Dx pins are unused in design, they must be connected to GND. So are NC pins.

PCB Layout Consideration

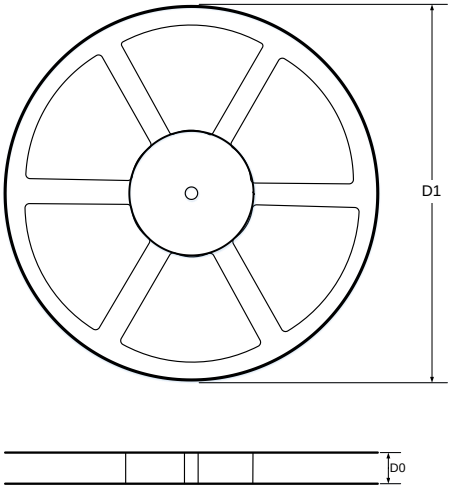
AW35622 is a USB Type-C Port Protector IC, to obtain the optimal performance, PCB Layout should be considered carefully. Here are some guidelines.

1. Place the bypass capacitors as close as possible to VPWR pin and ESD support capacitor as close as possible to VBIAS pin. Keep these capacitors away from signal traces.
2. The CC and SBU lines should be as straight as possible and minimize the sharp bends.
3. If SBU channels are used for USB2.0 D+/D- data, the following tips should be concerned additionally:
   (a) The differential characteristic impedance of D+ and D- traces is suggested to be 90Ω, and it's better to shield D+ and D- traces by ground planes.
   (b) Route the high-speed USB2.0 traces using minimum of vias and corners to reduce impedance changes and signal reflections.
   (c) Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or Ics that use or duplicate clock signals.
   (d) Avoid stubs on the high-speed USB signals because they cause signal reflections.
   (e) Route all high-speed USB signal traces over continuous GND planes, with no interruptions.

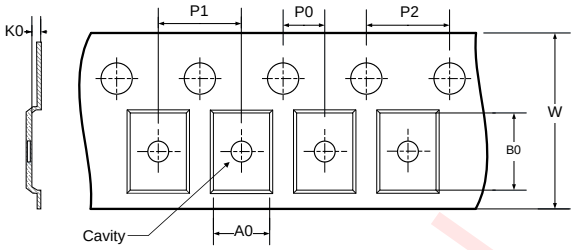


Tape And Reel Information

REEL DIMENSIONS

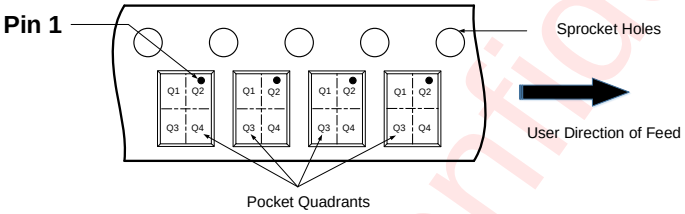


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



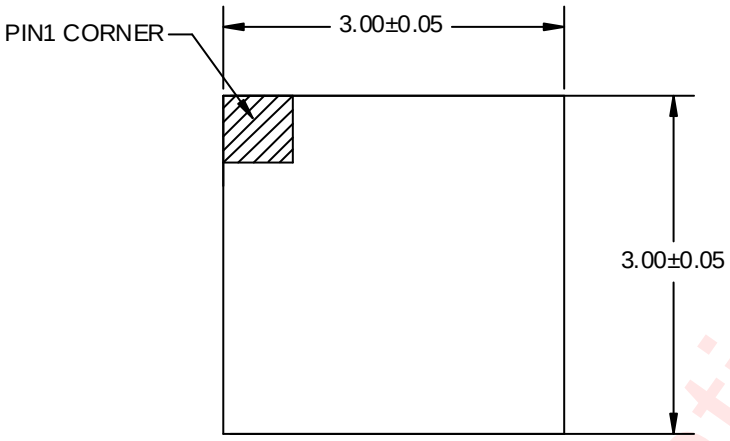
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

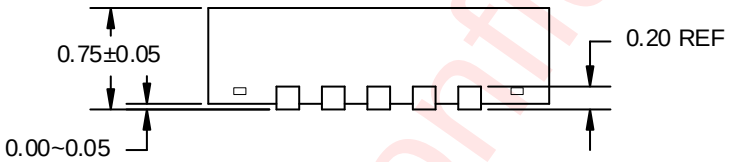
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	3.3	3.3	1.1	2	8	4	12	Q2

All dimensions are nominal

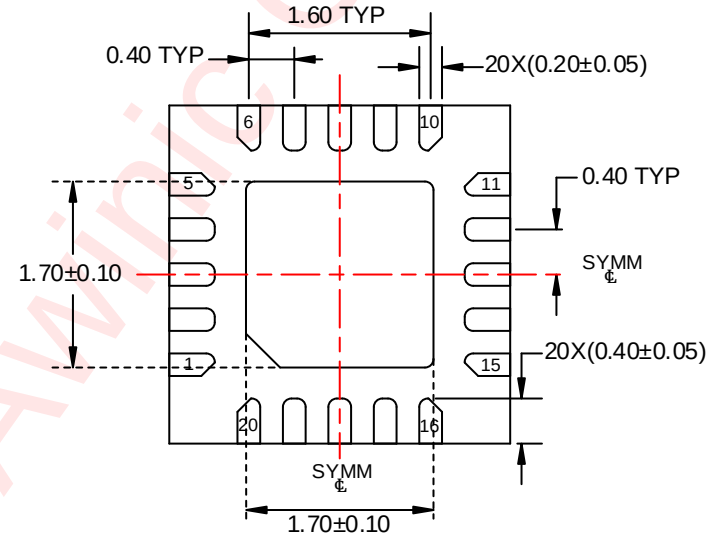
Package Description



Top View



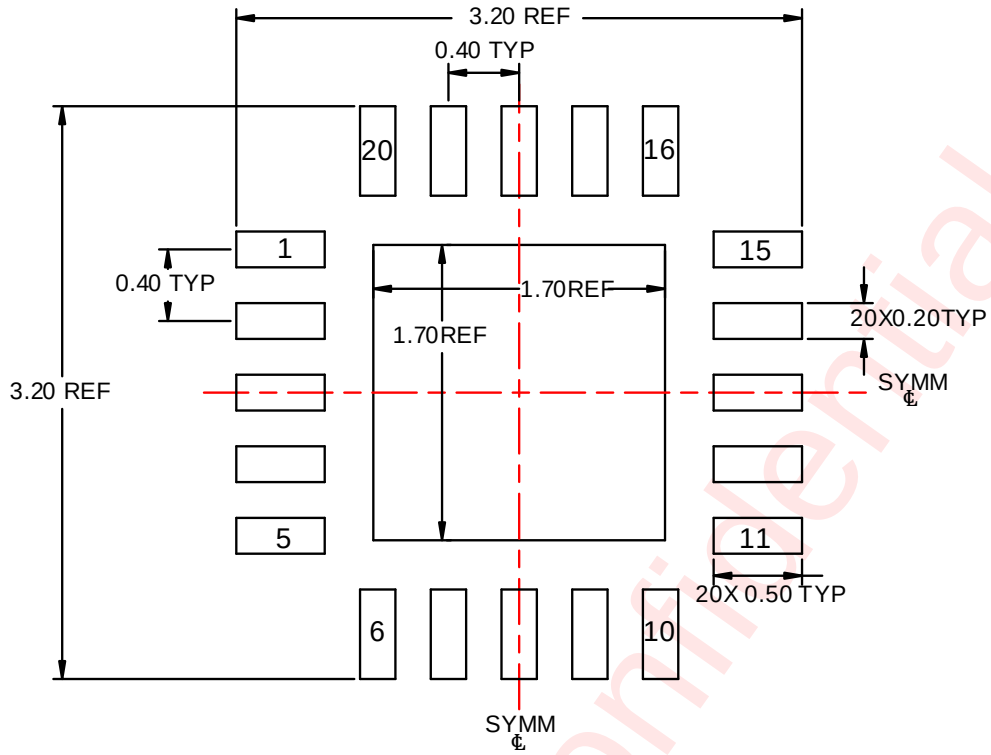
Side View

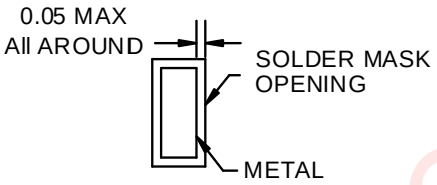


Bottom View

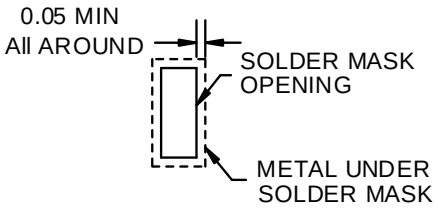
Unit：mm

Land Pattern Data





NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Dec. 2023	Officially released
V1.1	Mar. 2025	Update the CC SBU AMR to 32V
V1.2	Apr. 2025	Update the typical application circuit

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