3-Channel LED Drivers with I²C Interface

FEATURES

- 3-channel constant current LED drivers
  - 4-level global maximum current: 5mA, 10mA, 15mA, 30mA
  - 16-level individual current, 4096 mixed-color available
  - 256-level individual PWM dimming
- Automatic breathing lighting
  - Three individual pattern controllers
  - Individual and sync control selectable
- LED current accuracy: ±3%
- LED matching accuracy: ±3%
- Low dropout voltage: 50mV
- Low power consumption
  - I_{STB}<5uA in standby mode
- UVLO and OT protection
- Single power supply, 2.5V~5.5V
- 1.8V~3.3V,400kHz I²C interface (address 0x45)
- DFN 2mm×2mm×0.75mm-10L package

GENERAL DESCRIPTION

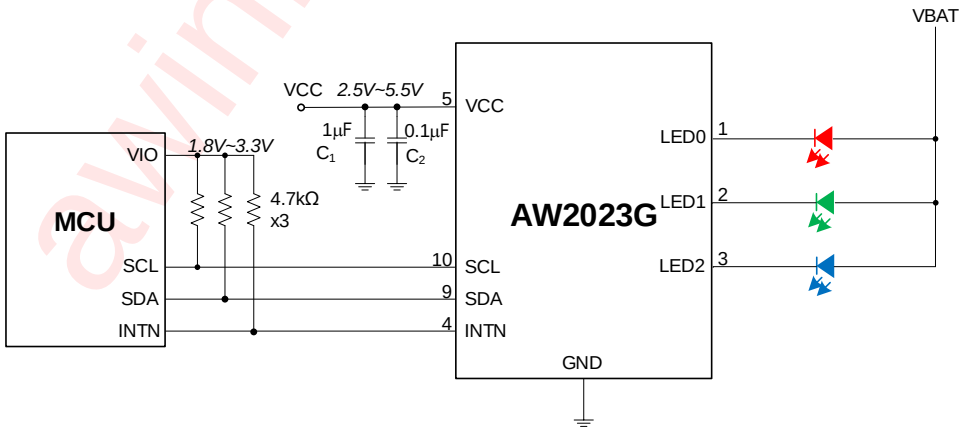
AW2023G is a three channels constant current LED driver. The max output current is 4-level selectable (5mA/10mA/15mA/30mA). Each LED is 16 current levels configurable so as to achieve 4096 color mixing. The 256-level exponential PWM dimming creates fine and smooth dimming effect even in low brightness.

AW2023G contains three independent pattern controllers. All LEDs can be controlled to work synchronously or individually due to the practical application.

An I²C compatible interface in 400kHz fast mode is provided, the device address is 45H, and continuously writing and reading the internal registers is supported.

AW2023G is available in a DFN 2mm×2mm×0.75mm -10L package, only requires single power supply of 2.5V~5.5V

TYPICAL APPLICATION CIRCUIT



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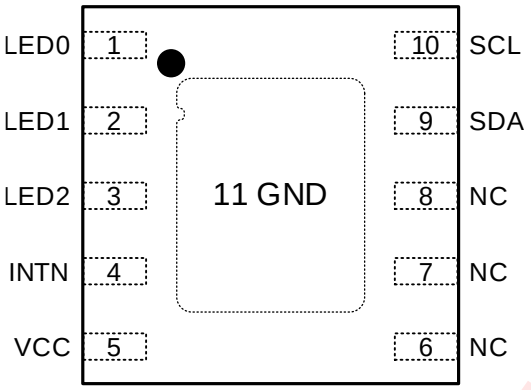
PIN CONFIGURATION AND TOP MARK

AW2023GDNR
(Top View)



AW2023GDNR Marking
(Top View)

AC23 - AW2023GDNR
XXXX - Production Tracing code

Figure 1 AW2023G Pin Configuration and Top Mark

PIN DEFINITION

No.	Name	Description
1	LED0	LED0 cathode driver, anode connected to VCC.
2	LED1	LED1 cathode driver, anode connected to VCC.
3	LED2	LED2 cathode driver, anode connected to VCC.
4	INTN	Interrupt pin. Open-drain output, be pulled low when interrupt is active.
5	VCC	Power supply (2.5V-5.5V).
6,7,8	NC	No internal connection.
9	SDA	Serial data I/O for I^2C interface.
10	SCL	Serial clock input for I^2C interface.
11	GND	Ground.

FUNCTIONAL BLOCK DIAGRAM

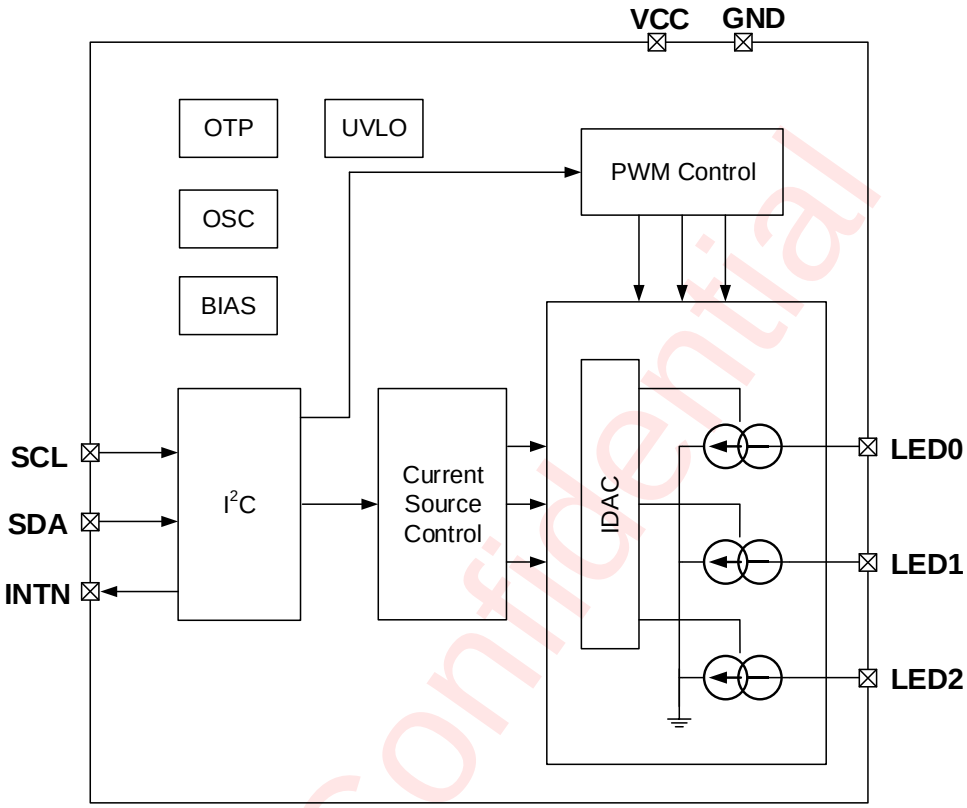


Figure 2 AW2023G Block Diagram

TYPICAL APPLICATION CIRCUITS

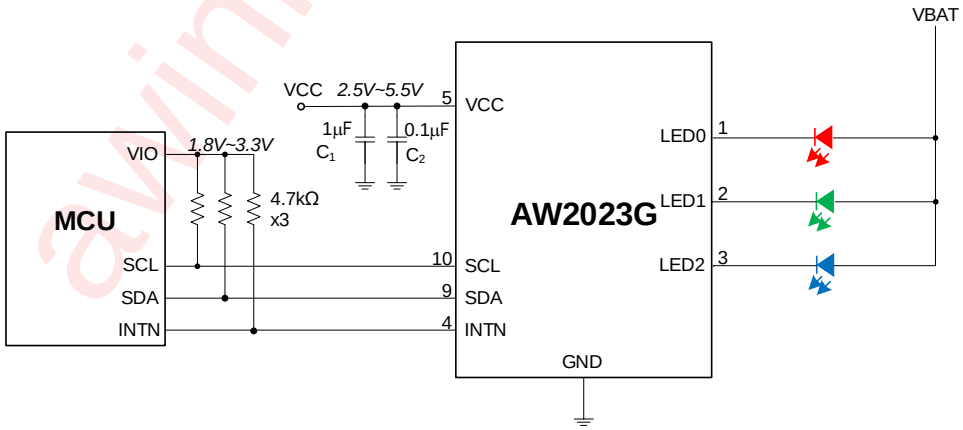
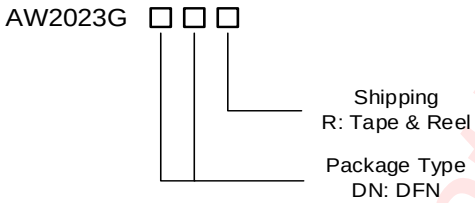


Figure 3 AW2023G Typical application Circuits

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	MSL Level	ROHS	Delivery Form
AW2023GDNR	-40°C～105°C	DFN 2mm×2mm-10L	AC23	MSL1	ROHS+HF	Tape and Reel 3000pcs/Reel



ABSOLUTE MAXIMUM RATINGS (NOTE 1)

PARAMETERS		RANGE
Supply voltage range V_{CC}		-0.3V to 6.0V
Input voltage range	SCL, SDA,	-0.3V to 6.0V
	LED0~LED2	-0.3V to 6.0V
Output voltage range	SDA, INTN	-0.3V to 6.0V
Junction-to-ambient thermal resistance θ_{JA}		45°C /W
Operating free-air temperature range		-40°C to 105°C
Maximum Junction temperature T_{JMAX}		150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)		260°C
ESD(NOTE 2)		
HBM		±2000V
CDM		±2000V
Latch-up		
Test Condition: JEDEC STANDARD NO.78B DECEMBER 2008		350mA

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	Symbol	Min	Typ	Max	Unit
Input voltage	VCC	2.5		5.5	V
Ambient temperature	T_A	-40		105	°C
Input capacitor	C_1	1		-	μF

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883G Method 3015.9.*

ELECTRICAL CHARACTERISTICS

V_{CC}=3.8V, T_A=25°C for typical values (unless otherwise noted)

Symbol	Description	Test Conditions	Min	Typ.	Max	Units
Power Supply						
V_{CC}	Input operation voltage		2.5		5.5	V
$I_{STANDBY}$	Current in Standby mode	SCL/SDA=1.8V		2	10	μA
I_{ACTIVE}	Quiescent Current in Active mode	register CHIPEN=1 all LEDs off		100	150	μA
V_{POR}	Power on reset voltage		0.95	1.25	1.55	V
V_{UVLO}	UVLO Voltage	GCR2.UVTH[1:0]=00	1.75	2	2.25	V
T_{OTP}	Over temperature Threshold			140		°C
T_{HYS}	Over temperature hysteresis			20		°C
F_{OSC}	Oscillator Frequency		0.973	1.024	1.075	MHz
LED Driver						
I_{ACC}	Current accuracy	I_{LED}=15mA	-3%		+3%	%
I_{MATCH}	Matching accuracy	I_{LED}=15mA	-3%		+3%	%
V_{DROP}	Dropout voltage	I_{LED}=15mA		50	100	mV
F_{PWM}	PWM frequency	Register LCTR.bit5=0	237.5	250	262.5	Hz
Digital Logical Interface						
V_{IL}	Logic input low level	SDA,SCL			0.4	V
V_{IH}	Logic input high level	SDA,SCL	1.3			V
I_{IL}	Low level input current	SDA,SCL		5		nA
I_{IH}	High level input current	SDA,SCL		5		nA
V_{OL}	Logic output low level	SDA, INTN, I_{OUT}=3mA			0.4	V
I_L	Output leakage current	SDA, INTN open drain			1	nA

I²C INTERFACE TIMING

Parameter Name			Min	Typ.	Max	Units
F_{SCL}	Interface Clock frequency				400	kHz
T_{DEG}	Deglitch time	SCL		200		ns
		SDA		250		ns
$T_{HD:STA}$	(Repeat-start) Start condition hold time		0.6			μs
T_{LOW}	Low level width of SCL		1.3			μs
T_{HIGH}	High level width of SCL		0.6			μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time		0.6			μs
$T_{HD:DAT}$	Data hold time		0			μs
$T_{SU:DAT}$	Data setup time		0.1			μs
T_R	Rising time of SDA and SCL				0.3	μs
T_F	Falling time of SDA and SCL				0.3	μs
$T_{SU:STO}$	Stop condition setup time		0.6			μs
T_{BUF}	Time between start and stop condition		1.3			μs

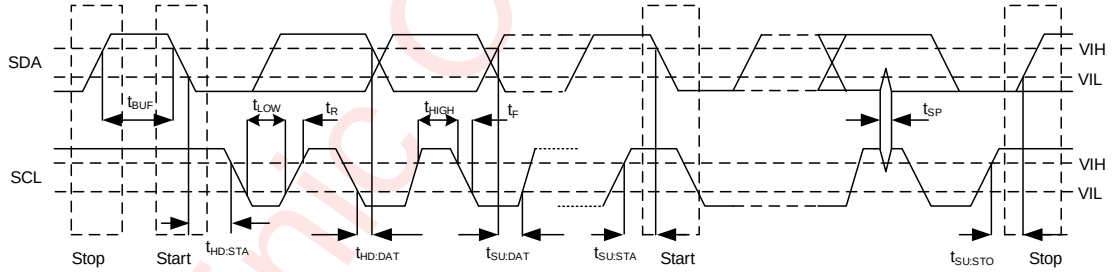


Figure 4 I²C Interface Timing

FUNCTIONAL DESCRIPTION

POWER ON RESET

When the supply voltage VCC of AW2023G drops below a predefined voltage VPOR (1.25V), the device enters standby mode, and generate a reset signal to perform a power-on reset operation, which reset all control circuits and configuration registers.

The status bit ISR.PUIS (register: 0x02 bit4) will be set to 1 when power-on reset operation occurs, which will be cleared after a read of ISR register. Usually the ISR.PUIS bit can be used to check whether an unexpected power-on event has taken place.

OPERATING MODE

There are two work modes available: Standby and Active mode.

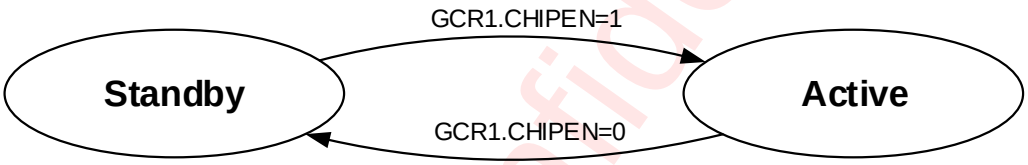


Figure 5 AW2023G Operating Modes Transition

STANDBY MODE

Once the bit GCR1.CHIPEN is clear in active mode, the AW2023G enters into standby mode.

In standby mode, only part of internal circuit work. The I2C interface is accessible, but only registers RSTR and GCR1 can be written, the internal OSC keep closed and there is no internal clock. The current consumption is less than 5μA.

ACTIVE MODE

In standby mode, once bit CHIPEN of GCR1 register is set to 1, the device enters into active mode.

In active mode, the internal OSC works to provide clock signal. User can configure the device to produce the specified breath lighting effects in pattern mode or turn each LED on or off directly.

SOFTWARE RESET

Writing 0x55 to register RSTR (register: 0x00) via I2C interface will reset the AW2023G, including all functional circuits and configuration registers.

UNDER VOLTAGE LOCK OUT (UVLO)

The voltage on pin VCC is monitored internally by the AW2023G. When voltage of VCC drops below predefined threshold by bit GCR2.UVTH (2.0v typically), the UVLOIS flag bit in ISR register is set to “1”. After a read, the flag register can be cleared.

When UVLO condition is met, the bit CHIPEN in register GCR1 will be cleared, and the device return to standby state. If VCC rises above the threshold and GCR1.CHIPEN bit is set to “1”, the device will enter into active mode again.

If the UVDIS bit in register GCR2 is set to “1”, the internal UVLO monitor is disabled. The default value of the UVDIS bit is “0”.

If the DUVP bit in register GCR2 is set to “1”, the UVLO protection function is closed, the device keeps working even though UVLO state is detected. The default value of the DUVP bit is “0”.

OVER TEMPERATURE PROTECTION

When the device reaches 140℃, the over-temperature protection be activated, and the OTPIS flag bit in register ISR is set to “1”, and after a read, the flag register can be cleared.

When OTP condition is met, the bit CHIPEN in register GCR1 will be cleared, and the device will be forced to standby state. Once the temperature of the device drops below 120℃, and GCR1.CHIPEN bit is set to “1”, the device will enter into active mode again.

If the OTDIS bit in register GCR2 is set to “1”, the OTP function is disabled. The default value of the OTDIS bit is “0”.

If the DOTP bit in register GCR2 is set to “1”, the OTP protection function is closed, the device keeps working even though over-temperature condition is detected. The default value of the DOTP bit is “0”.

I²C INTERFACE

The AW2023G supports the I²C serial bus and data transmission protocol in fast mode at 400 kHz, and operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. Different I2C interface voltage of 1.8V ~ 3.3V are all supported.

DEVICE ADDRESS

The I2C device address (7-bit) of AW2023G is 0x45, followed by the R/W bit (Read=1/Write=0).

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

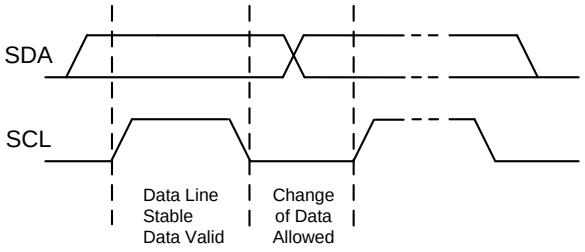


Figure 6 Data Validation Diagram

I2C START/STOP

I2C start: SDA changes form high level to low level when SCL is high level.

I2C stop: SDA changes form low level to high level when SCL is high level.

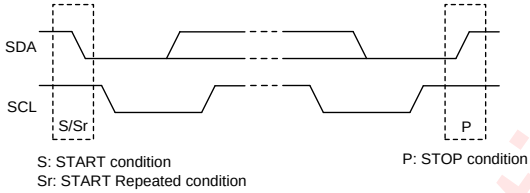


Figure 7 I²C Start/Stop Condition Timing

ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I2C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I2C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I2C stop.

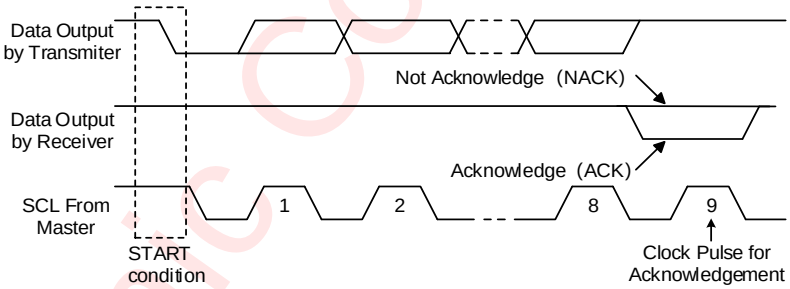


Figure 8 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit).

e) Slave sends acknowledge signal.

f) Master sends data byte to be written to the addressed register.

g) Slave sends acknowledge signal.

h) If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step f,g).

i) Master generates STOP condition to indicate write cycle end.

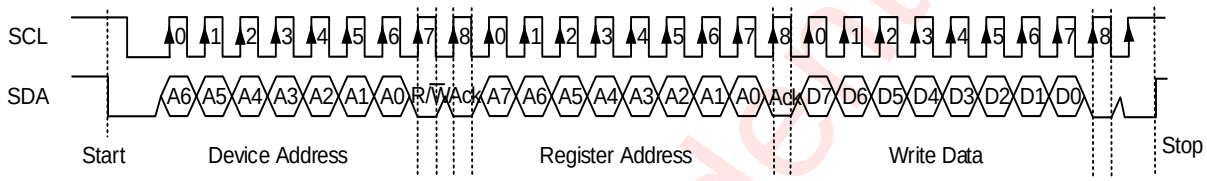


Figure 9 I²C Write Byte Cycle

READ CYCLE

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends data byte from addressed register.

j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.

k) If the master device generates STOP condition, the read cycle is ended.

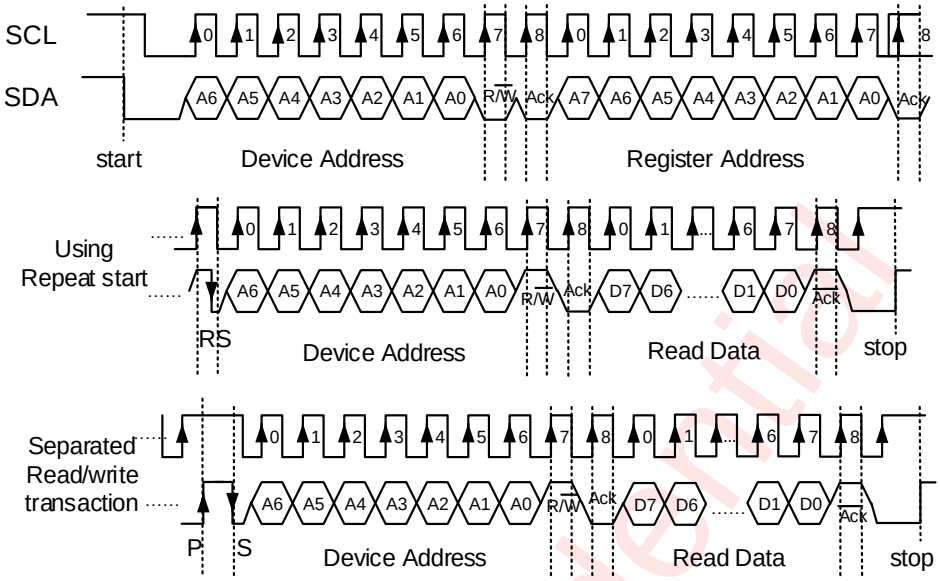


Figure 10 I²C Read Byte Cycle

LED DRIVER

AW2023G has 3 LED drivers to drive one RGB LED or three single-color LEDs. Each LED is driven by constant current source with duty cycle controlled by PWM. Both current and PWM level can be configured via I2C interface.

LED CURRENT

Globally, the maximum output current for three LEDs is 4-level selectable among 5mA, 10mA, 15mA and 30mA via register GCR2.IMAX (address 0x04). In general, GCR2.IMAX is used to set the max brightness of LED.

For each LED, there is 16 current levels configurable by 4-bit registers LCFGx.CUR[3:0] (x=0~2). In RGB application it is possible to combine into 16x16x16 color-mixing schemes totally.

PWM DIMMING CONTROL

The LED output current source is gated by exponent 256-level PWM signal to create better dimming effect. The registers PWMx (address 0x34, 0x35, 0x36) define 8-bit PWM level for each LED.

When register PWMx being modified or working in PATTERN mode, the smooth dimming effect is available by continuously adjusting PWM duty. The slope of ramp up/down, are separately set via configuring the bit4~bit7 in registers LEDxT0~LEDxT2 (x=0~2).

The ramping curve can be configured to be linear and exponential by setting bit3 (EXP) in register LCTR (address 0x30).

LED CONTROL

All LEDs in AW2023G can be independently turned on or off via setting bit Lex (x=0~2) of register LCTR

- LCTR.Lex=0, LEDx is switched off.
- LCTR.Lex=1, LEDx is switched on.

PATTERN MODE

When register bit LCFGx.MD (address 0x31, 0x32, 0x33, x=0~2) is set to “1”, the corresponding LEDx operates in pattern mode.

In this mode, the LEDx is controlled by internal pattern controller to produce breathing lighting effect with user-defined timing parameter. In AW2023G, each LED has an independent pattern controller with respective pattern parameter configuration register, and work independently.

The waveform of a breathing pattern is shown in the diagram below. The parameter T0~T4 define 4 key primary time in a complete breathing period. T0 is the delay time before pattern starting, T1~T4 composite a breathing cycle, denoting the rise-time, on-time, fall-time and off- time respectively.

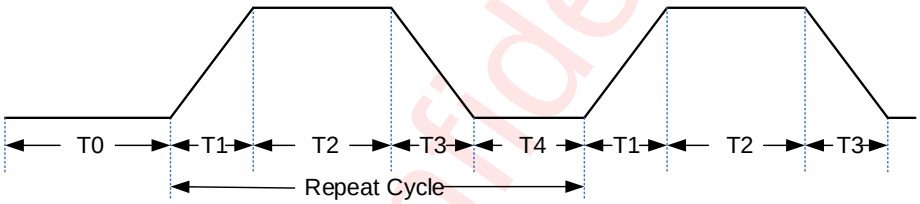


Figure 11 LED Breath Timing in Pattern Mode

The repeat times of pattern is configured by bit0~3 (REPEAT) in register LEDxT2. A pattern can repeat for 1 to 15 times if LEDxT2.REPEAT is not “0000”, or loop continuously if LEDxT2.REPEAT is “0000”

After defined times of pattern repeat is finished, the status bit ISR.LISx (address 0x02, x=0~2) will be set to “1” automatically, which only can be cleared after reading register ISR via I2C.

In pattern mode, each LED can be configured individually. The breath effect will start once LEDxT2 is written. If user wants to sync the three patterns start at the same time, please follow the following steps:

a) Set LCTR to 00h
b) Set LCFGx.MD to “0”
c) Configure LEDxT0,LEDxT1, LEDxT2 for parameters T0~T4, repeat time .
d) Set LCFGx.MD to “1”
e) Set LCTR to 07h

MANUAL CONTROL MODE

When control bit LCFGx.MD (address 0x31, 0x32, 0x33, bit4) is set to 0, the corresponding LEDx is work in manual control mode.

In manual control mode, the pattern controller is disabled and the LED is directly controlled by setting current and PWM level register via I2C interface.

Even in manual control mode, smooth dimming is supported. If LCFGx.FO and/or LCFGx.FI (address 0x31, 0x32 0x33, bit6/bit5) is set to 1, automatic fade-out and/or fade-out is enabled. If a new value is set on register PWMx when LCFGx.FO and/or LCFGx.FI is set, the brightness of LED output ramp up/down smoothly, with

its transition time defined by parameter T1,T3 sourced from corresponding pattern configuration registers (LEDxT0 and LEDxT1).

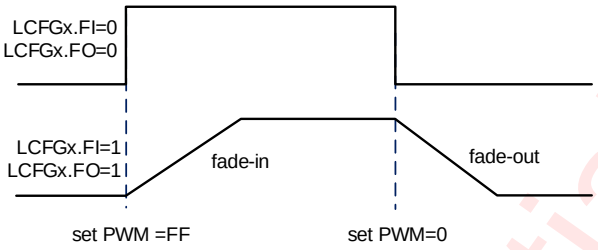


Figure 12 Manual Control Mode

SYNC CONTROL MODE

In order to simplify configuration and control in the case of all LEDs synchronously dimming, especially in application of RGB LED, the AW2023G can be configured to work on sync control mode.

When LCFG0.SYNC is set to 1, the device works in sync control mode. In this mode, user can control all LEDs to turn on, turn off, or output breathing lighting synchronously by controlling LED0 only.

In sync control mode, the output currents of all LEDs are still defined via register LCFGx.CUR individually, but their PWM levels of LED1,LED2 are both sourced from LED0, the setting of register PWM1,PWM2 are ignored. The control bit LCFG0.MD defines operating mode globally for all LEDs. If LCFG0.MD is 0, manual mode is selected for all LEDs, user can set all LEDs on or off by simply setting register PWM0, and fade-in or fade-out effect are selected by bit LCFG0.FI and LCFG0.FO. If register LCFG0.MD is set 1, all LEDs work in pattern mode, user only need to configured and control the pattern of LED0.

REGISTER DESCRIPTION

REGISTER LIST

Addr	Name	W/R	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	RSTR	WR	0	0	0	0	1	0	0	1
01h	GCR1	WR	LIE2	LIE1	LIE0		UVLOIE	OTPIE	-	CHIPEN
02h	ISR	R	LIS2	LIS1	LIS0	PUIS	UVLOIS	OTPIS	-	-
03h	PATST	R	0	0	0	0	0	ST2	ST1	ST0
04h	GCR2	WR	DUVP	DOTP	UVDIS	OTDIS	UVTH		IMAX	
30h	LCTR	WR	-	-	FREQ	-	EXP	LE2	LE1	LE0
31h	LCFG0	WR	SYNC	FO	FI	MD	CUR			
32h	LCFG1	WR	-	FO	FI	MD	CUR			
33h	LCFG2	WR	-	FO	FI	MD	CUR			
34h	PWM0	WR	PWM							
35h	PWM1	WR	PWM							
36h	PWM2	WR	PWM							
37h	LED0T0	WR	T1				T2			
38h	LED0T1	WR	T3				T4			
39h	LED0T2	WR	T0				REPEAT			
3Ah	LED1T0	WR	T1				T2			
3Bh	LED1T1	WR	T3				T4			
3Ch	LED1T2	WR	T0				REPEAT			
3Dh	LED2T0	WR	T1				T2			
3Eh	LED2T1	WR	T3				T4			
3Fh	LED2T2	WR	T0				REPEAT			

DETAILED REGISTER DESCRIPTION

RSTR, Chip ID and Software Reset Register

Address: 0x00, R/W, default: 0x09

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Symbol	Description
7:0	RSTR	Reset Control. Write 0x55 will reset internal logic and register. Read out is fixed to 0x09 as chip ID.

GCR1, Global Control Register

Address: 0x01, R/W, default: 0x00

7	6	5	4	3	2	1	0
LIE2	LIE1	LIE0	-	UVLOIE	OTPIE	-	CHIPEN

Bit	Symbol	Description
7:5	LIEx	LEDx Interrupt enable for pattern complete 0: Disable pattern complete interrupt for LEDx (default) 1: Enable pattern complete interrupt for LEDx
4	-	Reserved

3	UVLOIE	UVLO Interrupt enable 0: Disable UVLO interrupt (default) 1: Enable UVLO interrupt
2	OTPIE	Over Temperature Interrupt enable 0: Disable OT interrupt (default) 1: Enable OT interrupt
1	-	Reserved
0	CHIPEN	Device operating Enable 0: Disable, the device is in standby state (default) 1: Enable, the device enters active state

ISR, Chip Status Register

Address: 0x02, Read only, Cleared after Read, default: 0x10

7	6	5	4	3	2	1	0
LIS2	LIS1	LIS0	PUIS	UVLOIS	OTPIS	-	-

Bit	Symbol	Description
7:5	LISx	LEDx Interrupt Status
4	PUIS	Power Up Interrupt Status 0: No power-up reset has taken place 1: Power-up reset has taken place
3	UVLOIS	UVLO Detection Status 0: no UVLO detected 1: UVLO detected
2	OTIS	Over-temperature Detection Status 0: No Over-Temperature detected 1: Over-Temperature detected
1:0	-	Reserved

PATST, Pattern Status Register

Address: 0x03, Read only, default: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	-	ST2	ST1	ST0

Bit	Symbol	Description
7:3	-	Reserved
2	ST2	LED2 Pattern Status 0: Pattern is not running 1: Pattern is running
1	ST1	LED1 Pattern Status 0: Pattern is not running 1: Pattern is running

0	ST0	LED0 Pattern Status 0: Pattern is not running 1: Pattern is running

GCR2, LED Maximum Current Register

Address: 0x04, R/W, default: 0x00

7	6	5	4	3	2	1	0
DUVP	DOTP	UVDIS	OTDIS	UVTH		IMAX	

Bit	Symbol	Description
7	DUVP	Disable UVLO Protection 0: enable UVLO protection, clear GCR1.CHIPEN when UVLOIS=1 (default) 1: disable UVLO protection
6	DOTP	Disable Over－temperature Protection 0: enable OTP protection, clear GCR1.CHIPEN when OTPIS=1 (default) 1: disable OTP protection
5	UVDIS	Disable UVLO Detection Function 0: enable UVLO detection (default) 1: disable UVLO detection
4	OTDIS	Disable Over-Temperature Detection Function 0: enable Over-temperature detection (default) 1: disable Over-Temperature detection
3:2	UVTH	UVLO Threshold Voltage Selection 00: 2.0v (default) 01: 2.1v 10: 2.2v 11: 2.3v
1:0	IMAX	Global Max Output Current Selection 00: 15mA (default)） 01: 30mA 10: 5mA 11: 10mA

LCTR, LED Control Register

Address: 0x30, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	-	FREQ	-	EXP	LE2	LE1	LE0

Bit	Symbol	Description
5	FREQ	PWM Carrier Frequency Selection 0: 250Hz (default) 1: 125Hz
4	-	Reserved. Should be set 0.
3	EXP	PWM Transition Mode Selection 0: Exponential transition (default) 1: Linear transition

2	LE2	LED2 Enable Control 0: disable LED2 (default) 1: enable LED2
1	LE1	LED1 Enable 0: disable LED1 (default) 1: enable LED1
0	LE0	LED0 Enable 0: disable LED0 (default) 1: enable LED0

LCFG0, LED0 Mode Configuration Register

LCFG0: Address: 0x31, R/W, default: 0x00

7	6	5	4	3	2	1	0
SYNC	FO	FI	MD	CUR			

Bit	Symbol	Description
7	SYNC	Sync Mode Enable 0: Individual control mode (default) 1: Sync control mode
6	FO	Fade-out enable control, only active in manual mode 0: PWM fade-out is disable (default) 1: PWM fade-out is enable, the dimming time defined by T3
5	FI	Fade-in enable control, only active in manual mode 0: PWM fade-in is disable (default) 1: PWM fade-in is enable, the dimming time defined by T1
4	MD	LED0 Operating Mode Select. 0: Manual mode (default) 1: Pattern mode
3:0	CUR	LED0 output Current Setting. LED0 output current Io = Imax*CUR/15 (mA) when PWM0 is 255.

LCFG1, LED1 Mode Configuration Register

LCFG1: Address: 0x32, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	FO	FI	MD	CUR			

Bit	Symbol	Description
6	FO	Fade-out enable control, only active in manual mode 0: PWM fade-out is disable (default) 1: PWM fade-out is enable, the dimming time defined by T3
5	FI	Fade-in enable control, only active in manual mode 0: PWM fade-in is disable (default) 1: PWM fade-in is enable, the dimming time defined by T1

4	MD	LED1 Operating Mode Select. 0: Manual mode (default) 1: Pattern mode
3:0	CUR	LED1 output Current Setting. LED1 output current I_O = Imax*CUR/15 (mA) when PWM1 is 255.

LCFG2, LED2 Mode Configuration Register

LCFG2: Address: 0x33, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	FO	FI	MD	CUR			

Bit	Symbol	Description
6	FO	Fade-out enable control, only active in manual mode 0: PWM fade-out is disable (default) 1: PWM fade-out is enable, the dimming time defined by T3
5	FI	Fade-in enable control, only active in manual mode 0: PWM fade-in is disable (default) 1: PWM fade-in is enable, the dimming time defined by T1
4	MD	LED2 Operating Mode Select. 0: Manual mode (default) 1: Pattern mode
3:0	CUR	LED2 output Current Setting. LED2 output current Io = Imax*CUR/15 (mA) when PWM2 is 255.

PWM0/PWM1/PWM2 , PWM Dimming Level Register

PWM0: Address: 0x34, R/W, default:0x00
PWM1: Address: 0x35, R/W, default:0x00
PWM2: Address: 0x36, R/W, default:0x00

7	6	5	4	3	2	1	0
PWM							

Bit	Symbol	Description
7:0	PWM	PWM Dimming level for LEDx (x=0~2)

LEDxT0, T1 & T2 Configuration Register

LED0T0: Address: 0x37, R/W, default: 0x00
LED1T0: Address: 0x3A, R/W, default: 0x00
LED2T0: Address: 0x3D, R/W, default: 0x00

7	6	5	4	3	2	1	0
T1				T2			

Bit	Symbol	Description
7:4	T1	T1 (Rise-time) selection

0000:	0.00s (default)	1000:	2.1s
0001:	0.13s	1001:	2.6s
0010:	0.26s	1010:	3.1s
0011:	0.38s	1011:	4.2s
0100:	0.51s	1100:	5.2s
0101:	0.77s	1101:	6.2s
0110:	1.04s	1110:	7.3s
0111:	1.6s	1111:	8.3s

3:0 T2 T2 (On-time) selection

0000:	0.04s (default)	1000:	2.1s
0001:	0.13s	1001:	2.6s
0010:	0.26s	1010:	3.1s
0011:	0.38s	1011:	4.2s
0100:	0.51s	1100:	5.2s
0101:	0.77s	1101:	6.2s
0110:	1.04s	1110:	7.3s
0111:	1.6s	1111:	8.3s

LEDxT1, T3 & T4 Configuration Register

LED0T1: Address: 0x38, R/W, default: 0x00
LED1T1: Address: 0x3B, R/W, default: 0x00
LED2T1: Address: 0x3E, R/W, default: 0x00

7	6	5	4	3	2	1	0
T3				T4			

Bit Symbol Description

7:4 T3 T3 (Fall-time) selection

0000:	0.00s (default)	1000:	2.1s
0001:	0.13s	1001:	2.6s
0010:	0.26s	1010:	3.1s
0011:	0.38s	1011:	4.2s
0100:	0.51s	1100:	5.2s
0101:	0.77s	1101:	6.2s
0110:	1.04s	1110:	7.3s
0111:	1.6s	1111:	8.3s

3:0 T4 T4 (Off-time) selection

0000:	0.04s (default)	1000:	2.1s
0001:	0.13s	1001:	2.6s
0010:	0.26s	1010:	3.1s

0011:	0.38s	1011:	4.2s
0100:	0.51s	1100:	5.2s
0101:	0.77s	1101:	6.2s
0110:	1.04s	1110:	7.3s
0111:	1.6s	1111:	8.3s

LEDxT2, T0 & Repeat Times Configuration Register

LED0T2: Address: 0x39, R/W, default: 0x00
LED1T2: Address: 0x3C, R/W, default: 0x00
LED2T2: Address: 0x3F, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	T0			REPEAT			

Bit	Symbol	Description
7:4	T0	T0 (delay time of pattern startup) selection

0000:	0.04s (default)	1000:	2.1s
0001:	0.13s	1001:	2.6s
0010:	0.26s	1010:	3.1s
0011:	0.38s	1011:	4.2s
0100:	0.51s	1100:	5.2s
0101:	0.77s	1101:	6.2s
0110:	1.04s	1110:	7.3s
0111:	1.6s	1111:	8.3s

3:0 REPEAT Pattern Repeat Time

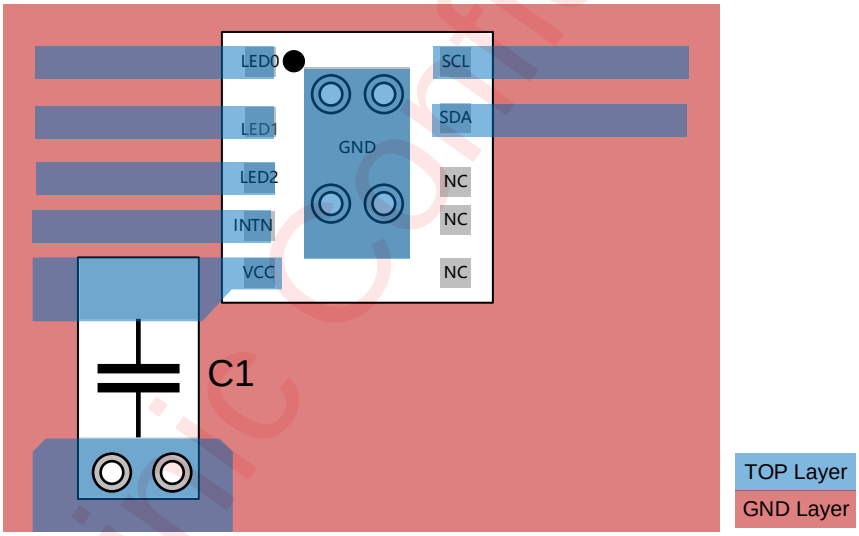
0000: don’t stop
0001: pattern repeats 1 time
0010: pattern repeats 2 times
……
1111: pattern repeats 15 times

PCB LAYOUT CONSIDERATION

LAYOUT GUIDELINES

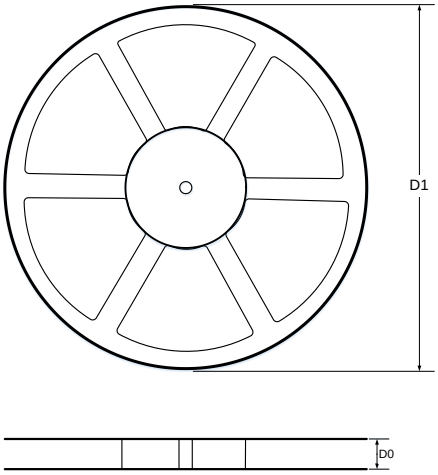
AW2023G is a three channels constant current LED driver. The maximum output current is 30mA. To obtain the good thermal performance, PCB layout should be considered carefully. Here are some guidelines:

1. The power decoupling capacitor C_1 should be placed as close to the VCC pin as possible. In order to prevent high-frequency burrs, C_2 can be reserved at VCC pin.
2. The Thermal PAD and GND pin of chip must be well connecting to the GND of the PCB, and add as many thermal vias as possible beneath the thermal PAD on the PCB for the heat conductivity of the device and PCB.
3. SCL and SDA shall be package handed with GND.
4. To avoid EMI interference, ensure that the chip is placed far away from the wireless transmitter, radio frequency and power amplifier modules.

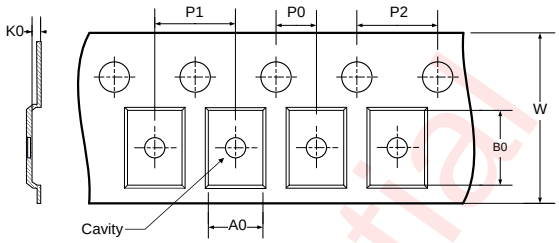


TAPE AND REEL INFORMATION

REEL DIMENSIONS

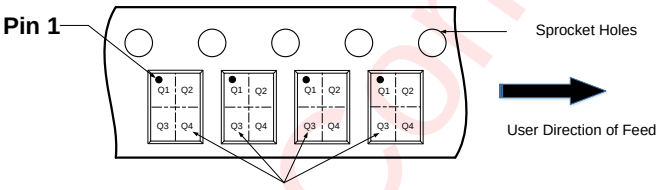


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

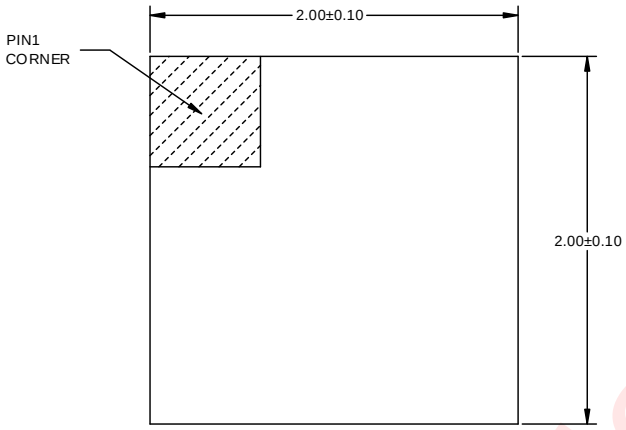


DIMENSIONS AND PIN1 ORIENTATION

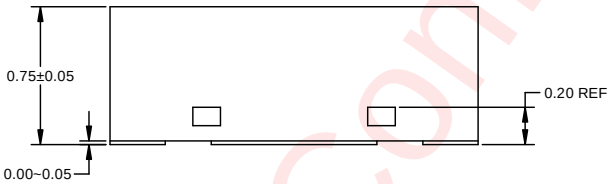
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2.3	2.3	1	2	4	4	8	Q1

All dimensions are nominal

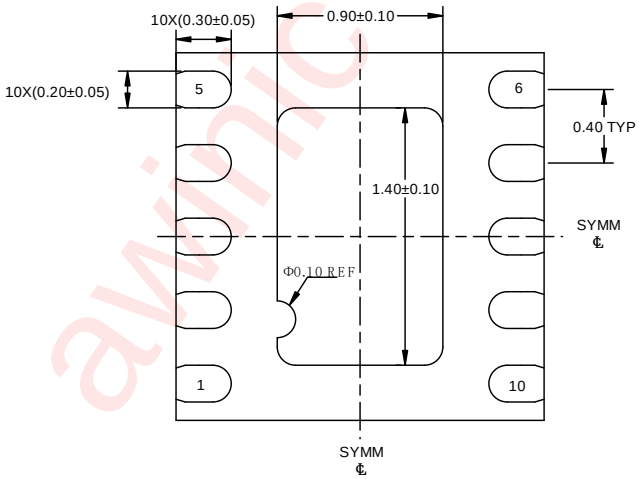
PACKAGE DESCRIPTION



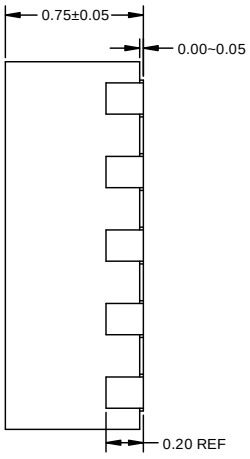
TOP VIEW



SIDE VIEW



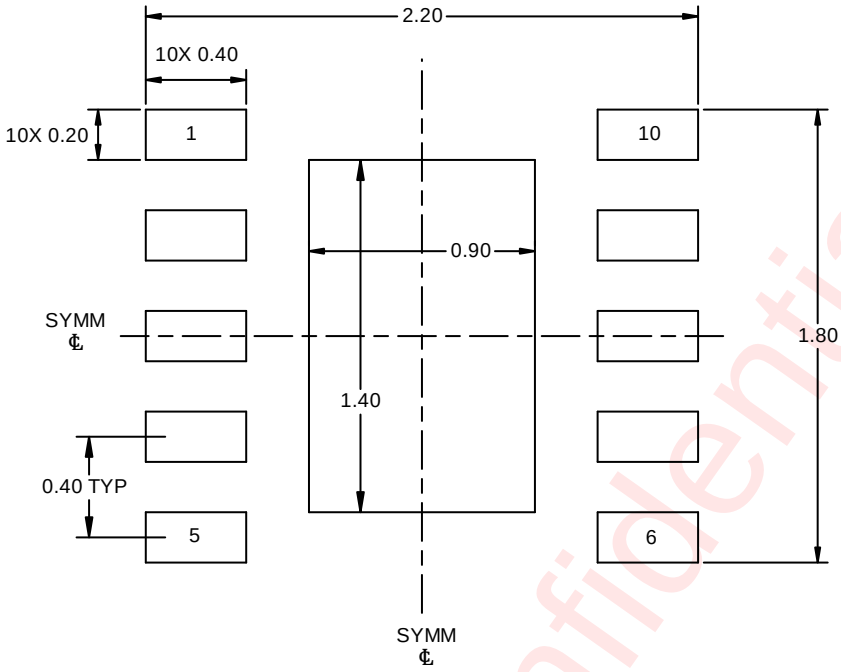
BOTTOM VIEW

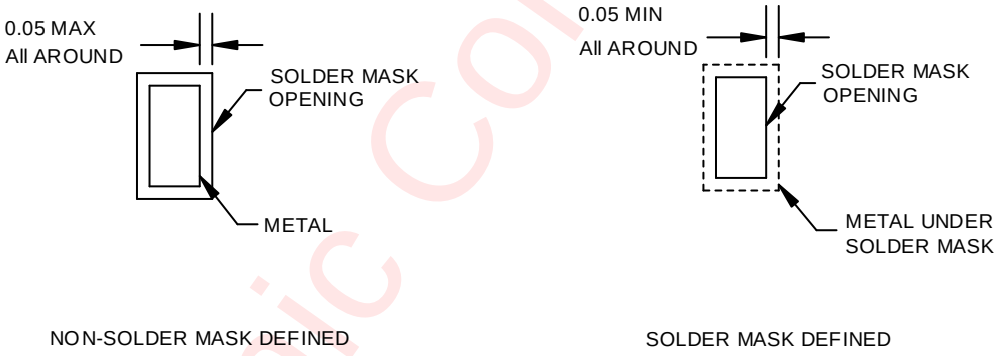


SIDE VIEW

Unit：mm

LAND PATTERN EXAMPLE



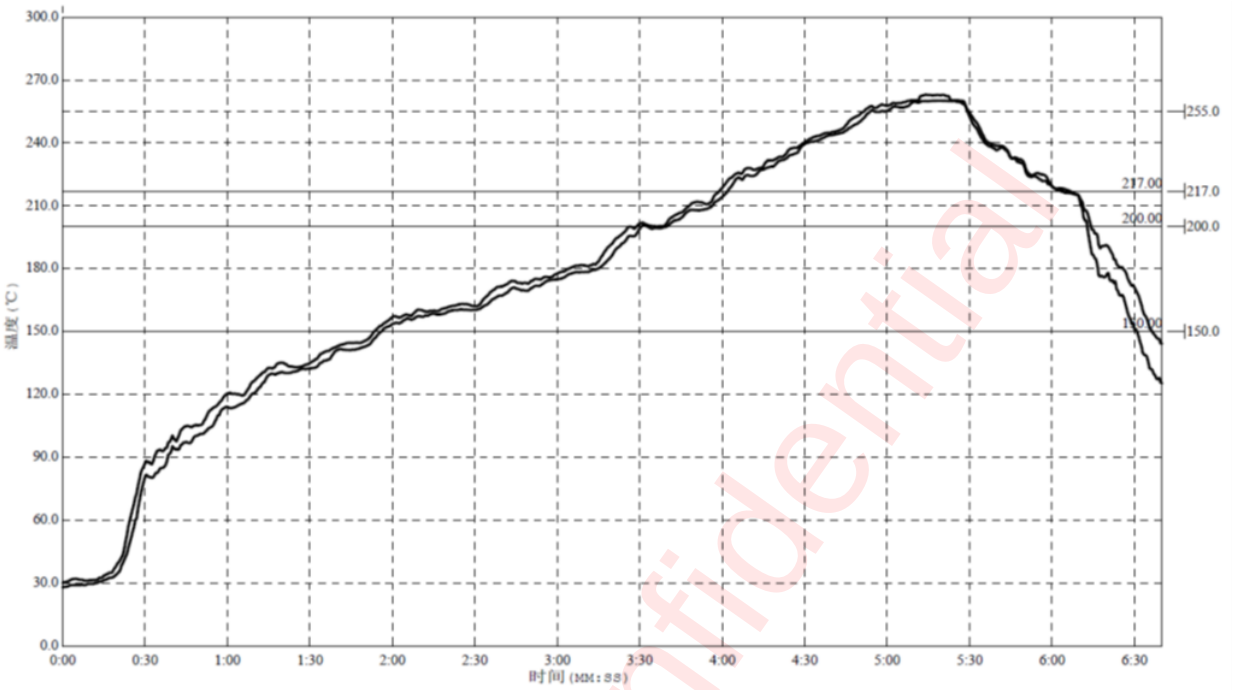


NON-SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit: mm

REFLOW



Reflow Note	Spec
Average ramp-up rate (217°C to peak)	Max. 3°C /sec
Time of Preheat temp. (from 150°C to 200°C)	60-120sec
Time to be maintained above 217°C	60-150sec
Peak Temperature	>260°C
Time within 5°C of actual peak temp	20-40sec
Ramp-down rate	Max. 6°C /sec
Time from 25°C to peak temp	Max. 8min

Package Reflow Standard Profile

NOTE 1: All data are compared with the package-top temperature, measured on the package surface;

NOTE 2: AW2023G adopted the Pb-Free assembly.

REVISION HISTORY

Vision	Date	Revision Record
V1.0	Mar 2017	Initial release

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