钍地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65HVD1050DR

EMC Optimized CAN Bus Transceiver

网址 www.sztdbdt.com

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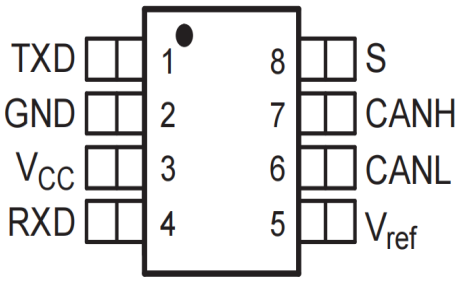
semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

●Improved Replacement for the TJA1050
●High Electromagnetic Immunity(EMI)
●Very Low Electromagnetic Emissions(EME)
●Meets or Exceeds the Requirements ofSO 11898-2
●CAN Bus-Fault Protection of-27 V to 40V
●Dominant Time-Out Function
●Power-Up and Power-Down Glitch-Free CAN Bus Inputs and Outputs
-High Input Impedance With Low Vcc
-Monotonic Outputs During Power Cyclng



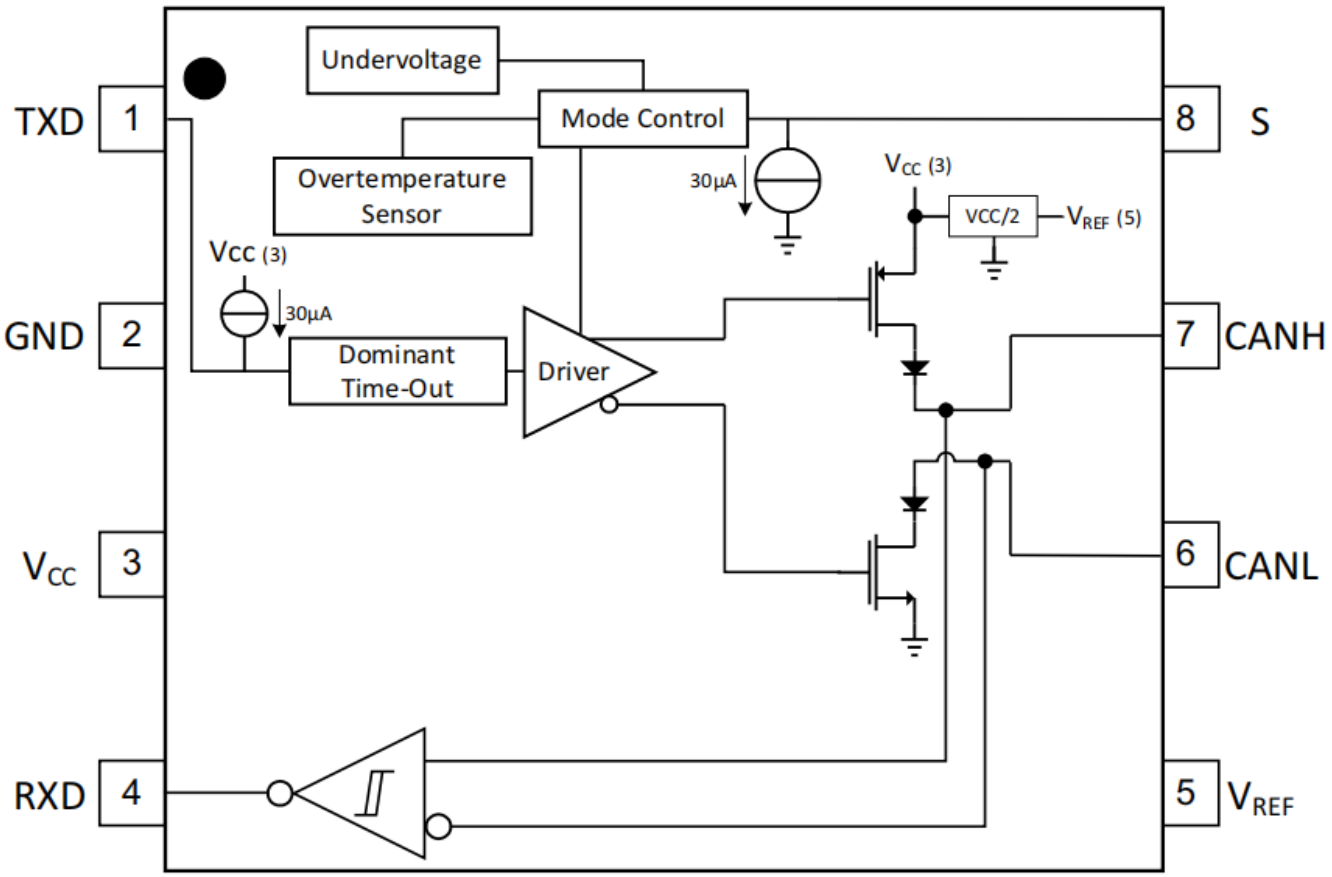
Applications

●Industrial Automation
-DeviceNetTM Data Buses(Vendor ID#806)
●SAE J2284 High-Speed CAN Bus for Automotive Applications
●SAE J1939 Standard Data Bus Interface
●ISO 11783 Standard Data Bus Interface
●NMEA 2000 Standard Data Bus Interface

Description

The SN65HVD1050 meets or exceeds thespecifications of the ISO 11898 standard for use inapplications employing a Controller Area Network(CAN).
As a CAN transceiver,this device provides differentialtransmit capability to the bus and differential receivecapability to a CAN controller at signaling rates up to1 megabit per second (Mbps)(1).
The SN65HVD1050 is designed for operation inespecially harsh environments.As a result,the devicefeatures cross-wire,overvoltage and loss of groundprotection from-27 V to 40 V, overtemperatureshutdown,a-12-V to 12-V common-mode range,andwill withstand voltage transients from-200V to 200 Vaccording to ISO 7637.

Functional Block Diagram



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
TXD	1	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
GND	2	GND	Device ground
V_{CC}	3	Supply	Transceiver 5-V supply
RXD	4	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
V_{REF}	5	O	Reference output voltage
CANL	6	I/O	Low level CAN bus line
CANH	7	I/O	High level CAN bus line
S	8	I	Mode select pin (Logic LOW places the device in high-speed mode and logic HIGH places the device in a listen-only silent mode)

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	–0.3	7	V
	Voltage range at any bus terminal (CANH, CANL, V_{ref})	–27	40	V
I_O	Receiver output current		20	mA
V_I	Voltage input, transient pulse(3) (CANH, CANL)	–200	200	V
V_I	Voltage input range (TXD, S)	–0.5	6	V
T_J	Junction temperature	–55	170	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with ISO 7637, test pulses 1, 2, 3a, 3b, 5, 6, and 7.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±8000	V
			Bus pins vs GND	±4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1500	
		Machine Model, ANSI/ESDS5.2-1996		±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5		5.5	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–12		12	V
V_{IH}	High-level input voltage	TXD, S	2.1		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{ID}	Differential input voltage		–7		7	V
I_{OH}	High-level output current	Driver	–70			mA
		Receiver	–2			
I_{OL}	Low-level output current	Driver			70	mA
		Receiver			2	
T_J	Junction temperature	See *Absolute Maximum Ratings*(1), 1-Mbps minimum signaling rate with R_L = 54 Ω	–40		150	°C
	Signaling Rate		20			kbps

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.4 Thermal Information

THERMAL METRIC(1)		SN65HVD1050 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-air, Low-K thermal resistance(2)	211	°C/W
	Junction-to-air, High-K thermal resistance	131	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79	
$R_{\theta JB}$	Junction-to-board thermal resistance	53	
ψ_{JT}	Junction-to-top characterization parameter	10.3	
ψ_{JB}	Junction-to-board characterization parameter	56.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	112	
P_D	Average power dissipation, V_{CC} = 5.0V, T_j = 27°C, R_L = 60 Ω, S at 0V, Input to TXD a 500 kHz, 50% duty cycle square wave. CL at RXD = 15 pF	170	mW
	Average power dissipation, V_{CC} = 5.5V, T_j = 130°C, R_L = 45 Ω, S at 0V, Input to TXD a 500 kHz, 50% duty cycle square wave. CL at RXD = 15 pF	170	
$T_{J\_shutdown}$	Junction temperature, thermal shutdown(3)	190	°C

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface-mount packages.
(3) Extended operation in thermal shutdown may affect device reliability, see APPLICATIONS INFORMATION.

7.5 Driver Electrical Characteristics

over recommended operating conditiions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
$V_{O(D)}$	Bus output voltage (Dominant)	CANH	V_I = 0V, S at 0V, R_L = 60 Ω, See Figure 11 and Figure 12	4.75V < V_{CC} < 5.25V	2.9	3.4	4.5	V
				4.5V < V_{CC} < 5.5V	2.75		5.2	
		CANL		4.75V < V_{CC} < 5.25V	0.8		1.5	
				4.5V < V_{CC} < 5.5V			1.6	
$V_{O(R)}$	Bus output voltage (Recessive)		V_I = 3V, S at 0V, R_L = 60 Ω, See Figure 11 and Figure 12	4.75V < V_{CC} < 5.25V	2	2.3	3	V
				4.5V < V_{CC} < 5.5V	1.8		3	
$V_{OD(D)}$	Differential output voltage (Dominant)		V_I = 0V, R_L = 60 Ω, S at 0V, See Figure 11, Figure 12, and Figure 13	4.75V < V_{CC} < 5.25V	1.5		3	V
				4.5V < V_{CC} < 5.5V	1.4		3	
			V_I = 0V, R_L = 45 Ω, S at 0V, See Figure 11, Figure 12, and Figure 13	4.75V < V_{CC} < 5.25V	1.4		3	
				4.5V < V_{CC} < 5.5V	1.3		3	
$V_{OD(R)}$	Differential output voltage (Recessive)		V_I = 3V, S at 0V, See Figure 11 and Figure 12		–0.012		0.012	V
			V_I = 3V, S at 0V, No Load		–0.5		0.05	
$V_{OC(ss)}$	Steady state common-mode output voltage		S at 0V, Figure 18	4.75V < V_{CC} < 5.25V	2	2.3	3	V
				4.5V < V_{CC} < 5.5V	1.9		3	
$\Delta V_{OC(ss)}$	Change in steady-state common-mode output voltage					30		mV
I_{IH}	High-level input current, TXD input		V_I at V_{CC}		–2		2	µA
I_{IL}	Low-level input current, TXD input		V_I at 0V		–50		–10	
$I_{O(off)}$	Power-off TXD output current		V_{CC} at 0V, TXD at 5V				1	
$I_{OS(ss)}$	Short-circuit steady-state output current		V_{CANH} = -12V, CANL Open, See Figure 21		–105	–72		mA
			V_{CANH} = 12V, CANL Open, SeeFigure 21			0.36	1	
			V_{CANL} = -12V, CANH Open, See Figure 21		–1	–0.5		
			V_{CANL} = 12V , CANH Open, See Figure 21			71	105	
C_O	Output capacitance		See receiver input capacitance					

(1) All typical values are at 25°C with a 5-V supply.

7.6 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	S at 0V, See Table 1			800	900	mV
V_{IT-}	Negative-going input threshold voltage			500	650		
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			100	125		
V_{OH}	High-level output voltage	I_O = –2 mA, See Figure 16	4.75V < V_{CC} < 5.25V	4	4.6		V
			4.5V < V_{CC} < 5.5V	3.8			
V_{OL}	Low-level output voltage	I_O = 2 mA, See Figure 16			0.2	0.4	V
$I_{I(off)}$	Power-off bus input current	CANH or CANL = 5V, Other pin at 0V, V_{CC} at 0V, TXD at 0V			165	250	µA
$I_{O(off)}$	Power-off RXD leakage current	V_{CC} at 0V, RXD at 5V				20	µA
C_I	Input capacitance to ground, (CANH or CANL)	TXD at 3V, V_I = 0.4 sin (4E6πt) + 2.5V			13		pF
C_{ID}	Differential input capacitance	TXD at 3V, V_I = 0.4 sin (4E6πt)			5		
R_{ID}	Differential input resistance	TXD at 3V, S at 0V		30		80	kΩ
R_{IN}	Input resistance, (CANH or CANL)			15	30	40	
$R_{I(m)}$	Input resistance matching [1 – ($R_{IN\ (CANH)}$ / $R_{IN\ (CANL)}$)] x 100%	$V_{(CANH)}$ = $V_{(CANL)}$		–3%	0%	3%	

(1) All typical values are at 25°C with a 5-V supply.

7.7 Device Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(LOOP1)}$	Total loop delay, driver input to receiver output, recessive to dominant	Figure 19, S at 0V	4.75V < V_{CC} < 5.25V	90		190	ns
			4.5V < V_{CC} < 5.5V	85		195	
$t_{d(LOOP2)}$	Total loop delay, driver input to receiver output, dominant to recessive		4.75V < V_{CC} < 5.25V	90		190	
			4.5V < V_{CC} < 5.5V	85		195	

7.8 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	S at 0V, See Figure 14		25	65	120	ns
t_{PHL}	Propagation delay time, high-to-low-level output			25	45	90	
t_r	Differential output signal rise time				25		
t_f	Differential output signal fall time				50		
t_{en}	Enable time from silent mode to dominant	See Figure 17				1	µs
$t_{(dom)}$	Dominant time-out	↓V_I, See Figure 20	4.75V < V_{CC} < 5.25V	300	450	700	µs
			4.5V < V_{CC} < 5.5V	280		700	

7.9 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	S at 0V or V_{CC}, See Figure 16	4.75V < V_{CC} < 5.25V	60	100	130	ns
			4.5V < V_{CC} < 5.5V	60		135	
t_{PHL}	Propagation delay time, high-to-low-level output		4.75V < V_{CC} < 5.25V	45	70	90	
			4.5V < V_{CC} < 5.5V	45		95	
t_r	Output signal rise time				8		
t_f	Output signal fall time				8		

7.10 Supply Current

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	5-V Supply current	Silent mode	S at V_{CC}, V_I = V_{CC}			6	10	mA
		Dominant	V_I = 0V, 60 Ω Load, S at 0V	4.75V < V_{CC} < 5.25V		50	70	
				4.5V < V_{CC} < 5.5V			75	
		Recessive	V_I = V_{CC}, No Load, S at 0V			6	10	

7.11 S-Pin Characteristics

over recommended operating conditiions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High level input current	S at 2V	20	40	70	μA
I_{IL}	Low level input current	S at 0.8V	5	20	30	

7.12 VREF-Pin Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Reference output voltage	–50 μA < I_O < 50 μA	0.4V_{CC}	0.5V_{CC}	0.6V_{CC}	V

8 Parameter Measurement Information

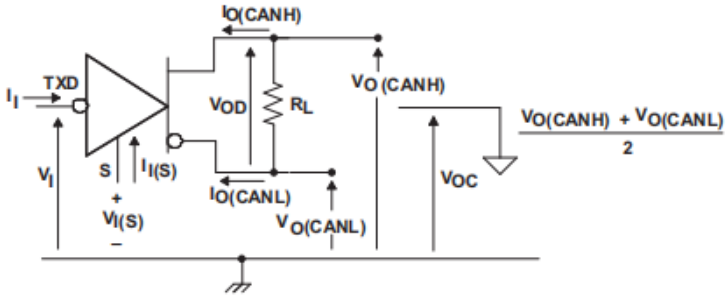


Figure 11. Driver Voltage, Current, and Test Definition

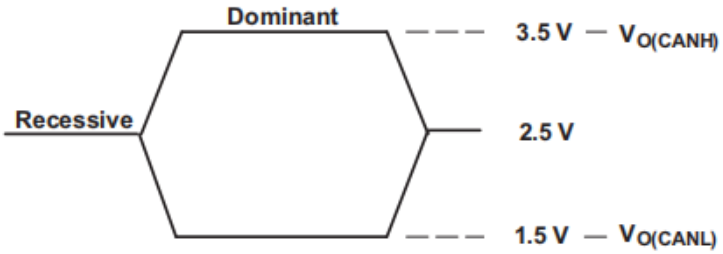


Figure 12. Bus Logic State Voltage Definitions

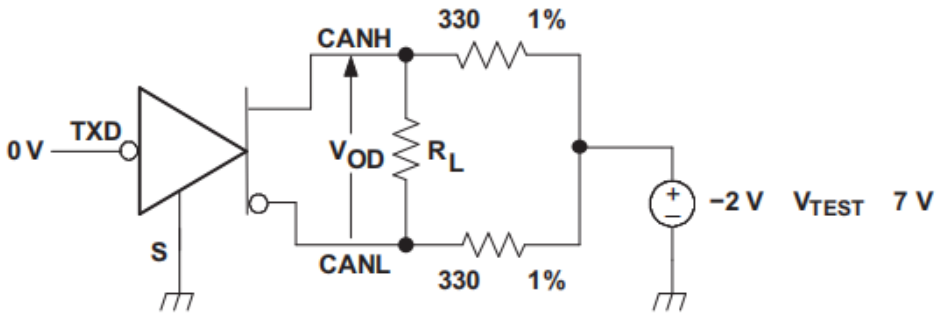


Figure 13. Driver V_{OD} Test Circuit

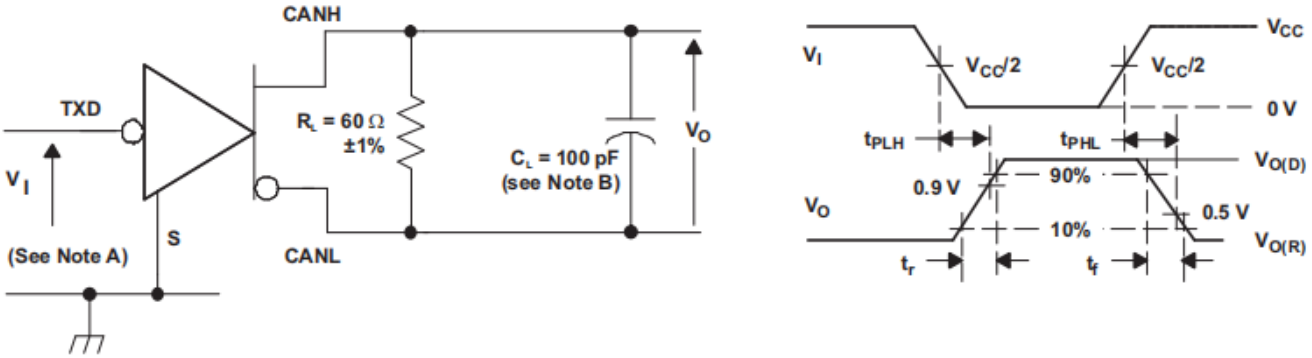


Figure 14. Driver Test Circuit and Voltage Waveforms

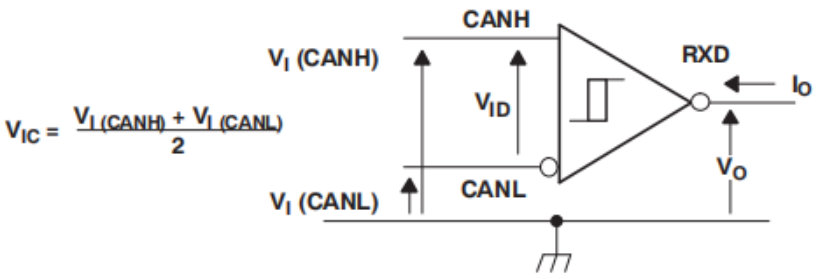
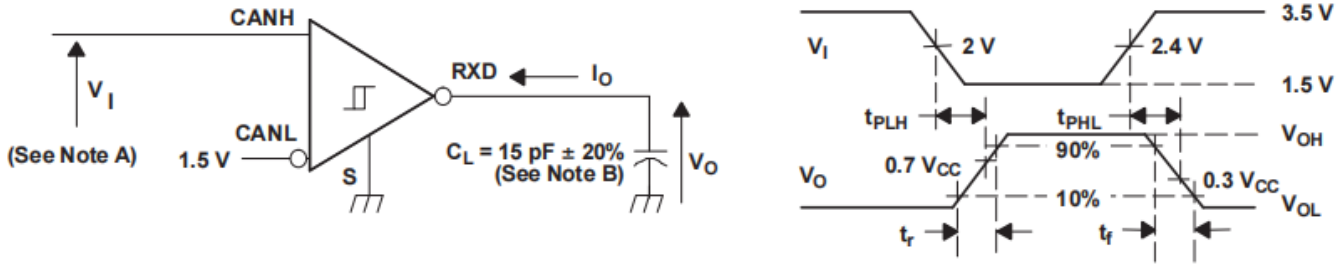


Figure 15. Receiver Voltage and Current Definitions

Parameter Measurement Information (continued)



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 16. Receiver Test Circuit and Voltage Waveforms

Table 1. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R	
–11.1V	–12V	900 mV	L	V_{OL}
12V	11.1V	900 mV	L	
–6V	–12V	6V	L	
12V	6V	6V	L	
–11.5V	–12V	500 mV	H	V_{OH}
12V	11.5V	500 mV	H	
–12V	–6V	6V	H	
6V	12V	6V	H	
Open	Open	X	H	

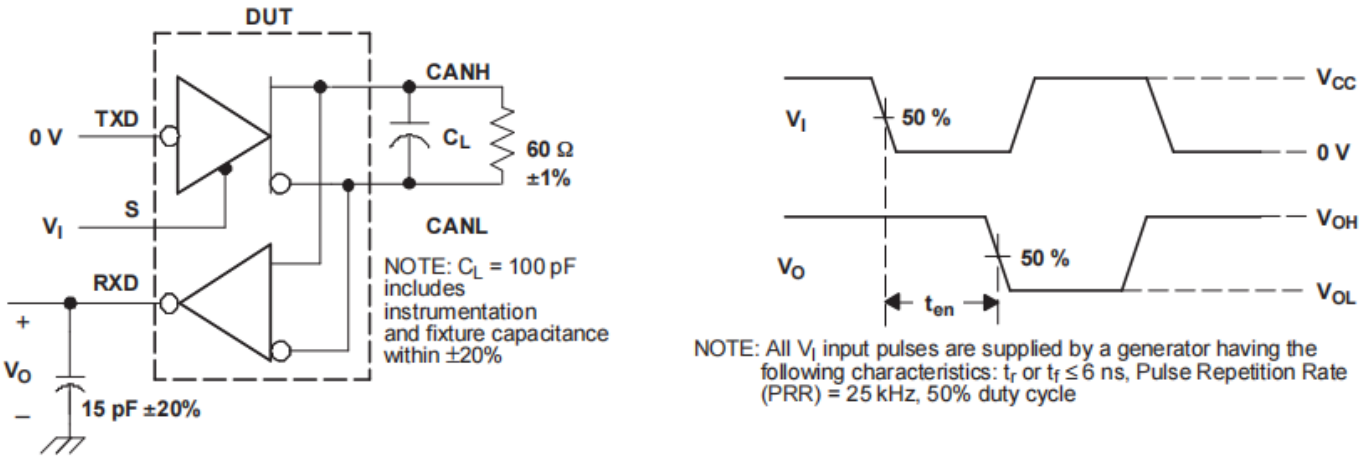
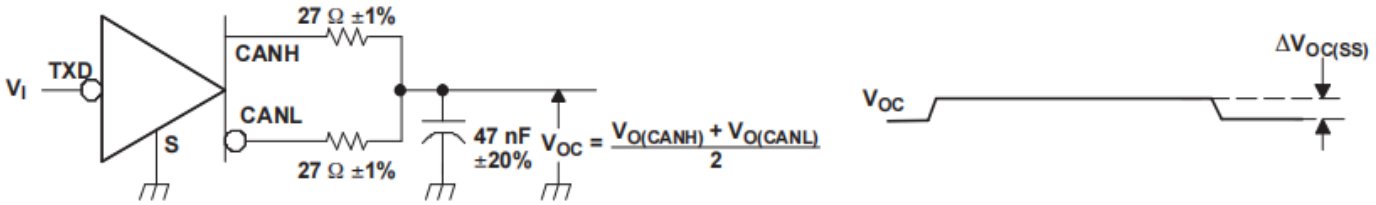
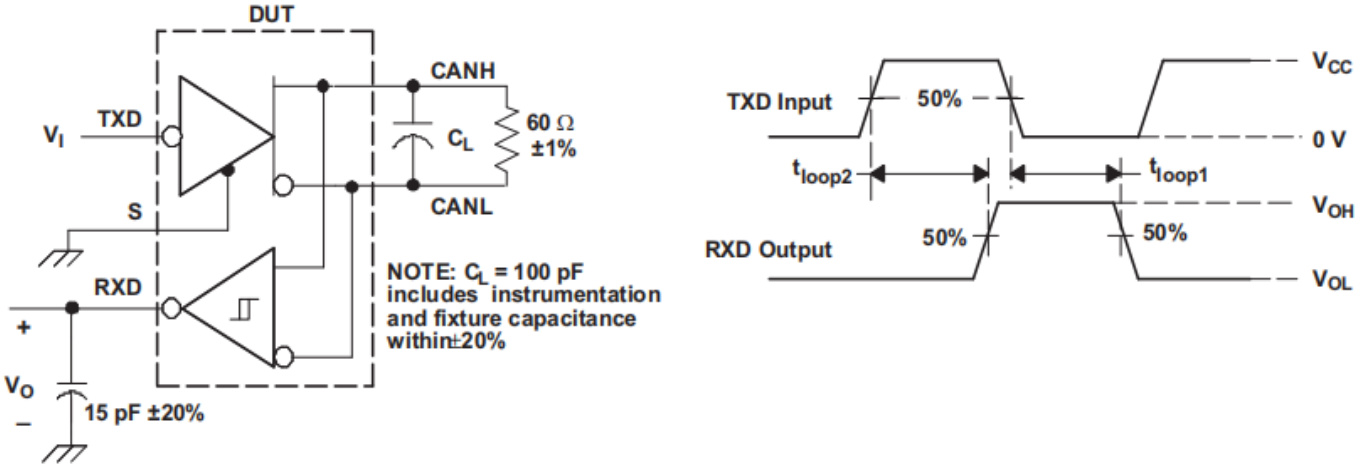


Figure 17. T_{EN} Test Circuit and Waveform



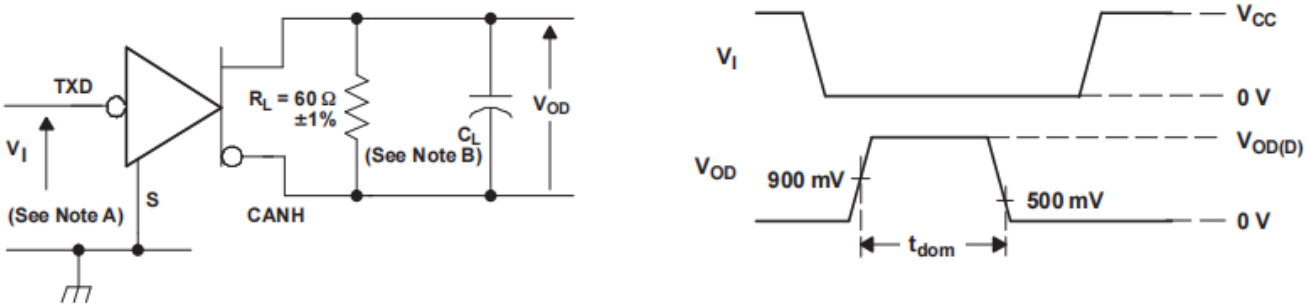
NOTE: All V_I input pulses are from 0V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 18. Common Mode Output Voltage Test and Waveforms



A. All V_I input pulses are from 0V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 19. $T_{(LOOP)}$ Test Circuit and Waveform



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 500 Hz, 50% duty cycle.

B. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

Figure 20. Dominant Time-Out Test Circuit and Waveforms

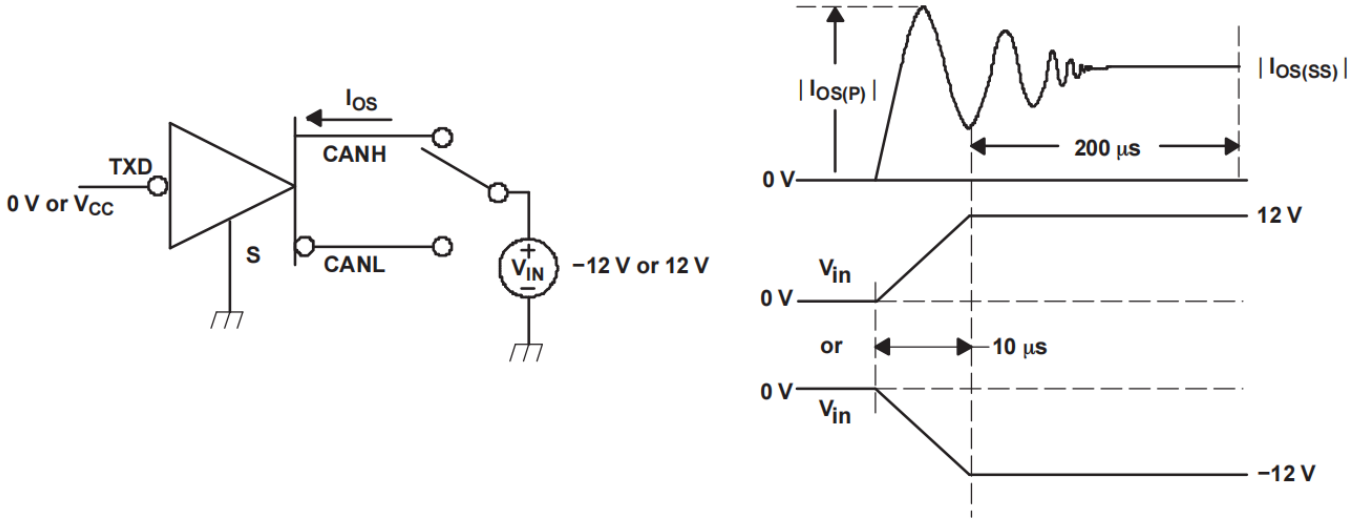


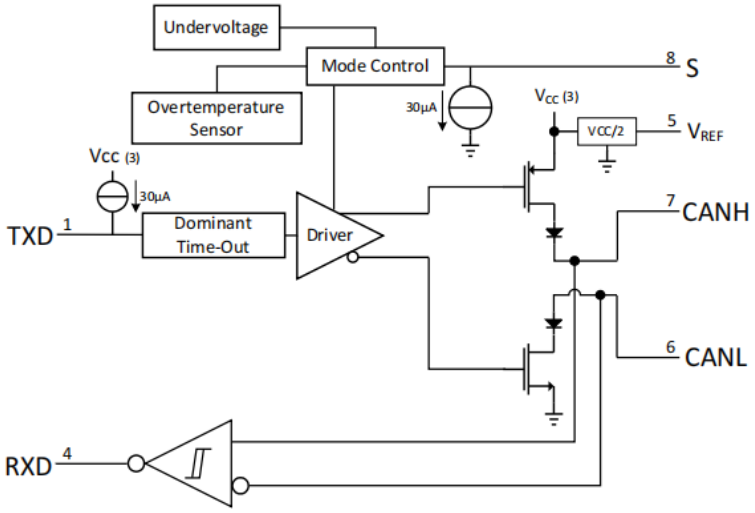
Figure 21. Driver Short-Circuit Current Test and Waveform

9 Detailed Description

9.1 Overview

The SN65HVD1050 CAN tranceivers is compatible with the ISO1189-2 High Speed CAN (Controller Area Network) physical layer standard. It is designed to interface between the differential bus lines in controller area network and the CAN protocol controller at data rates up to 1 Mbps.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Mode Control

9.3.1.1 Normal Mode

Select the normal mode of the device operation by setting the S pin low. The CAN bus driver and receiver are fully operational and the CAN communication is bidirectional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD.

9.3.3 Thermal Shutdown

The SN65HVD1050 has a thermal shutdown feature that turns off the driver outputs when the junction temperature nears 190°C. This shutdown prevents catastrophic failure from bus shorts, but does not protect the circuit from possible damage. The user should strive to maintain recommended operating conditions and not exceed absolute-maximum ratings at all times. If an SN65HVD1050 is subjected to many, or long-duration faults that can put the device into thermal shutdown, it should be replaced.

9.3.4 V_{REF}

A reference voltage of $V_{CC}/2$ is available through the V_{REF} output pin. The V_{REF} voltage should be tied to the common mode point in a split termination network to help stabilize the output common mode voltage. See Figure 27 for more application specific information on properly terminating the CAN bus.

If the V_{REF} output pin is not used it can be left floating.

9.3.5 Operating Temperature Range

The SN65HVD1050 is characterized for operation from –40°C to 125°C.

9.4 Device Functional Modes

Table 2. Driver

INPUTS		OUTPUTS		BUS STATE
TXD(1)	S(1)	CANH(1)	CANL(1)	
L	L or Open	H	L	DOMINANT
H	X	Z	Z	RECESSIVE
Open	X	Z	Z	RECESSIVE
X	H	Z	Z	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

Table 3. Receiver

DIFFERENTIAL INPUTS V_{ID} = V(CANH) – V(CANL)	OUTPUT RXD(1)	BUS STATE
$V_{ID} \geq 0.9V$	L	DOMINANT
$0.5V < V_{ID} < 0.9V$	?	?
$V_{ID} \leq 0.5V$	H	RECESSIVE
Open	H	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

Table 4. Parametric Cross Reference With the TJA1050

TJA1050[1]	PARAMETER	HVD1050
TRANSMITTER SECTION		
V_{IH}	High-level input voltage	Recommended V_{IH}
V_{IL}	Low-level input voltage	Recommended V_{IL}
I_{IH}	High-level input current	Driver I_{IH}
I_{IL}	Low-level input current	Driver I_{IL}
BUS SECTION		
I_{LI}	Power-off bus input current	Receiver $I_{I(off)}$
$I_{O(SC)}$	Short-circuit output current	Driver $I_{OS(SS)}$
$V_{O(dom)}$	Dominant output voltage	Driver $V_{O(D)}$
$V_{i(dif)(th)}$	Differential input voltage	Receiver V_{IT} and recommended V_{ID}
$V_{i(dif)(hys)}$	Diffrential input hysteresis	Receiver V_{hys}
$V_{O(reces)}$	Recessive output voltage	Driver $V_{O(R)}$
$V_{O(dif)(bus)}$	Differential bus voltage	Driver $V_{OD(D)}$ and $V_{OD(R)}$
$R_{i(cm)}$	CANH, CANL input resistance	Receiver R_{IN}
$R_{i(dif)}$	Differential input resistance	Receiver R_{ID}
$R_{i(cm)(m)}$	Input resistance matching	Receiver $R_{I\ (m)}$
C_i	Input capacitance to ground	Receiver C_I
$C_{i(dif)}$	Differential input capacitance	Receiver C_{ID}
RECEIVER SECTION		
I_{OH}	High-level output current	Recommended I_{OH}
I_{OL}	Low-level output current	Recommended I_{OL}
Vref PIN SECTION		
V_{ref}	Reference output voltage	V_O
TIMING SECTION		
$t_{d(TXD-BUSon)}$	Delay TXD to bus active	Driver t_{PLH}
$t_{d(TXD-BUSoff)}$	Delay TXD to bus inactive	Driver t_{PHL}
$t_{d(BUSon-RXD)}$	Delay bus active to RXD	Receiver t_{PHL}
$t_{d(BUSoff-RXD)}$	Delay bus inactive to RXD	Receiver t_{PLH}
	$t_{d(TXD-BUSon)} + t_{d(BUSon-RXD)}$	Device t_{LOOP1}
	$t_{d(TXD-BUSoff)} + t_{d(BUSoff-RXD)}$	Device t_{LOOP2}
$t_{dom(TXD)}$	Dominant time out	Driver $t_{(dom)}$
S PIN SECTION		
V_{IH}	High-level input voltage	Recommended V_{IH}
V_{IL}	Low-level input voltage	Recommended V_{IL}
I_{IH}	High-level input current	I_{IH}
I_{IL}	Low-level input current	I_{IL}

(1) From TJA1050 Product Specification, Philips Semiconductors, 2002 May 16.

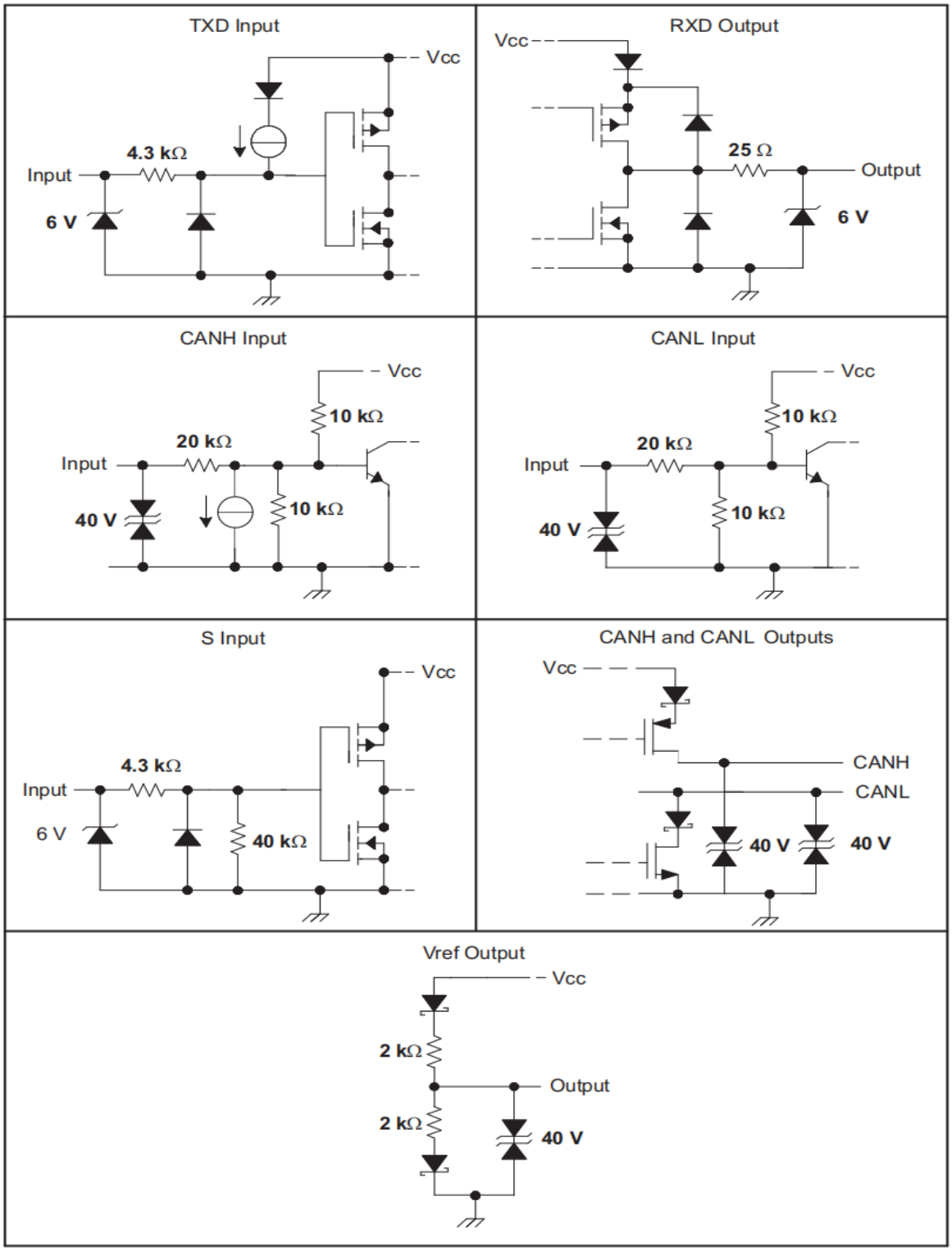
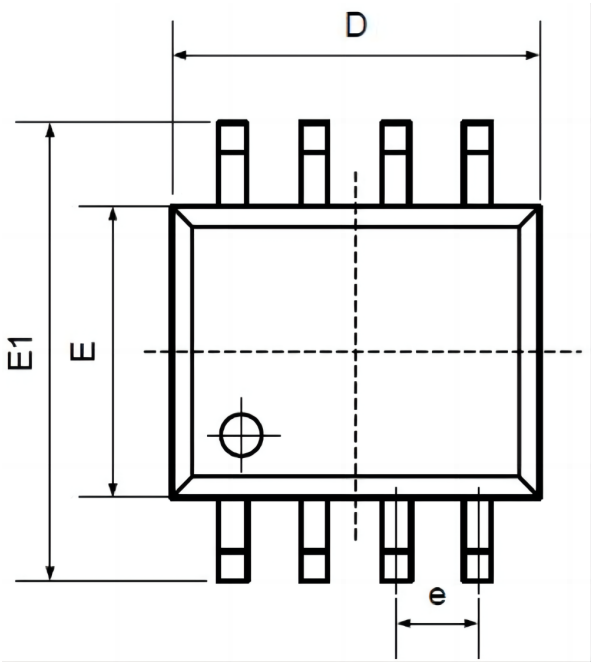


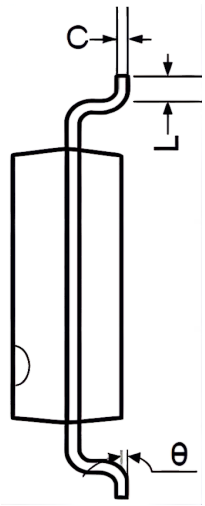
Figure 22. Equivalent Input and Output Schematic Diagrams

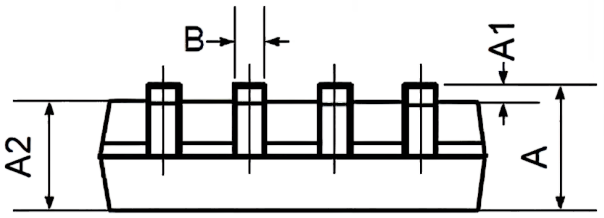
Order information

Order Number	Package	Package Quantity	Marking On The park
SN65HVD1050DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD1050DR

Package SOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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