1A Low-Dropout Linear Regulator

Features

- Input voltage range: 1.6V to 5.5V
- Fixed output of 0.8V, 1.2V, 1.8V, 3.0V, 3.3V
  Adjustable output of 0.8V~4.5V
- Rated output current: 1A,when V_{IN} - $V_{OUT(SET)}$>1V rated output current reduce to 750mA
- Quiescent current: typical 140μA
- Typical 0.3μA shutdown current
- Typical 141mV dropout voltage
  (I_{OUT}=1A, 3.3V output)
- Power supply rejection ratio: typical 70dB (I_{OUT}=30mA, freq=1kHz)
- Noise: typical 23μVrms (I_{OUT}=30mA, BW=10Hz to 100kHz)
- Built-in output short protection: typical 130mA when output short to ground
- Output auto discharge function version available
- DFN 1.6mm×1.2mm×0.37mm-8L package

Applications

Battery-powered equipment

Smart phone

Digital camera

STB

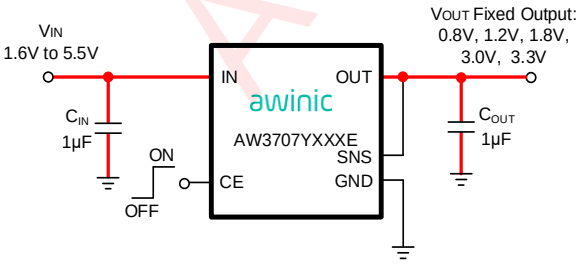
General Description

AW3707YXXXE is a low dropout voltage regulator featuring low ON resistance, high PSRR, low Noise, good load/line transient response and smooth soft-start.

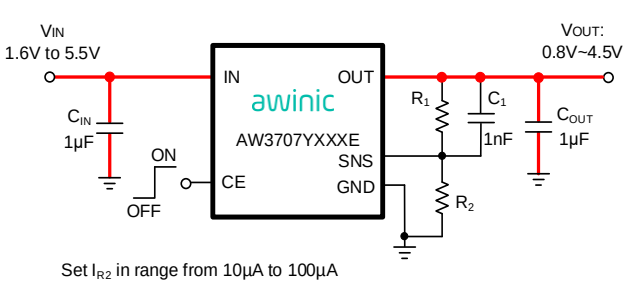
AW3707YXXXE integrates current limit, short circuit protection, thermal shutdown, sufficiently protecting IC from being damaged. Meanwhile AW3707YXXXE integrates a reverse current protection circuit.

AW3707YXXXE is designed to work with a 1μF or more input ceramic capacitor and a 1μF or more output ceramic capacitor. The low power dissipation and good dynamic response make AW3707YXXXE very suitable for hand-held communication equipment. Tiny package makes high density mounting of the IC on boards possible.

Typical Application Circuit



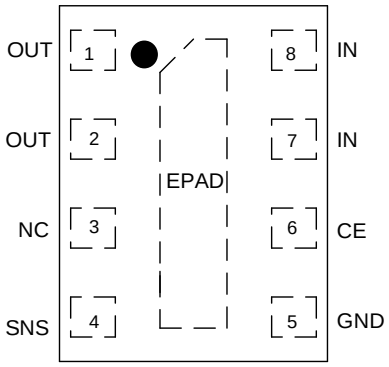
Fixed Output Voltage Application



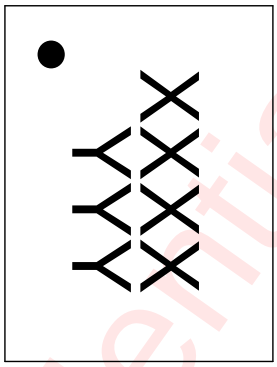
Adjustable Output Voltage Application

Pin Configuration and Top Mark

AW3707YXXXEDNR (Top View)



AW3707YXXXEDNR Marking (Top View)



XXXX - AW3707YXXXEDNR
YYY - Production Tracing Code

Pin Definition

No.	NAME	DESCRIPTION
1	OUT	Regulated output voltage pin. Put a 1μF or more ceramic capacitor at the output pin.
2	OUT	Regulated output voltage pin. Put a 1μF or more ceramic capacitor at the output pin.
3	NC	Not connect
4	SNS	Output voltage sense
5	GND	Ground.
6	CE	Chip enable pin. Built-in pull-down resistor. (High Active)
7	IN	Input supply pin. Put a 1μF or more bypass capacitor at the power supply.
8	IN	Input supply pin. Put a 1μF or more bypass capacitor at the power supply.
EPAD	EPAD	It's recommended to connect the EPAD to GND, but leaving it open is also acceptable.

Device Comparison Table

Part Number	$V_{OUT(SET)}$	Rated Current	CE Active	Auto Discharge
AW3707D080EDNR	0.8V or ADJ	1A	High	YES
AW3707D120EDNR	1.2V	1A	High	YES
AW3707D180EDNR	1.8V	1A	High	YES
AW3707D300EDNR	3.0V	1A	High	YES
AW3707D330EDNR	3.3V	1A	High	YES

Name Rule

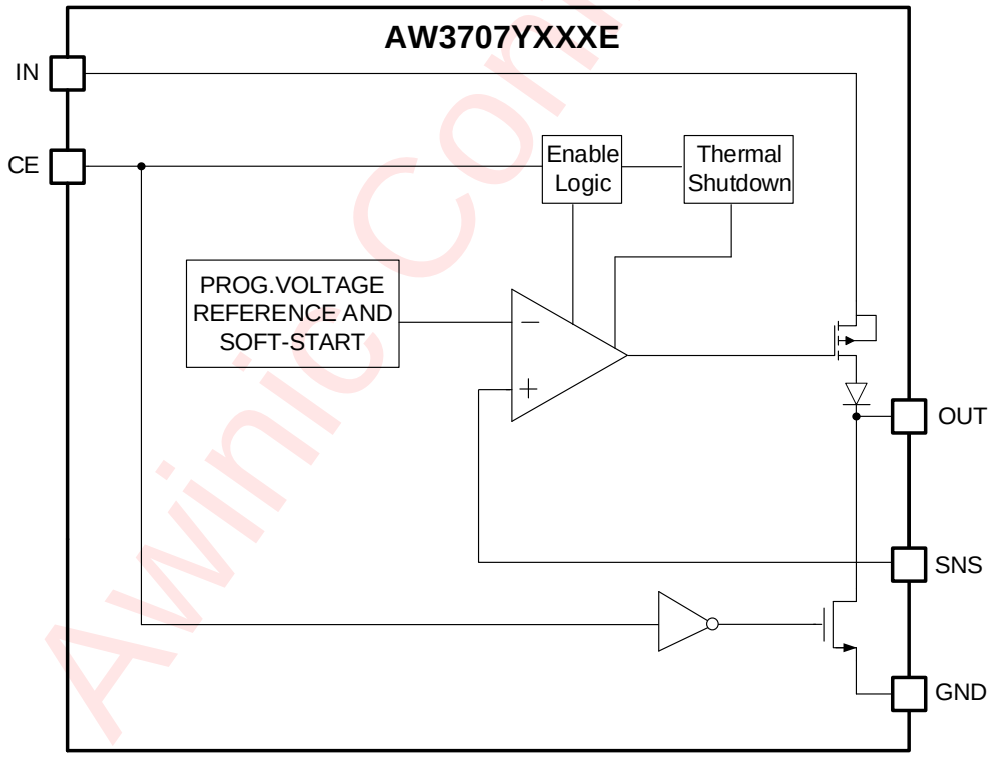
AW3707 Y XXX E ZZZ

Package
DNR: DFN 1.6mm×1.2mm×0.37mm-8L

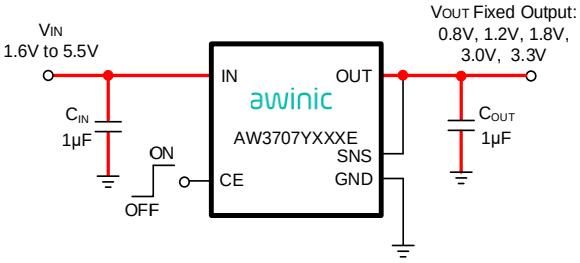
Output Voltage
E.g.
120: Output Voltage 1.2V

Auto-discharge Function
D: Available
B: Not available

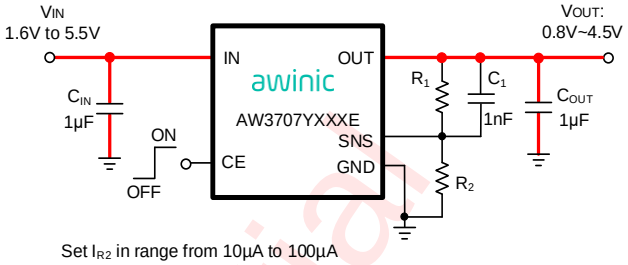
Functional Block Diagram



Typical Application Circuits



Fixed Output Voltage Application



Adjustable Output Voltage Application

Notice for typical application circuits:

Capacitance of C_{IN} and C_{OUT} should be 1μF or more.

The input and output capacitor must be located a distance of not more than 1 cm.

For adjustable output voltage application, V_{OUT_ADJ} =0.8 *(1+R_1/R_2), and set I_{R1}, I_{R2} in range from 10μA to 100μA for better performance.

For fixed output voltage application, the SNS pin should be connected to the OUT pin.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW3707D080EDNR	-40°C～125°C	DFN 1.6mm×1.2mm -8L	653G	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW3707D120EDNR	-40°C～125°C	DFN 1.6mm×1.2mm -8L	EH9G	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW3707D180EDNR	-40°C～125°C	DFN 1.6mm×1.2mm -8L	DC8N	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW3707D300EDNR	-40°C～125°C	DFN 1.6mm×1.2mm -8L	TQ34	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW3707D330EDNR	-40°C ~ 125°C	DFN 1.6mm×1.2mm -8L	P9B0	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS	RANGE
Input voltage range V_{BUS}	-0.3V to 6.5V
Enable control voltage range	-0.3V to 6.5V
Output voltage range	-0.3V to 6.5V
Junction-to-ambient thermal resistance θ_{JA} (NOTE2)	144°C/W
Operating free-air temperature range	-40°C to 125°C
Maximum operating junction temperature T_{JMAX}	150°C
Recommended operating junction temperature T_{J_REC}	-40°C to 125°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD	
HBM (Human body model)(NOTE3)	±2kV
CDM(Charged device model) (NOTE4)	±1.5kV
Latch-Up	
Latch-Up(NOTE5)	+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Thermal resistance from junction to ambient is highly dependent on PCB layout.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS-001-2017.

NOTE4: All pins. Test Condition: ESDA/JEDEC JS-002-2018.

NOTE5: Test Condition: JESD78E.

Electrical Characteristics

V_{IN}=$V_{OUT(SET)}$+1V, V_{CE}>1V, I_{OUT}=1mA, C_{IN}=C_{OUT}=1μF, T_A=25°C (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range			1.6		5.5	V
V_{OUT_ACC}	Output Voltage Accuracy			-1		1	%
V_{SNS}	Output Sense Voltage Range			0.792	0.8	0.808	V
$LOAD_{Reg}$	Load Regulation	1 mA≤ I_{OUT} ≤1A			6	30	mV
$LINE_{Reg}$	Line Regulation	$V_{OUT(SET)}$+0.5V≤ V_{IN} ≤5.5V			2	10	mV
$V_{dropout}$	Dropout Voltage	I_{OUT}=1A,When V_{OUT} falls below $V_{OUT(SET)}$*98%	$V_{OUT(SET)}$=0.8V		948		mV
			$V_{OUT(SET)}$=1.2V		609		
			$V_{OUT(SET)}$=3.3V		141		
I_{SD}	Shutdown Current	V_{CE}<0.4V			0.3	1	μA
I_Q	Quiescent Current	I_{OUT}=0mA			140		μA
V_{CEH}	CE Input Voltage “H”	-40°C ≤ T_A ≤125°C		1			V
V_{CEL}	CE Input Voltage “L”	-40°C ≤ T_A ≤125°C				0.4	V
PSRR		I_{OUT}=30mA, f=1kHz			70		dB
V_N	Output Voltage Noise	I_{OUT}=30mA, BW=10Hz to 100kHz			23		μVrms
I_{CL}	Output Current Limit	V_{OUT}=90%*$V_{OUT(SET)}$		1			A
I_{SC}	Short Current Limit	V_{OUT} < 250mV			130		mA
VTC	Output Voltage Temperature Coefficient	-40°C ≤ T_A ≤125°C			±80		ppm/°C
R_{DISC}	Auto Discharge Resistance	V_{CE}<0.4V, V_{IN}=2.8V			66		Ω
R_{CE}	CE Pull Down Resistance				4.5		MΩ
T_{SDH}		Temperature Rising			165		°C
T_{SDL}		Temperature Falling			135		°C
I_{REV}	Reverse Current	$V_{OUT(SET)}$ =3.3V, V_{OUT}=$V_{OUT(SET)}$+1V, 0≤ V_{IN} ≤V_{OUT}			0.7		μA
V_{REV_DET}	Detection Offset Voltage in Reverse Current Protection Mode	V_{OUT}≥0.7V, 0≤ V_{IN} ≤5.5V V_{REV_DET} = V_{OUT} - V_{IN}			30		mV
V_{REV_REL}	Release Offset Voltage in Reverse Current Protection Mode				20		mV

Typical Characteristics

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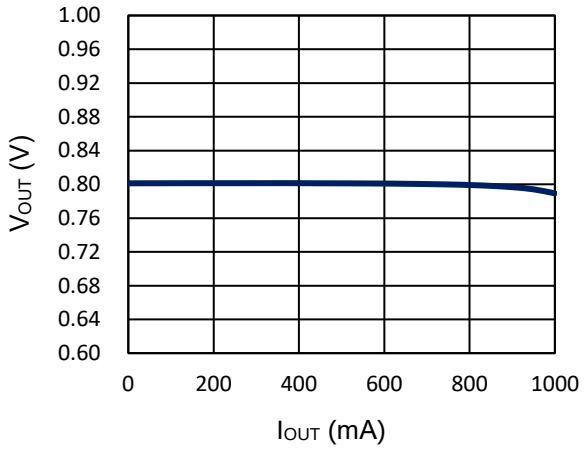

Output Voltage vs Output Current

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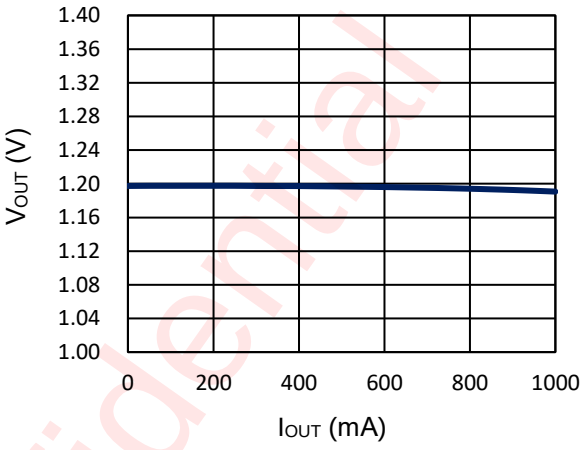

Output Voltage vs Output Current

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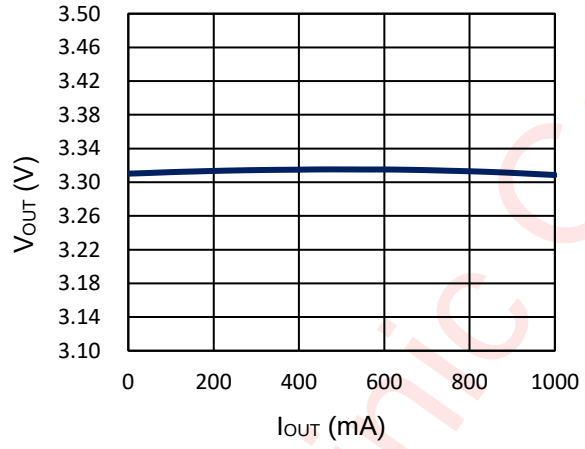

Output Voltage vs Output Current

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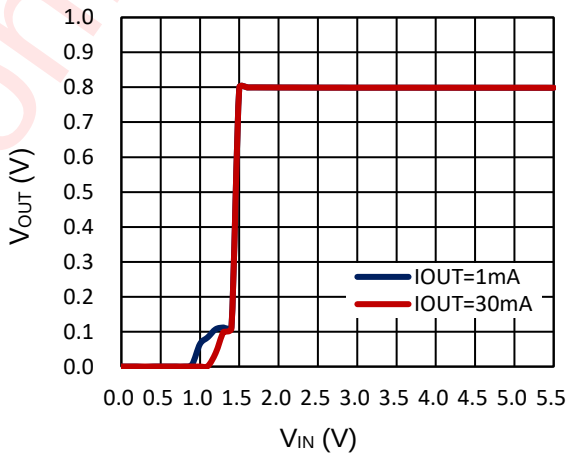

Output Voltage vs Input Voltage

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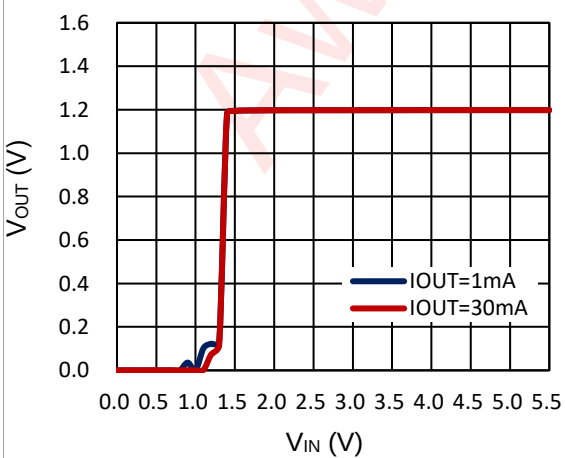

Output Voltage vs Input Voltage

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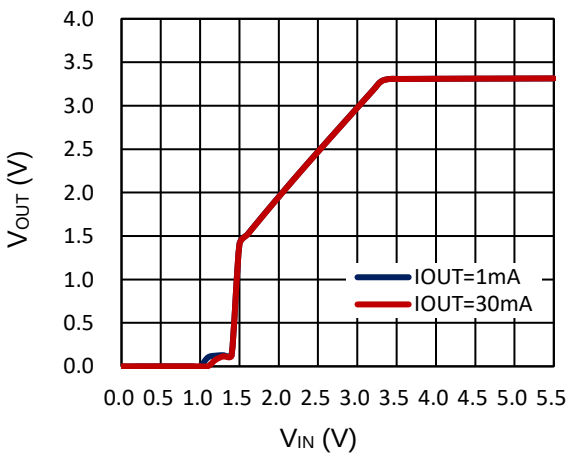

Output Voltage vs Input Voltage

Typical Characteristics (Continued)

$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25°C$, in Typical Application Circuit, unless otherwise noted.

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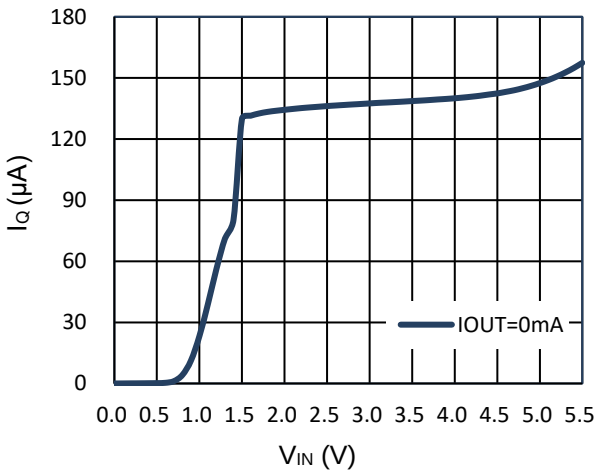

Quiescent Current vs Input Voltage

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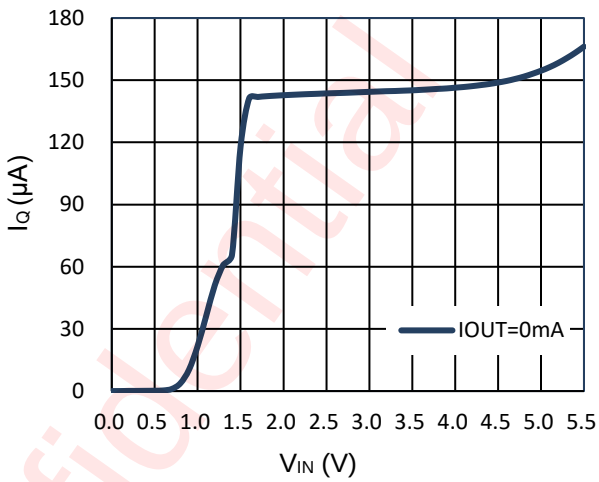

Quiescent Current vs Input Voltage

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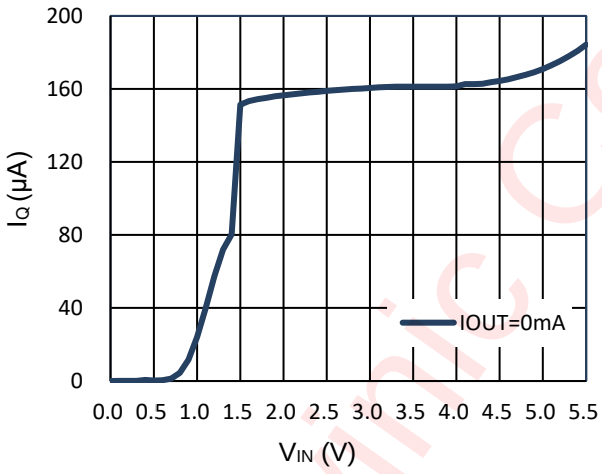

Quiescent Current vs Input Voltage

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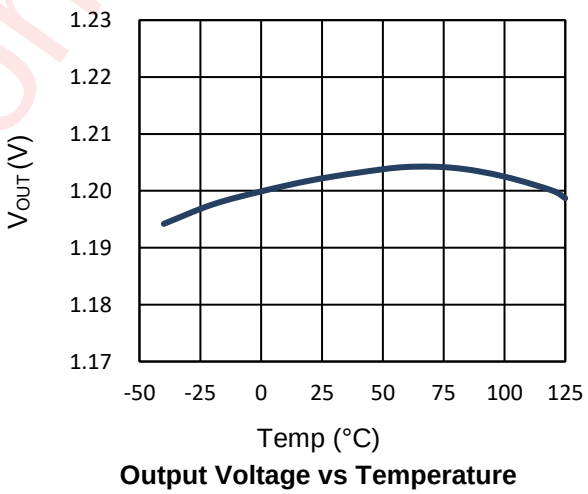

Output Voltage vs Temperature

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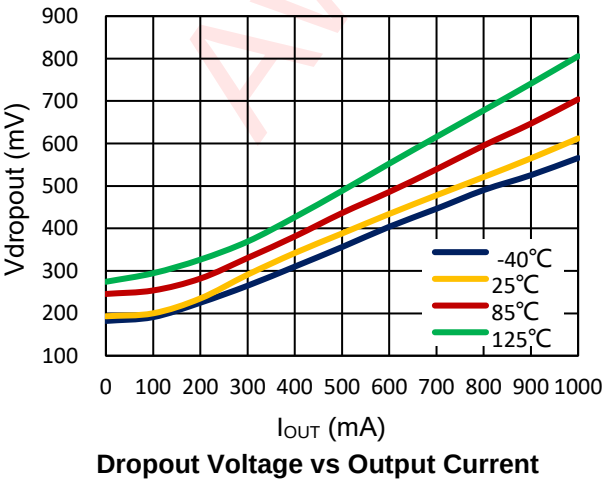

Dropout Voltage vs Output Current

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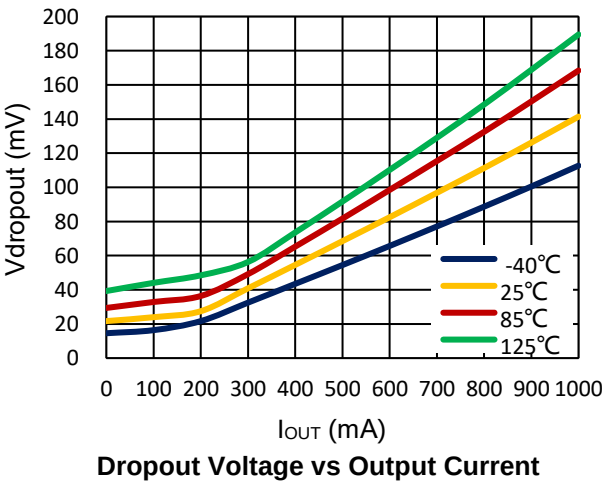

Dropout Voltage vs Output Current

Typical Characteristics (Continued)

$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25°C$, in Typical Application Circuit, unless otherwise noted.

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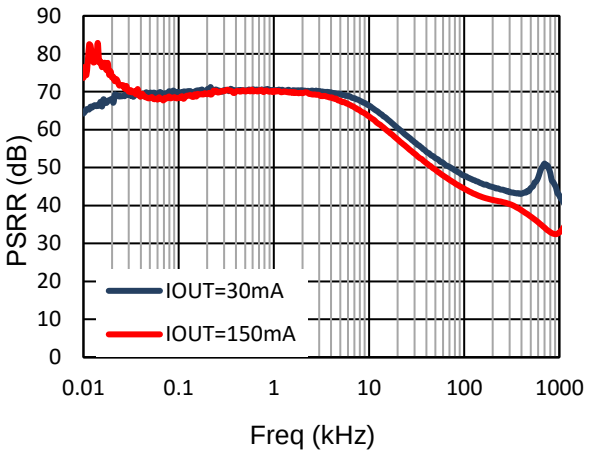

PSRR vs Frequency

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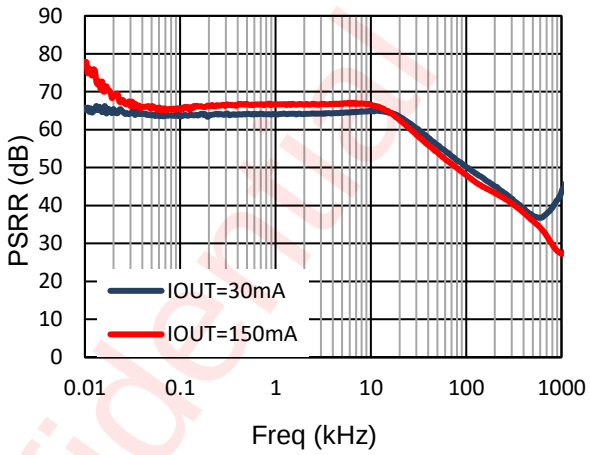

PSRR vs Frequency

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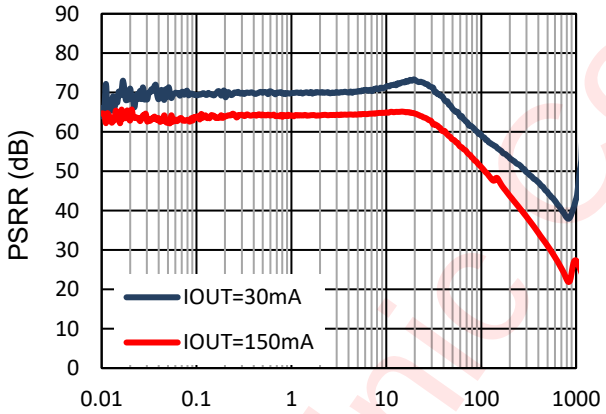

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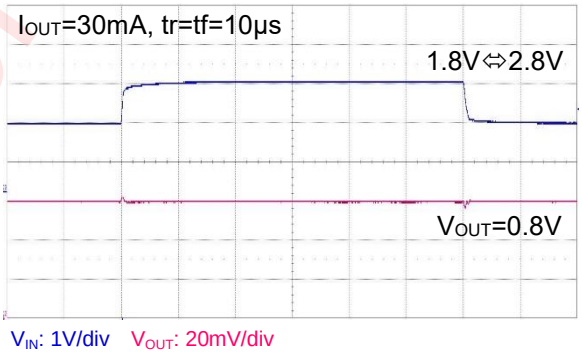

Time(50μs/div)

Input Transient Response

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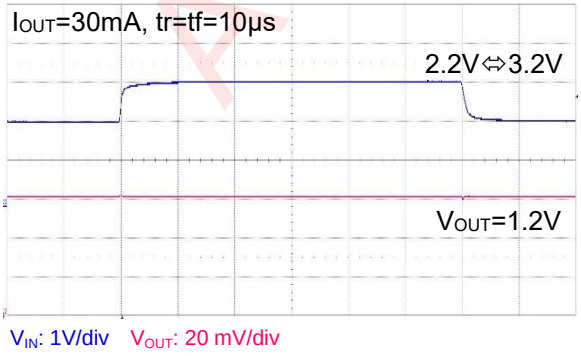

Time(50μs/div)

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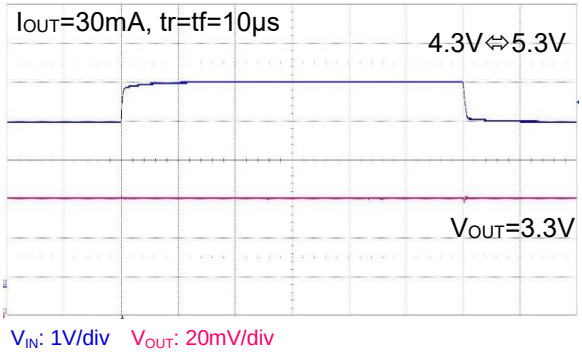

Time(50μs/div)

Input Transient Response

Typical Characteristics (Continued)

V_{IN}=$V_{OUT(SET)}$+1V, V_{CE}>1V, I_{OUT}=1mA, C_{IN}=C_{OUT}=1μF, T_A=25°C, in Typical Application Circuit, unless otherwise noted.

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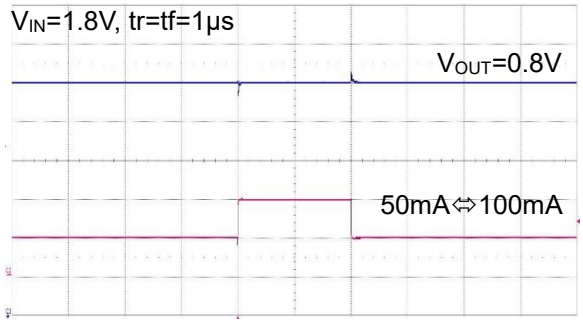

Time(50μs/div)

Load Transient Response

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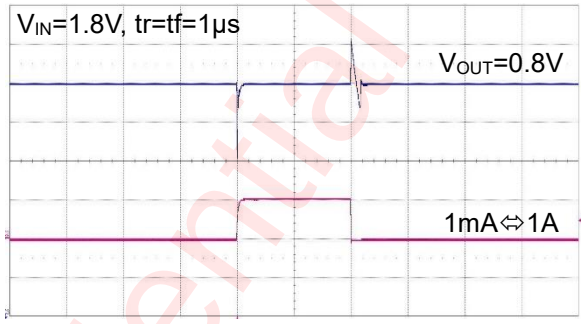

Time(50μs/div)

Load Transient Response

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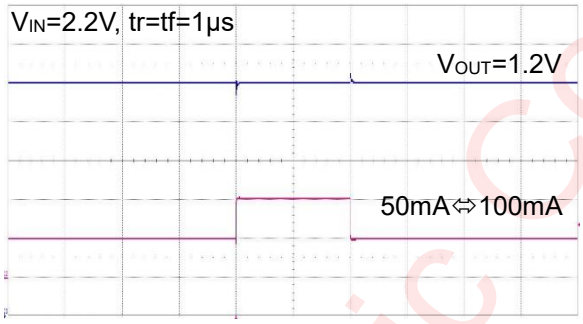

Time(50μs/div)

Load Transient Response

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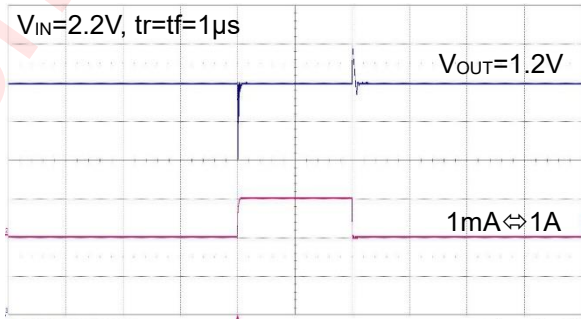

Time(50μs/div)

Load Transient Response

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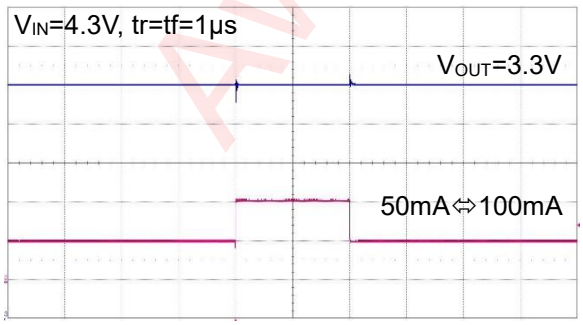

Time(50μs/div)

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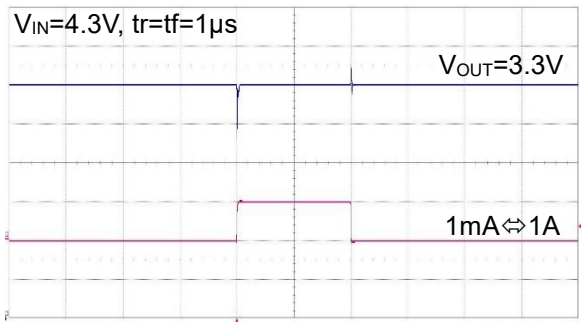

Time(50μs/div)

Load Transient Response

Typical Characteristics (Continued)

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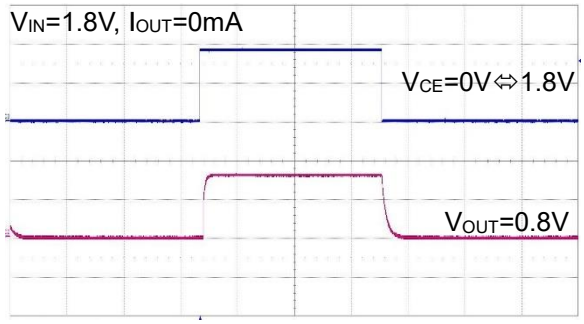
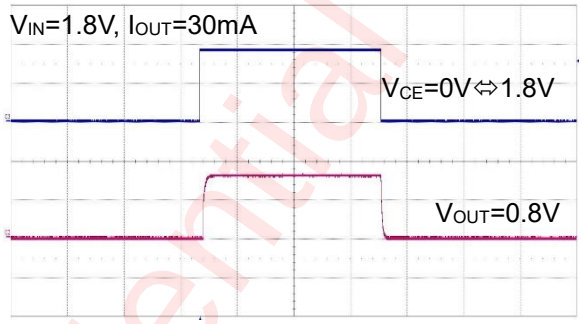


Turn On & Off Speed with CE pin

AW3707D080E



Turn On & Off Speed with CE pin

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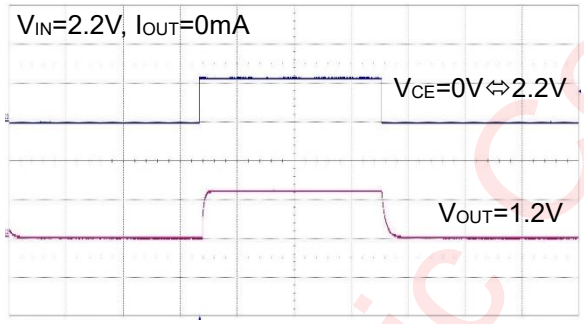

Turn On & Off Speed with CE pin

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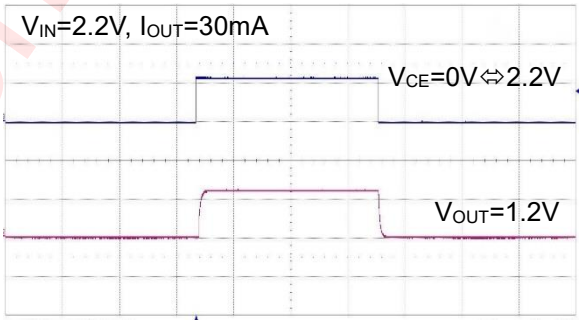
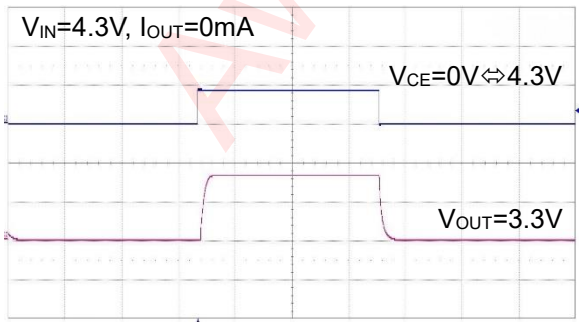


Turn On & Off Speed with CE pin

AW3707D330E



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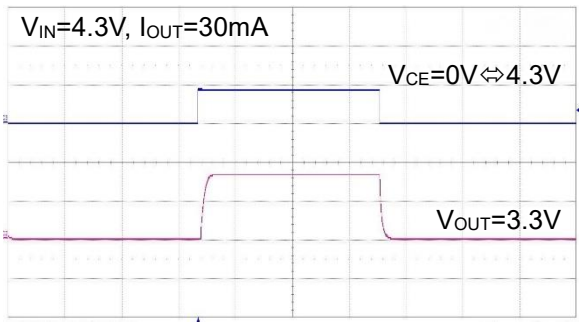


Turn On & Off Speed with CE pin

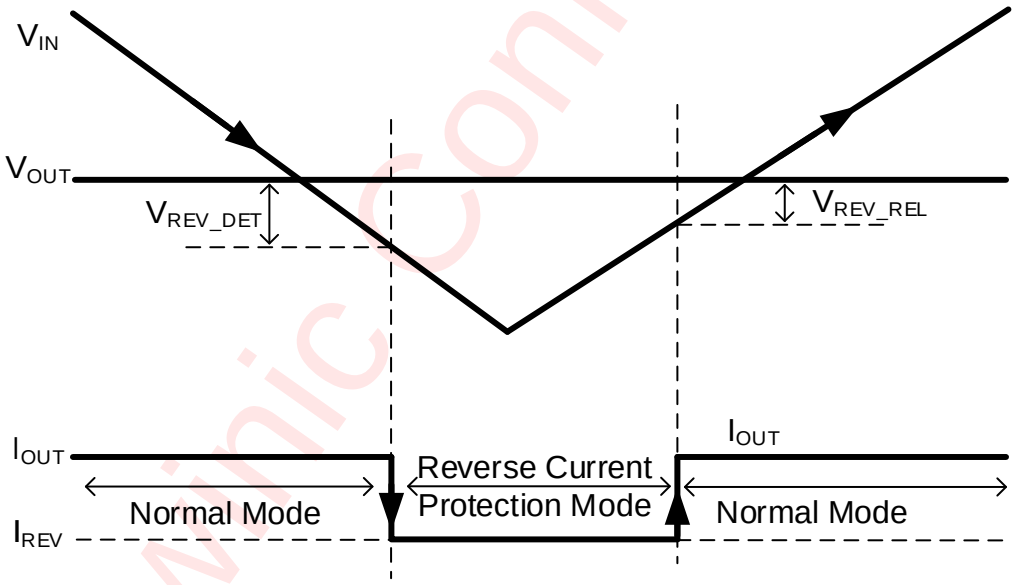
Detailed Functional Description

AW3707YXXXE is a low dropout voltage regulator. After powered on, with CE pin assertion, feedback voltage and a voltage related to the voltage reference are transmit to positive input terminal and negative input terminal of an error amplifier (EA) respectively. The output signal of EA is used to control the open-state of power MOSFET. After soft-start, feedback voltage signal compares with the established reference voltage, making output voltage stable and accurate.

Reverse Current Protection Circuit

Usually, the LDO using PMOS output transistor contains a parasitic diode between V_{IN} pin and V_{OUT} pin. Therefore, if V_{OUT} is higher than V_{IN}, the parasitic diode becomes forward direction. As a result, the current flows from OUT pin to IN pin. The AW3707YXXXE integrates a reverse current protection circuit, which stops the reverse current from OUT pin to IN pin when V_{OUT} becomes higher than V_{IN}.

Following figure shows the principle of each mode. When giving OUT pin a constant voltage and decreasing the IN voltage . When the IN voltage become lower than V_{OUT}-V_{REV_DET}, the reverse current protection starts to function to stop the load current. By increasing the IN voltage higher than V_{OUT}-V_{REV_REL}, the protection mode will be released to let the load current to flow.



Enable Operation

AW3707YXXXE uses CE pin to realize enable operation. Applying proper value of voltage to CE pin can make IC enable/disable.

If the voltage of CE pin is less than 0.4V, AW3707YXXXE is guaranteed to be disabled. In this state, function modules of IC and power MOSFET are turned off. And the auto discharge function is open making output discharge through a 66Ω resistor to Ground. In disable state, AW3707YXXXE only consumes a typical 0.3μA current.

If the voltage of CE pin is more than 1V, AW3707YXXXE is guaranteed to be enabled. In this state, the auto discharge MOSFET is closed, and AW3707YXXXE regulates output voltage to the designed value of voltage.

A 4.5MΩ resistor to Ground is built-in at CE pin, making sure that the IC is disabled when CE pin floats. If Enable function is not required, CE pin should be connected directly to IN pin.

Output Current Limit

AW3707YXXXE integrates output current limit function, protecting IC from excessive current . When the load is excessively heavy, AW3707YXXXE limits the current flowing through the IC to a typical value current which is about 50% more than the rated output current. This value is specially designed, so that IC is protected properly and the output capability is not influenced either.

Meanwhile, AW3707YXXXE integrates fold-back current limit function, lowering the system dissipation when output overload or short to ground.

Thermal Shutdown

AW3707YXXXE integrates thermal shutdown function, protect IC from excessively high temperature.

When the chip temperature exceeds 165°C, AW3707YXXXE detects it as an over-temperature event, triggering thermal shutdown, which will turn off the main function module, including power MOSFET. This inhibits increase of chip's temperature. IC would keep the protection-state on until the chip's temperature falls below to 135°C. At this moment, the over-temperature protection-state is released, IC resumes to work again .The hysteresis avoids IC's turning off and on frequently around the Thermal Shutdown threshold.

Auto Discharge

AW3707YXXXE makes output voltage decrease quickly when in disable state or thermal shutdown state, benefit from integrating auto discharge function.

Application Information

Power Dissipation and Device Operation

The permissible power dissipation is dependent on the ambient temperature T_A and the junction-to-ambient thermal resistance $R_{\Theta ja}$.

The absolute maximum allowable power dissipation for the device in a given package can be calculated using Equation below, where T_{J_MAX} = 150°C :

$$PD_{MAX\_ABS} = (T_{J\_MAX} - T_A) / R_{\Theta ja}$$

The recommended maximum allowable power dissipation for the device in a given package can be calculated using Equation below, where T_{J_REC} = 125°C :

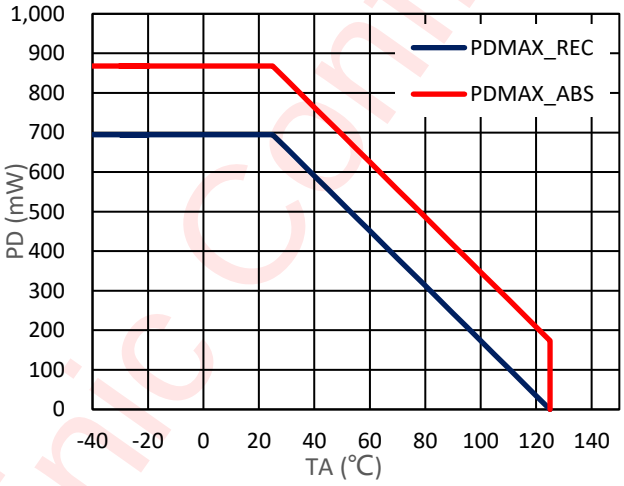
$$PD_{MAX\_REC} = (T_{J\_REC} - T_A) / R_{\Theta ja}$$

The actual power being dissipated in the device can be represented by Equation below:

$$PD_{ACT} = (V_{IN} - V_{OUT}) \times I_{OUT}$$

These equations above establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device.

The graphs of Power Dissipation vs. Ambient Temperature are showed below :



The above graphs show the maximum power dissipation of the respective package at T_{J_REC} = 125°C and T_{J_MAX} = 150°C. Operating the device in the region between PD_{MAX_REC} and PD_{MAX_ABS} might have a negative influence on its lifetime.

Capacitors Selection

IN pin: Input Capacitor C_{IN}

The input decoupling capacitor should be placed as close as possible to the IN pin for ensuring the device stability. 1μF or larger X5R or X7R ceramic capacitor is selected to get good dynamic performance.

When VIN is required to provide large current instantaneously, a large effective input capacitor is advised. Adding more input capacitors is available to restrict the ringing and to keep output voltage below the device absolute maximum ratings.

OUT pin: Output Capacitor C_{OUT}

AW3707YXXXE advises to use a 1μF or more X5R or X7R ceramic capacitor at OUT pin as shown in Typical Application Circuit.

Recommended Components List

Component	PART No.	DESCRIPTION	MFR	TYP.	UNIT
C_{IN}	GRM155R61A105KE15	10V, X5R, 0402	MURATA	1	μF
	CL05A105K05NNNC	16V, X5R, 0402	Samsung	1	
C_{OUT}	GRM155R61A105KE15	10V, X5R, 0402	MURATA	1	
	CL05A105K05NNNC	16V, X5R, 0402	Samsung	1	
	GRM155R61A225KE95	10V, X5R, 0402	MURATA	2.2	

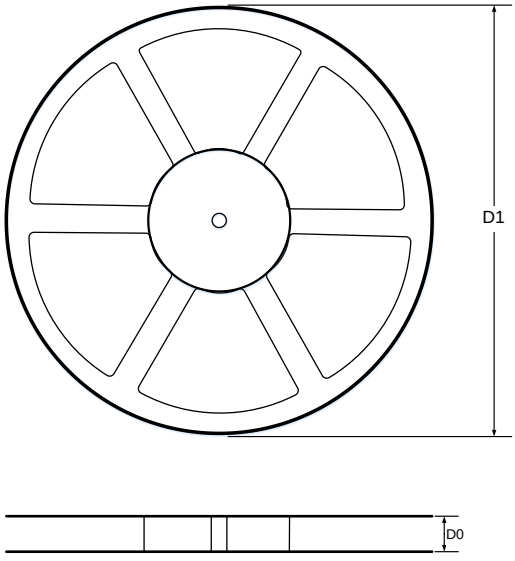
PCB Layout Consideration

The performance of a power source circuit using this device is highly dependent on a peripheral circuit. To obtain the optimal performance, A peripheral component or the device mounted on PCB should not exceed its rated voltage, rated current or rated power. When designing a peripheral circuit, guidelines below for PCB layout of AW3707YXXXE should be obeyed:

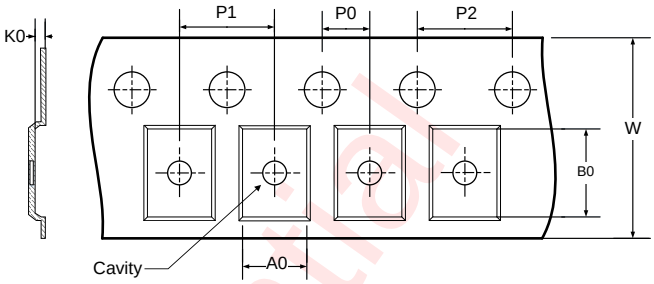
1. All peripheral components should be placed as close as possible to the device with shortest-distance wirings. Connect an input capacitor (C_{IN}) between the IN and GND pins with shortest-distance wiring. Avoid connecting device and chip pins with two different layers of copper, use the same layer of copper instead.
2. IN and OUT pin are the large current input and output of the chip, ensure the wirings are sufficiently robust make IN, OUT, and meanwhile GND lines sufficient.
3. The connection lines between the planes of C_{IN} or C_{OUT} and respective chip pin should be as short and wide as possible, to reduce noise and EMI interference. If the impedance of wiring between the IN, OUT and GND pins is high, it may cause noise pickup or unstable operation.
4. Connect an output capacitor (C_{OUT}) between the OUT and GND pins with shortest-distance wiring.
5. It's recommended to connect the EPAD to GND substantial , and GND pin must be connected to the large-area ground layer of PCB directly, meanwhile place sufficient vias below the exposed plane. Thus we can decrease the thermal resistor on the board to optimize heat-diffusion performance.

Tape And Reel Information

REEL DIMENSIONS

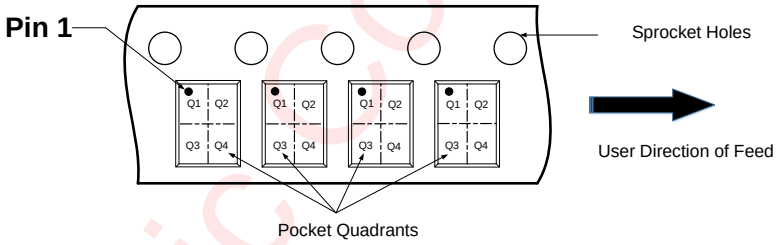


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



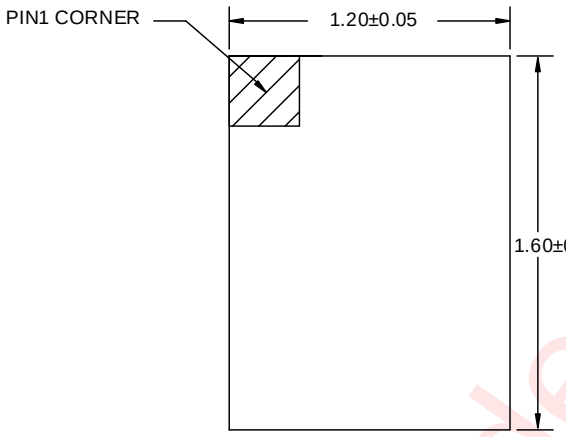
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

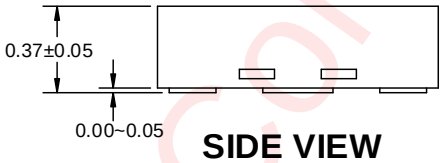
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
180	8.4	1.37	1.77	0.55	2	4	4	8	Q1

All dimensions are nominal

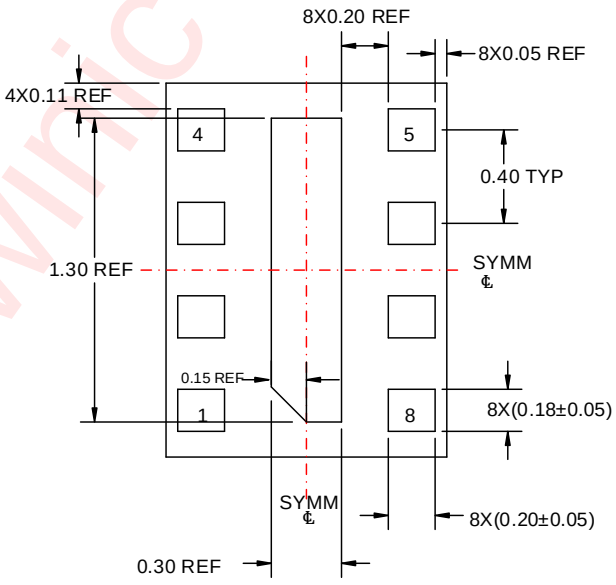
Package Description



TOP VIEW



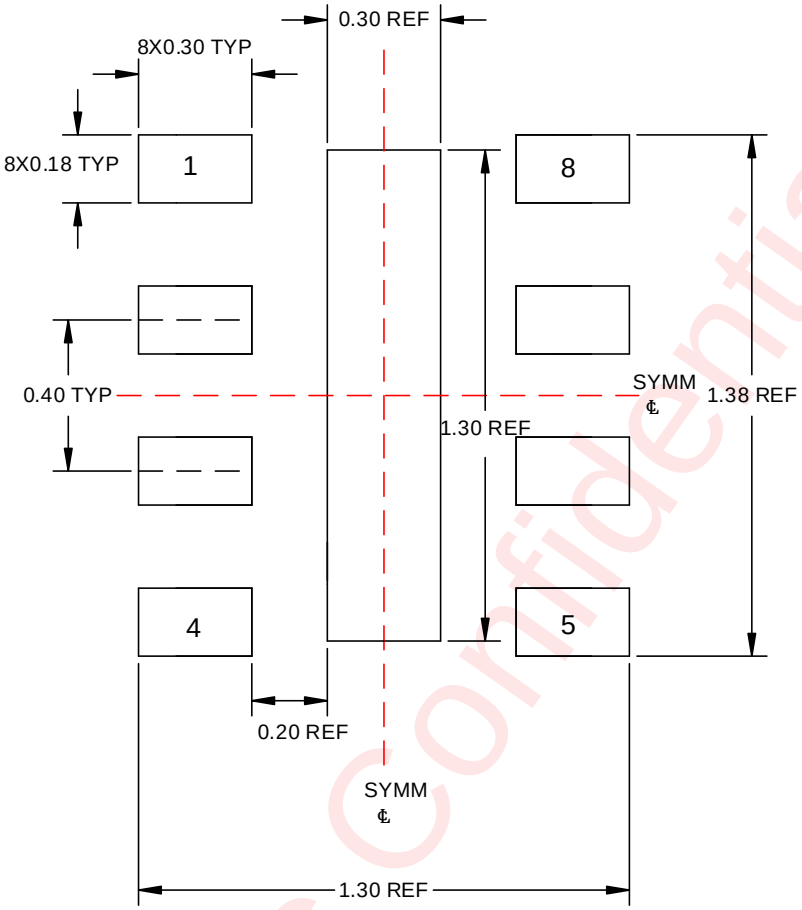
SIDE VIEW

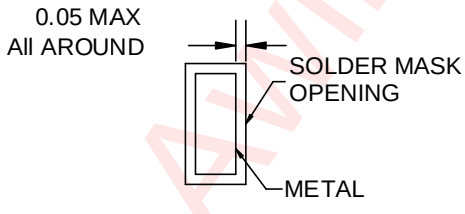


BOTTOM VIEW

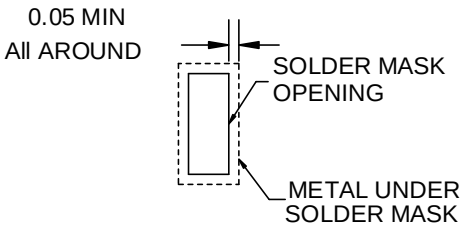
Unit:mm

Land Pattern Data





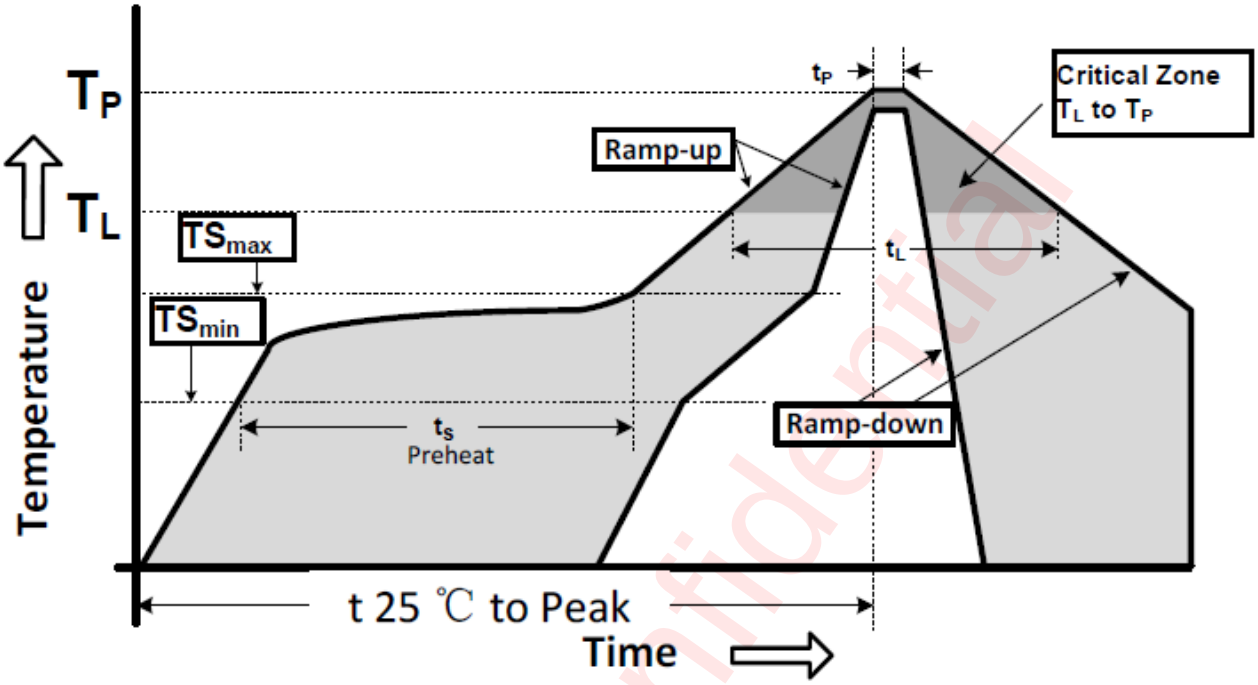
NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit：mm

Reflow



Reflow Note	Spec
Ramp-up rate（Tsmax to T_P）	3°C/second max.
Preheat temperature（Tsmin to Tsmax）	150°C to 200°C
Preheat time（t_s）	60 – 180 seconds
Time above T_L , 217°C（t_L）	60 – 150 seconds
Peak temperature（T_P）	260°C
Time within 5°C of peak temperature(t_P)	20 – 40 seconds
Ramp-down rate	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

Revision History

Version	Date	Change Record
V1.0	Oct. 2024	Officially released
V1.1	May 2025	Modify the maximum output voltage of the adjustable version from 3.3V to 4.5V.
V1.2	May 2025	Add “V_{SNS}” in the Electrical Characteristics(P6).
V1.3	Jul. 2025	Add the information of AW3707D180EDNR and AW3707D300EDNR.

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