18-Channel Intelligent RGB LED Driver

Features

- 18-channel RGB LED Driver
- Independent color mixing register per channel
- Maximum output current: 25.5mA
- High-precision current sinks
  - Device to device error：±7%
  - Channel to channel error：±7%
- Power save mode when all LED off > 30ms
- 400kHz I²C interface, 4 independent addresses, 1 broadcast address
- Power supply: 2.7V to 5.5V
- QFN 4mm x 4mm x 0.85mm 32L package

Applications

- Smart speaker
- E-sports devices
- Smart home appliances

General Description

AW21018C is a 18-channel high precision constant current LED driver. The maximum current of each channel is recommended to be configured via external resistor R_{EXT}.

AW21018C can be turned off with minimum current consumption by pulling the EN pin low. When EN pin pull high and all LEDs off >30ms, AW21018C enters power save mode.

AW21018C is available in QFN 4mm x 4mm x 0.85mm-32L package. It operates from 2.7V to 5.5V over the temperature range of -40℃ to 105℃.

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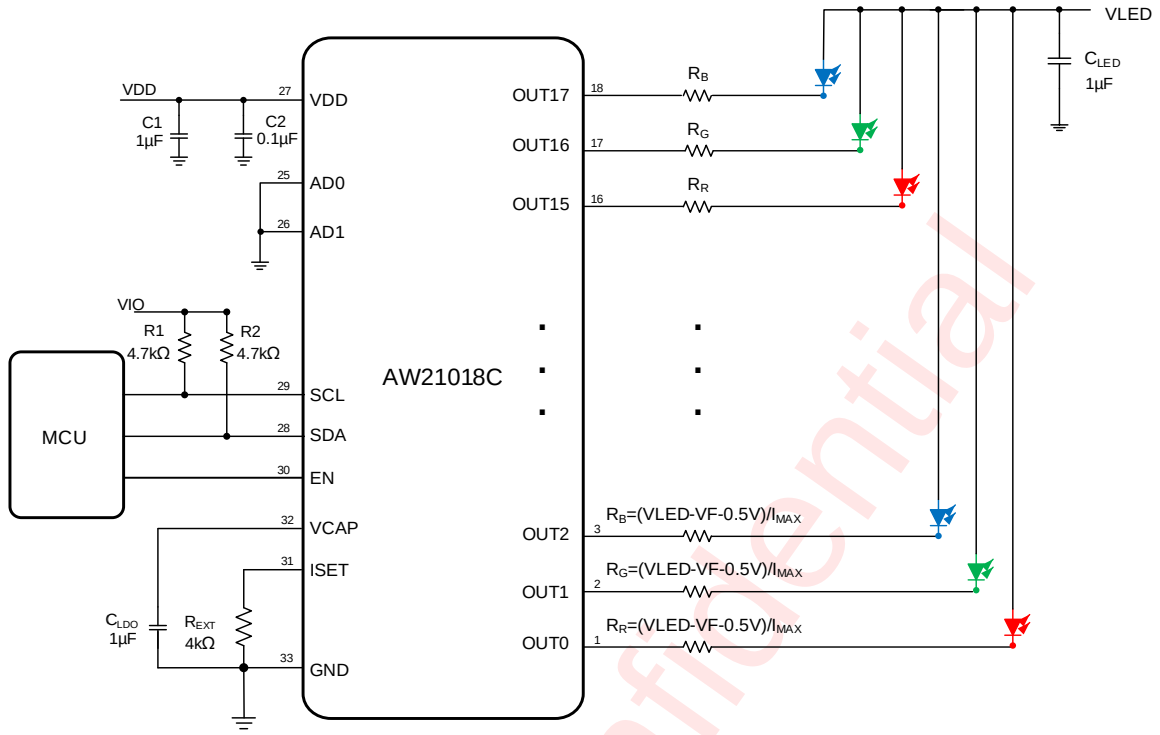
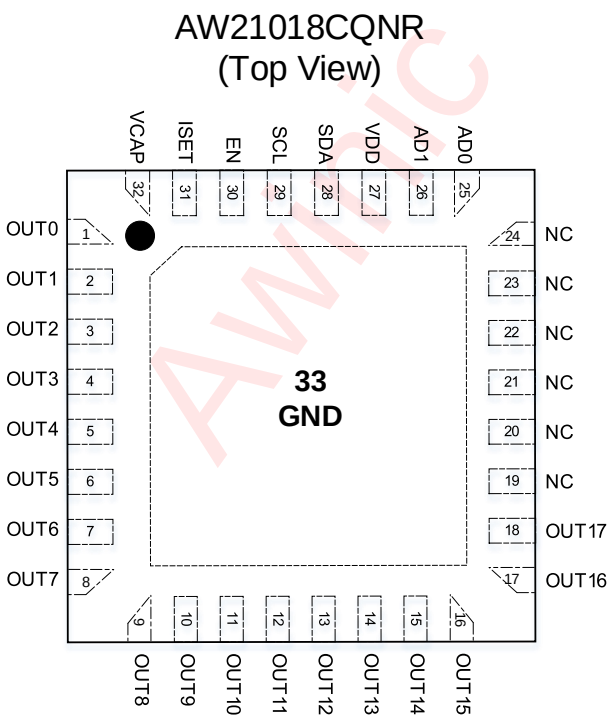
Typical Application Circuit

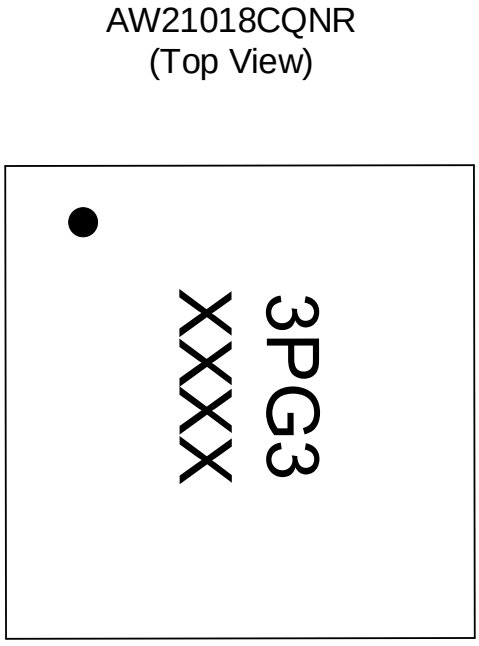


Note: The resistors(R_R, R_G, R_B) between LED and IC are only for thermal reduction. For more information, please refer to application information.

Figure 1 Application Circuit

Pin Configuration And Top Mark





3PG3 – AW21018CQNR
XXXX – Production Tracing Code

Figure 2 Pin Configuration and Marking

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Pin Definition

No.	NAME	DESCRIPTION
1~18	OUT0~OUT17	Constant current sink, connect to LED's cathode
25~26	AD0, AD1	I²C address setting, connects to GND or VDD for different device address of I²C
27	VDD	Power supply
28	SDA	Serial data I/O for I²C interface
29	SCL	Serial clock input for I²C interface
30	EN	Shutdown the chip when pulled low.
31	ISET	Input terminal used to connect an external resistor. This regulates the global output current
32	VCAP	Connect a 1μF capacitor to GND.
33	GND	Ground

Functional Block Diagram

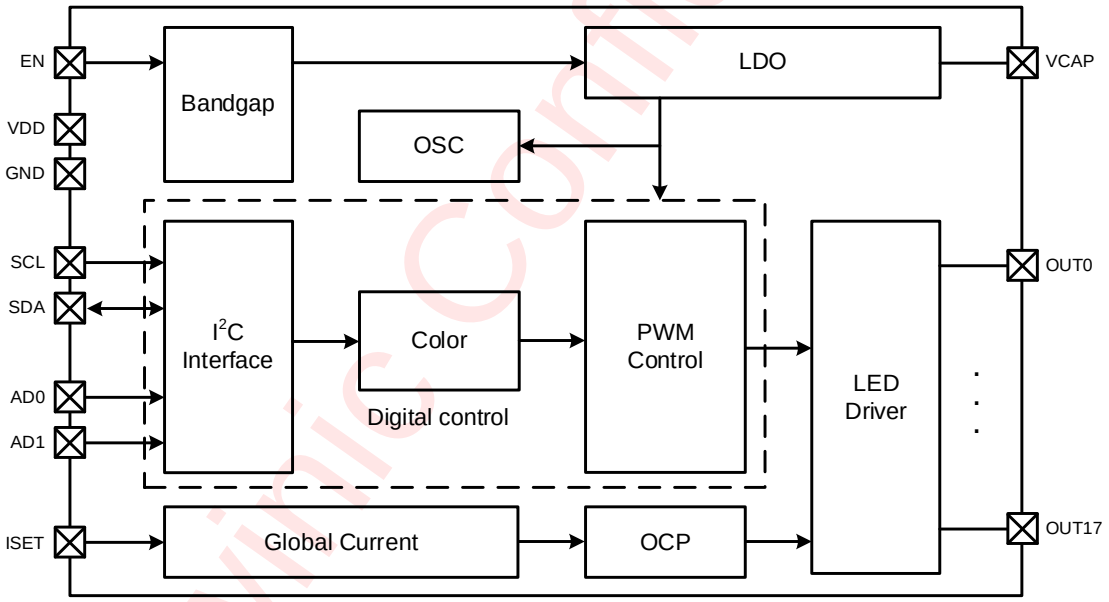

Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW21018CQNR	-40℃～105℃	QFN 4X4-32L	3PG3	MSL3	ROHS+HF	3000 units/ Tape and Reel

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Absolute Maximum Ratings(NOTE1)

Over operating ambient temperature range (unless otherwise noted)(1)

PARAMETERS		RANGE
Supply voltage range V_{DD}		-0.3V to 6V
Input voltage range	EN, ADx, SCL, SDA	-0.3V to 6V
Output voltage range	OUTx, ISET	-0.3V to 6V
	VCAP	-0.3V to 2.5V
Junction-to-ambient thermal resistance θ_{JA}		36.4℃/W
Maximum operating junction temperature T_{J-MAX}		150°C
Storage temperature, T_{stg}		-65°C to 150°C
ESD (NOTE 2)		
HBM		±2kV
CDM		±1.5kV
Latch-Up		
Test condition: JESD78F		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. HBM test method: ESDA/JEDEC JS-001-2023, CDM test method: ESDA/JEDEC JS -002-2022.

Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted)

Symbol	Parameter	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage	2.7		5.5	V
$V_{PULL-UP}$	SCL/SDA pull-up voltage	1.7		5.5	V
C_1, C_{LED}	Input capacitance	1			μF
C_2	Input capacitance	0.1			μF
C_{LDO}	Internal LDO capacitance	1			μF
R_{EXT}	Output current setting resistance	2			kΩ
T_A	Operating free-air temperature range	-40	25	105	°C

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Electrical Characteristics

T_A=25°C, VDD=3.6V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Power supply voltage and current						
V_{DD}	Supply voltage		2.7		5.5	V
I_{SD}	Shutdown supply current	V_{EN}=0		0.1	2	μA
I_{STB}	Standby supply current	V_{EN}=3.3V, CHIPEN=0		6	20	
I_{PS}	Power-save mode supply current NOTE(1)	V_{EN}=3.3V,CHIPEN=0,POWER_SAVE_EN=1,all the LEDs off duration > 30ms(typical)		6	20	
I_{ACT}	Normal-mode supply current	I_{OUTx}=10mA, PWM=100%		1.5	6	mA
I_{MAX}	Maximum output current	V_{OUTX}=1V, PWM=100%			25.5	mA
I_{LIM}	Internal output current limit	V_{OUTX}=1V, PWM=100%	35	50		
I_{lkg}	Leakage current	PWM=0		0.1	1	μA
$I_{accuracy}$	Device to device current error, $I_{ERR_DD}=(I_{AVE}-I_{SET})/I_{SET}$x100%	I_{OUTx}=15mA, V_{OUTX}=1V, PWM=100%	-7%		7%	
I_{MATCH}	Channel to channel current error, $I_{ERR_CC}=(I_{OUTX}-I_{AVE})/I_{AVE}$x100%	I_{OUTx}=15mA, V_{OUTX}=1V, PWM=100%	-7%		7%	
V_{ISET}	ISET voltage			0.7		V
K_{IREF}	IREF ratio			105		
$V_{Dropout}$	Voltage when LED current has dropped 5%	I_{OUTx}=20mA, PWM=100%		0.15	0.3	V
LOGIC INPUTS (EN, SCL, SDA, ADx)						
V_{IL}	Low level input voltage				0.4	V
V_{IH}	High level input voltage		1.4			
I_{LOGIC}	Input current		-1		1	μA
V_{SDA}	SDA output low level	I_{PULLUP}=5mA			0.4	V

Note1：Guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

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I²C Interface Timing Requirements

PARAMETER		MIN	TYP	MAX	UNIT
F_{SCL}	Interface Clock frequency	-		400	kHz
$T_{HD:STA}$	(Repeat-start) Start condition hold time	0.6		-	μs
T_{LOW}	Low level width of SCL	1.3		-	μs
T_{HIGH}	High level width of SCL	0.6		-	μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time	0.6		-	μs
$T_{HD:DAT}$	Data hold time	0		-	μs
$T_{SU:DAT}$	Data setup time	0.1		-	μs
T_R	Rising time of SDA and SCL	-		0.3	μs
T_F	Falling time of SDA and SCL	-		0.3	μs
$T_{SU:STO}$	Stop condition setup time	0.6		-	μs
T_{BUF}	Time between start and stop condition	1.3		-	μs

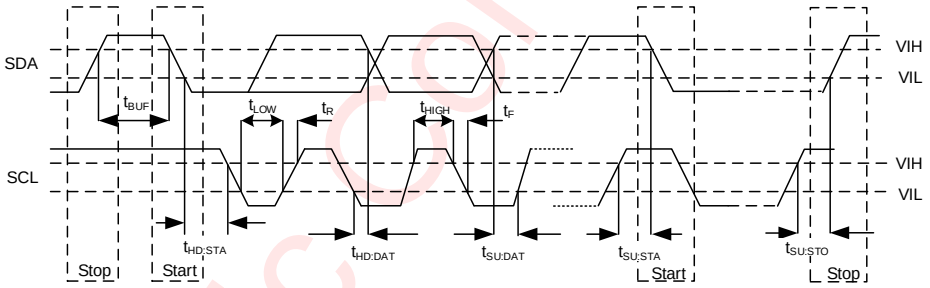

Figure 4 I2C Interface Timing

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Detailed Functional Description

Reset

Power on Reset and Hardware Reset

After VDD powering on and the EN pin pulling up, I²C communication can be performed after 3ms.

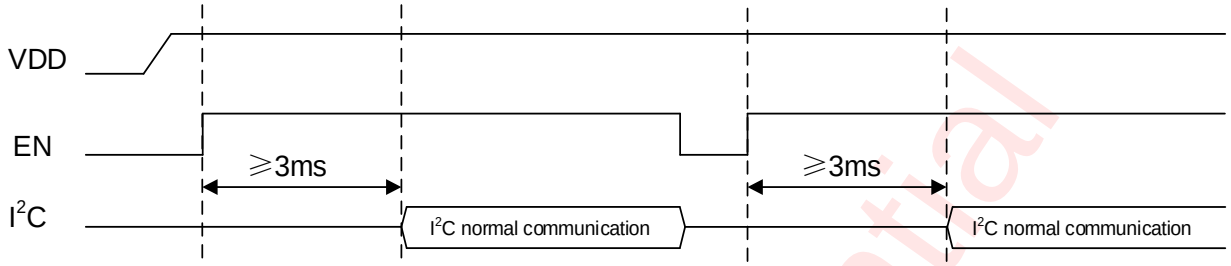

Figure 5 Power Up Timing

Soft Reset

Writing 0xFF into register RESET (address: 0x27), all configure registers will be reset. I²C communication can be performed after a delay of 3ms.

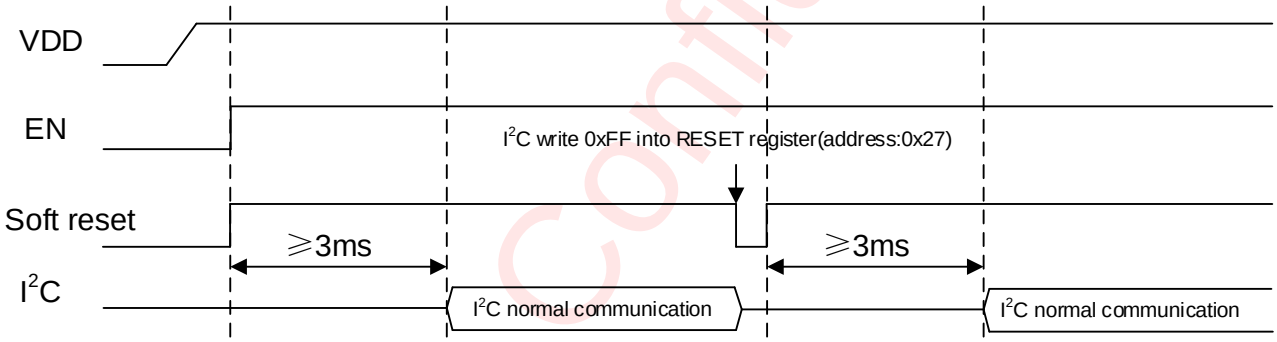

Figure 6 Software Reset Timing

Operation Mode

Shutdown

The device enters into shutdown mode automatically when EN is pulled low from any state, and all registers are reset and cannot be configured via I²C communication interface.

Initialization

The device enters initialization mode automatically from shutdown mode when EN is pulled high. If writing 0xFF into register RESET (address: 0x27), all configure registers will be reset, and the device will also enter initialization mode.

Standby

If the device completes initialization or the bit CHIPEN of register DEVICE_CFG0 (address: 0x00.bit6) is set to “0”, the device will enter standby mode. In this mode, the light control circuit is turned off, the power consumption is low, the registers data is retained, and the registers can be accessed through the I²C communication interface.

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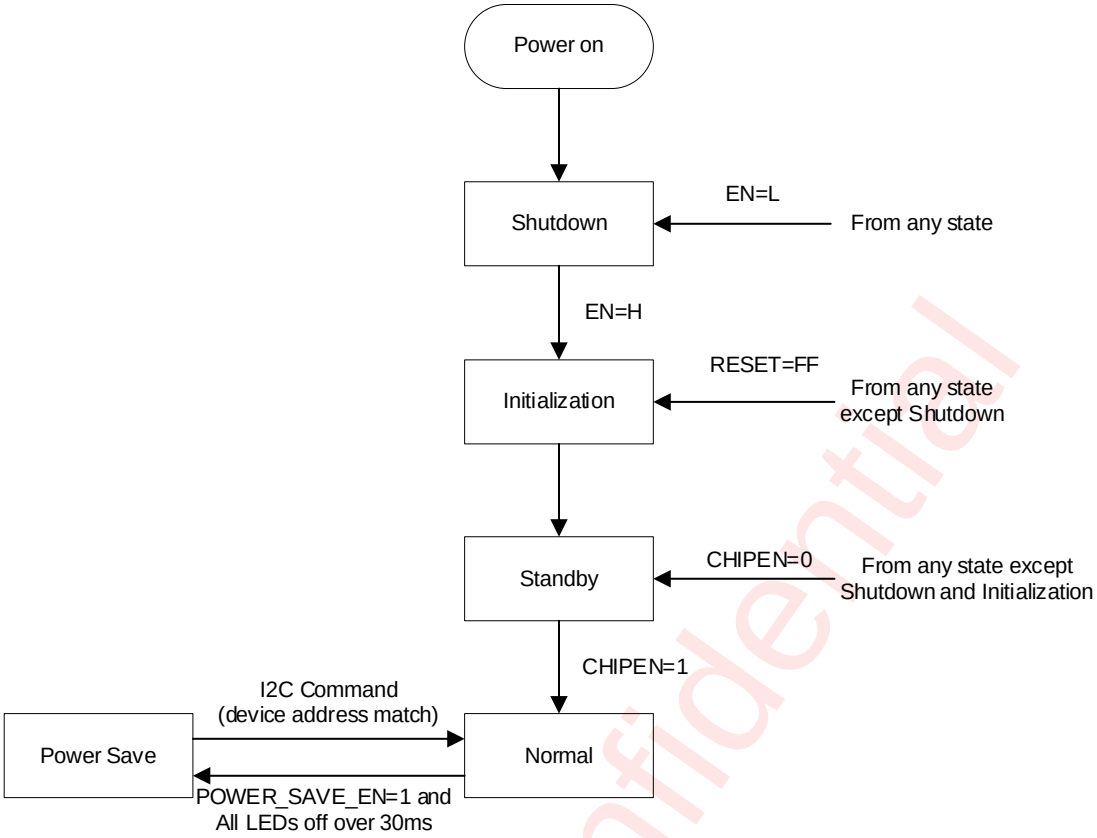

Figure 7 Operating Mode Transition

Normal

In the following three situations, the device will enter normal mode.

(1) In standby mode, the register CHIPEN is set to "1";

(2) In thermal shutdown mode, the temperature reaches the recovery temperature;

(3) In power save mode, the device is accessed with I²C device address matching.

Power Save

If the bit POWER_SAVE_EN of register DEVICE_CFG1 (address: 0x01.bit4) is set to "1" and all LEDs off over 30ms, the device will enter power save mode. In this mode, the light control circuit is turned off, the power consumption is low, the registers data is retained, and the registers can be accessed through the I²C communication interface.

PWM Control

The device supports independent color mixing control, providing smooth and rich lighting effects.

The frequency of the output PWM signal is about 29kHz, which is greater than the audible range and can eliminate audible noise.

Independent Color Mixing

Each OUT channel has an independent 8-bit color mixing register OUT3n/3n+1/3n+2_COL (RGB，n=0~7, address: 0x0F~0x26). Each RGB LED can achieve 256 x 256 x 256 mixed color effects.

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Maximum Current Setting

The maximum output current of OUTx is set by external resistor R_{EXT} and can be expressed by the following formula:

$$I_{MAX} = K \times \frac{V_{ISET}}{R_{EXT}}$$

Where V_{ISET}=0.7V, K=105;

If ISET pin is connected to a small resistor or shorted to ground. The max current is limit by internal OCP circuit. More information about current limit please refer to section OCP.

General I²C Operation

The device supports the I²C protocol in fast mode at 400kHz. The two communication lines are a serial data line (SDA) and a serial clock line (SCL).The pull-up resistor for the SDA and SCL can be selected from 1k to 10kΩ. Usually, 4.7kΩ is recommended for 400kHz I²C. The voltage level 1.8V , 3.3V and 5.0V is allowed for the I2C interface.

Device Address

The device is defined by connecting GND or VDD to the AD0 and AD1 pins from the address. When GND or VDD is connected to the AD0 and AD1 pins, four independent device addresses can be combined (see Tables 1). Regardless of the settings of the AD0 and AD1 pins, the device will respond with a broadcast from the address. Perform global write operations on broadcast addresses to configure all devices simultaneously. This device supports global reading using broadcast addresses; However, the read data is only valid when all devices on the I²C bus contain the same value.

Table 1 I²C Device Address Configuration

AD1 Connection	AD0 Connection	Device Address	
		Independent	Broadcast
GND	GND	0x28	0x3C
GND	VDD	0x29	
VDD	GND	0x2A	
VDD	VDD	0x2B	

Data Validation

When SCL is high level, SDA level must be stable. SDA can be changed only when SCL is low level.

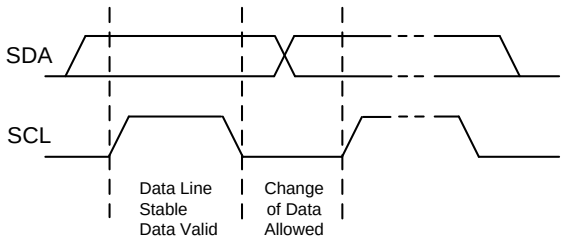

Figure 8 Data Validation Diagram

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I²C Start/Stop

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

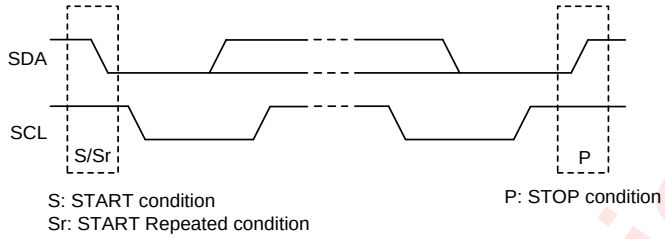

Figure 9 I2C Start/Stop Condition Timing

Acknowledge(ACK)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

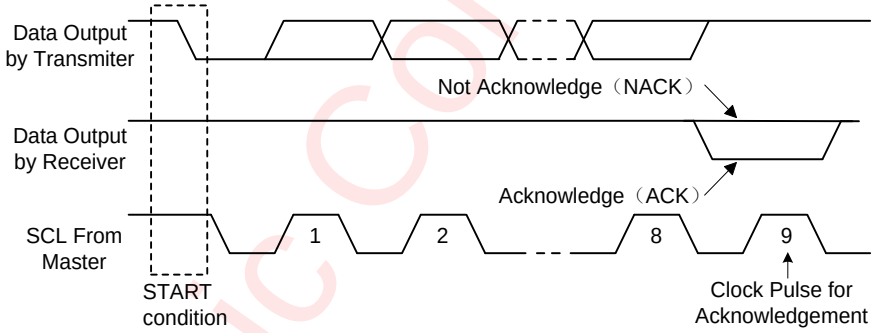

Figure 10 I2C ACK Timing

Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

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d) Master sends control register address (8-bit)
e) Slave sends acknowledge signal
f) Master sends data byte to be written to the addressed register
g) Slave sends acknowledge signal
h) If master will send further data bytes, the control register address will be incremented by one after acknowledge signal (repeat step f and g)
i) Master generates STOP condition to indicate write cycle end

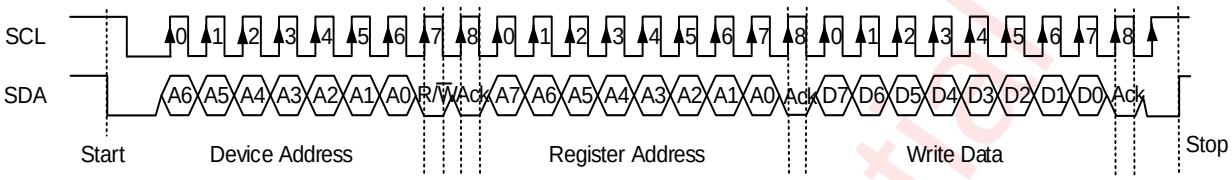

Figure 11 I2C Write Byte Cycle

Read Cycle

In a read cycle, the following steps should be followed:

a) Master device generates START condition
b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).
c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends control register address (8-bit)
e) Slave sends acknowledge signal
f) Master generates STOP condition followed with START condition or REPEAT START condition
g) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).
h) Slave device sends acknowledge signal if the slave address is correct.
i) Slave sends data byte from addressed register.
j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.
k) If the master device generates STOP condition, the read cycle is ended.

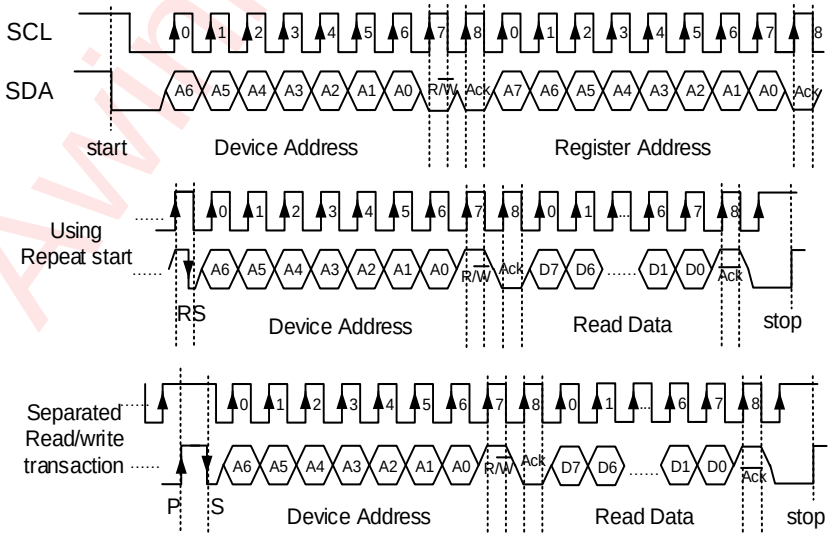

Figure 12 I2C Read Byte Cycle

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Over Current Protection (OCP)

The device monitors the current of ISET pin. When the current above the threshold, the surplus portion cannot be mirrored to the output pin, thereby limiting the maximum current.. Please refer to the electrical parameter table for specific parameters.

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REGISTER CONFIGURATION

REGISTER LIST

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	DEVICE_CFG0	RW		CHIPEN							0x00
0x01	DEVICE_CFG1	RW				POWER_SAVE_EN				LED_GLOBAL_OFF	0x3C
0x0F~0x20	OUT0_COL_CFG ~ OUT17_COL_CFG	RW	OUT0_COL~ OUT17_COL								0x00
0x27	RESET	WO	SOFT_RESET								0x00
0x6E	CHIP_ID	RO	CHIPID								0x41

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REGISTER DETAILED DESCRIPTION

DEVICE_CFG0: (Address 00h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RO	Not used	0x0
6	CHIPEN	RW	Chip enable 0 : Disable 1 : Enable	0x0
5:0	Reserved	RO	Not used	0x0

DEVICE_CFG1: (Address 01h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:5	Reserved	RO	Not used	0x1
4	POWER_SAVE_EN	RW	Power save mode enable 0 : Disable 1 : Enable	0x1
3:1	Reserved	RO	Not used	0x6
0	LED_GLOBAL_OFF	RW	All LEDs off enable 0 : Disable 1 : Enable	0x0

OUT0_COL_CFG~OUT17_COL_CFG: (Address 0Fh~20h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	OUT0_COL~ OUT17_COL	RW	OUT3n、OUT3n+1、OUT3n+2 color mixing setting when LEDn bank mode disable (n=0~5) 00h : The color mixing rate is 0% ... 80h : The color mixing rate is 50% ... FFh : The color mixing rate is 100%	0x0

RESET: (Address 27h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	SOFT_RESET	WO	Soft reset, reset all register when FFh is written	0x0

CHIP_ID: (Address 6Eh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	CHIPID	RO	The CHIPID number. AW21018CQNR	0x41

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Application Information

R_{EXT}

The maximum output current of OUTx is set by external resistor R_{EXT} and can be expressed by the following formula:

$$I_{MAX} = K \times \frac{V_{ISET}}{R_{EXT}}$$

Where V_{ISET}=0.7V, K=105;

To set the LED current to 15mA, R_{EXT} should be set to 4.9kΩ.

R_R, R_G, R_B

The resistance(R_X) used for thermal reduction can be calculated according to the following formula:

$$R_X = \frac{VLED - VF_x - V_{DROPOUT}}{I_{MAX}}$$

VLED: LED power supply voltage.

VF_X: LED forward voltage.

$V_{DROPOUT}$: Voltage on LEDx, recommended values is 0.5V.

I_{MAX}: Maximum output current.

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PCB Layout Consideration

AW21018C is a 18-channel LEDs driver programmed via I²C compatible interface. When all LEDs are operating, the device power dissipation is large. To obtain the good thermal performance and avoid thermal shutdown, PCB layout should be considered carefully. Here are some guidelines:

1. The C_1, C_2, C_{LED} should be placed as close to the chip as possible.
2. The C_{LDO} should be placed as close to the PIN 32 as possible.
3. The R_{EXT} should be placed as close to the PIN 31 as possible.
4. The Thermal PAD must be well connecting to the GND of the PCB, and add as many thermal vias as possible beneath the thermal PAD on the PCB for the heat conductivity of the device and PCB.

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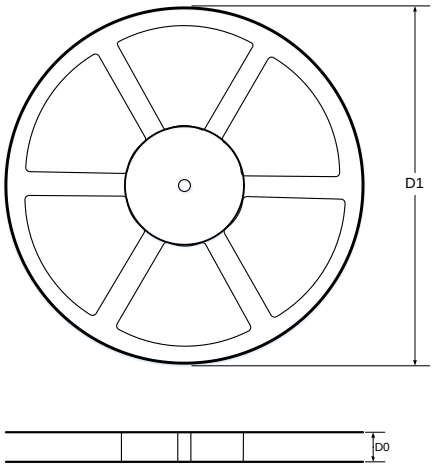
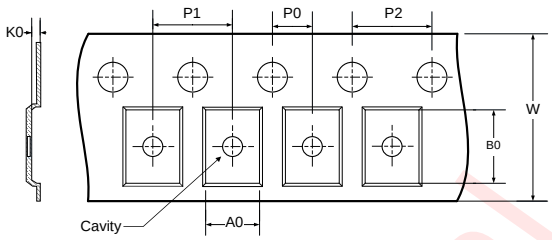
Tape And Reel Information

REEL DIMENSIONS

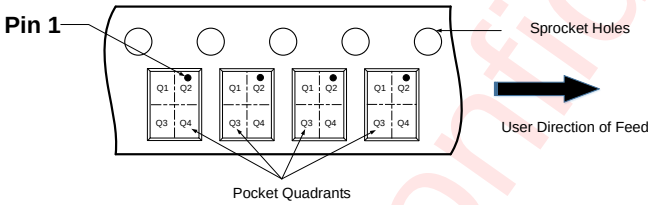


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	4.3	4.3	1.1	2	8	4	12	Q2

All dimensions are nominal

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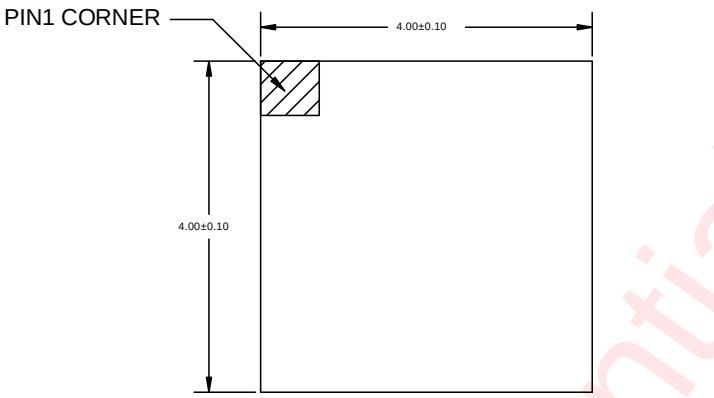
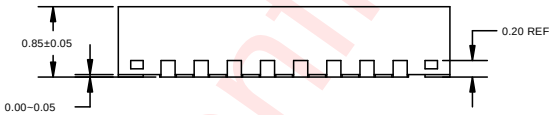
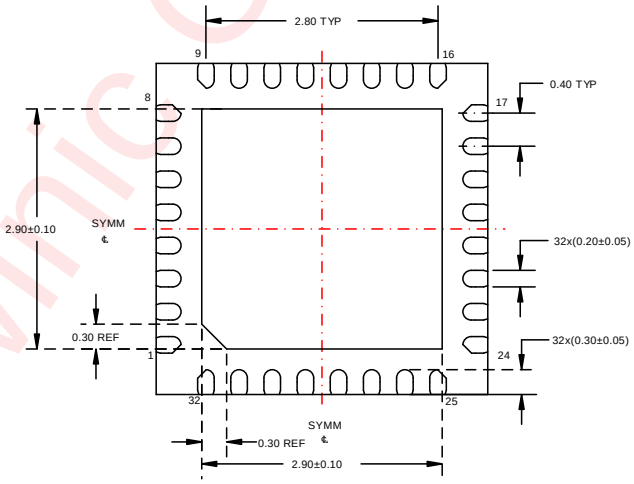
Package Description



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Unit：mm

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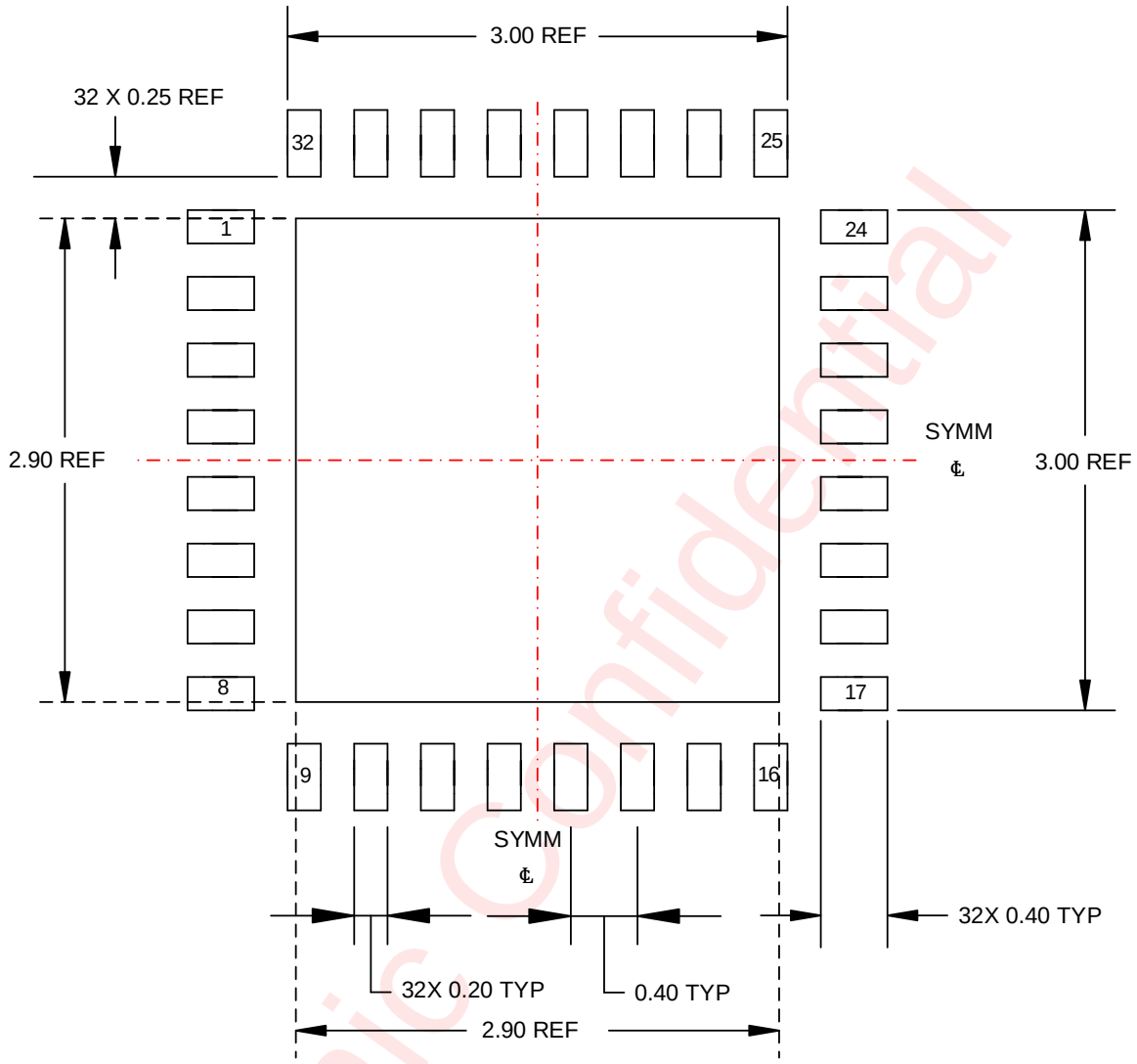
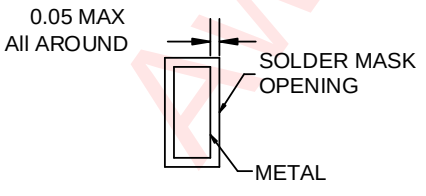
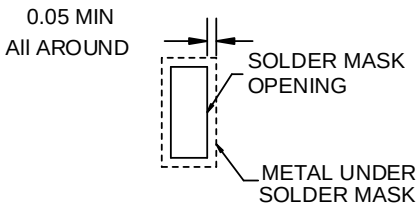
Land Pattern Data





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit：mm

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Revision History

Version	Date	Change Record
V1.0	Nov. 2025	Officially released

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