钍地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65LBC184/SN75LBC184

Differential transceiver with transient voltage suppression function

网址 www.sztdbdt.com

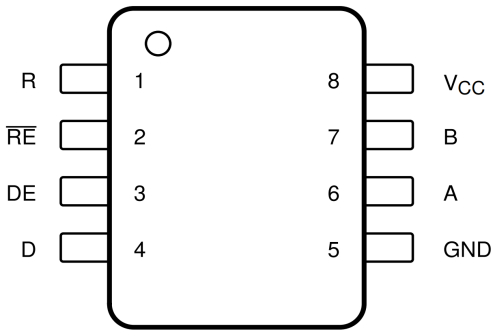
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- Integrated transient voltage suppression
- ESD protection for bus terminals exceeds:
±30kV IEC 61000--2, contact discharge
±30kV IEC 61000-4-2, air gap discharge
±15kV EIA/JEDEC human body model
- 400W peak (typical) circuit damage protection, compliant with IEC 61000-4-5
- Controlled driver output voltage slew rate allows cable stub lengths
- Data rates up to 250kbps in electrically noisy environments
- Open-circuit fault protection receiver design
- 1/4 unit load supports 128 devices on the bus
- Thermal shutdown protection
- Power-up and power-down interference protection
- Each transceiver meets or exceeds the requirements of T/EIA-485 (RS-485) and ISO/IEC 8482:1993(E) standards
- Low disabled current (maximum 300μA)
- Pin compatible with SN75176



Package SOIC Package PDIP
(Top View)

Applications

- Industrial networks
- Utility meters
- Motor control

Description

The SN75LBC184 and SN65LBC184 devices are differential data line transceivers in the-standard SN75176 package, featuring built-in protection against high-energy noise transients. This feature significantly improves reliability, providing better resistance to noise transients coupled the data cable compared to most existing devices. These circuits provide a reliable, low-cost, directly coupled (transformerless) data line interface without the need for any external components.The SN75LBC184 and SN65LBC184 can withstand 400W peak (typical) overvoltage transients. The standard combination specified in IEC 61000-4-5 can simulate overvoltage transients and model unidirectional surges caused by overvoltages from switching operations and secondary lightning transients

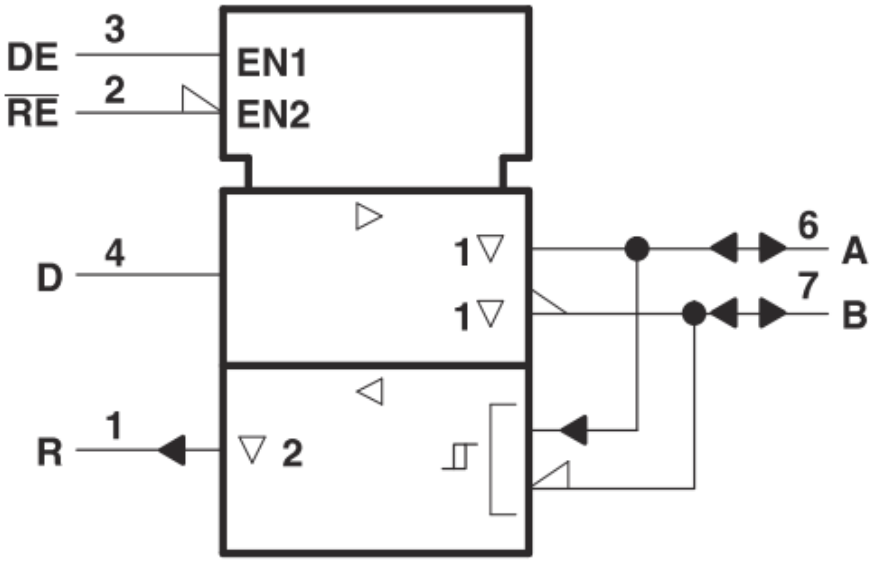


表 **4-1. Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Active-HIGH driver enable
GND	5	Reference potential	Local device ground
R	1	Digital output	Receiver data output
$\overline{RE}$	2	Digital input	Active-LOW receiver enable
V_{CC}	8	Supply	4.75V to 5.25V supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	- 0.5	7	V
	Continuous voltage range at any bus terminal	- 15	15	V
	Data input/output voltage	- 0.3	7	V
I_O	Receiver output current	- 20	20	mA
	Continuous total power dissipation(3)	Internally Limited		
T_{stg}	Storage temperature		160	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 5.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
(3) The driver shuts down at a junction temperature of approximately 160°C. To operate below this temperature, see the 节 5.9 .

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	A, B, GND	±15000	V
			All pins	±3000	
		Contact discharge (IEC61000-4-2)(2)	A, B, GND(3)	±30000	
		Air discharge (IEC61000-4-2)	A, B, GND(3)	±30000	
		All pins (Class 3A)		±8000	
		All pins (Class 3B)		±200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
(3) GND and bus pin ESD protection is beyond readily available test equipment capabilities for IEC 61000-4-2, EIA/JEDEC test method A114-A and MIL-STD-883C method 3015. Ratings listed are limits of test equipment; device performance exceeds these limits.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN(1)	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		- 7		12	V
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
$\|V_{ID}\|$	Differential input voltage				12	V
I_{OH}	High-level output current	Driver	- 60			mA
		Receiver	- 8			
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			4	
T_A	Operating free-air temperature	SN75LBC184	0		70	°C
		SN65LBC184	- 40		85	

(1) The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet.

5.4 Thermal Information

THERMAL METRIC(1)		P (PDIP)	D (SOIC)	UNIT
		8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.7	116.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.8	41.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.6	61.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12	4.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.5	60.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		ALTERNATE SYMBOLS	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current	NA	DE = $\overline{RE}$ = 5V No Load		12	25	mA
			DE = 0 V, $\overline{RE}$ = 5V No Load		175	300	μA
I_{IH}	High-level input current (D, DE, $\overline{RE}$)	NA	V_I = 2.4V			50	μA
I_{IL}	Low-level input current (D, DE, $\overline{RE}$)	NA	V_I = 0.4V	−50			μA
I_{OS}	Short-circuit output current OS(2)	NA	V_O = −7V	−250	−120		mA
			V_O = V_{CC}			250	
			V_O = 12V			250	
I_{OZ}	High-impedance output current	NA	See Receiver I_I				mA
V_O	Output voltage	V_{oa}, V_{ob}	I_O = 0	0		V_{CC}	V
$V_{OC(PP)}$	Peak-to-peak change in common-mode output voltage during state transitions	NA	See 图 6-4 and 图 6-5		0.8		V
V_{OC}	Common-mode output voltage	$\lvert V_{os}\rvert$	See 图 6-3	1		3	V
$\lvert\Delta V_{OC(SS)}\rvert$	Magnitude of change, common-mode steady-state output voltage	$\lvert V_{os} - V_{os}\rvert$	See 图 6-5			0.1	V
$\lvert V_{OD}\rvert$	Magnitude of differential output voltage $\lvert V_A - V_B\rvert$	V_o	I_O = 0	1.5		6	V
			R_L = 54Ω, See 图 6-3	1.5			V
$\Delta\lvert V_{OD}\rvert$	Change in differential voltage magnitude between logic states	$\lvert\lvert V_t\rvert - \lvert V_t\rvert\rvert$	R_L = 54Ω			0.1	V

(1) All typical values are measured with T_A = 25°C and V_{CC} = 5V.
(2) This parameter is measured with only one output being driven at a time.

5.6 Electrical Characteristics: Receiver

over recommended operation conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current (total package)	DE = $\overline{RE}$ = 0 V, No Load				3.9	mA
		$\overline{RE}$ = 5V, DE = 0 V, No Load				300	μA
I_I	Input current	Other input = 0 V	V_I = 12V			250	μA
			V_I = 12V, V_{CC} = 0			250	
			V_I = −7V	−200			
			V_I = −7V, V_{CC} = 0	−200			
I_{OZ}	High-impedance-state output current	V_O = 0.4V to 2.4V				±100	μA
V_{hys}	Input hysteresis voltage				70		mV
V_{IT+}	Positive-going input threshold voltage					200	mV
V_{IT-}	Negative-going input threshold voltage			−200			mV
V_{OH}	High-level output voltage	I_{OH} = −8mA, See 图 6-6		2.8			V

5.6 Electrical Characteristics: Receiver（续）

over recommended operation conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{OL}	Low-level output voltage	I_{OL} = 4mA, See 图 6-6			0.4	V

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

5.7 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(DH)}$	Differential output delay time, low-to-high-level output	R_L = 54Ω, C_L = 50pF, See 图 6-4			1.3	μs
$t_{d(DL)}$	Differential output delay time, high-to-low-level output				1.3	μs
t_{PLH}	Propagation delay time, low-to-high-level output			0.5	1.3	μs
t_{PHL}	Propagation delay time, high-to-low-level output			0.5	1.3	μs
$t_{sk(p)}$	Pulse skew ($\lvert t_{d(DH)} - t_{d(DL)} \rvert$)			75	150	ns
t_r	Rise time, single-ended		0.25		1.2	μs
t_f	Fall time, single-ended		0.25		1.2	μs
t_{PZH}	Output enable time to high level	R_L = 110Ω, See 图 6-1			3.5	μs
t_{PZL}	Output enable time to low level	R_L = 110Ω, See 图 6-2			3.5	μs
t_{PHZ}	Output disable time from high level	R_L = 110Ω, See 图 6-1			2	μs
t_{PLZ}	Output disable time from low level	R_L = 110Ω, See 图 6-2			2	μs

5.8 Receiver Switching Characteristics

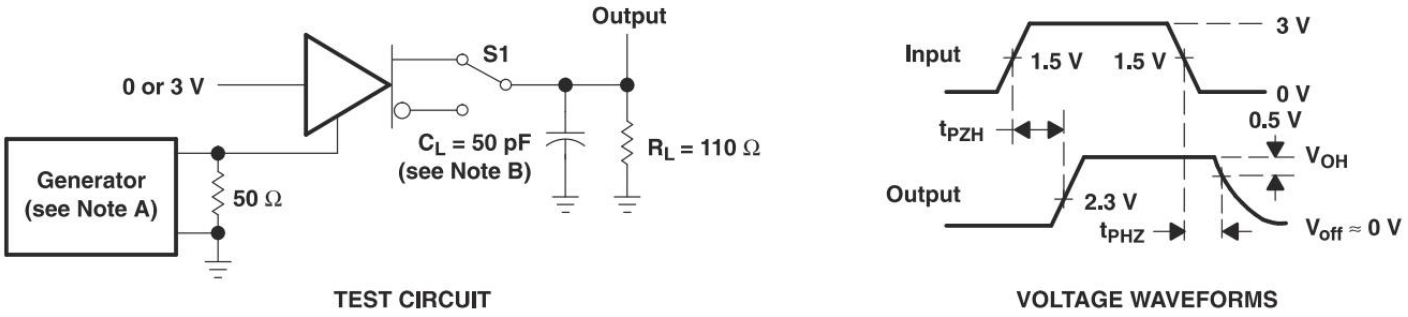
over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, See 图 6-6			150	ns
t_{PHL}	Propagation delay time, high-to-low-level output				150	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)				50	ns
t_r	Rise time, single-ended	See 图 6-6		20		ns
t_f	Fall time, single-ended			20		ns
t_{PZH}	Output enable time to high level	See 图 6-7			100	ns
t_{PZL}	Output enable time to low level				100	ns
t_{PHZ}	Output disable time from high level				100	ns
t_{PLZ}	Output disable time from low level				100	ns

5.9 Dissipation Ratings

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1150 mW	9.2 mW/°C	736 mW	598 mW

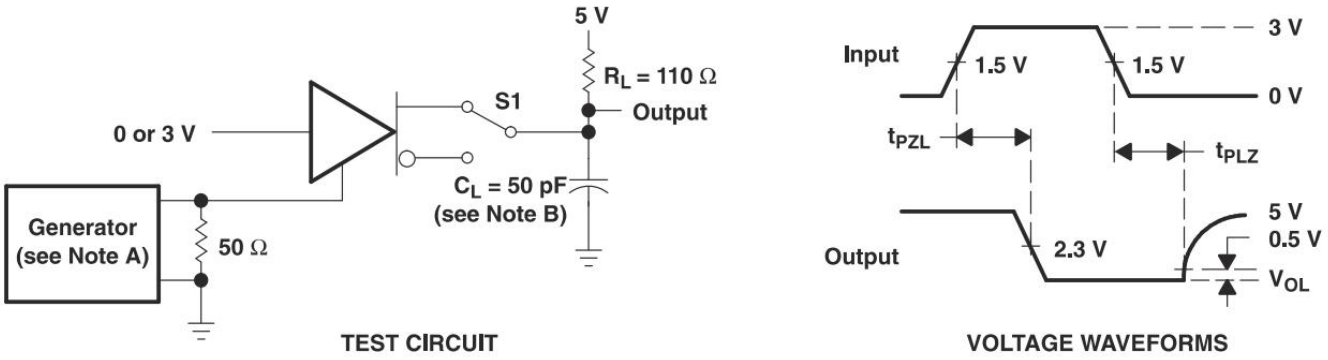
6 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, t_r ⩽ 10 ns, t_f ⩽ 10 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

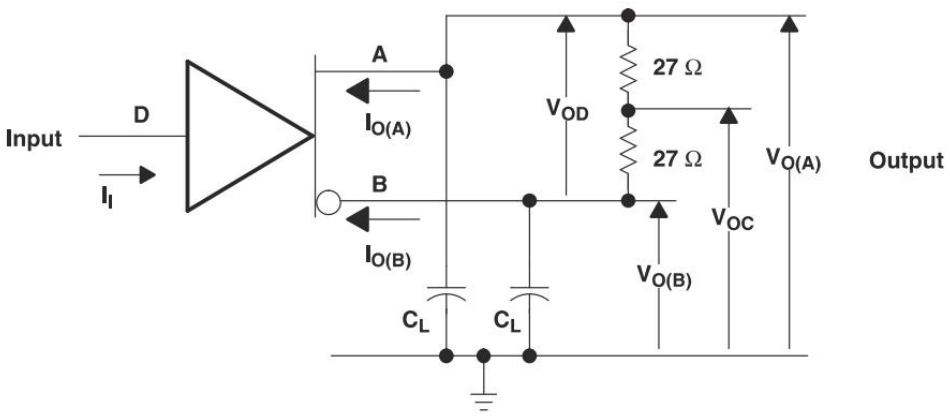
图 6-1. Driver t_{PZH} and t_{PHZ} Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, t_r ⩽ 10 ns, t_f ⩽ 10 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

图 6-2. Driver t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms



A. Resistance values are in ohms and are 1% tolerance.

B. C_L includes probe and jig capacitance.

图 6-3. Driver Test Circuit, Voltage, and Current Definitions

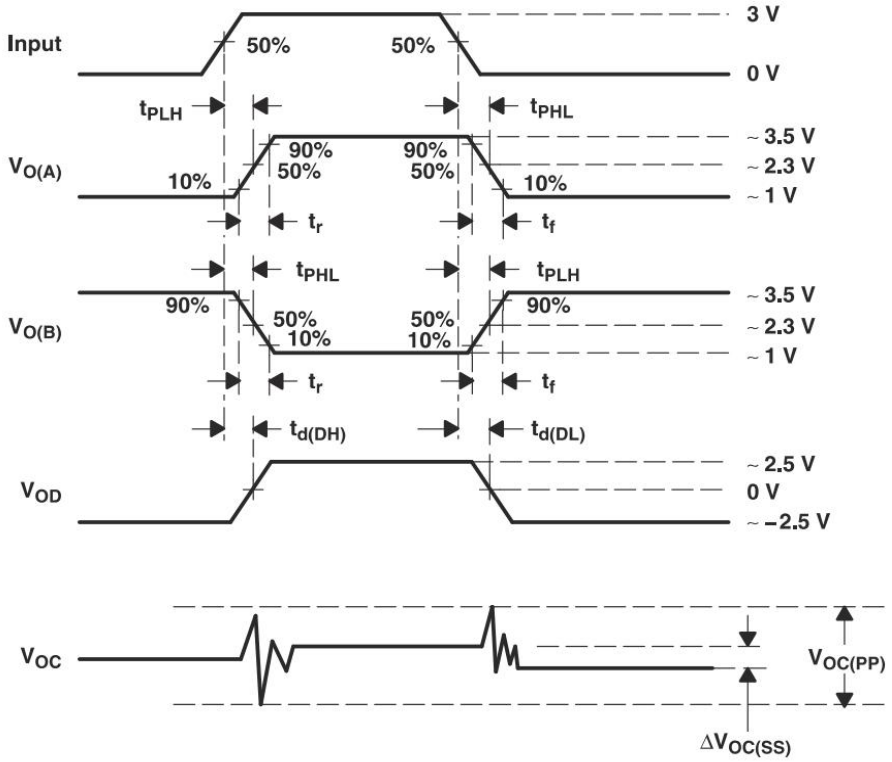
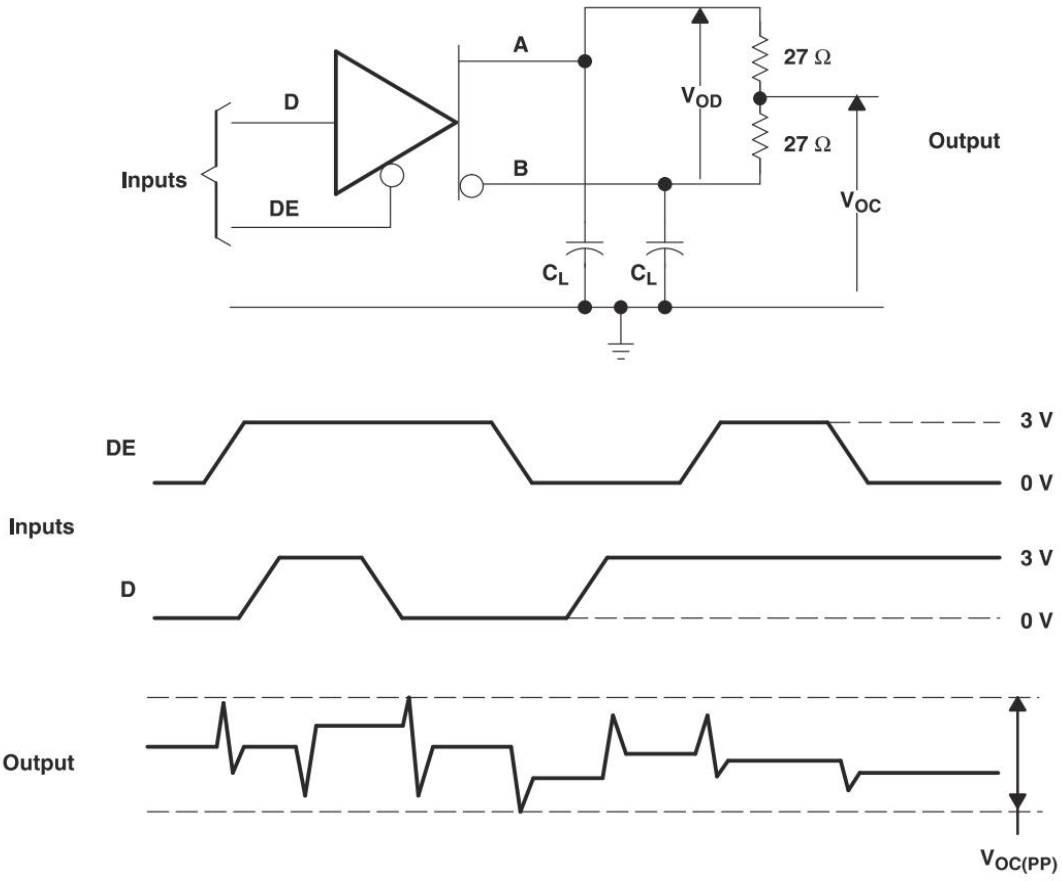


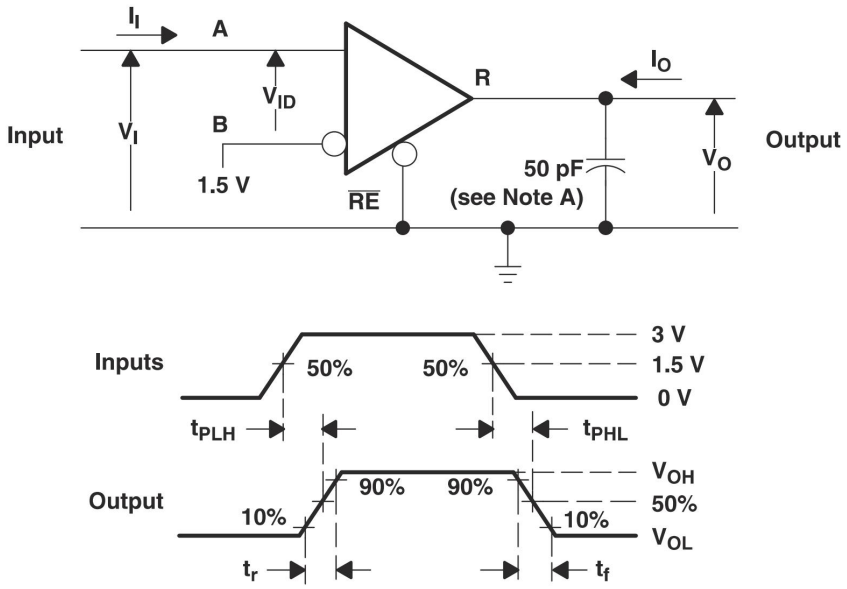
图 6-4. Driver Timing, Voltage, and Current Waveforms



A. Resistance values are in ohms and are 1% tolerance.

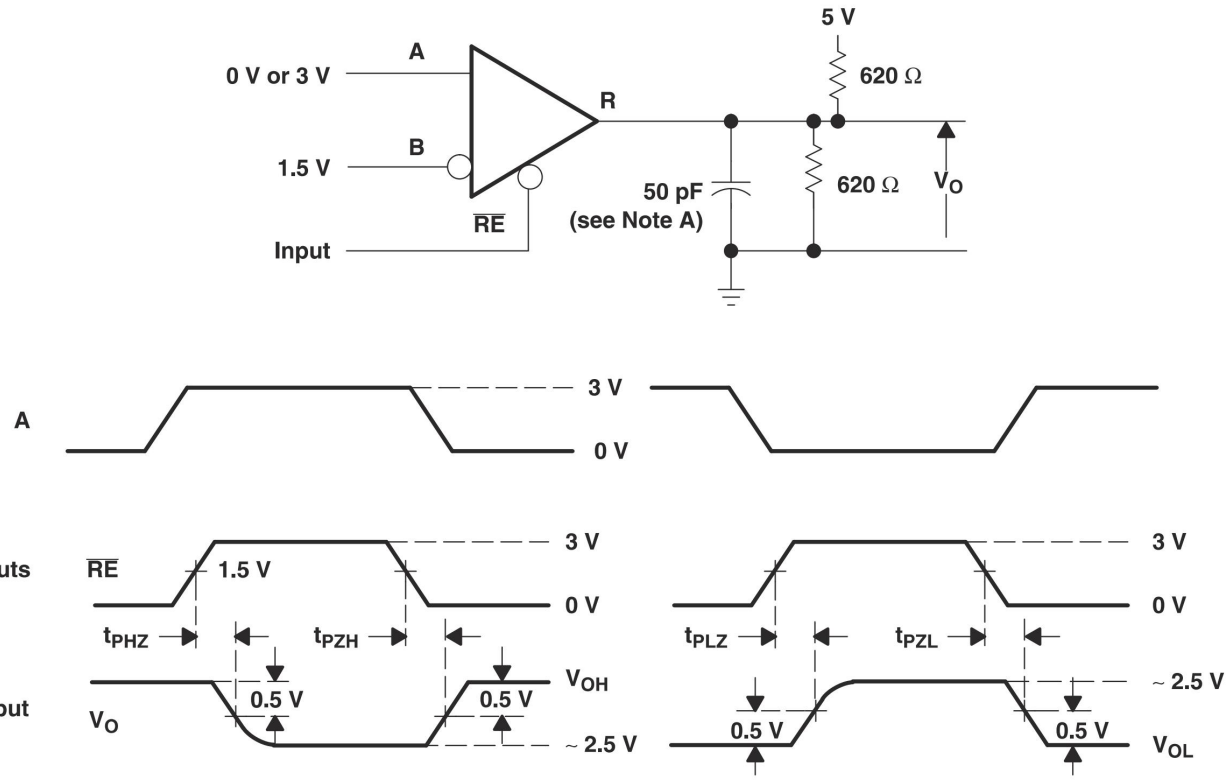
B. C_L includes probe and jig capacitance (±10%).

图 6-5. Driver $V_{OC(PP)}$ Test Circuit and Waveforms



A. This value includes probe and jig capacitance (±10%).

图 6-6. Receiver t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms



A. This value includes probe and jig capacitance (±10%).

图 6-7. Receiver t_{PZL}, t_{PLZ}, t_{PZH}, and t_{PHZ} Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SNx5LBC184 device is a 5V, half-duplex, RS-485 transceiver with integrated transient voltage suppressors that prevent circuit damage in the presence of high-energy transients of up to 400W peak power. This transceiver has an active-HIGH driver enable and active-LOW receiver enable. The differential driver is suitable for data transmission up to 250kbps.

7.2 Functional Block Diagram

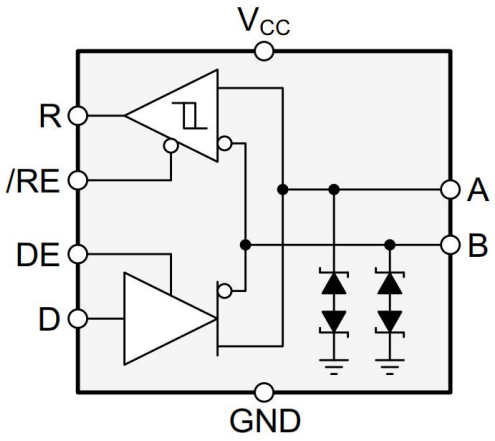


图 **7-1. Functional Logic Diagram**

7.3 Feature Description

Integrated transient voltage suppressors protect the transceiver against Electrostatic Discharges (ESD) according to IEC 61000-4-2 of up to ±30kV and surge transients according to IEC 61000-4-5 of up to 400W peak.

The differential driver incorporates slew-rate controlled outputs sufficient to transmit data up to 250kbps. Slew-rate control allows for longer unterminated cable runs and longer stub lengths from the main cable trunk than with faster voltage transitions. A unique receiver design provides a high level failsafe output when the inputs are left floating.

The SN65LBC184 is characterized from －40°C to 85°C and the SN75LBC184 is characterized from 0°C to 70°C.

7.4 Device Functional Modes

When the driver enable pin (DE) is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition, the logic state at D is irrelevant.

表 7-1. Driver Functions

INPUT(1)	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output (R) turns high. When V_{ID} is negative and lower than the negative input threshold, V_{IT-}, the receiver output turns low. If V_{ID} is between V_{IT+} and V_{IT-}, the output is indeterminate.

When $\overline{RE}$ is logic high, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. When the transceiver is disconnected from the bus, the receiver provides a failsafe high output.

表 7-2. Receiver Functions

DIFFERENTIAL INPUT	ENABLE(1)	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{ID} > V_{IT+}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
OPEN	L	H	Receiver failsafe High

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

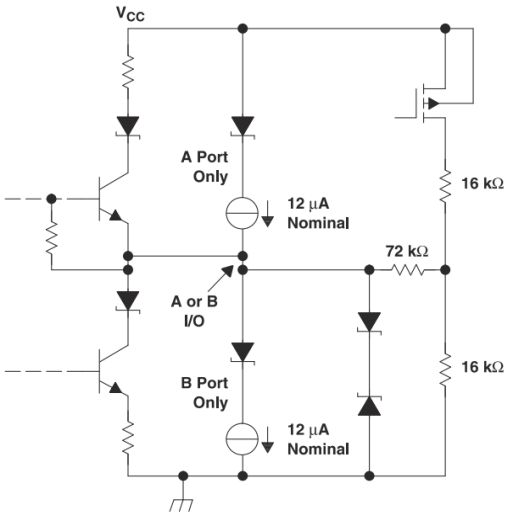
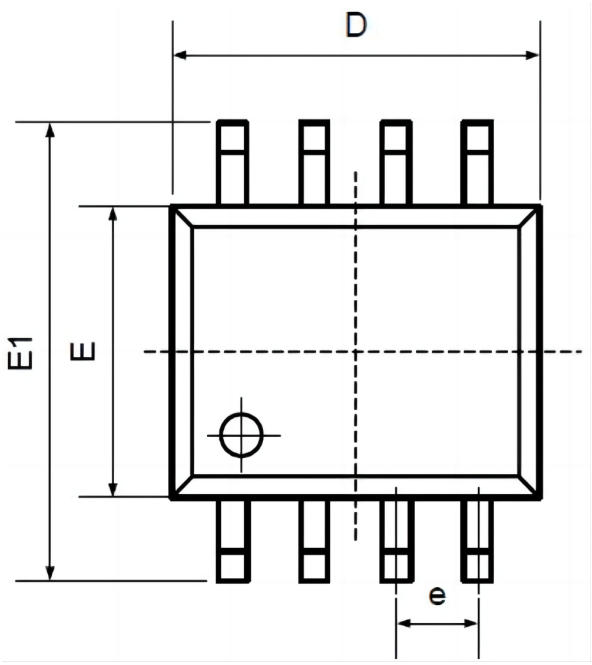


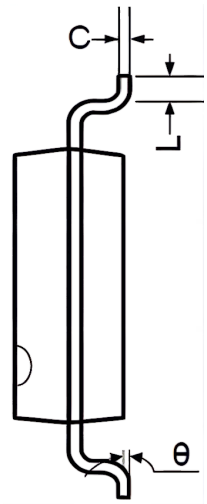
图 7-2. Schematic of Inputs and Outputs

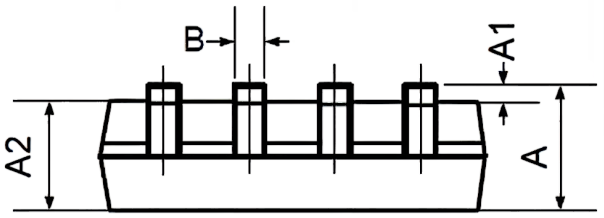
Order information

Order Number	Package	Package Quantity	Marking On The park
SN65LBC184DR-TUDI	SOP8	Tape,Reel,2500	SN65LBC184DR
SN65LBC184P-TUDI	DIP8	Tube,50,A box of 2000	SN65LBC184P
SN75LBC184DR-TUDI	SOP8	Tape,Reel,2500	SN75LBC184DR
SN75LBC184P-TUDI	DIP8	Tube,50,A box of 2000	SN75LBC184P

Package SOP8

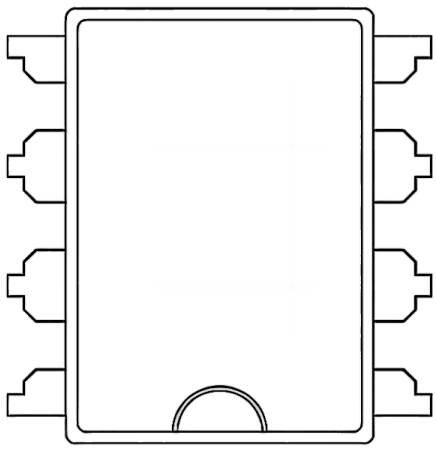


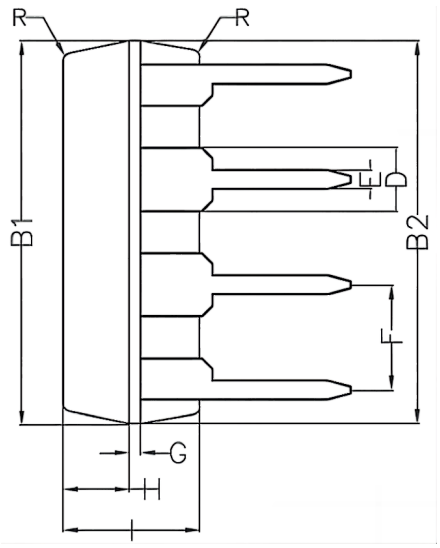


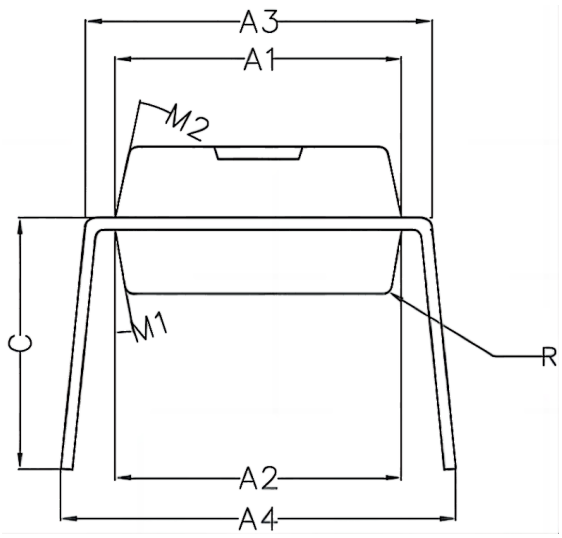


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package DIP8







Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

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