

## 36-Channel Intelligent 16-Bit RGB LED Driver

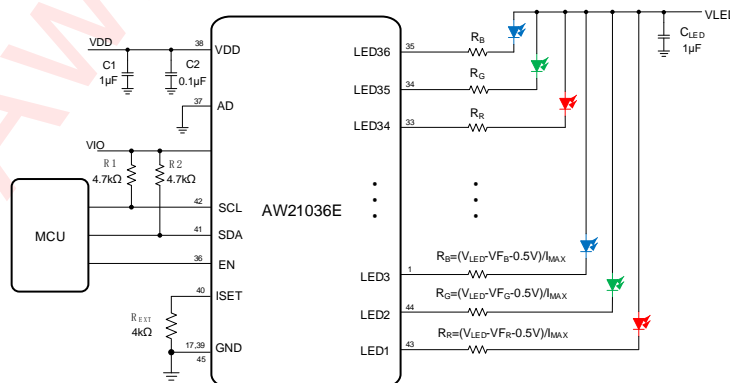
### Features

- 36-channel RGB LED Driver
  - Global 256-level DC current configuration
  - Maximum individual 65536-level PWM for dimming
  - Individual 256-level current for color-mixing
- High-precision current sinks
  - Device-to-device error:  $\pm 5\%$
  - Channel-to-channel error:  $\pm 5\%$
- EMI and audible noise reduction
  - Spread spectrum function
- Flexible LED lighting pattern control
- LED open/short detection per channel
- Auto power saving mode when all LEDs off > 32ms
- Over-temperature protection
- 400kHz I<sup>2</sup>C interface, 4 selectable addresses
- Power supply: 2.7V~5.5V
- QFN 5mmX5mmX0.75mm-44L package

### Applications

Smart speaker  
E-sports devices  
Smart home appliance

### Typical Application Circuit



Note: The resistors ( $R_b, R_g, R_r$ ) between LED and IC are only for thermal reduction. For more information, please refer to application information.

Figure 1 AW21036E Application Circuit

### General Description

AW21036E is a 36-channel high precision constant current LED driver. Each channel has individual 8-bit DC current setting for color-mixing and 16-bit PWM current for brightness control. The maximum global current of each channel is recommended to be 50mA configured via internal register and external resistor  $R_{EXT}$ .

Group control mode, autonomous breathing pattern and rapid RGB control mode are provided for flexible, high efficiency lighting effect programming and fast display updating.

Programmable spread spectrum technology are utilized to reduce EMI and audible noise caused by MLCC when LEDs turn on or off simultaneously.

AW21036E can be turned off with minimum current consumption by either pulling the EN pin low or setting bit GCR.CHIPEN=0.

AW21036E is available in QFN 5mmX5mmX0.75mm-44L package. It operates from 2.7V to 5.5V over the temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

### Pin Configuration And Top Mark

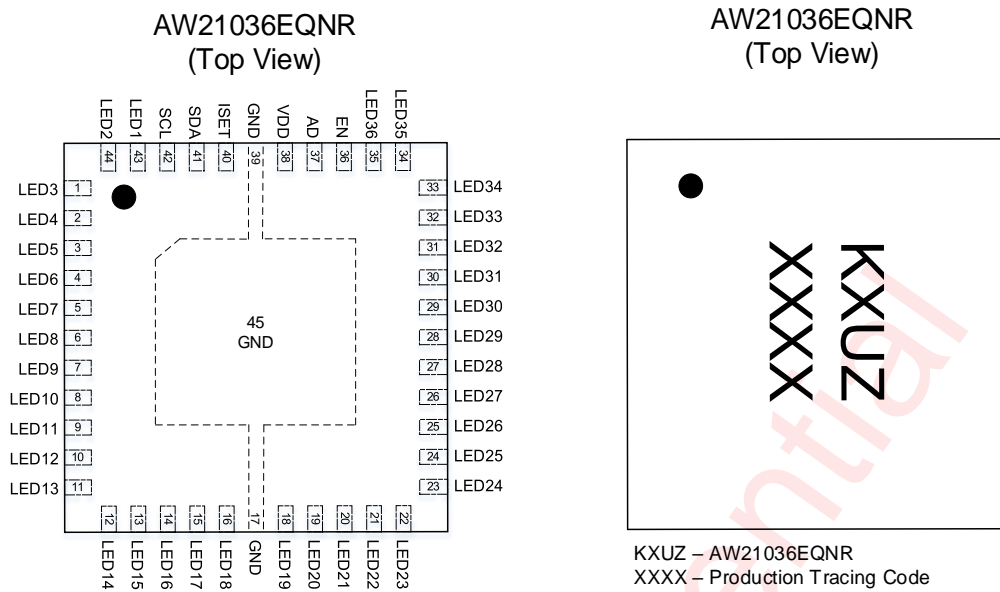


Figure 2 Pin Configuration and Marking

## Pin Definition

No.	NAME	DESCRIPTION
1~16	LED3~LED18	Constant current sink, connect to LED's cathode.
17, 39	GND	Ground.
18~35	LED19~LED36	Constant current sink, connect to LED's cathode.
36	EN	Shutdown the chip when pulled low.
37	AD	I <sup>2</sup> C address setting, connects to GND, VDD, SCL or SDA for different device address of I <sup>2</sup> C. Internally pulled down to GND with a resistor of 1M $\Omega$ .
38	VDD	Power supply: 2.7V~5.5V
40	ISET	When R <sub>EXT</sub> =4.0k $\Omega$ , global current of LED is 20mA.
41	SDA	Serial data I/O for I <sup>2</sup> C interface.
42	SCL	Serial clock input for I <sup>2</sup> C interface.
43, 44	LED1, LED2	Constant current sink, connect to LED's cathode.
45	GND	Ground.

## Functional Block Diagram

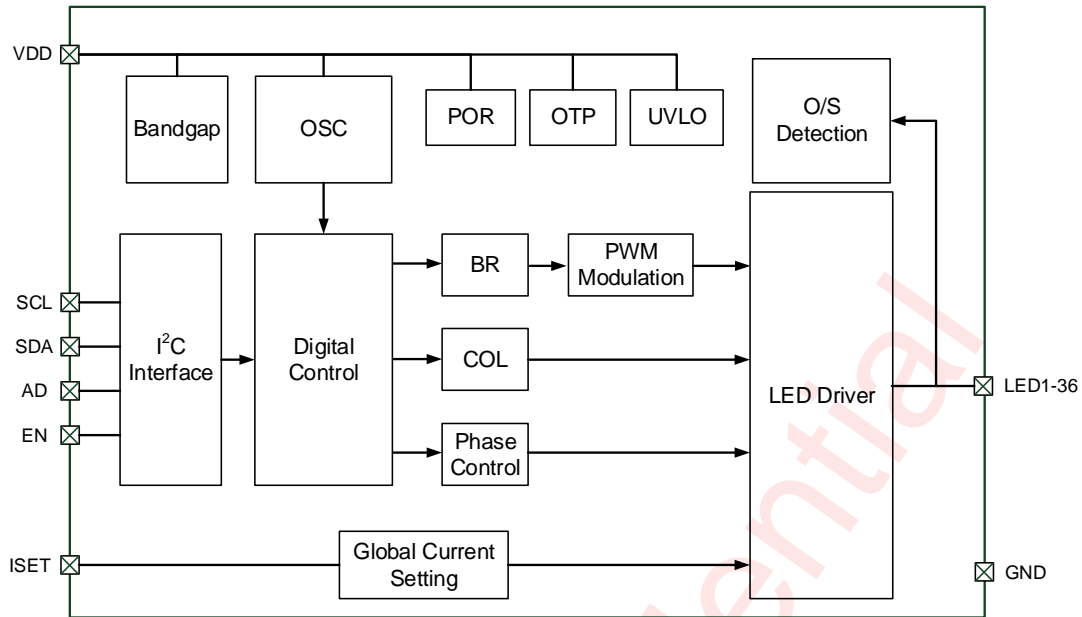
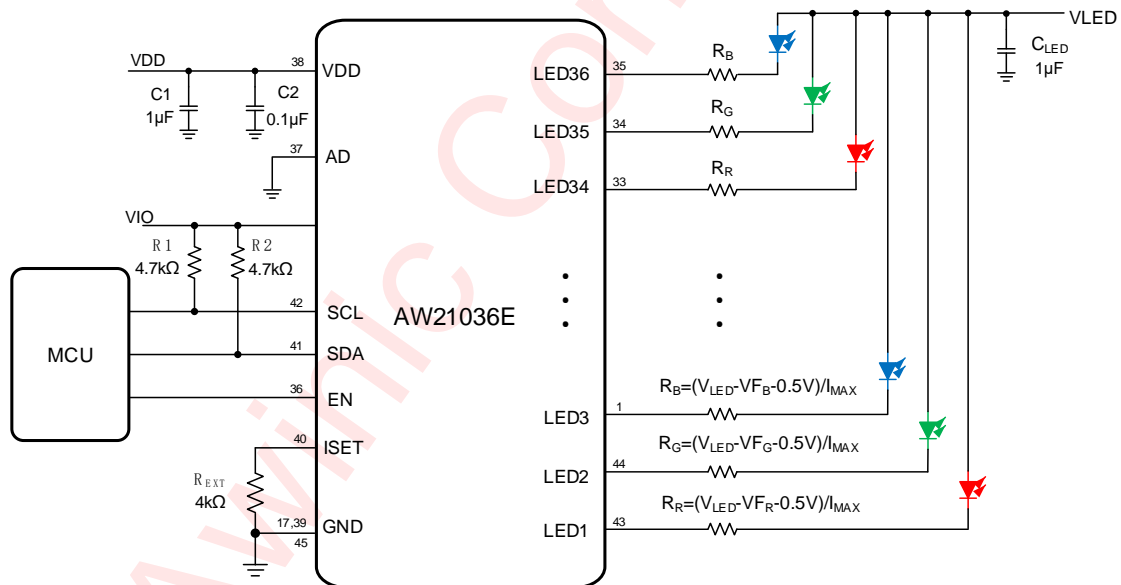


Figure 3 Functional Block Diagram

### Typical Application Circuits



Note: The resistors (R<sub>R</sub>, R<sub>G</sub>, R<sub>B</sub>) between LED and IC are only for thermal reduction. For more information, please refer to application information.

Figure 4 AW21036E Application Circuit

## Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW21036EQNR	-40°C~85°C	QFN 5X5-44L	KXUZ	MSL3	ROHS+HF	6000 units/ Tape and Reel

## Absolute Maximum Ratings<sup>(NOTE1)</sup>

PARAMETERS		RANGE
Supply voltage range VDD		-0.3V to 6V
Input voltage range	SCL, SDA, EN, AD	-0.3V to VDD
Output voltage range	LED1~LED36	-0.3V to VDD
Junction-to-ambient thermal resistance $\theta_{JA}$		43.07°C/W
Operating free-air temperature range		-40°C to 85°C
Maximum operating junction temperature $T_{JMAX}$		160°C
Storage temperature $T_{STG}$		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD (NOTE 2)		
HBM		±2kV
CDM		±1.5kV
Latch-Up		
Test condition: JEDEC EIA/JESD78E		+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ANSI/ESDA/JEDEC JS-001-2017(HBM) JEDEC EIA/JESD22-C101F(CDM).

## Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_A$	Operating free-air temperature range	-40		85	°C
VDD	Input voltage	2.7		5.5	V
LED1~LED36	Voltage on LEDx	0		5.5	V
$C_1, C_{LED}$	Input capacitance	1		22	μF
$C_2$	Input capacitance	0.1		1	μF
$R_1, R_2$	External resistor for I <sup>2</sup> C	1	4.7	10	kΩ
$R_{EXT}$	External resistor for setting sink current	1.6	4	20	kΩ

## Electrical Characteristics

T<sub>A</sub>=25°C, R<sub>EXT</sub>=4kΩ, BRRES=16bit, VDD=3.6V (unless otherwise noted).

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
<b>Power supply voltage and current</b>						
VDD	Power supply voltage	2.7		5.5	V	
I <sub>STB_VDD</sub>	Standby current of VDD	V <sub>EN</sub> =3.6V, CHIPEN=0		3	10	μA
	Power-save mode current consumption	V <sub>EN</sub> =3.6V, GCR.APSE=1, All LEDs off >32ms		3	10	μA
I <sub>ACT_VDD</sub>	Quiescent current in active mode	V <sub>EN</sub> =VDD, GCR.CHIPEN=1,		2	4	mA
		V <sub>EN</sub> =VDD, GCR.CHIPEN=1, GCCR.GCC=0xFF, COL <sub>x</sub> =0xFF		10	12	mA
I <sub>LEAKAGE</sub>	Output leakage current	V <sub>EN</sub> =0V, VLED <sub>x</sub> =5.5V		0.1	1	μA
I <sub>MAX</sub>	Maximum global current of LED <sub>x</sub>	GCCR.GCC=0xFF, BR <sub>x</sub> =COL <sub>x</sub> =0xFF	-5%	20.0	+5%	mA
I <sub>MATCH</sub>	Output current match accuracy	GCCR.GCC=0xFF, COL <sub>x</sub> =0xFF, BR <sub>x</sub> =0xFFFF	-5		+5	%
V <sub>DROPOUT</sub>	Dropout voltage when the LED current has dropped 10%	I <sub>LED<sub>x</sub></sub> =20mA		120	250	mV
F <sub>OSC</sub>	OSC clock frequency		-5%	16	+5%	MHz
T <sub>SD</sub>	Thermal shutdown threshold			150		°C
	Thermal shutdown hysteresis			20		°C
<b>AD, EN</b>						
V <sub>IL</sub>	Input low level	AD, EN			0.4	V
V <sub>IH</sub>	Input high level	AD, EN	1.2			V
R <sub>ADPD</sub>	Internal pull down resistance	AD, VDD=3.6V		1M		Ω
R <sub>ENPD</sub>	Internal pull down resistance	EN, VDD=3.6V		400k		Ω
<b>I<sup>2</sup>C Interface</b>						
V <sub>OL</sub>	Output low level	SDA, I <sub>OL</sub> = 10 mA			0.1	V
V <sub>IH</sub>	Input high level	SCL, SDA	1.2			V
V <sub>IL</sub>	Input low level	SCL, SDA			0.4	V

## I<sup>2</sup>C Interface Timing

PARAMETER		MIN	TYP	MAX	UNIT
F <sub>SCL</sub>	Interface Clock frequency	-		400	kHz
T <sub>HD:STA</sub>	(Repeat-start) Start condition hold time	0.6		-	μs
T <sub>LOW</sub>	Low level width of SCL	1.3		-	μs
T <sub>HIGH</sub>	High level width of SCL	0.6		-	μs
T <sub>SU:STA</sub>	(Repeat-start) Start condition setup time	0.6		-	μs
T <sub>HD:DAT</sub>	Data hold time	0		-	μs
T <sub>SU:DAT</sub>	Data setup time	0.1		-	μs
T <sub>R</sub>	Rising time of SDA and SCL	-		0.3	μs
T <sub>F</sub>	Falling time of SDA and SCL	-		0.3	μs
T <sub>SU:STO</sub>	Stop condition setup time	0.6		-	μs
T <sub>BUF</sub>	Time between start and stop condition	1.3		-	μs

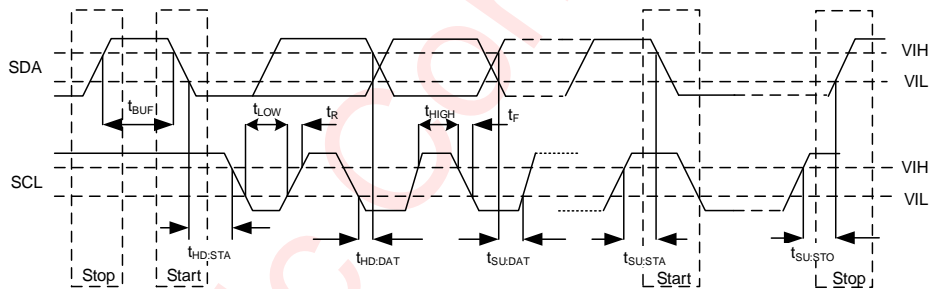


Figure 5 I<sup>2</sup>C Interface Timing

## Detailed Functional Description

### Operation Mode and Reset

#### Power On Reset

Upon initial power-up, the AW21036E is reset by internal power-on-reset, and all registers are reset to default value, and LED driver is shut down.

Once the supply voltage VDD drops below the threshold voltage  $V_{POR\_VDD}$  (2.0V), the power-on-reset will be activated to reset the device again. By reading the bit PORST of the register UVCR (address 79h), whether the device has been reset can be determined.

Below is the recommended operation timing:

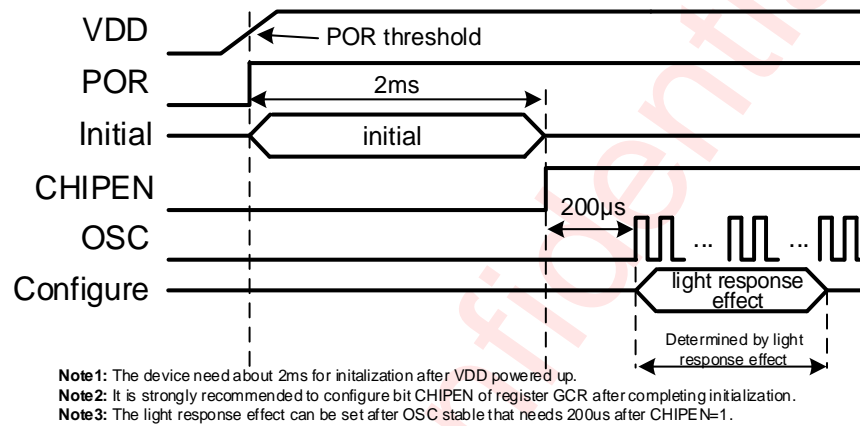


Figure 6 Power Up Timing

#### Software Reset

By writing 00H to register RESET (address 7Fh), the software reset is triggered. After software reset, all registers will be reset to the default value and enter into standby mode.

After the software reset command is input through I<sup>2</sup>C or power on reset, it needs to wait at least 2ms before any other I<sup>2</sup>C command can be accepted.

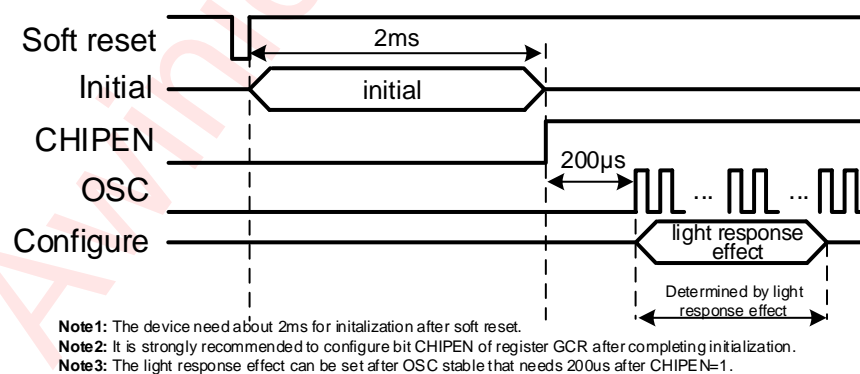


Figure 7 Software Reset Timing

#### Standby Mode

The AW21036E enters into standby mode after VDD powered up. In standby mode all analog blocks except POR are powered down. I<sup>2</sup>C interface is accessible and all registers can be configured.

**Active Mode**

When EN is in high level, and the bit CHIPEN of the register GCR (address 00h) is set to "1", the AW21036E enters into the active mode.

**Auto Power-Save Mode**

The bit APSE of the register GCR (address 00h) is set to "1", the auto power-save mode is enabled. When all LEDs are off and the value of all register BR0~BR35 are 0x00 for more than 32ms, AW21036E automatically enters into standby mode for power saving. Once writing a non-zero value into any register among BR0~BR35, the device exits power-save mode immediately.

In addition, the auto power-save mode is disabled under autonomous breathing mode.

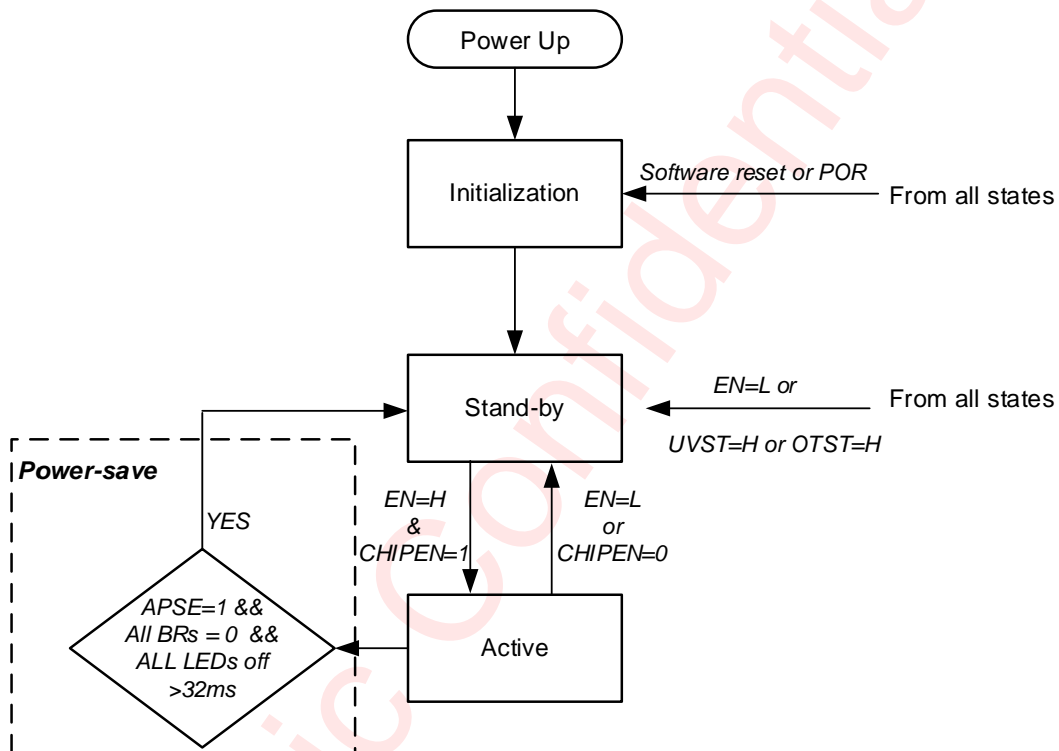


Figure 8 AW21036E Operating Mode Transition

## I<sup>2</sup>C Interface

The AW21036E supports the I<sup>2</sup>C protocol. The maximum frequency supported by the I<sup>2</sup>C is 400kHz. The pull-up resistor for the SDA and SCL can be selected from 1kΩ to 10kΩ. Usually, 4.7kΩ is recommended for 400kHz I<sup>2</sup>C. The voltage from 1.8V to 3.3V is allowed for the I<sup>2</sup>C interface. Additionally, the I<sup>2</sup>C device supports continuous read and write operations.

### Device Address

The I<sup>2</sup>C device address is 7-bit (A7~A1), followed by a R/W bit A0 (Read=1/Write=0). Set A0 to “0” for writing and “1” for reading. The values of bit A1 and bit A2 are depended on the connection of pin AD, there are 4 options: VDD, GND, SCL and SDA. The A7 to A3 is “01101” constantly. The device also supports using a broadcast slave address of 1Ch to access registers. All slave addresses as followed.

AD PIN	A7:A3	A2:A1	A0	Device Address	Broadcast Address
GND	01101	00	0/1	34h	1Ch
VDD		01		35h	
SCL		10		36h	
SDA		11		37h	

### I<sup>2</sup>C Start/Stop

I<sup>2</sup>C start: SDA changes from high level to low level when SCL is high level.

I<sup>2</sup>C stop: SDA changes from low level to high level when SCL is high level.

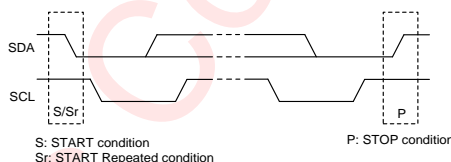


Figure 9 I<sup>2</sup>C Start/Stop Condition Timing

### Data Validation

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

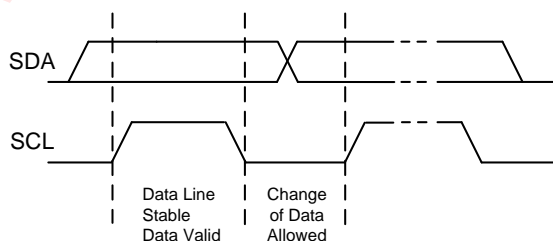


Figure 10 Data Validation Diagram

### ACK (Acknowledgement)

ACK means the successful transfer of I<sup>2</sup>C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is sent and I<sup>2</sup>C stop is not sent by master, slave device sends the next data. If ACK is not sent by master, slave device stops to send data and waits for I<sup>2</sup>C stop.

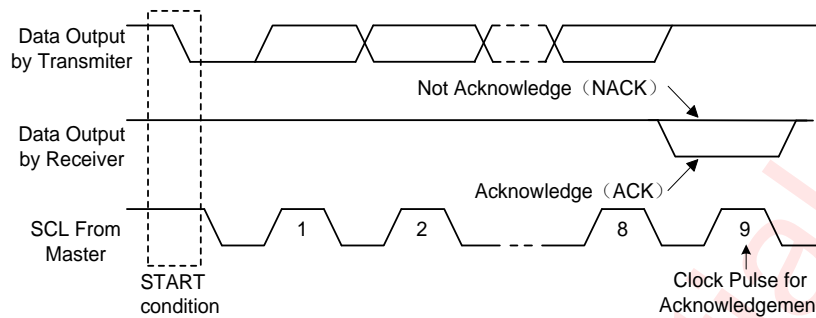


Figure 11 I<sup>2</sup>C ACK Timing

### Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

- Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.
- Master device sends slave address (7-bit) and the data direction bit (R/W = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8-bit).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step f and g).
- Master generates STOP condition to indicate write cycle end.

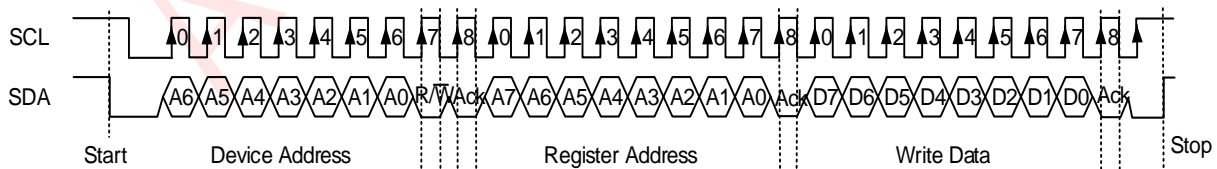


Figure 12 I<sup>2</sup>C Write Byte Cycle

### Read Cycle

In a read cycle, the following steps should be followed:

- Master device generates START condition.
- Master device sends slave address (7-bit) and the data direction bit (R/W = 0).

- c) Slave device sends acknowledge signal if the slave address is correct.
- d) Master sends control register address (8-bit).
- e) Slave sends acknowledge signal.
- f) Master generates STOP condition followed with START condition or REPEAT START condition.
- g) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).
- h) Slave device sends acknowledge signal if the slave address is correct.
- i) Slave sends data byte from addressed register.
- j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.
- k) If the master device generates STOP condition, the read cycle is ended.

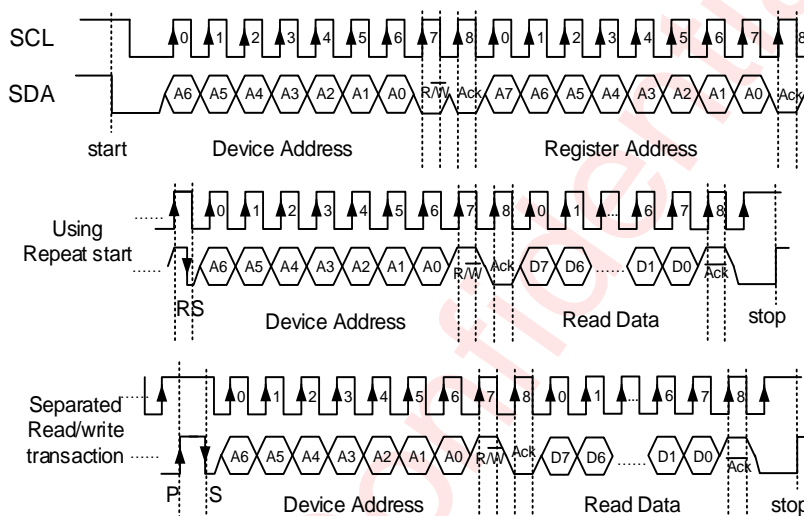


Figure 13 I<sup>2</sup>C Read Byte Cycle

## Under Voltage Lock Out (UVLO)

When bit UVDIS of the register UVCR (address 79h) is set to “0”, the device monitors the voltage of VDD. If the voltage drops below threshold (2.4V typically), the bit UVST of the register UVCR (address 79h) will be set to “1”. After read-out, the register UVCR will be clear.

If both bit UVDIS and bit UVPD of the register UVCR (address 79h) is set to “0”, UVLO protection function is enabled. Once the event of under voltage occurs, the bit CHIPEN of the register GCR (address 00h) will be cleared to “0”, and then the device will enter into standby mode. If the voltage of VDD rises above the UVLO threshold and then write “1” to bit CHIPEN, the device will enter into active mode again.

By default, control bits UVDIS, UVPD are all “0”. Both UVLO monitor and protection are enabled.

## Over Temperature Protection (OTP)

When bit OTDIS of the register OTCR (address 77h) is set to “0”, the over-temperature detection is enabled. Once the temperature of this device reaches 150°C, the over-temperature condition is detected, and the bit OTST of the register OTCR (address 77h) will be set to “1”. The OTST will be cleared to “0” after reading the register OTCR.

If both bit OTDIS and bit OTPD of the register OTCR (address 77h) is set to “0”, the Over-Temperature Protection (OTP) function is enabled. Once the event of over-temperature occurs, the bit CHIPEN of the register GCR (address 00h) will be cleared to “0”, and then the device will enter into standby mode. When the temperature returns below 130°C, the device will enter into active mode again after writing “1” to bit CHIPEN.

By default, control bits OTDIS and OTPD are all “0”, both OT monitor and OT protection are enabled.

## LED Open/Short Detection

AW21036E supports LED open/short detection. When bit OSDE[1:0] of the register OSDCR(address 71h) is set to “11”, open detection is enabled, and the detection results can be read out via the registers OSST0~4 (72h~76h). Similarly, when set bit OSDE [1:0] of the register OSDCR (address 71h) to “10”, short detection is enabled, and the results also can be read out via the registers OSST0~4.

We recommend the bit PWMDIS [6:5] of the register SSCR (address 78h) being set to “11” and maintain about 1mA current of each LED when the open/short function is enabled.

## Current setting

The average output current of LED<sub>n</sub> (n=1, 2, ..., 36) can be expressed by the following formula,

$$I_{OUT(n)} = \frac{K}{R_{EXT}} * \frac{GCC}{255} * \frac{WB}{255} * \frac{COLn}{255} * \frac{BRn}{65536} \quad n=1, 2, 3, \dots, 36$$

Where K=80V, R<sub>EXT</sub> is the value of external resistor, GCC is the 8bit global current configured by the register GCCR (address 6Eh), WB is 8bit white balance parameter configured by the register WBR/WBG/WBB (address 90h/91h/92h), COL<sub>n</sub> is 8bit individual constant current parameter, and BR<sub>n</sub> is 16bit individual PWM modulated current parameter.

The average output current is determined by the global current(controlled by R<sub>EXT</sub>, GCC, WB and COL) and PWM duty cycle(controlled by BR). For example R<sub>EXT</sub>=4kΩ, GCC=COL=WB=0xFF, BR=0xFFFF. The global current is 20mA, the average output current is slightly less than 20mA because the maximum PWM duty cycle(=65535/65536) can't reach 100%.

**Note:** If application needs 100% duty cycle please refer to PWM Disable.

AW21036E supports white balance calibration via 3 registers consisting of register WBR, WBG, and WBB. Therein, WBR is used for LED<sub>x</sub> (X=1, 4, 7, ..., 34), WBG is used for LED<sub>y</sub> (Y=2, 5, 8, ..., 35), WBB is used for LED<sub>z</sub> (Z=3, 6, 9, ..., 36). The default value of registers WBR/WBG/WBB is 0xFF.

Each LED current of AW21036E features 8bit DC current and 16bit PWM modulated current that are decided by COL source and BR source respectively. The BR and COL sources are as follows.

Mode	General Mode			Breathing Pattern Controller (BPC)			Group Control Mode		
Parameter	GEn=0			GEn=1 and PATEN=1			GEn=1 and PATEN=0		
Source	BR Source		COL Source	BR Source	COL Source		BR Source	COL Source	
LED NO.	RGBMD=0	RGBMD=1			GCOLDIS=0	GCOLDIS=1		GCOLDIS=0	GCOLDIS=1
#1	BR0	BR0	COL0	BPC	GCOLR	COL0	FADE	GCOLR	COL0
#2	BR1	BR0	COL1		GCOLG	COL1		GCOLG	COL1
#3	BR2	BR0	COL2		GCOLB	COL2		GCOLB	COL2
#4	BR3	BR1	COL3		GCOLR	COL3		GCOLR	COL3
#5	BR4	BR1	COL4		GCOLG	COL4		GCOLG	COL4
#6	BR5	BR1	COL5		GCOLB	COL5		GCOLB	COL5
...	...	...	...		...	...		...	...
#34	BR33	BR11	COL33		GCOLR	COL33		GCOLR	COL33
#35	BR34	BR11	COL34		GCOLG	COL34		GCOLG	COL34
#36	BR35	BR11	COL35		GCOLB	COL35		GCOLB	COL35

### Notes:

GEn (n=0~7) refers to BPC/Group-Control-Mode control bit in register GCFG0 (address ABh). PATEN is BPC

control bit in register PATCFG (address A0h), GCOLDIS is group color disable bit in register GCFG1(address ACh), GCOLR/GCOLG/GCOLB is for group color control decided by register GCOLR/GCOLG/GCOLB (address A8h~A9h). More details will be introduced later.

BRn includes 8bit BRn\_L and 8bit BRn\_H; FADE includes 8bit FADEL and 8bit FADEH.

## Update

After configuring the BR parameters, should write 0x00 to register UPDATE (address 49h) to update the data.

## PWM Modulation

### PWM Frequency

The PWM frequency is decided by bits CLKFRQ[2:0] and BRRES[1:0] in register GCR (address 00h). Following table shows the relationship of PWM frequency, the CLKFRQ[2:0] and BRRES[1:0]. To avoid the MLCC audible noise, it's recommended to use the PWM frequency lower than 500Hz or higher than 20kHz.

BR Resolution	CLKFRQ[2:0]							
	000	001	010	011	100	101	110	111
8bit	62k	32k	4k	2k	1k	500	244	122
9bit	32k	16k	2k	1k	488	244	122	-
12bit	4k	2k	244	122	-	-	-	-
16bit	244	122	-	-	-	-	-	-

### PWM Disable

If the bits PWMDIS0~2 in register SSCR (address 78h) is set to "111", the PWM output is disabled, and the duty of each PWM is forced to 100%. In this mode, the BR parameter is not valid, but the COL parameter is still effective. And the PWM outputs of LED1~12, LED13~24 and LED25~36 enabled or not are decided by PWMDIS0/PWMDIS1/PWMDIS2 respectively.

It should be noted that when performing open-short detection, the bits PWMDIS0~2 need to be set to "111".

### Spread Spectrum

PWM is a troublesome for some application which is concerned about EMI. AW21036E has spread spectrum function to optimize the EMI performance. If bit SSE in register SSCR (address 78h) is set to "1", spread spectrum function is enabled. By setting the bit SSR in register SSCR, four spread spectrum range 5%/15%/25%/35% can be selected. The total electromagnetic emitting energy can spread into a wider range of frequency band that significantly degrades the peak energy of EMI.

## RGB Configure Mode

To achieve fast register configuration for RGB applications, AW21036E provides an RGB configuration mode by setting the bit RGBMD in register GCR2 (address 7Ah). In RGB mode, every 3 adjacent LEDs share a same BR parameter.

If RGBMD=1, register BR0~BR11 configure brightness parameters for corresponding 12 RGB groups (every 3 adjacent LEDs form a RGB group). In other words, in RGB mode, only registers BR0~BR11 need to be configured, and the registers BR12~BR35 not valid any more.

If RGBMD=0, register BR0~BR35 configure brightness parameters for corresponding 36 LEDs independently, more details as follows.

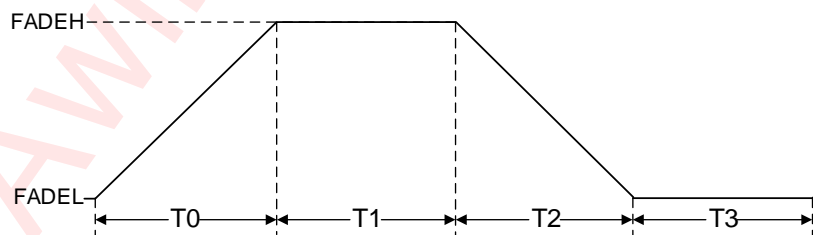
LED No.	BR parameter source	
	RGBMD=0	RGBMD=1
#1	BR0	BR0
#2	BR1	
#3	BR2	
#4	BR3	BR1
#5	BR4	
#6	BR5	
...	...	...
#34	BR33	BR11
#35	BR34	
#36	BR35	

## Pattern Controllers

There is a breathing pattern controller (BPC) in the device. When bit PATEN in register PATCGF (address A0h) is set to “1”, breathing pattern controller is enabled. Pattern controller can be configured as autonomous breathing mode or manual-controlled mode. Each RGB consisting of every three adjacent LEDs can be configured as pattern controlled mode or normal mode by register GCFG0~1. For example, when setting GCFG0 = 0x01, GCFG1 = 0x00 and PATEN=1, the RGB1 which consists of LED1~LED3 will work in BPC mode and other LED will work in normal mode.

### Autonomous Breathing Mode

When bit PATMD in register PATCFG is set to “1”, the pattern controller works in autonomous breathing mode. In this mode, the pattern controller will generate a breathing lighting effect, which is configured by the user-defined timing parameter. The waveform of the breathing lighting effect is shown in the following figure. The parameter T0~T3 define 4 key periods in a complete breathing cycle. T0~T3 composite a breathing loop, denoting the rise-time, on-time, fall-time and off- time respectively. Register FADEH (A6h) and FADEL (A7h) control the max and min brightness of the breathing respectively.



**Figure 14 LED Breath Timing in Pattern Mode**

The start point and end point of autonomous breathing loop are configurable. The loop starting point could be selected among T0~T3, which is set by bits LB [1:0] in register PATT2 (address A4h). The end point of the loop can only be selected between the end of T0 and the end of T2, which is determined by bits LE [1:0] in register PATT2. The repeat times is determined by the end point defined. If bits LE [1:0] is not “00”, the end point of breathing loop is the end of T0, and the loop counter increment by 1 at the end of T0. If bit LE [1:0] is “00”, the loop end point is the end of T2, and the loop counter increment by 1 at the end of T2.

The repeat times is decided by bit RPT [11:8] of register PATT2 (address A4h) and RPT [7:0] of register PATT3

(address A5h). When setting RPT [11:0] to "0", the breathing pattern will run unlimited times.

After the breathing pattern is over, the status bit ENDFLAG in register PATGO (address A2h) will be set to "1", and ENDFLAG will be cleared to "1" after reading out through I<sup>2</sup>C bus. Once breathing loop start again or pattern controller switches to manual mode by setting PATMD bit to "0", the ENDFLAG will also be cleared.

When bit RUN in register PATGO is set to "1", breathing pattern is started. The full process of the autonomous breathing is as follows:

- Set GCOLR/G/B, FADEH/L parameter.
- Set GCFG0 to select the LED in breathing pattern mode or not.
- Configure PATT0, PATT1, PATT2, and PATT3 for parameters T0~T3, start/stop point, and repeat times.
- Set PATEN=1 to enable breathing pattern mode.
- Set PATMD=1 and RAMPE=1 to select auto breathing mode and enable breathing ramp.
- Set RUN=1 to start the breath pattern.

### Manual Control Mode

If bit PATMD is set to "0", manual control mode is selected. In manual control mode, user could program the bit SWITCH of register PATCFG to control the output of pattern controller. When bit SWITCH is "1", the output of pattern controller is decided by register FADEH. When bit SWITCH is set as "0", the output is the decided by register FADEL.

If bit RAMPE in register PATCFG is set to "1", the smooth ramp up/down will be enabled. At the same time, if SWITCH changes from "0" to "1", the output will be ramp up to FADEH smoothly. Similarly, if SWITCH changes from "1" to "0", the output of the pattern controller will ramp down to FADEL smoothly.

However, if the RAMPE is set to "0", the output of the pattern controller will change to FADEH or FADEL directly with no ramp as the SWITCH changes.

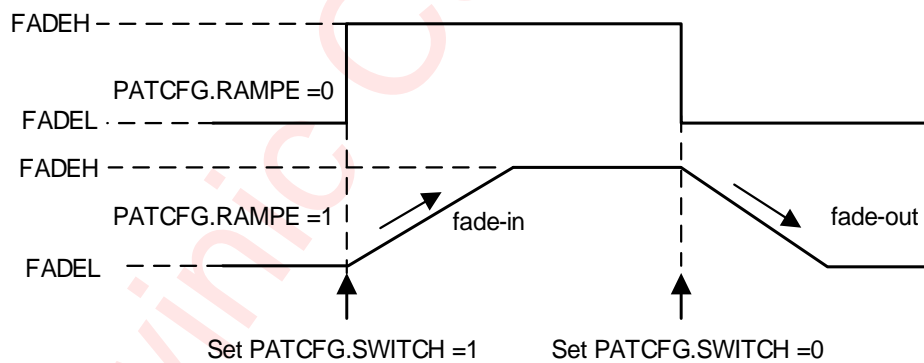


Figure 15 Manual Control Mode

## Register Configuration

## Register List

ADDR	NAME	W/R	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default		
00H	GCR	W/R	APSE	CLKFRQ			-	BRRES		CHIPEN	00H		
01H	BR0_L	W/R	BR0_L									00H	
02H	BR0_H	W/R	BR0_H									00H	
...	...	...	...									00H	
47H	BR35_L	W/R	BR35_L									00H	
48H	BR35_H	W/R	BR35_H									00H	
49H	UPDATE	W	UPDATE									00H	
4AH ~ 6DH	COL0 ~ COL23	W/R	COL0-COL35									00H	
6EH	GCCR	W/R	GCC									00H	
71H	OSDCR	W/R	-				OTH	STH	OSDE			00H	
72H	OSST0	R	OSST [7:0]									00H	
73H	OSST1	R	OSST [15:8]									00H	
74H	OSST2	R	OSST [23:16]									00H	
75H	OSST3	R	OSST [31:24]									00H	
76H	OSST4	R	OSST [35:32]									00H	
77H	OTCR	W/R	TROF		TRST	OTST	OTPD	OTDIS	TRTH			00H	
78H	SSCR	W/R	-	PWMDIS		SSE	SSR		CLT			00H	
79H	UVCR	W/R	REXT_ST		UVST	PORS T	OCPH	OCPD	UVPD	UVDIS	00H		
7AH	GCR2	W/R	-								RGBMD	00H	
7CH	GCR4	-	-					SRR	SRF			00H	
7EH	VER	R	VERSION									88H	
7FH	RESET	W/R	RESET/ID									18H	
90H	WBR	W/R	WBR									FFH	
91H	WBG	W/R	WBG									FFH	
92H	WBB	W/R	WBB									FFH	
A0H	PATCFG	W/R	-				SWITCH	RAMP E	PATM D	PATEN			00H
A1H	PATGO	W/R	-					ENDF LAG	PATS T	RUN			00H
A2H	PATT0	W/R	T0				T1					00H	
A3H	PATT1	W/R	T2				T3					00H	
A4H	PATT2	W/R	LE		LB		RPT[11:8]					00H	
A5H	PATT3	W/R	RPT[7:0]									00H	
A6H	FADEH	W/R	FADEH									00H	
A7H	FADEL	W/R	FADEL									00H	
A8H	GCOLR	W/R	GCOLR									00H	
A9H	GCOLG	W/R	GCOLG									00H	
AAH	GCOLB	W/R	GCOLB									00H	

ADDR	NAME	W/R	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
ABH	GCFG0	W/R	GE7	GE6	GE5	GE4	GE3	GE2	GE1	GE0	00H
ACH	GCFG1	W/R	-	-	-	GCOL DIS	GE11	GE10	GE9	GE8	00H

## Register Detailed Description

### GCR : Global Control Register(Address 00H)

Bit	Symbol	R/W	Description	Default
7	APSE	RW	Auto power-saving mode enable 0: Disable 1: Enable	0
6:4	CLKFRQ	RW	OSC frequency selection 000: 16MHz 001: 8MHz 010: 1MHz 011: 512kHz 100: 256kHz 101: 125kHz 110: 62.5kHz 111: 31.25kHz	000
3	RESERVED	R	Reserved	0
2:1	BRRES	RW	Brightness resolution selection 00: 8bit 01: 9bit 10: 12bit 11: 16bit	00
0	CHIPEN	RW	Chip enable 0: Disable 1: Enable	0

### BR0~BR35 : BR Register(Address 01H~48H)

Bit	Symbol	R/W	Description	Default
7:0	BRx_L	RW	LSB 8bit BR parameter for LED1~36. BRx_L address: 01h, 03h ..., 47h. After configuring the BR registers, should write 0x00 to register UPDATE to update the data.	0x00
7:0	BRx_H	RW	MSB 8bit BR parameter for LED1~36. After configuring the BR registers, should write 0x00 to register UPDATE to update the data. BRx_H address: 02h, 04h ..., 48h.	0x00

### UPDATE : Update Register(Address 49H)

Bit	Symbol	R/W	Description	Default
7:0	UPDATE	W	Write 0x00 to update BR register.	0x00

**COL0~COL35 : COL Register(Address 4AH~6DH)**

Bit	Symbol	R/W	Description	Default
7:0	COL	RW	Individual 8bit COL parameter for LED1~36.	0x00

**GCCR : Global Control Register(Address 6EH)**

Bit	Symbol	R/W	Description	Default
7:0	GCC	RW	Global current control.	0x00

**OSDCR : Open Short Detect Control Register(Address 71H)**

Bit	Symbol	R/W	Description	Default
7:4	RESERVED	R	Reserved	0000
3	OTH	RW	Open threshold 0: 0.1V 1: 0.2V	0
2	STH	RW	Short threshold 0: VDD-1V 1: VDD-0.5V	0
1:0	OSDE	RW	Open short detect enable 0x: Detect disable 10: Short detect enable 11: Open detect enable	00

**OSST0~3 : Open/Short Status Register (Address 72H~75H)**

Bit	Symbol	R/W	Description	Default
7:0	OSST	R	Open/short status of LED1~LED32 0: No open/short event detected 1: Open/short event detected	0x00

**OSST4 : Open/Short Status Register (Address 76H)**

Bit	Symbol	R/W	Description	Default
7:4	RESERVED	R	Reserved	0000

3:0	OSST	R	Open/short status of LED33~LED36 0: No open/short detected 1: Open/short detected	0000
-----	------	---	-----------------------------------------------------------------------------------------	------

**OTCR : Over Temperature Control Register (Address 77H)**

Bit	Symbol	R/W	Description	Default
7:6	TROF	RW	Thermal roll off percentage of I <sub>OUT</sub> 00: 100% 01: 75% 10: 55% 11: 30%	00
5	TRST	R	Thermal roll off status 0: None roll off 1: Roll off	0
4	OTST	R	Over-temperature status 0: None over-temperature 1: Over-temperature	0
3	OTPD	RW	Over-temperature(OT) protect disable 0: OT protect enable, when OT event occurs, device will clear GCR.CHIPEN to 0. 1: OT protect disable	0
2	OTDIS	RW	Over-temperature detect disable 0: OT detect enable, when OT event occurs, OTCR.OTST will be set. 1: OT detect disable	0
1:0	TRTH	RW	Thermal roll off threshold 00: 140°C 01: 120°C 10: 100°C 11: 90°C	00

**SSCR : Spread Spectrum Control Register (Address 78H)**

Bit	Symbol	R/W	Description	Default
7	PWMDIS2	RW	0: PWM duty of LED 25~36 determined by BR24~BR35 1: PWM duty of LED 25~36 fixed as 100%	0
6	PWMDIS1	RW	0: PWM duty of LED 13~24 determined by BR12~BR23 1: PWM duty of LED 13~24 fixed as 100%	0
5	PWMDIS0	RW	0: PWM duty of LED 1~12 determined by BR0~BR11 1: PWM duty of LED 1~12 fixed as 100%	0
4	SSE	RW	Spread spectrum enable 0: Disable 1: Enable	0

3:2	SSR	RW	Spread spectrum range 00: ±5% 01: ±15% 10: ±25% 11: ±35%	00
1:0	CLT	RW	Spread spectrum cycle time 00: 1980µs 01: 1200µs 10: 820µs 11: 660µs	00

**UVCR : UVLO Control Register (Address 79H)**

Bit	Symbol	R/W	Description	Default
7:6	REXT_ST	R	REXT status 00: Normal 10: REXT is open 01: REXT is short or OCP 11: Not defined	00
5	UVST	R	UVLO status 0: No UVLO detected 1: UVLO detected	0
4	PORST	R	Power-up reset status 0: No power-on reset 1: Power-on reset (cleared after read out)	0
3	OCPH	RW	OCP Threshold 0: 85mA 1: 55mA	0
2	OCPD	RW	OCP disable 0: Enable OCP 1: Disable OCP	0
1	UVPD	RW	UVLO protect disable 0: UVLO protect enable, when under-voltage event occurs, device will clear GCR.CHIPEN to 0. 1: UVLO protect disable	0
0	UVDIS	RW	UVLO detect disable 0: UVLO detect enable, when under-voltage event occurs, UVCR.UVST will be set. 1: UVLO detect disable	0

**GCR2 : Global Control Register 2(Address 7AH)**

Bit	Symbol	R/W	Description	Default
7:1	RESERVED	R	Reserved	0000 000
0	RGBMD	RW	RGB configure mode enable 0: Disable	0

			1: Enable, every 3 LEDs share a common brightness.	
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**GCR4 : Global Control Register 4(Address 7CH)**

Bit	Symbol	R/W	Description	Default
7:3	RESERVED	R	Reserved	0000 0
2	SRR	RW	Slew rate control for LED output rising time 0: 1ns                    1: 6ns	0
1:0	SRF	RW	Slew rate control for LED output falling time 00: 1ns                10: 6ns 01: 3ns                11:10ns	00

**VER : Version Register (Address 7Eh)**

Bit	Symbol	R/W	Description	Default
7:0	VER	R	Chip version	0x88

**RESET : Software Reset Register (Address 7FH)**

Bit	Symbol	R/W	Description	Default
7:0	RESET	RW	Write 00H to the register will reset all registers to their default value. The chip ID 0x18 will be read out from the register.	0x18

**WBR : Red Scaling for White Balance(Address 90H)**

Bit	Symbol	R/W	Description	Default
7:0	WBR	RW	Red Scaling for White Balance.	0xFF

**WBG : Green Scaling for White Balance(Address 91H)**

Bit	Symbol	R/W	Description	Default
7:0	WBG	RW	Green Scaling for White Balance.	0xFF

**WBB : Blue Scaling for White Balance(Address 92H)**

Bit	Symbol	R/W	Description	Default
7:0	WBB	RW	Blue Scaling for White Balance.	0xFF

**PATCFG : Pattern Configure Register(Address A0H)**

Bit	Symbol	R/W	Description	Default
7:4	RESERVED	R	Reserved	0000
3	SWITCH	RW	Switch on or off at manual mode. 0: LED off 1: LED on	0
2	RAMPE	RW	Ramp enable 0: Ramp disable 1: Ramp enable	0
1	MODE	RW	Breath pattern control mode selection 0: Manual mode (default) 1: Auto breath pattern mode	0
0	PATEN	RW	Auto breath pattern controller enable 0: Disable 1: Enable	0

**PATGO : Pattern Configure Register(Address A1H)**

Bit	Symbol	R/W	Description	Default
7:3	RESERVED	R	Reserved	0000 0
2	ENDFLG	R	Auto breath pattern loop end flag 0: Loop is not over 1: Loop is over (will be cleared after reading out)	0
1	STATE	R	Auto breath pattern status 0: Pattern is stop 1: Pattern is running	0
0	RUN	RW	Auto breath pattern run control Write "1" to run auto breath pattern Note: You shall write "0" and then write "1" to this bit to restart a new auto breath pattern.	0

**PATT0 : Pattern Timer0(Address A2H)**

Bit	Symbol	R/W	Description	Default
7:4	RISE	RW	Ramp rise time T0 Time T0 Time 0000 0s 1000 2.1s 0001 0.13s 1001 2.6s	0000

			0010	0.26s	1010	3.1s	
			0011	0.38s	1011	4.2s	
			0100	0.51s	1100	5.2s	
			0101	0.77s	1101	6.2s	
			0110	1.04s	1110	7.3s	
			0111	1.6s	1111	8.3s	
3:0	ON	RW	Hold on time				0000
			T1	Time	T1	Time	
			0000	0.04s	1000	2.1s	
			0001	0.13s	1001	2.6s	
			0010	0.26s	1010	3.1s	
			0011	0.38s	1011	4.2s	
			0100	0.51s	1100	5.2s	
			0101	0.77s	1101	6.2s	
			0110	1.04s	1110	7.3s	
			0111	1.6s	1111	8.3s	

**PATT1 : Pattern Timer1(Address A3H)**

Bit	Symbol	R/W	Description				Default
7:4	FALL	RW	Ramp fall time				0000
			T2	Time	T2	Time	
			0000	0s	1000	2.1s	
			0001	0.13s	1001	2.6s	
			0010	0.26s	1010	3.1s	
			0011	0.38s	1011	4.2s	
			0100	0.51s	1100	5.2s	
			0101	0.77s	1101	6.2s	
			0110	1.04s	1110	7.3s	
			0111	1.6s	1111	8.3s	
3:0	OFF	RW	Hold off time				0000
			T3	Time	T3	Time	
			0000	0.04s	1000	2.1s	
			0001	0.13s	1001	2.6s	
			0010	0.26s	1010	3.1s	
			0011	0.38s	1011	4.2s	
			0100	0.51s	1100	5.2s	
			0101	0.77s	1101	6.2s	
			0110	1.04s	1110	7.3s	
			0111	1.6s	1111	8.3s	

**PATT2 : Pattern Control Register 1(Address A4H)**

Bit	Symbol	R/W	Description	Default
7:6	LE	RW	End point of the auto-breath pattern 00: Pattern finally stop at OFF state Other: Pattern finally stop at ON state	00
5:4	LB	RW	Start point of the auto-breath loop pattern 00: Pattern start from RISE state 01: Pattern start from ON state 10: Pattern start from FALL state 11: Pattern start from OFF state	00
3:0	RPT[11:8]	RW	4 MSB of loop times.	0000

**PATT3 : Pattern Control Register 2 (Address A5H)**

Bit	Symbol	R/W	Description	Default
7:0	RPT[7:0]	RW	8 LSB of auto-breath pattern repeat times Note: when RPT[11:0]=0, the pattern will run forever. In this case, you can switch auto-breath mode to manual mode and then turn the pattern off.	0x00

**FADEH : Maximum Brightness for Auto Breath (Address A6H)**

Bit	Symbol	R/W	Description	Default
7:0	FADEH	RW	Maximum brightness configure for auto breath.	0x00

**FADEL : Minimum Brightness for Auto Breath(Address A7H)**

Bit	Symbol	R/W	Description	Default
7:0	FADEL	RW	Minimum brightness configure for auto breath.	0x00

**GCOLR : Red Mixing for Group Color (Address A8H)**

Bit	Symbol	R/W	Description	Default
7:0	GCOLR	RW	Red mixing for group color.	0x00

**GCOLG : Green Mixing for Group Color(Address A9H)**

Bit	Symbol	R/W	Description	Default
7:0	GCOLG	RW	Green mixing for group color.	0x00

**GCOLB : Blue Mixing for Group Color(Address AAH)**

Bit	Symbol	R/W	Description	Default
7:0	GCOLB	RW	Blue mixing for group color.	0x00

**GCFG0 : Group Configure Register0 (Address ABH)**

Bit	Symbol	R/W	Description	Default
7:0	GE[7:0]	RW	<p>Group-Control-Mode/Pattern-Control-Mode enable for LED1~LED24</p> <p>If bit PATEN in register PATCFG is set to “0”,</p> <p>GE[0]=1: LED1~3 work in group mode            GE[1]=1: LED4~6 work in group mode            GE[2]=1: LED7~9 work in group mode            GE[3]=1: LED10~12 work in group mode            GE[4]=1: LED13~15 work in group mode            GE[5]=1: LED16~18 work in group mode            GE[6]=1: LED19~21 work in group mode            GE[7]=1: LED22~24 work in group mode</p> <p>If bit PATEN in register PATCFG is set to “1”,</p> <p>GE[0]=1: LED1~3 work in auto breath pattern mode            GE[1]=1: LED4~6 work in auto breath pattern mode            GE[2]=1: LED7~9 work in auto breath pattern mode            GE[3]=1: LED10~12 work in auto breath pattern mode            GE[4]=1: LED13~15 work in auto breath pattern mode            GE[5]=1: LED16~18 work in auto breath pattern mode            GE[6]=1: LED19~21 work in auto breath pattern mode            GE[7]=1: LED22~24 work in auto breath pattern mode</p>	0x00

**GCFG1 : Group Configure Register1 (Address ACH)**

Bit	Symbol	R/W	Description	Default
7:5	RESERVED	R	Reserved	000
4	GCOLDIS	RW	<p>Group/pattern color disable</p> <p>0: Group/pattern color enable, all LEDs in group/pattern mode share the common COL parameters decided by GCOL_R/G/B.</p> <p>1: Group/pattern color disable, all LEDs' color parameter in group/pattern mode is configured by their respective register COL.</p>	0
3:0	GE[11:8]	RW	<p>Group-Control-Mode/Pattern-Control-Mode enable for LED25~LED36</p> <p>If bit PATEN in register PATCFG is set to “0”,</p> <p>GE[8]=1: LED25~27 work in group mode</p>	0000

			<p>GE[9]=1: LED28~30 work in group mode GE[10]=1: LED31~33 work in group mode GE[11]=1: LED34~36 work in group mode</p> <p>If bit PATEN in register PATCFG is set to "1", GE[8]=1: LED25~27 work in auto breath pattern mode GE[9]=1: LED28~30 work in auto breath pattern mode GE[10]=1: LED31~33 work in auto breath pattern mode GE[11]=1: LED34~36 work in auto breath pattern mode</p>	
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## Application Information

### R<sub>EXT</sub>

The selection of R<sub>EXT</sub> determined the maximum LED1~LED36 current I<sub>MAX</sub> as described in below formula (1).

$$I_{MAX} = \frac{K}{R_{EXT}} \quad (1)$$

Where K = 80V, the recommended minimum value of R<sub>EXT</sub> is 1.6kΩ.

When R<sub>EXT</sub> = 2kΩ, I<sub>MAX</sub> = 40mA.

When R<sub>EXT</sub> = 4kΩ, I<sub>MAX</sub> = 20mA.

### R<sub>R</sub>, R<sub>G</sub>, R<sub>B</sub>

The resistance(R<sub>X</sub>) used for thermal reduction can be calculated according to the following formula:

$$R_X = \frac{V_{LED} - V_{F_X} - V_{DROPOUT}}{I_{MAX}} \quad (2)$$

V<sub>LED</sub>: LED power supply voltage.

V<sub>F<sub>X</sub></sub>: LED forward voltage.

V<sub>DROPOUT</sub>: Voltage on LED<sub>x</sub>, recommended values is 0.5V.

I<sub>MAX</sub>: Global current.

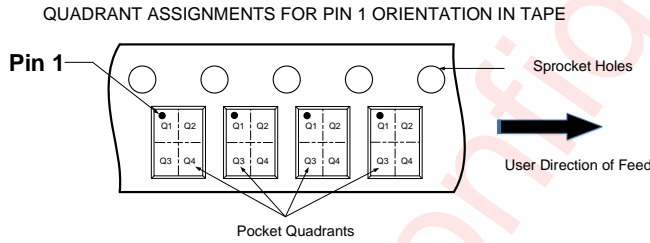
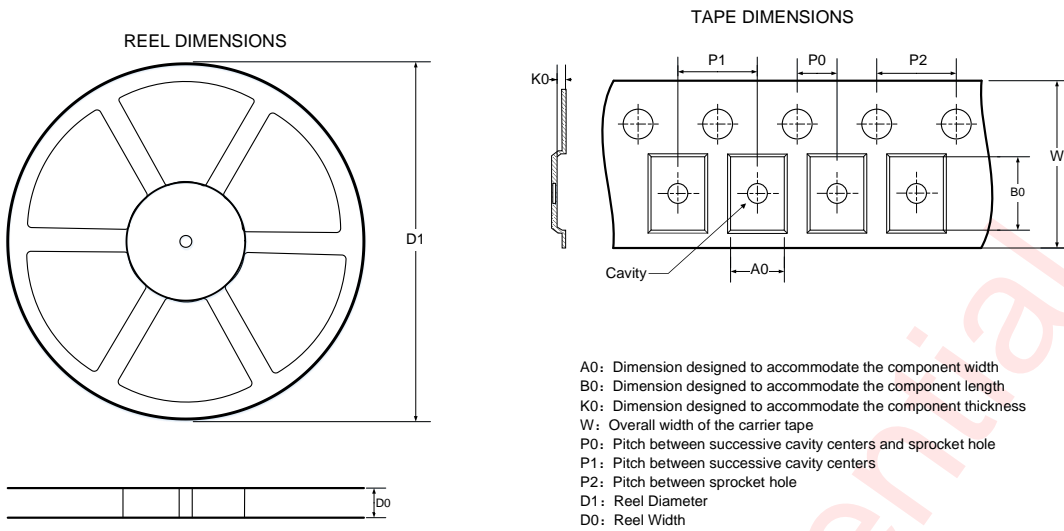
## PCB Layout Consideration

AW21036E is a 36-channel LEDs driver programmed via I<sup>2</sup>C compatible interface. When all LEDs are operating, the device power dissipation is large. To obtain the good thermal performance and avoid thermal shutdown, PCB layout should be considered carefully. Here are some guidelines:

1. The C<sub>1</sub>, C<sub>2</sub>, C<sub>LED</sub> should be placed as close to the chip as possible.
2. The R<sub>EXT</sub> should be placed as close to the chip as possible.
3. The Thermal PAD must be well connecting to the GND of the PCB, and add as many thermal vias as possible beneath the thermal PAD on the PCB for the heat conductivity of the device and PCB.

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## Tape And Reel Information

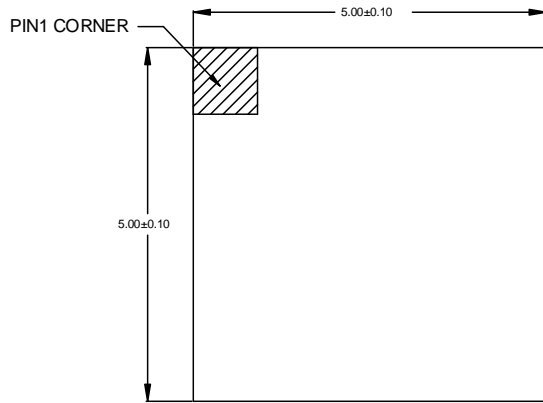


DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	5.3	5.3	1.1	2	8	4	12	Q1

All dimensions are nominal

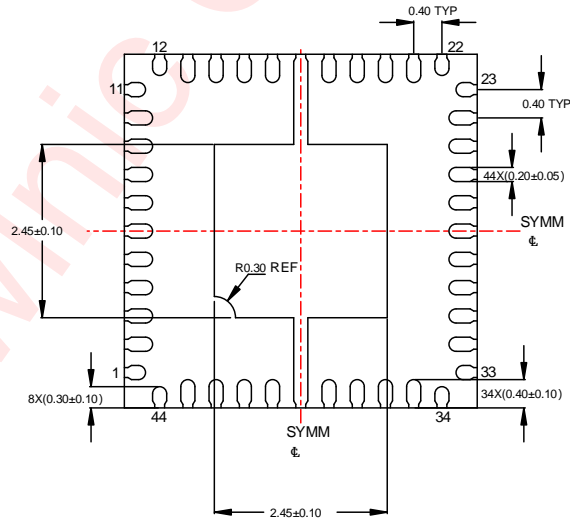
Package Description



Top View



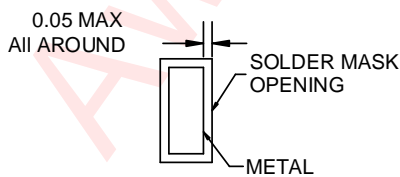
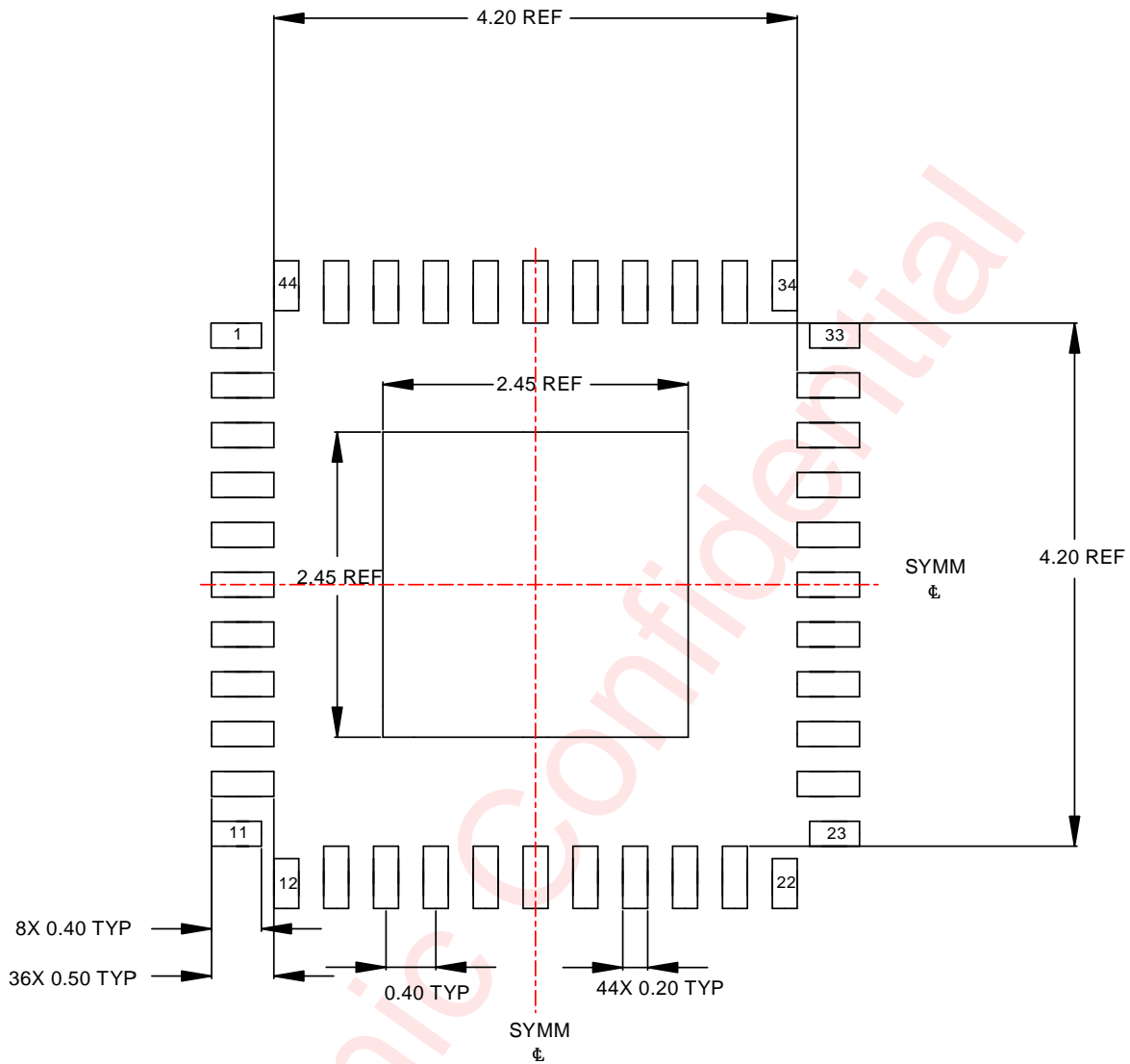
Side View



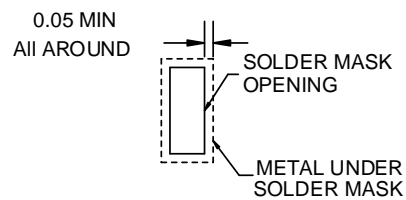
Bottom View

Unit: mm

Land Pattern Data



NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

## Revision History

Version	Date	Change Record
V1.0	May.2019	Officially released
V1.1	Nov.2023	<p>Modified General Description (P1).</p> <p>Modified Typical Application Circuit(replace Iout to I<sub>MAX</sub>) (P1, P3).</p> <p>Modified Pin Configuration And Top Mark (P2).</p> <p>Updated the <math>\theta_{JA}</math> and corrected HBM and CDM test method in the part of Absolute Maximum Ratings (P4).</p> <p>Added Recommended Operating Conditions (P4).</p> <p>Modified test condition and values of Dropout Voltage in EC table (P5).</p> <p>Deleted item I<sub>SD_VDD</sub> in EC table (P5).</p> <p>Modified figure Power Up Timing and Software Reset Timing (P7).</p> <p>Deleted Shutdown Mode (P7).</p> <p>Modified the description of Standby Mode (P7).</p> <p>Added description of the auto power-save mode is disabled under autonomous breathing mode (P8).</p> <p>Modified register BR0~BR23 to register BR0~BR35 (P8).</p> <p>Modified figure AW21036E Operating Mode Transition (P8).</p> <p>Modified bit A7 to A3 is "01101" in Device Address (P9).</p> <p>Modified figure I<sup>2</sup>C Write Byte Cycle (P10).</p> <p>Modified the description of Current Setting (P12).</p> <p>Modified bit RAMPEN to bit RAMPE (P16).</p> <p>Modified register UVCR description (P22).</p> <p>Modified the minimum value of R<sub>EXT</sub> in Application Information (P28).</p> <p>Added thermal reduction resistance formula in Application Information (P28).</p>
V1.2	Apr.2024	<p>Modified the description of Standby Mode (P7).</p> <p>Modified figure AW21036E Operating Mode Transition (P8).</p>
V1.3	Dec.2024	Remove unnecessary registers and functional descriptions (P14).

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