XPC2963

60-V Input 3.5-A Asynchronous Step-Down Converter

FEATURES

- 4.5-V to 60-V input voltage
- Adjustable output voltage from 0.8V to VIN
- ±1% reference accuracy
- Peak current mode control
- Integrated 80mΩ high-Side MOSFET
- Low quiescent current : 100μA
- Low shutdown current : 2μA
- 100kHz to 2.5MHz adjustable switching frequency
- Synchronizes to external clock
- PSM mode for light load operation
- Built-In Spread-Spectrum frequency modulation
- Low dropout at light loads with integrated boot recharge FET
- Option for adjustable soft-start
- Option for power good indication
- Adjustable UVLO and Hysteresis
- Enable control
- Inherent UVLO, UVP, OVP, OCP, OTP

DESCRIPTION

The XPC2963 is a 3.5A, high-efficiency, peak current mode control asynchronous step-down converter. The device operates with input voltages from 4.5V to 60V and is protected from load dump transients up to 65V, eases input surge protection design. The low quiescent current design with the integrated low RDS(ON) of high-side MOSFET achieves high efficiency over the entire load range.

The peak current mode control with simple external compensation allows the use of small inductors and results in fast transient response and good loop stability.

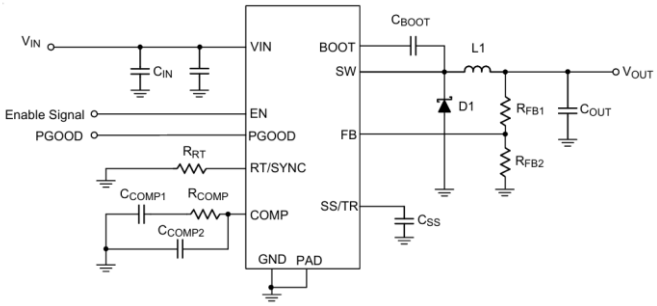
For switching noise sensitive applications, the XPC2963 can be externally synchronized to clock signal from 300kHz to 2200kHz frequency. The build-in spread-spectrum frequency modulation further helps system designers with better EMC management.

The XPC2963 is available in DFN-10 4x4 and SOP-8 (Exposed pad) packages.

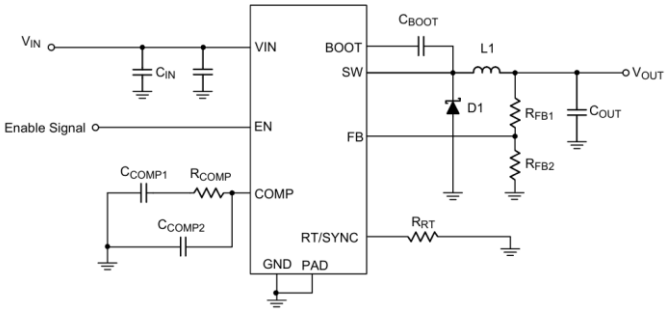
APPLICATIONS

- Communications and industrial 12V, 24V and 48V power systems

TYPICAL APPLICATION



DFN-10 package



SOP-8 package

REVISION HISTORY

Release	Rev	Changes	Date
Released	1.0	Finalized	3/15/2025

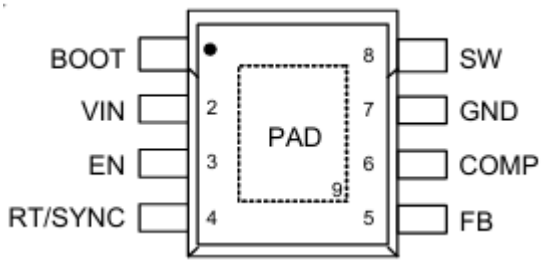
ORDERING INFORMATION

Part Number	Output Current (A)	Package	Top Marking	MPQ
XPC2963D5R	3.5	DFN-10	2963	3,000
XPC2963S5R	3.5	SOP-8	2963	3,000

MPQ = Minimum Packaging Quantity.
For production orders greater than MPQ, the order must be a multiple of MPQ per package size above.

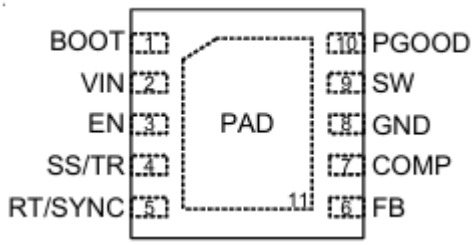
PIN CONFIGURATION AND DESCRIPTION

Top view



SOP-8

Top view



DFN-10

Pin Configuration

Pin No.		Pin Name	Description
SOP-8	DFN-10		
1	1	BOOT	Connect a 100nF ceramic capacitor between this pin and SW pin.
2	2	VIN	Input supply voltage with 4V to 60V operating range.
3	3	EN	Enable terminal, with internal pull-up current source. Pull below 1.2 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors.
-	4	SS/TR	Soft-start and tracking control input. Connect a capacitor from SS to GND to set the soft-start period. ”Do Not” leave this pin floating to avoid inrush current during power up. It also can be used to track and sequence because the SS/TR pin voltage can override the internal reference voltage.
4	5	RT/SYNC	Frequency setting and external synchronous signal input. Connect a resistor from this pin to GND to set the switching frequency. Tie to a clock source for synchronization to an external frequency.
5	6	FB	Output voltage sense. Sense the output voltage at the FB pin through a resistive divider.
6	7	COMP	Compensation node. Connect external compensation elements to this pin to stabilize the control loop.
7	8	GND	Ground.
8	9	SW	Switch node.
-	10	PGOOD	Open-drain power-good indication output.
9 (EP)	11 (EP)	PAD	Exposed pad. The exposed pad is internally unconnected and must be soldered to a large PCB copper area for maximum power dissipation.

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
VIN	-0.3	65	V
EN	-0.3	65	V
PGOOD	-0.3	65	V
SW	-0.3	65	V
SW (t<5ns)	-7	70	V
SW (t<100ns)	-5	70	V
BOOT to SW	-0.3	6	V
All other pins	-0.3	6	V
Lead temperature (soldering, 10 seconds)		260	°C
Storage temperature	-65	+150	°C
Junction temperature		+150	°C
Electrostatic Discharge (HBM)	-2000	+2000	V
Electrostatic Discharge (CDM)	-1000	+1000	V

(1) Operation of the device outside of these parameters may cause permanent damage.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Input voltage	V_{IN}	4		60	V
Output voltage	V_{OUT}	0.8		VIN	V
Junction temperature range	T_{OJ}	-40		150	°C

Thermal Information

Junction to ambient thermal resistance is a function of board layout and ambient air flow condition. This data is based on four layers PCB (30mm x 30mm; 70µm Cu top signal layer) in still air box in accordance with JEDEC standard JESD51 on natural convection.

Parameter	Symbol	DFN-10	SOP-8	Units
Junction-to-Ambient Thermal Resistance	θ_{JA}	30.2	29.8	°C/W
Junction-to-Case (Top) Thermal Resistance	$\theta_{JC(Top)}$	46.6	73.5	°C/W
Junction-to-Case (Bottom) Thermal Resistance	$\theta_{JC(Bottom)}$	3.8	3.5	°C/W

ELECTRICAL SPECIFICATIONS

T_J = -40˚C to 125˚C and V_{IN} = 12V. Typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply						
Quiescent current into VIN	I_Q	No Load, device not switching		100	140	uA
Shutdown current into VIN	I_{SHDN}	EN = Low		2	5	uA
Undervoltage lockout threshold	V_{UVLOH}	V_{IN} rising	4.1	4.3	4.5	V
	V_{UVLOL}	V_{IN} falling	3.8	3.9	4.0	V
Thermal shutdown threshold	T_{JSD}	T_J rising		175		°C
		T_J falling		160		°C
Logic Interface: EN						
Enable threshold voltage	V_{TH_EN}		1.1	1.2	1.3	V
Pull-up current	I_{EN}	V_{TH_EN} + 50mV		-4.6		uA
		V_{TH_EN} − 50mV	-0.58	-1.2	-1.8	uA
Hysteresis current	I_{EN_Hys}		-2.2	-3.4	-4.5	µA
Voltage Reference						
Voltage reference	V_{REF}		0.792	0.8	0.808	V
High-side MOSFET						
On-Resistance	$R_{DS(ON)\_H}$	VIN = 12V, VBOOT − VSW = 5V		75	160	mΩ
Error Amplifier						
Input current				50		nA
Error amplifier trans conductance	gm	Normal operation −2µA < ICOMP < 2µA, VCOMP = 1V		400		uA/V
		During SS, −2µA < ICOMP < 2µA VCOMP = 1V, VFB = 0.4V		77		
Error amplifier DC gain		V_{FB} = 0.8V		10000		V/V
Error amplifier bandwidth				2500		kHz
Source/Sink current		V_{COMP} = 1V, 100mV overdrive		±30		uA
COMP to current sense trans-conductance	gm_cs			12		A/V
Current Limit						
Current limit	I_{LIM}	f_{SW} = 500kHz, VOUT = 5V	4.5	5.5	6.5	A
On-Time Timer Control						
Minimum On-Time	t_{ON_MIN}	VIN=12V,T_A=25°C		120		ns
Timing Resistor and External Clock						
Switching frequency range using RT mode	f_{SW}		100		2500	kHz
Switching frequency		RT = 200 kΩ	450	500	550	kHz
Switching frequency range using CLK mode			300		2200	kHz

T_J = -40˚C to 125˚C and V_{IN} = 12V. Typical values are at T_J = 25°C, unless otherwise noted.

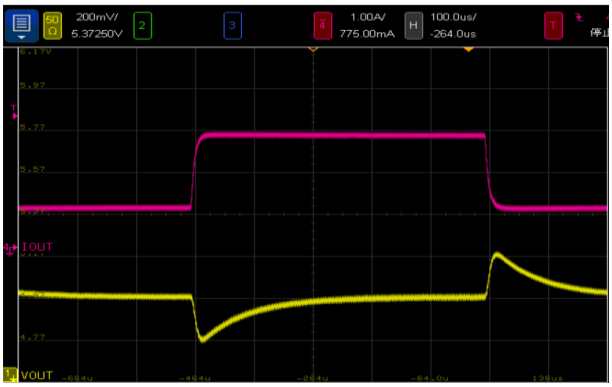
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Minimum sync pulse width				20		ns
SYNC threshold voltage	V_{IH_SYNC}			1.55		V
	V_{IL_SYNC}			1.2		V
RT/SYNC falling edge to SW rising edge delay				70		ns
Soft-Start and Tracking						
Internal charge current	I_{SS}	VSS/TR = 0.4V, XPC2963D5R		1.7		uA
SS/TR to FB offset		VSS/TR = 0.4V, XPC2963D5R		40		mV
SS/TR to reference crossover		98% nominal, XPC2963D5R		1.2		V
SS/TR discharge voltage		VFB = 0V, XPC2963D5R		50		mV
Internal Soft-Start time		10% to 90%, XPC2963S5R		2		ms
Power Good						
Power good threshold	V_{TH_PGLH1}	VFB rising, % of VREF, PGOOD from low to high XPC2963D5R	90	94	98	%
	V_{TH_PGHL1}	VFB rising, % of VREF, PGOOD from high to low XPC2963D5R	105	109	113	
	V_{TH_PGHL2}	VFB falling, % of VREF, PGOOD from low to high XPC2963D5R	88	92	96	
	V_{TH_PGLH2}	VFB falling, % of VREF, PGOOD from high to low XPC2963D5R	102	106	110	
Power good hysteresis		VFB falling, XPC2963D5R		2		%
Power Good leakage current	I_{LK_PGOOD}	VPGOOD = 5.5V, T_A = 25°C, XPC2963D5R		10	500	nA
Minimum VIN for defined output		VPGOOOD < 0.5V, IPGOOD = 100μA, XPC2963D5R		1	2	V
Output Under-Voltage protection						
UVP Trip Threshold	V_{UVP}	UVP detection		0.4		V

TYPICAL PERFORMANCE AND OPERATING CHARACTERISTICS

Efficiency vs. Output current

Vout=5V, f_{SW}=400kHz

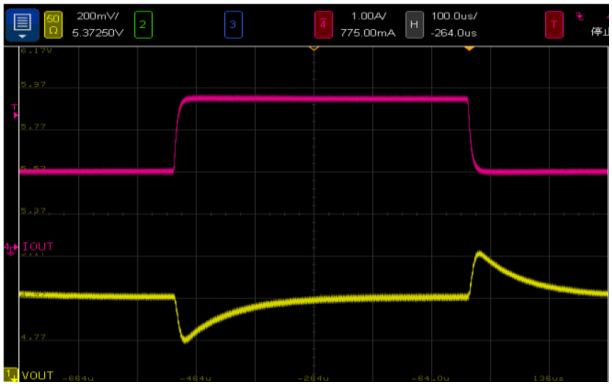
Load Transient



VIN = 12V, VOUT = 5V, 0.875A to 2.625A, f_{SW}=400kHz

COUT = 47µF x 2, L = 10µH

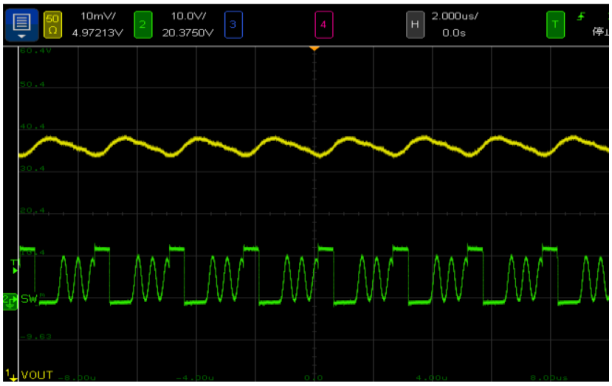
Load Transient



VIN = 12V, VOUT = 5V, 1.75A to 3.5A, f_{SW}=400kHz

COUT = 47µF x 2, L = 10µH

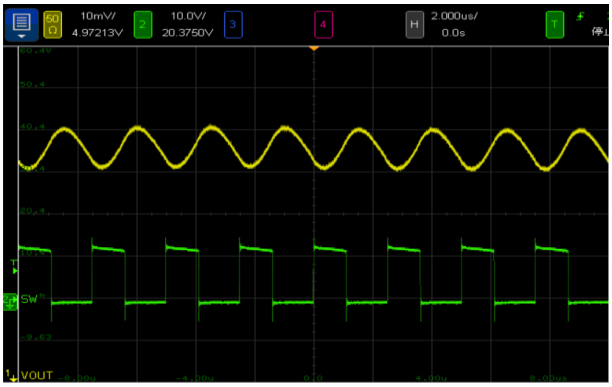
Ripple Voltage



VIN = 12V, VOUT = 5V, Iout=5mA, f_{SW}=400kHz

COUT = 47µF x 2, L = 10µH

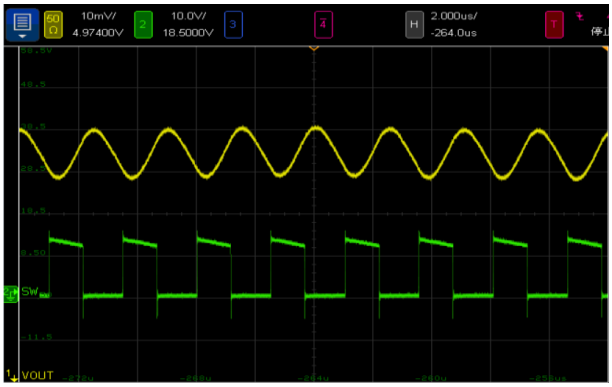
Ripple Voltage



VIN = 12V, VOUT = 5V, Iout=1.75A, f_{SW}=400kHz

COUT = 47µF x 2, L = 10µH

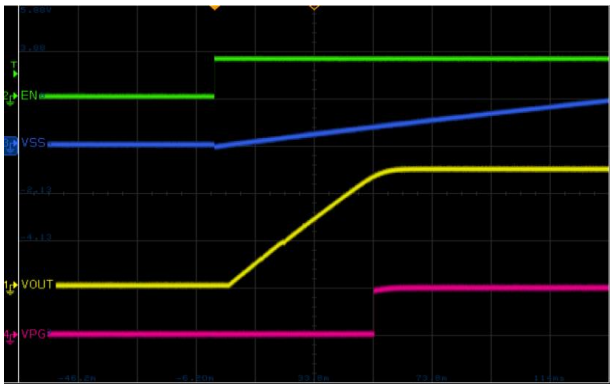
Ripple Voltage



VIN = 12V, VOUT = 5V, Iout=3.5A, f_{SW}=400kHz

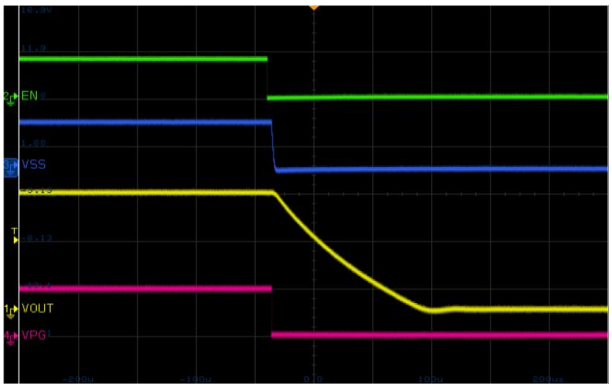
COUT = 47µF x 2, L = 10µH

Power On from EN



VIN = 12V, VOUT = 5V, Iout=3.5A, f_{SW}=400kHz

Power Off from EN

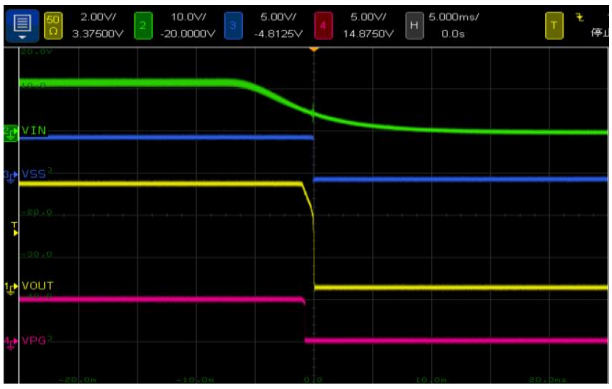


VIN = 12V, VOUT = 5V, Iout=3.5A, f_{SW}=400kHz

Power On from VIN

VIN = 12V, VOUT = 5V, Iout=3.5A, f_{SW}=400kHz

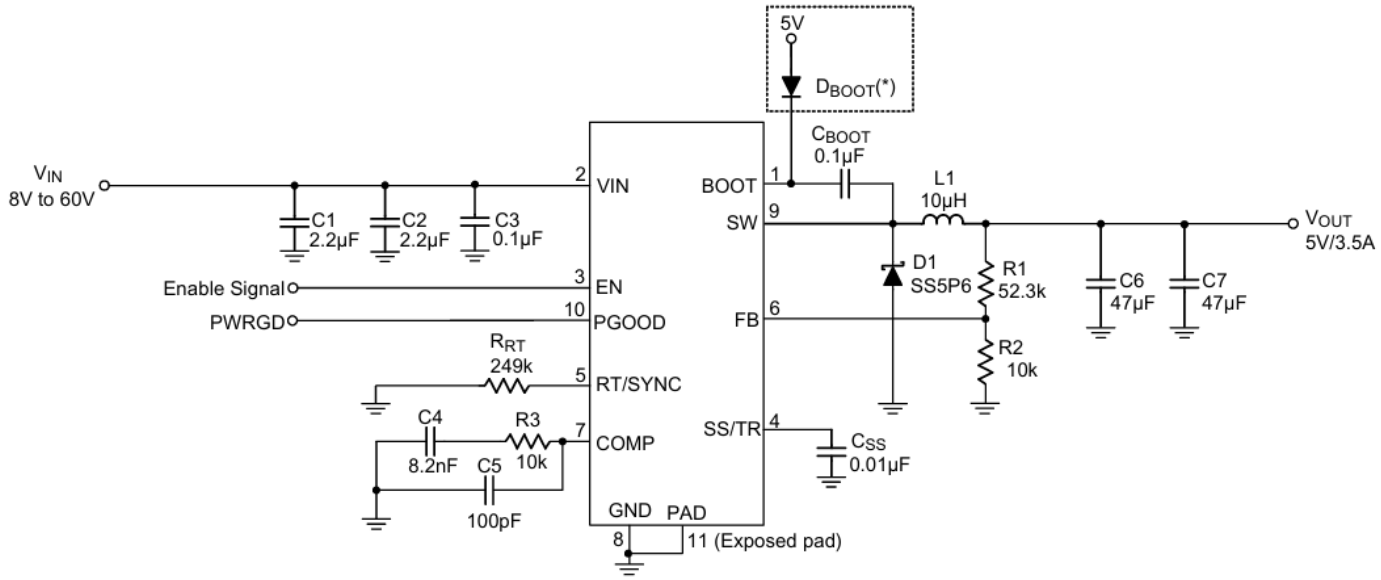
Power Off from VIN



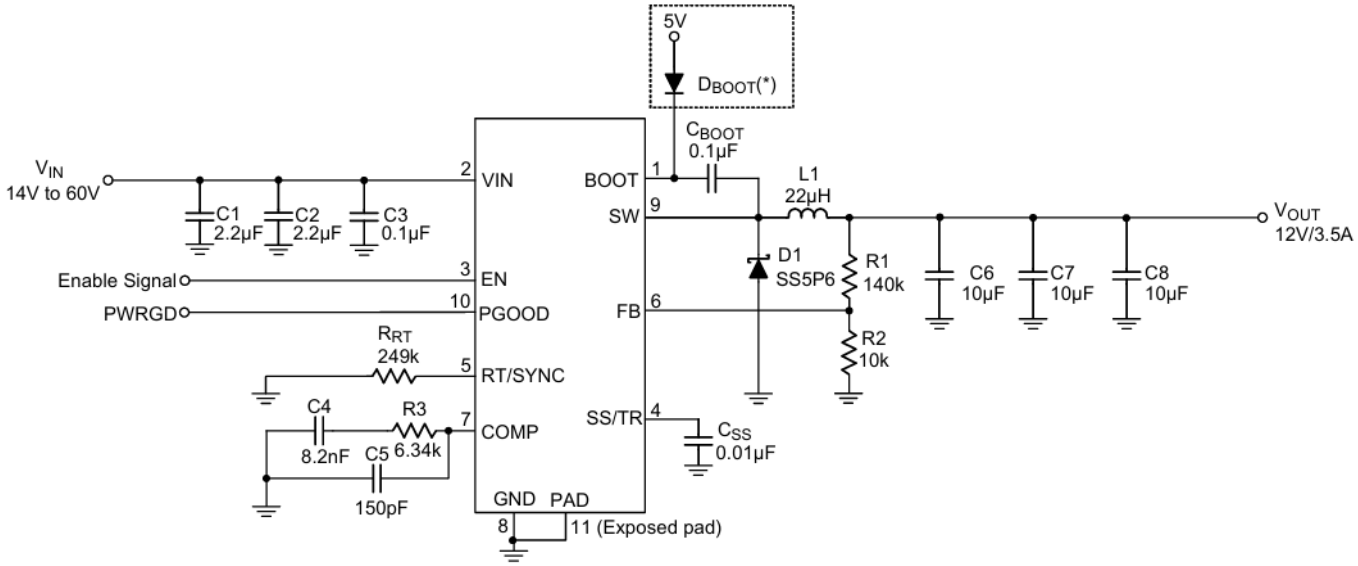
VIN = 12V, VOUT = 5V, Iout=3.5A, f_{SW}=400kHz

TYPICAL APPLICATION CIRCUIT

400kHz, 5Vout use case

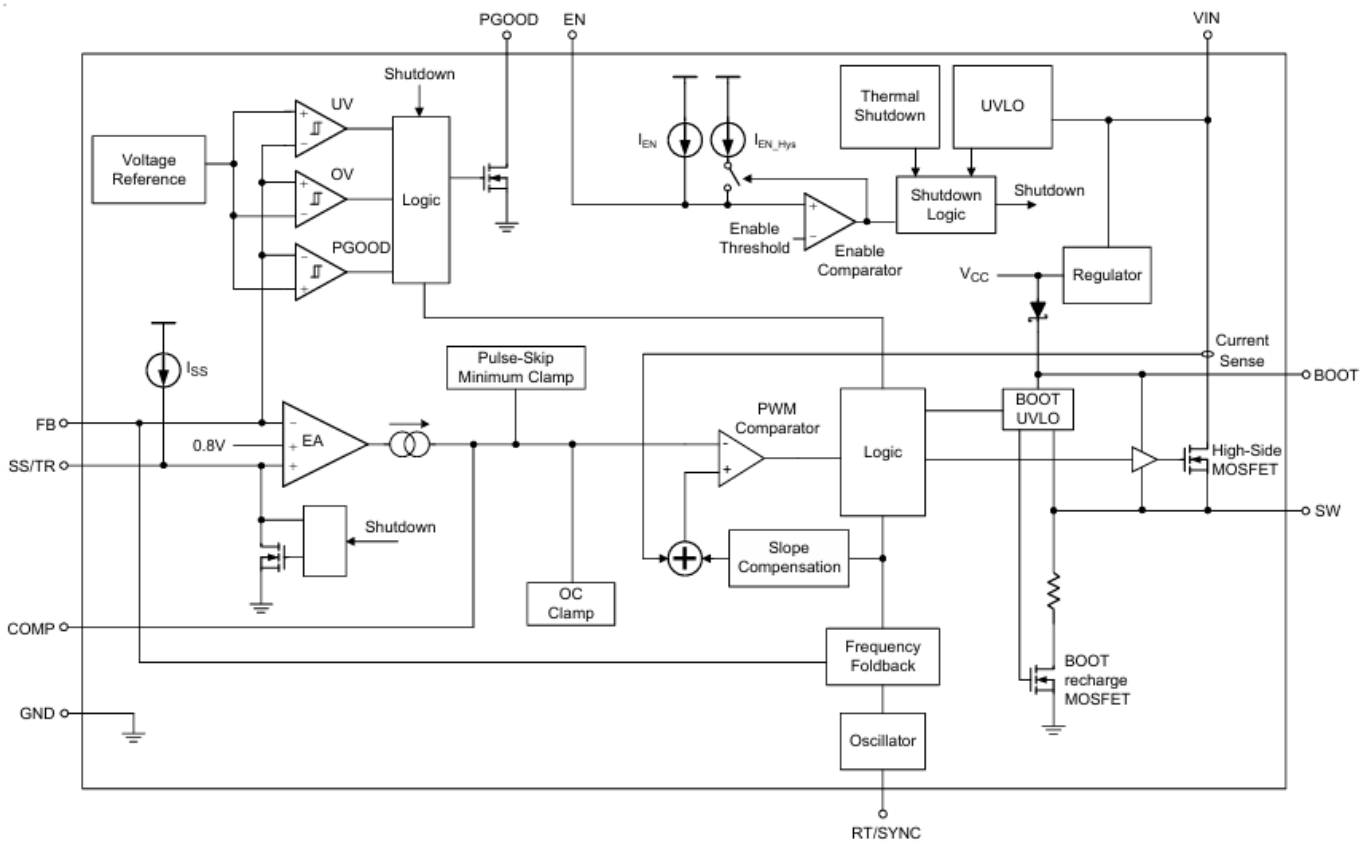


400kHz, 12Vout use case



* : While the input voltage is below 5.5V or duty cycle is higher than 65%, an external bootstrap diode must be added between an external 5V voltage supply and the BOOT pin to enhance the driving capability of high-side MOSFET.

FUNCTIONAL DESCRIPTION



Block Diagram

Overview

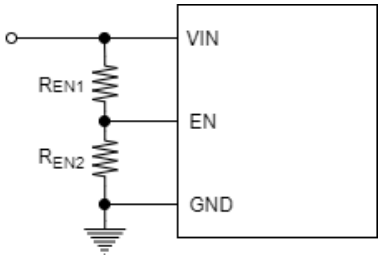
The XPC2963 is a high efficiency asynchronous step-down converter utilizes the peak current mode control. An internal oscillator initiates the turn-on of the high-side MOSFET. At the beginning of each clock cycle, the internal high-side MOSFET turns on, allowing current to ramp-up in the inductor. The inductor current is internally monitored during each switching cycle. The output voltage is sensed on the FB pin via the resistor divider, R1 and R2, and compared with the internal reference voltage (VREF) to generate a compensation signal (VCOMP) on the COMP pin. A control signal derived from the inductor current is compared to the voltage at the COMP pin, derived from the feedback voltage. When the inductor current reaches its threshold, the high-side MOSFET is turned off and inductor current ramps down. While the high-side MOSFET is off, the inductor current is supplied through the external low-side diode, freewheel diode, connected between the SW pin and GND. This cycle repeats at the next clock cycle. In this way, duty-cycle and output voltage are controlled by regulating inductor current.

Light Load Operation

The XPC2963 operates in power saving mode (PSM) at light load to improve light load efficiency. IC starts to switch when VFB is lower than PSM threshold (VREF x 1.005, typically) and stops switching when VFB is high enough. During PSM, the peak inductor current (IL_PEAK) is controlled by the minimum on-time of high-side MOSFET to ensure the low output voltage ripple. During non-switching period, most of the internal circuit is shut down, and the supply current drops to quiescent current (100μA, typically) to reduce power consumption. The lower output loading, the longer non-switching period, so the effective switching frequency becomes lower to reduce the switching loss and driving loss.

Enable

The XPC2963 provides an EN pin to enable or disable the device. If VEN is held below the enable threshold voltage, switching is inhibited even if the VIN voltage is above VIN under-voltage lockout threshold (VUVLOH). If VEN is held below 0.4V, the converter will enter into shutdown mode. During shutdown mode, the supply current can be reduced to ISHDN (2μA, typically). If the EN voltage rises above the enable threshold voltage while the VIN voltage is higher than VUVLOH, the device will be turned on, when switching being enabled and soft-start sequence being initiated. The EN pin has an internal pull up current source IEN (1.2μA, typically) that enables operation of the XPC2963 when the EN pin floats. The EN pin can be used to adjust the under-voltage lockout (UVLO) threshold and hysteresis by using two external resistors. The XPC2963 implements additional hysteresis current source I_{EN_Hys} (3.4μA, typically) to adjust the UVLO. The I_{EN_Hys} is sourced out of the EN pin when VEN is larger than enable threshold voltage. When the VEN falls below enable threshold voltage, the I_{EN_Hys} will be stopped sourcing out of the EN pin.



Soft-Start and Tracking Control

The soft-start function is used to prevent large inrush currents while the converter is being powered up. The XPC2963S5R provides internal soft-start and the XPC2963D5R provides external soft-start function for inrush currents control. The XPC2963D5R provides an SS/TR pin so that the soft-start time can be programmed by selecting the value of the external soft-start capacitor CSS/TR connected from the SS/TR pin to ground or controlled by external ramp voltage to SS/TR pin. During the start-up sequence, the soft-start capacitor is charged by an internal current source ISS (1.7μA, typically) to generate a soft-start ramp voltage as a reference voltage to the PWM comparator. The high-side MOSFET will start switching if the voltage difference between SS/TR pin and FB pin is equal to 40mV (i.e. VSS/TR − VFB = 40mV, typically) during power-up period. If the output is pre biased to a certain voltage during start-up for some reason, the device will not start switching until the voltage difference between SS/TR pin and FB pin is equal to 40mV (typically). Only when this ramp voltage is higher than the feedback voltage VFB, the switching will be resumed. The FB voltage will track the SS/TR pin ramp voltage with a SS/TR to FB offset voltage (40mV, typically) during soft start interval. The output voltage can then ramp up smoothly to its targeted regulation voltage, and the converter can have a monotonic smooth start-up. For soft-start control, the SS pin should never be left unconnected. After the FB pin voltage rises above 94% of VREF (typically), the PGOOD pin will be in high impedance and the VPGOOD will be held high.

Power Good Indication

The XPC2963D5R features an open-drain power-good output (PGOOD) to monitor the output voltage status. The output delay of comparator prevents false flag operation for short excursions in the output voltage, such as during line and load transients. Pull-up PGOOD with a resistor to an external voltage source and it is recommended to use pull-up resistance between the values of 1 and 10kΩ to reduce the switching noise coupling to PGOOD pin. The PGOOD assertion requires input voltage above 2V. The power-good function is controlled by a comparator connected to the feedback signal VFB. If VFB rises above the power-good high threshold (VTH_PGLH1) (94% of the reference voltage, typically), the PGOOD pin will be in high impedance and VPGOOD will be held high after a certain delay elapsed. When VFB falls below power-good low threshold (VTH_PGHL2) (92% of the reference voltage, typically) or exceeds VTH_PGHL1 (109% of the reference voltage, typically), the PGOOD pin will be pulled low. For VFB higher than VTH_PGHL1, VPGOOD can be pulled high again if VFB drops back by a power-good high threshold (VTH_PGLH2) (106% of the reference voltage, typically). Once being started-up, if any internal protection is triggered, PGOOD will be pulled low to GND. The internal open-drain pull-down device will hold the PGOOD pin low.

High-Side MOSFET Peak Current Limit Protection

The XPC2963 includes a cycle-by-cycle high-side MOSFET peak current-limit protection against the condition that the inductor current increasing abnormally, even over the inductor saturation current rating. The inductor current through the high-side MOSFET will be measured after a certain amount of delay when the high side MOSFET being turned on. If an over-current condition occurs, the converter will immediately turn off the high side MOSFET to prevent the inductor current exceeding the high-side MOSFET peak current limit (ILIM).

Switching Frequency Setting

The XPC2963 offers adjustable switching frequency setting and the switching frequency can be set by using external resistor RRT/SYNC. The switching frequency range is from 100kHz to 2.5MHz. The selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge and transition losses, but requires larger inductance values and/or capacitance to maintain low output ripple voltage. The additional constraints on operating frequency are the minimum on-time and minimum off-time. The minimum on-time, t_{ON_MIN}, is the smallest duration of time in which the high-side switch can be in its "on" state. The minimum on-time of the XPC2963 is 120ns (typically). In continuous mode operation, the maximum operating frequency, fSW_MAX, can be derived from the minimum on time according to the formula below:

$$f_{SW\_MAX} = \frac{V_{OUT}}{t_{ON\_MIN} \times V_{IN\_MAX}}$$

where VIN_MAX is the maximum operating input voltage.

The minimum off-time, t_{OFF_MIN}, is the smallest amount of time that the XPC2963 is capable of tripping the current comparator and turning the high-side MOSFET back off. The minimum off-time of the XPC2963 is 130ns (typically). If the switching frequency should be constant, the required off-time needs to be larger than minimum off-time. Below shows minimum off-time calculation with loss terms consideration :

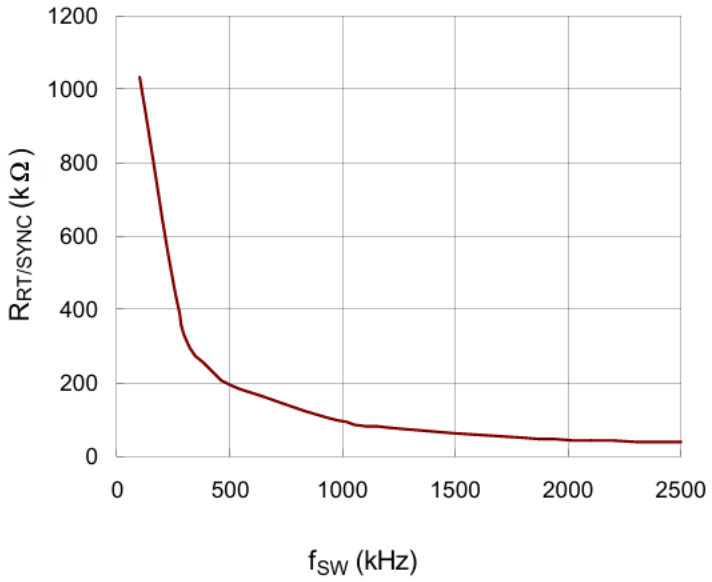
$$t_{OFF\_MIN} \le \frac{1 - \left[\frac{V_{OUT} + \left(I_{OUT\_MAX} \times R_L\right) + V_D}{V_{IN\_MIN} - \left(I_{OUT\_MAX} \times R_{DS(ON)\_H}\right) + V_D}\right]}{f_{SW}}$$

where RDS(ON)_H is the on-resistance of the high-side MOSFET; VD is the forward conduction voltage of the freewheel diode; RL is the DC resistance of inductor.

The switching frequency fSW is set by the external resistor RRT/SYNC connected between the RT/SYNC pin and ground. The failure mode and effects analysis (FMEA) consideration is applied to the RT/SYNC pin setting to avoid abnormal switching frequency operation at failure conditions. It includes failure scenarios of short-circuit to ground and the pin is left open. The switching frequency will be 900kHz (typically) when the RT/SYNC pin is shorted to ground, and 240kHz (typically) when the pin is left open. The equation below shows the relation between setting frequency and the RRT/SYNC value.

$$R_{RT/SYNC\ (k\Omega)} = \frac{120279}{f_{SW}^{1.033}}$$

where fSW (kHz) is the desired setting frequency. It is recommended to use 1% tolerance or better, and the temperature coefficient of 100 ppm or less resistors. Figure below shows the relationship between switching frequency and the RRT/SYNC resistor.



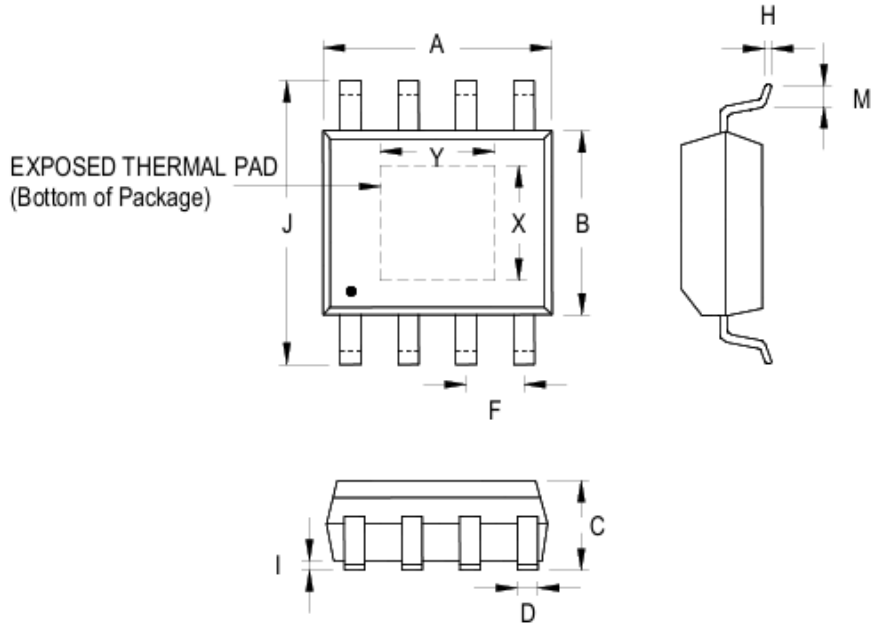
Layout Considerations

Layout is a critical portion of good power supply design. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade performance.

- To reduce parasitic effects, the VIN terminal should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric.
- Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN terminal, and the anode of the catch diode.
- The GND terminal should be tied directly to the power pad under the IC and the thermal pad.
- The thermal pad should be connected to internal PCB ground planes using multiple vias directly under the IC. The SW terminal should be routed to the cathode of the catch diode and to the output inductor.
- Since the SW connection is the switching node, the catch diode and output inductor should be located close to the SW terminals, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- For operation at full rated load, the top side ground area must provide adequate heat dissipating area.
- The RT/CLK terminal is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.

PHYSICAL DIMENSIONS

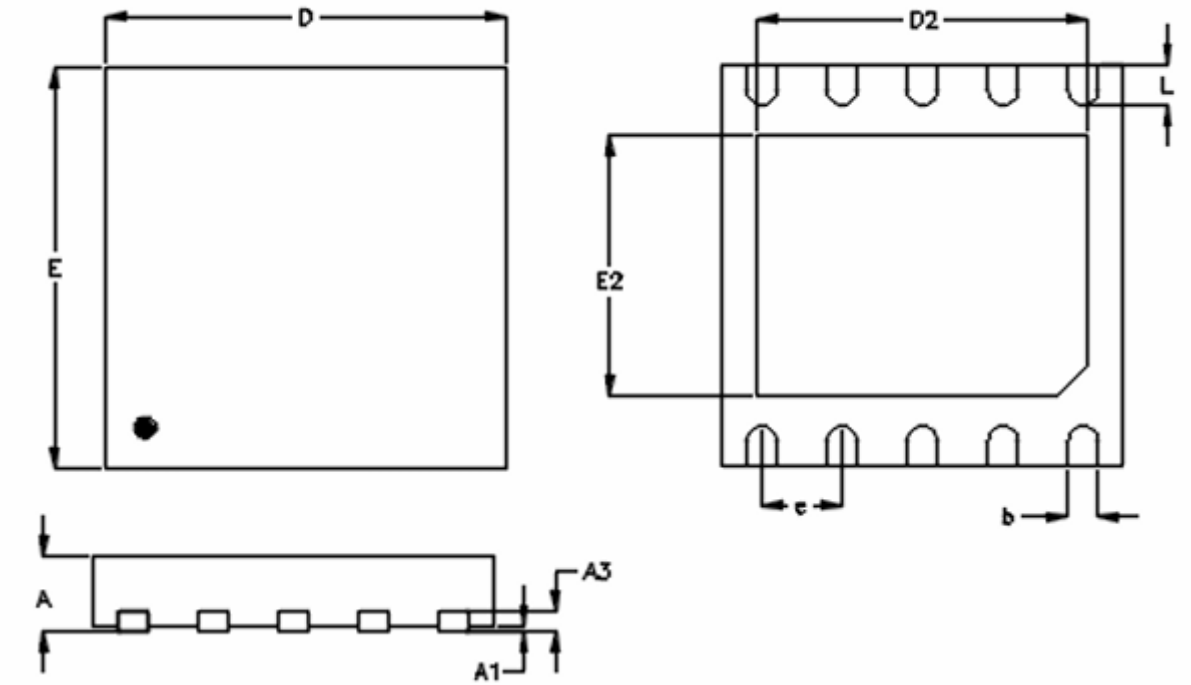
SOP-8:



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

PHYSICAL DIMENSIONS

DFN-10:



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.250	0.350	0.010	0.014
D	3.900	4.100	0.154	0.161
D2	3.250	3.350	0.128	0.132
E	3.900	4.100	0.154	0.161
E2	2.550	2.650	0.100	0.104
e	0.800		0.031	
L	0.350	0.450	0.014	0.018