TLK3114SA Planned Changes and Errata

High Performance Analog

Description	Change or Fix Detail
Transmit and receive dependent channel mode separation	**General description:** MDIO register configuration will permit dependent channel mode operation in the transmit direction while the receive data operates in independent channel mode. This is a feature enhancement. **Technical description:** When in channel sync mode, with PSYNC=high, the four transmit channels latch input data using the TCA clock. Receive channels clock data out by only one recovered clock, RCA. Under independent channel mode, with PSYNC=low, each channel uses its own transmit clock and recovered clock to latch data. A new operating mode will be created whereby only a single transmit clock will be required, but all four independent recovered clocks will be enabled. The new mode will be accessible through an MDIO configuration register.
CTC recovery	**General description:** Once overflowed or underflowed, the CTC FIFO did not recover automatically. **Technical description:** The CTC FIFO write pointer is driven by the recovered clock, while the CTC FIFO read pointer is driven by the reference clock. Under normal conditions, the recovered clock will follow reference clock any time that the serial receive inputs are disconnected. However, high amplitude noise can force the CDR to track an unknown frequency, causing an overflow or underflow. The CTC has been changed to recover from an overflow or underflow condition automatically. **Interim Workaround:** The recommended workaround steps for startup are enumerated below. 1. Poll MDIO register 1 (0x1), 4.1 (0x1), or 5.1 (0x1) until bit 0x2 indicates 1, link is up. The link is up indicator is set when the channel synchronization state machine for each channel has reached the SYNC state and the column deskew state machine has reached the ALIGN state. 2. Read MDIO register 24 (0x18), 4.32776 (0x8008), or 5.32776 (0x8008). A 1 in any of the bits 0x0-7 indicate a CTC failure. 0's in every bit 0x0-7 indicates an unrelated fault which may not require a reset. Issue a software reset by writing 0x0001 into register 0, 4.0, or 5.0. Repeat this procedure from step 1.
Portsync FIFO window	**General description:** Hot plug can introduce artificial skew into the portsync FIFO. This condition is rare, but has been experimentally confirmed. **Technical description:**

	The portsync FIFO write pointer is driven by the recovered clock for each individual channel. The FIFO read pointer is driven by either the recovered clock for the individual channel or by the recovered clock for channel A, depending on the device configuration. If the receive serial channels are driven by different frequencies, then the write pointers may be driven to different points across the four FIFO's. This uncorrelated movement of the write pointers can generate artificial skew across the four lanes. If artificial skew increases total skew above 40UI, then the TLK3114SA will not be able to deskew the data. In normal portsync operation, the receive channels are frequency locked at the data source and contain only controlled levels of skew. However, during hot plug of a connector, such as a Xenpak connector, it is possible for some lanes to not make contact simultaneously. For the moment between contact on one lane and contact on all lanes, only some lanes will be driven with receive serial data. Since unconnected lanes' recovered clocks lock to reference clock and connected lanes lock to the received data frequency, a ppm difference may exist briefly during hot plug. This frequency offset can be enough to drive the portsync FIFO pointers outside of the allowable skew range. This condition can only be seen infrequently during hot plug. The device will monitor alignment characters. Repeated appearances of 1-3 alignment characters indicates a skew problem and will generate a FIFO pointer reset. **Interim Workaround:** The TLK3114SA will report the artificial skew condition by not allowing the deskew state machine to reach the ALIGN state. The state of the deskew state machine can be read in MDIO registers 4.24 and 5.24 bit 12; the TLK3114SA will report local fault while the state machine is not in the ALIGN state. Issue a software reset by writing 0x0001 into register 0, 4.0, or 5.0.
CTC receive data skew	**General description:** When the device was brought out of reset, it was possible, but rare, for the CTC FIFO to induce one byte of skew across lanes. **Technical description:** The CTC FIFO write pointers are driven by the recovered clock, while the read pointers are driven by the reference clock. The internal RESET signal, however, was not synchronous to the reference clock. When internal RESET was released at each FIFO, a metastable condition existed on the read pointers. Some read pointers could advance by one position on the first reference clock transition, while others might not. The internal RESET signal at the FIFO's will be synchronized with the reference clock. **Interim Workaround:** The TLK3114SA does not recognize the error and there is no universal workaround. In synchronous operation, the reference clock to reset release phase can provide a workaround. Only certain reference clock to reset phase relationships are subject to the CTC skew.
Receive sensitivity	**General description:** Receiver sensitivity has been increased. At high VDD levels with low receive amplitude, it was possible to create a low level BER. **Interim Workaround:** Either providing a VDD less than 2.5V or higher amplitude receive data eliminates the BER.

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