Adaptive DO-Chargepump High Efficiency Low Noise Large Volume TLTR-AGC 6th Smart K Audio Amplifier

FEATURES

- Triple-Level Triple-Rate AGC algorithm：
  - Enhance bass, improve the dynamic range
  - Increase volume, eliminate noise, timely and effectively protect the speaker
- Adaptive DO-Chargepump technology：
  - Low Quiescent current：6mA@3.6V
  - Overall efficiency up to 81%
- Output Power：3.0W@8Ω，3.4W@6Ω
- Low Noise：9.5μV
- Low THD+N：0.008%
- Support high power receiver stereo application
- Support AB/D speaker，AB/D receiver 2-in-1 application
  - AB receiver：0dB，Vn=9.5μV，THD+N=0.2%
  - D receiver：0dB，Vn=11μV，THD+N=0.015%
- Support 1.8V I²C Control
- Over current protection, over-temperature protection and short-circuit protection
- Super TDD-Noise suppression
- Excellent pop-click suppression
- High PSRR：90dB（217Hz）
- FCQFN 2.0mmX2.5mmX0.55mm-16L package

APPLICATIONS

- Smart phone、Tablet PC、Tactile feedback

DESCRIPTION

AW87390G is specifically designed to improve the musical output dynamic range, enhance the overall sound quality, which is a new high efficiency, low noise, constant large volume, 6th Smart K audio amplifier. AW87390G integrates awinic's proprietary Triple-Level Triple-Rate AGC audio algorithm, effectively eliminating music noise and improving sound quality and volume. AW87390G integrated efficiency up to 90% of Adaptive DO-Chargepump technology, significantly improving the dynamic range of the music output and power consumption of audio system. AW87390G noise floor is as low as to 38μV at speaker mode, with 102dB high signal-to-noise-ratio (SNR). The ultra-low distortion 0.008% and unique Triple-Level Triple-Rate AGC technology bring high quality music enjoyment.

AW87390G support speaker and high power receiver stereo applications；supports speaker and receiver 2-in-1 applications，class AB/D receiver optional，ultra-low noise is 9.5μV.

AW87390G controls internal registers through the I²C interface. Register parameters include output voltage, power amplifier gain, Triple-Level Triple-Rate AGC parameters etc.

AW87390G built-in over current protection, over temperature protection and short circuit protection function, effectively protect the chip. AW87390G features small FCQFN 2.0mmX2.5mmX0.55mm-16L package.

TYPICAL APPLICATION CIRCUIT

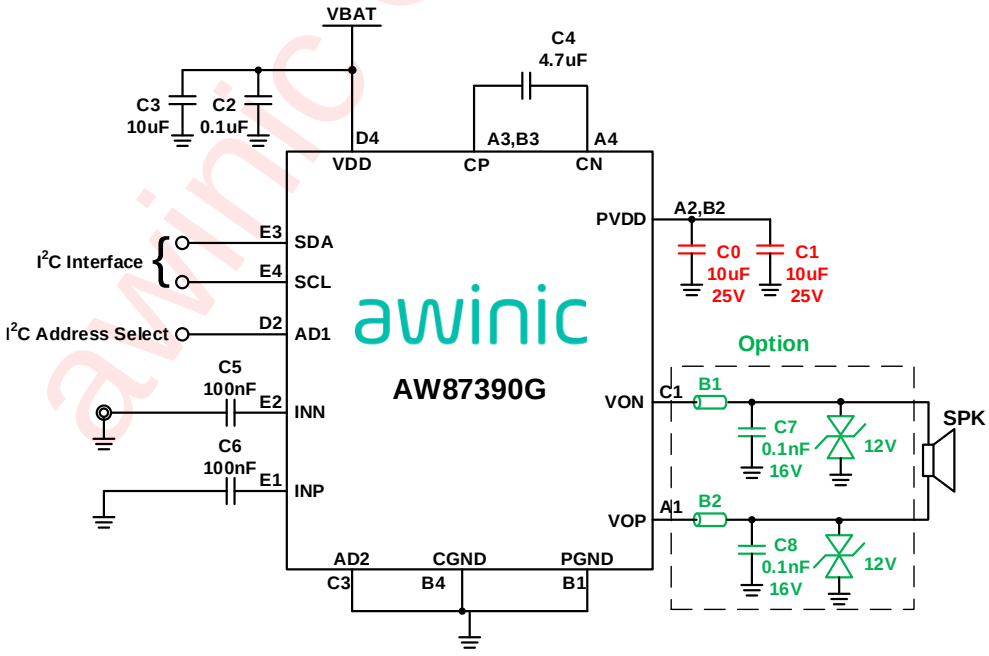


Figure 1 AW87390G Single-ended input mode Application Diagram

PIN CONFIGURATION ANG TOP MARK

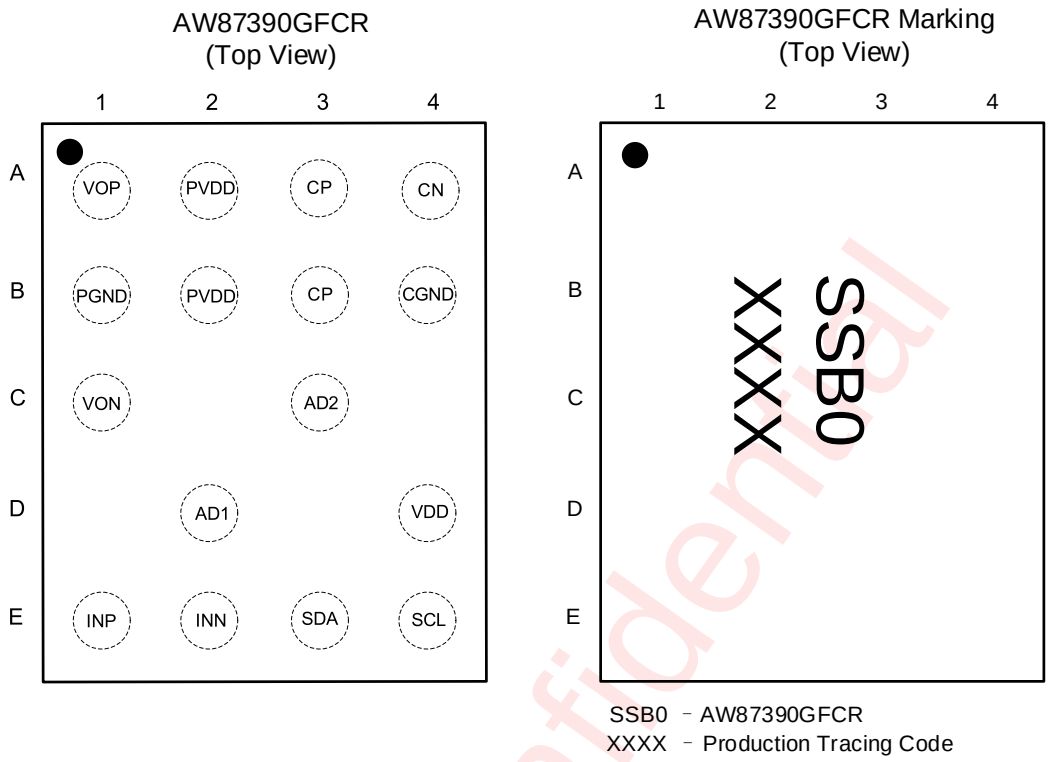


Figure 2 AW87390G Pin configuration and Top Mark

PIN DESCRIPTION

Number	Symbol	Description
A1	VOP	Positive audio output terminal
A2,B2	PVDD	Charge Pump output voltage
A3,B3	CP	Positive input Charge Pump Flying Capacitance
A4	CN	Negative input Charge Pump Flying Capacitance
B1	PGND	Amplifier power ground
B4	CGND	Charge Pump power ground
C1	VON	Negative audio output terminal
C3	AD2	I^2C address pin2
D2	AD1	I^2C address pin1
D4	VDD	Power supply
E1	INP	Positive audio input terminal
E2	INN	Negative audio input terminal
E3	SDA	I^2C-bus data input/output
E4	SCL	I^2C-bus clock input

FUNCTIONAL DIAGRAM

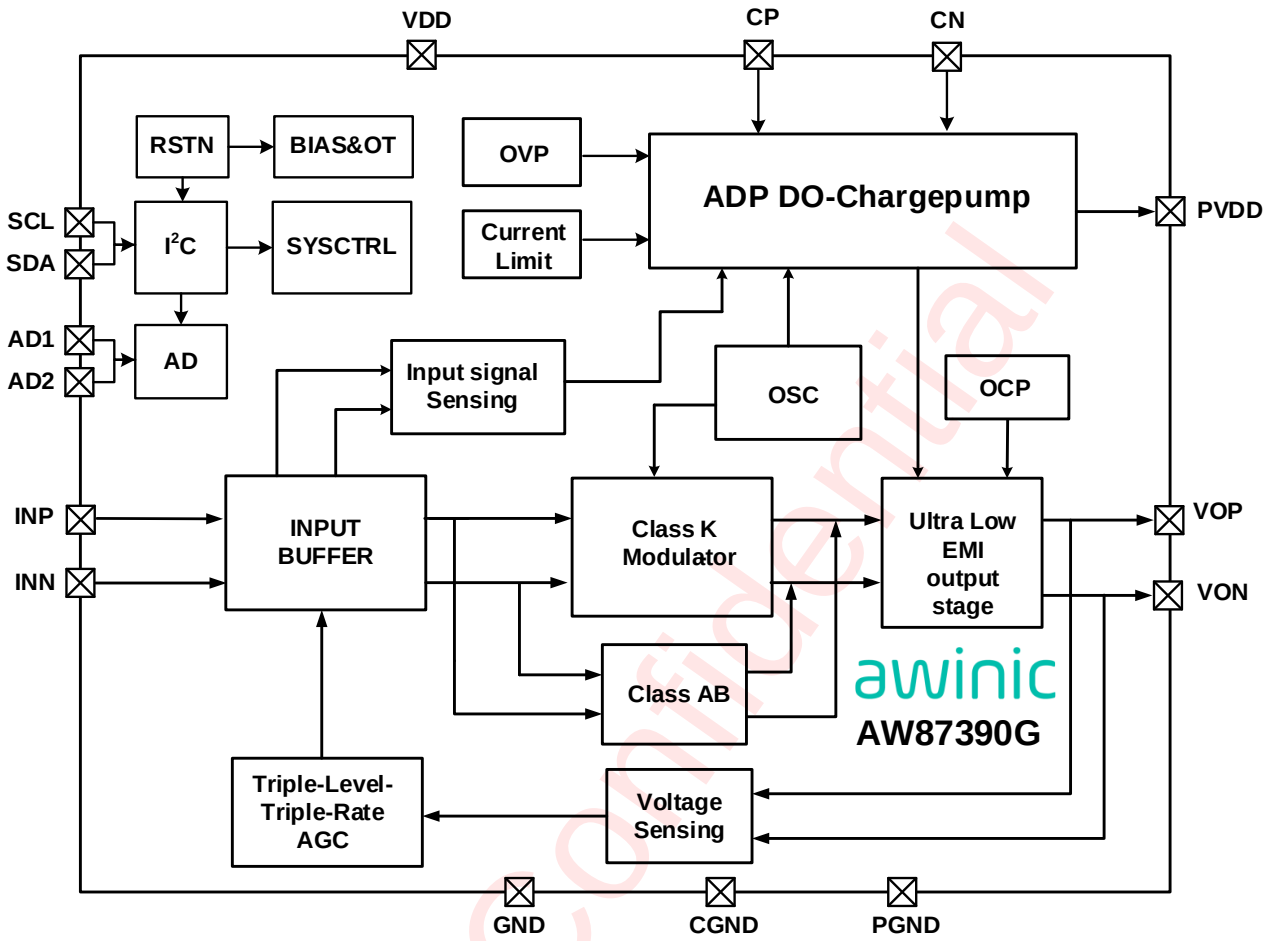


Figure 3 AW87390G Functional Diagram

TYPICAL APPLICATION CIRCUIT

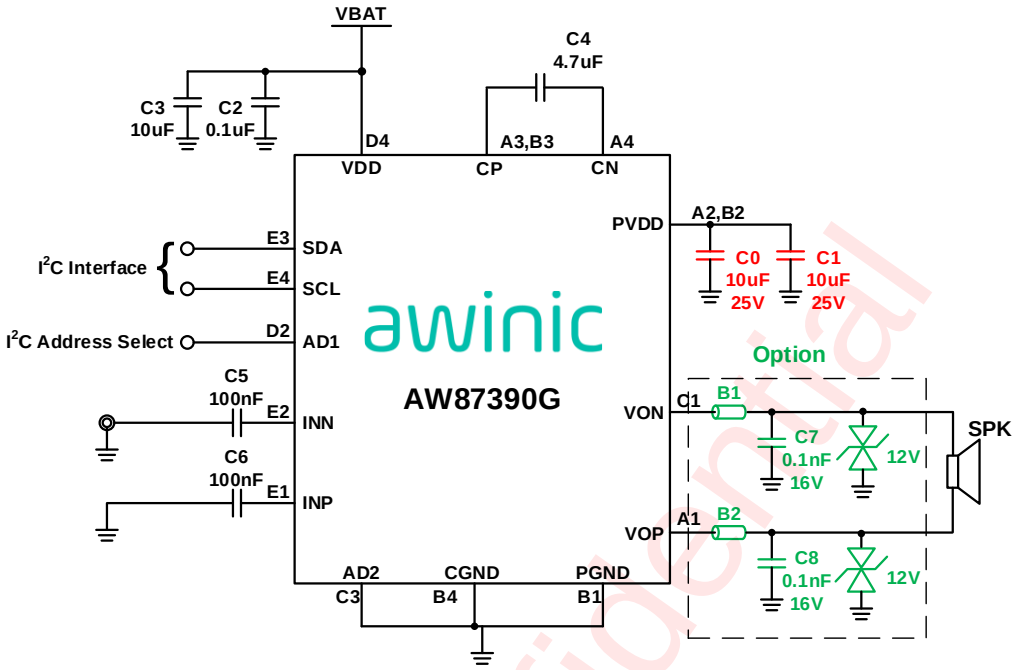


Figure 4 AW87390G Single-ended input mode Application Diagram(Note 1)

Note1： *When single-ended input, audio signal line from audio DAC (HPL or HPR) can arbitrarily connected to either of INN or INP input terminal. The other terminal must be connected to reference ground (HPREF) through input capacitor and resistor.*

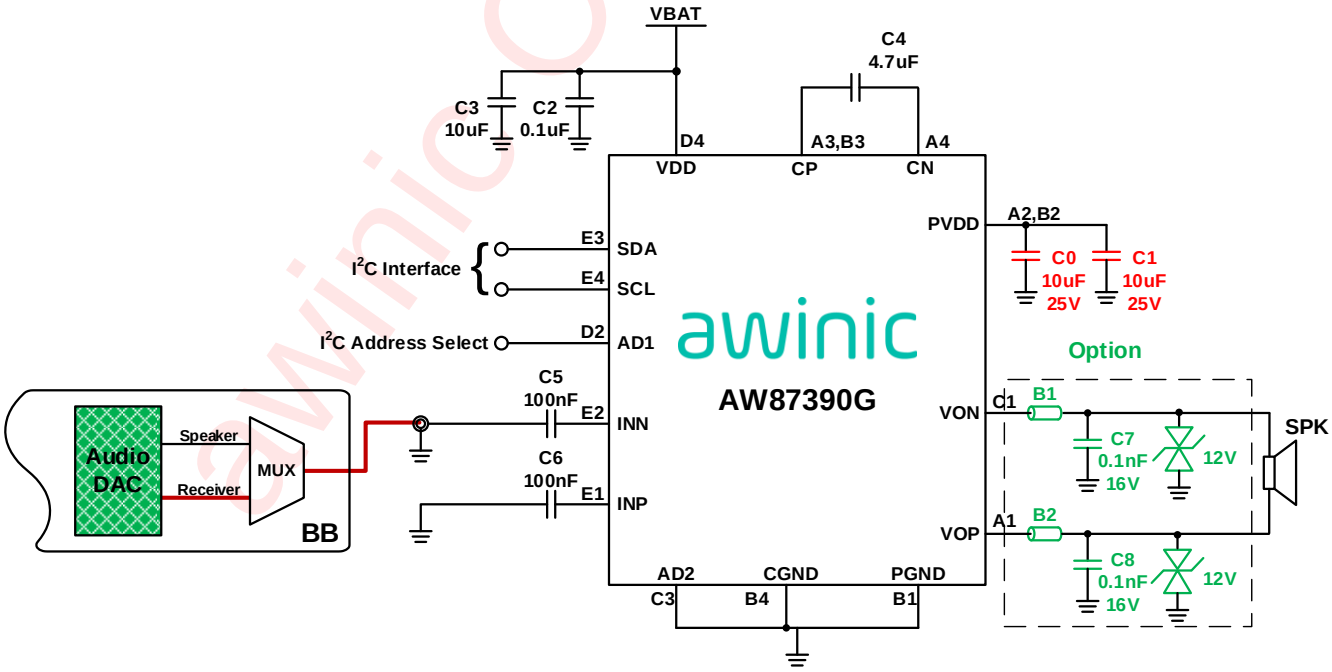


Figure 5 AW87390G Speaker & Receiver 2-in-1 Mode Application Diagram

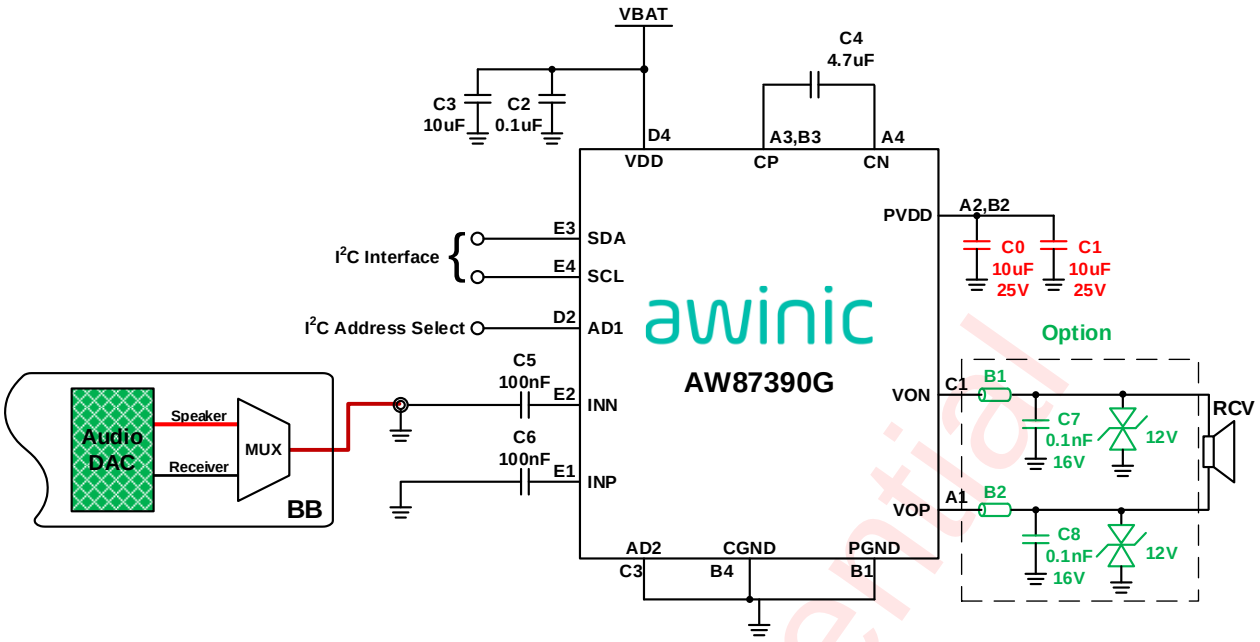


Figure 6 AW87390G High Power Receiver Stereo Mode Application

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW87390GFCR	-40°C ~105°C	FCQFN 2.0mmX2.5mmX0.55mm-16L	SSB0	MSL1	ROHS+HF	6000 units/ Tape and Reel

ABSOLUTE MAXIMUM RATING (Note2)

Parameter	Range
Supply Voltage V_{DD}	-0.3V to 6V
INN,INP	-0.3V to VDD+0.3V
Charge pump output voltage PVDD	-0.3V to 9.5V
VOP,VON	-0.6V to PVDD+0.6V
CP	-0.3V to PVDD+0.3V
CN	-0.3V to VDD+0.3V
Minimum load resistance R_L	5Ω
Package Thermal Resistance θ_{JA}	65.2°C/W
Ambient Temperature Range	-40°C to 105°C
Maximum Junction Temperature T_{JMAX}	165°C
Storage Temperature Range T_{STG}	-65°C to 150°C
Lead Temperature（Soldering 10 Seconds）	260°C
ESD Rating (Note 3)	
HBM（human body model）	±2kV
MM (machine model)	±400V
CDM（charged-device model）	±1.5kV
Latch-up	
Test Condition：JEDEC STANDARD NO.78E	+IT：450mA -IT：-450mA

NOTE2: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE3: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017

Test method of the charge device model: ESDA/JEDEC JS-002-2014

ELECTRICAL CHARACTERISTICS

Test condition：T_A=25°C, VDD=3.6V, PVDD OVP=8V, R_L=8Ω+33μH, f=1kHz（unless otherwise noted）

Parameter		Test conditions		Min	Typ	Max	Units
V_{DD}	Power supply voltage			3.0		5.5	V
UVLO	Under-voltage protection voltage				2.5		V
	Under-voltage protection hysteresis voltage				100		mV
V_{IH}	SCL, SDA, AD1, AD2 high-level input voltage			1.3		V_{DD}	V
V_{IL}	SCL, SDA, AD1, AD2 low-level input voltage			0		0.45	V
I_{SB}	Standby current	V_{DD}=3.6V			3		μA
T_{SD}	Over temperature protection threshold				160		°C
T_{SDR}	Over temperature protection recovery threshold				130		°C
T_{ON}	Turn-On time				45		ms
ADP DO-Chargepump							
PVDD	The maximum Output voltage	V_{DD}=3.0V to 4V, PVDD OVP=8V			2*VDD		V
		V_{DD} >4V			8 (Note4)		V
	Adption Output voltage	Po <Pth			VDD		V
		Po ≥Pth, V_{DD}=3.0V to 4V, PVDD OVP=8V			2*VDD		V
OVP	OVP voltage	V_{DD} >4V			8 (Note4)		V
	OVP hysteresis voltage	V_{DD} >4V			50		mV
F_{CP}	Chargepump operating frequency	V_{DD}=3.0V to 5.5V		1.08	1.45	1.8	MHz
η_{CP}	Chargepump efficiency	V_{DD}=4.2V, I_{load}=200mA			90		%
T_{ST}	Softstart Time	No load, COUT=20μF			2.1		ms
Class K MODE							
V_{OS}	Output offset voltage	No input		-30	0	30	mV
I_q	Speaker Quiescent current	V_{DD}=4.2V, input ac grounded, R_L=8Ω+33μH			12.3		mA
η	total efficiency（CP+Class D）	V_{DD}=4.2V, Po=2.5W, R_L=8Ω+33μH, PVDD OVP=8V			80		%
Vinp	Recommended input signal amplitude	V_{DD}=3.0V to 5.5V				1	Vp
Fosc	Modulation frequency	V_{DD}=3.0V to 5.5V		540	760	900	kHz
Pagc	TLTR AGC power	R_L=8Ω+33μH		0.72	0.8 (Note4)	0.88	W
		R_L=6Ω+33μH		0.96	1.067(Note4)	1.17	W
PSRR	Power supply rejection ratio	V_{DD}=4.2V, Vpp_sin=200mV	217Hz		80		dB
			1kHz		78		dB
SNR	Signal-to-noise ratio	V_{DD}=4.2V, PVDD OVP=8V, Po=3W, Av=18dB , THD+N=1%,R_L=8Ω+33μH,			102		dB

Parameter		Test conditions		Min	Typ	Max	Units
SNR	Signal-to-noise ratio	V_{DD}=4.2V, PVDD OVP=8V, Po=0.8W, Av=18dB, R_L=8Ω+33μH			94		dB
E_N	Speaker Output noise	Av=24dB	20Hz to 20kHz, input ac grounded, A-weighting		48		μV
E_N	Speaker Output noise	Av=18dB			38		μV
Av	Speaker gain	V_{DD}=3.0V to 5.5V			18 (Note4)		dB
Rini	Speaker Inner input resistance	Av=24dB			9		kΩ
	Speaker Inner input resistance	Av=18dB			18		
Fin	Speaker input Cut-off frequency	Cin=68nF, Av=24dB			260		Hz
	Speaker input Cut-off frequency	Cin=68nF, Av=18dB			130		
	Speaker input Cut-off frequency	Cin=100nF, Av=24dB			177		
	Speaker input Cut-off frequency	Cin=100nF, Av=18dB			89		
THD+N	Total harmonic distortion + noise	V_{DD}=4.2V, Po=0.6W, R_L=8Ω+33μH, f=1kHz, PVDD OVP=8V			0.008		%
Rdson	Drain-Source on-state resistance	High side MOS + Low side MOS			400		mΩ
Po	Speaker Output Power	THD+N=1%, R_L=8Ω+33μH, V_{DD}=4.2V, PVDD OVP=8V			3.0		W
		THD+N=10%, R_L=8Ω+33μH, V_{DD}=4.2V, PVDD OVP=8V			3.6		W
		THD+N=1%, R_L=6Ω+33μH, V_{DD}=4.2V, PVDD OVP=8V			3.4		W
		THD+N=10%, R_L=6Ω+33μH, V_{DD}=4.2V, PVDD OVP=8V			4.1		W
		THD+N=1%, R_L=8Ω+33μH, V_{DD}=3.6V, PVDD OVP=8V			2.3		W
		THD+N=10%, R_L=8Ω+33μH, V_{DD}=3.6V, PVDD OVP=8V			2.8		W
		THD+N=1%, R_L=6Ω+33μH, V_{DD}=3.6V, PVDD OVP=8V			2.5		W
		THD+N=10%, R_L=6Ω+33μH, V_{DD}=3.6V, PVDD OVP=8V			3.1		W
ADP MODE							
I_q	Speaker Quiescent current	V_{DD}=3.6V, input ac grounded, R_L=8Ω+33μH			6.0		mA
Pth	Boost power threshold	VDD=3V to 5.5V, RL=8Ω+33μH, PVDD OVP=8V			0.3 (Note4)		W
η	total efficiency（CP+Class D）	V_{DD}=3.6V, Po=0.3W, R_L=8Ω+33μH, PVDD OVP=8V			80		%
		V_{DD}=3.6V, Po=2.5W, R_L=8Ω+33μH, PVDD OVP=8V			81		%
PSRR	Power supply rejection ratio	V_{DD}=4.2V, Vpp_sin=200mV	217Hz		70		dB
			1kHz		71		dB
E_N	Speaker Output noise	Av=24dB	20Hz to 20kHz, input ac grounded, A-weighting		49		μV
		Av=18dB			38		μV

Parameter		Test conditions		Min	Typ	Max	Units
THD+N	Total harmonic distortion + noise	V_{DD}=4.2V, Po=0.6W, R_L=8Ω+33μH, f=1kHz, PVDD OVP=8V			0.007		%
AB Speaker & KAB Speaker MODE							
I_q	Speaker Quiescent current	V_{DD}=3.6V, input ac grounded, R_L=8Ω+33μH, PVDD OVP=6V			13.9		mA
		V_{DD}=3.6V, input ac grounded, R_L=8Ω+33μH			7.5		mA
η	total efficiency（CP+Class D）	V_{DD}=4.2V, Po=1.2W, R_L=8Ω+33μH, PVDD OVP=6V			40		%
		V_{DD}=4.2V, Po=0.8W, R_L=8Ω+33μH			68		%
E_N	Speaker Output noise	Av=24dB	20Hz to 20kHz, input ac grounded, A-weighting		46		μV
		Av=18dB			36		
Av	Speaker gain	V_{DD}=3.0V to 5.5V			18 (Note4)		dB
Rini	Speaker Inner input resistance	Av=24dB			9		kΩ
	Speaker Inner input resistance	Av=18dB			18		kΩ
Fin	Speaker input Cut-off frequency	Cin=68nF, Av=24dB			260		Hz
	Speaker input Cut-off frequency	Cin=68nF, Av=18dB			130		
	Speaker input Cut-off frequency	Cin=100nF, Av=24dB			177		
	Speaker input Cut-off frequency	Cin=100nF, Av=18dB			89		
PSRR	AB Speaker Power supply rejection ratio	V_{DD}=4.2V, Vp-p_sin=200mV	217Hz		76		dB
			1kHz		76		dB
	KAB Speaker Power supply rejection ratio	V_{DD}=4.2V, Vp-p_sin=200mV	217Hz		82		dB
			1kHz		82		dB
THD+N	Total harmonic distortion + noise	V_{DD}=4.2V, Po=1.2W, R_L=8Ω+33μH, f=1kHz, PVDD OVP=6V			0.1		%
Po	AB Speaker Output Power	THD+N=1%, R_L=8Ω+33μH, V_{DD}=4.2V, PVDD OVP=6V			2.0		W
		THD+N=10%, R_L=8Ω+33μH, V_{DD}=4.2V, PVDD OVP=6V			2.5		W
		THD+N=1%, R_L=8Ω+33μH, V_{DD}=3.6V，PVDD OVP=6V			2.0		W
		THD+N=10%, R_L=8Ω+33μH, V_{DD}=3.6V，PVDD OVP=6V			2.5		W
		THD+N=1%, R_L=8Ω+33μH, V_{DD}=4.2V			0.92		W
		THD+N=10%, R_L=8Ω+33μH, V_{DD}=4.2V			1.16		W
2-in-1 Receiver MODE（1X Chargepump）							
I_q	D Receiver quiescent current（overall）	V_{DD}=3.6V, input ac grounded, R_L=8Ω+33μH			6.0		mA
	AB Receiver quiescent current（overall）	V_{DD}=3.6V, input ac grounded, R_L=8Ω+33μH			6.3		mA
η	D Receiver efficiency	V_{DD}=4.2V, Po=0.8W, R_L=8Ω+33μH			88		%
	AB Receiver efficiency	V_{DD}=4.2V, Po=0.4W , R_L=8Ω+33μH			47		%

Parameter		Test conditions		Min	Typ	Max	Units
Av	D Receiver gain	V_{DD}=3.0V to 5.5V			0 (Note4)		dB
	AB Receiver gain	V_{DD}=3.0V to 5.5V			0 (Note4)		dB
Rini	D Receiver Inner input resistance	Av=4.5dB			48		kΩ
	AB Receiver Inner input resistance	Av=0dB			72		kΩ
Fin	D Receiver input cut-off frequency	Cin=68nF, Av=4.5dB			49		Hz
		Cin=100nF, Av=4.5dB			33		
	AB Receiver input cut-off frequency	Cin=68nF, Av=0dB			33		Hz
		Cin=100nF, Av=0dB			22		
E_N	D Receiver output noise	Av=0dB	20Hz to 20kHz, input ac grounded, A-weighting		11.9		μV
	AB Receiver output noise	Av=0dB			9.5		μV
THD+N	Total harmonic distortion + noise	V_{DD}=4.2V, Po=0.1W,R_L=8Ω+33μH, f=1kHz, D Receiver			0.015		%
		V_{DD}=4.2V, Po=0.1W,R_L=8Ω+33μH, f=1kHz, AB Receiver			0.2		%
PSRR	D Receiver Power supply rejection ratio	V_{DD}=4.2V, Vp-p_sin=200mV	217Hz		72		dB
			1kHz		71		dB
	AB Receiver Power supply rejection ratio	V_{DD}=4.2V, Vp-p_sin=200mV	217Hz		90		dB
			1kHz		90		dB
Po	D Receiver Output Power	THD+N=1%, R_L=8Ω+33μH, V_{DD}=4.2V			0.96		W
		THD+N=10%, R_L=8Ω+33μH, V_{DD}=4.2V			1.18		W
		THD+N=1%, R_L=8Ω+33μH, V_{DD}=3.6V			0.70		W
		THD+N=10%, R_L=8Ω+33μH, V_{DD}=3.6V			0.86		W
	AB Receiver Output Power	THD+N=1%, R_L=8Ω+33μH, V_{DD}=4.2V			0.35		W
		THD+N=10%, R_L=8Ω+33μH, V_{DD}=4.2V			0.47		W
Triple-Level Triple-Rate AGC							
T_{AT1}	AGC1 Attack Time				0.08 (Note4)		ms/dB
T_{AT2}	AGC2 Attack Time				0.64 (Note4)		ms/dB
T_{AT3}	AGC3 Attack Time				41 (Note4)		ms/dB
T_{RLT}	Release time				21 (Note4)		ms/dB
A_{MAX}	The maximum attenuation gain	V_{DD}=3.0V to 5.5V			-13.5		dB

Note 4：*Registers are adjustable; Refer to the list of registers.*

MEASUREMENT SETUP

AW87390G features switching digital output, as shown in Figure 7. Need to connect a low pass filter to VOP/VON output respectively to filter out switch modulation frequency, then measure the differential output of filter to obtain analog output signal.

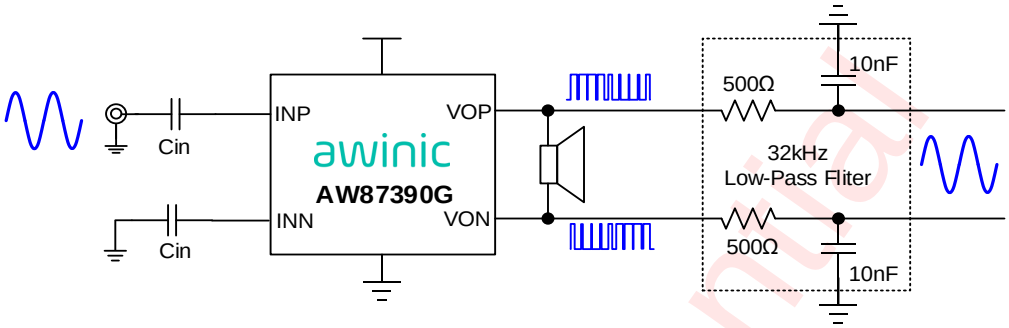


Figure 7 AW87390G Test Setup

Low pass filter uses resistance and capacitor values listed in Table 1.

R_{filter}	C_{filter}	Low-pass cutoff frequency
500Ω	10nF	32kHz
1kΩ	4.7nF	34kHz

Table 1 AW87390G Recommended Values for Low Pass Filter

Output Power Calculation

According to the above test methods, the differential analog output signal is obtained at the output of the low pass filter. The valid values Vo_rms of the differential signal , as shown in Figure 8：

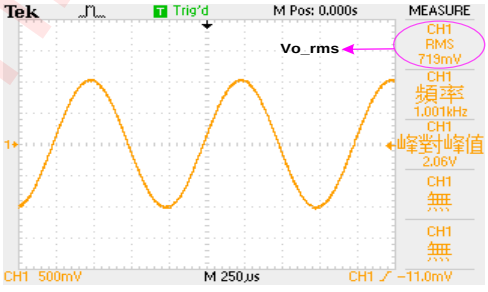
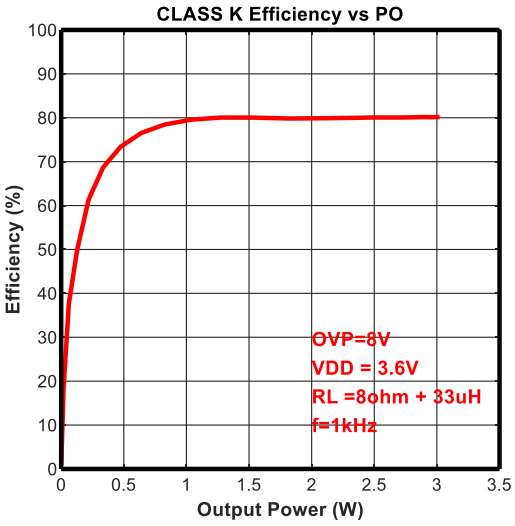


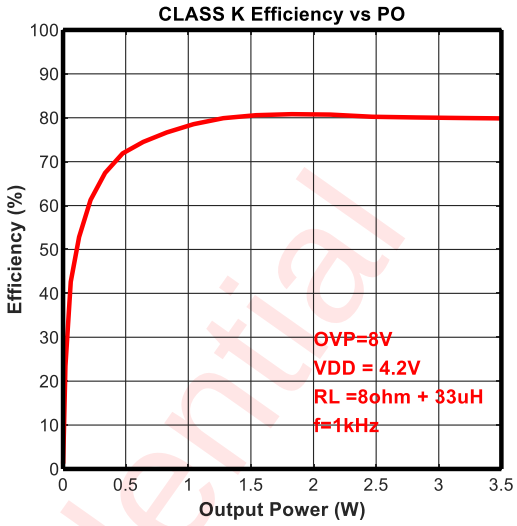
Figure 8 Output RMS Value

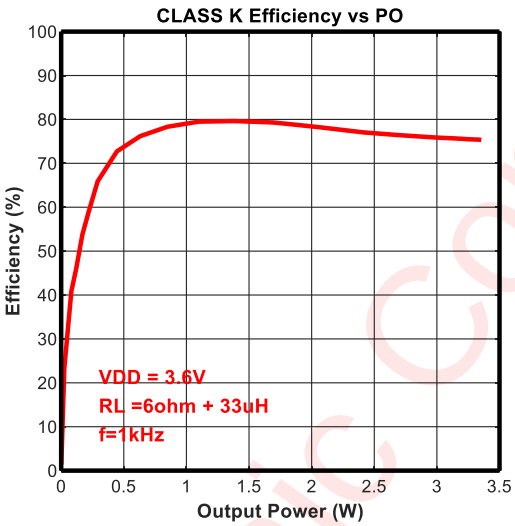
The power calculation of Speaker is as follows：

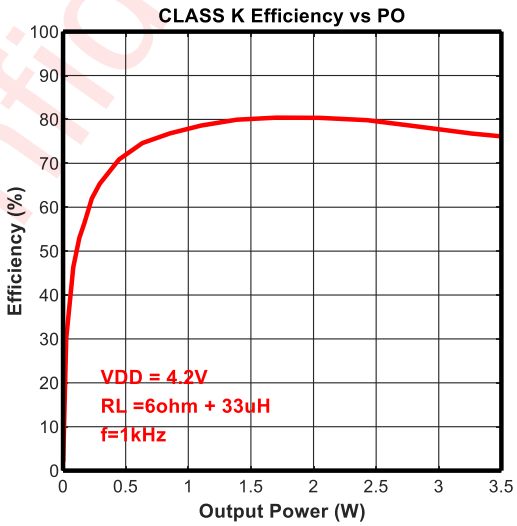
$$P_L = \frac{(V_{O\_rms})^2}{R_L}$$ R_L: load impedance of the speaker

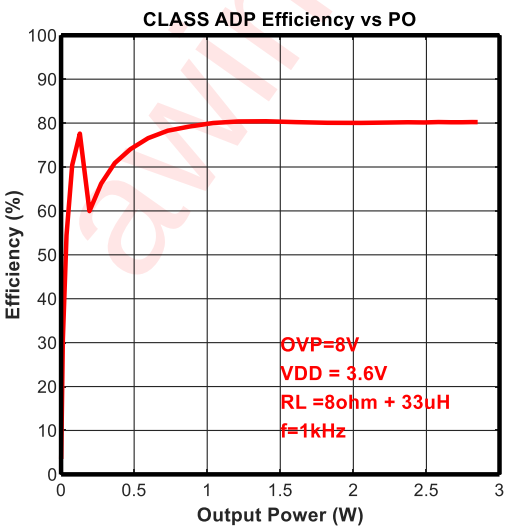
TYPICAL CHARATERISTICS

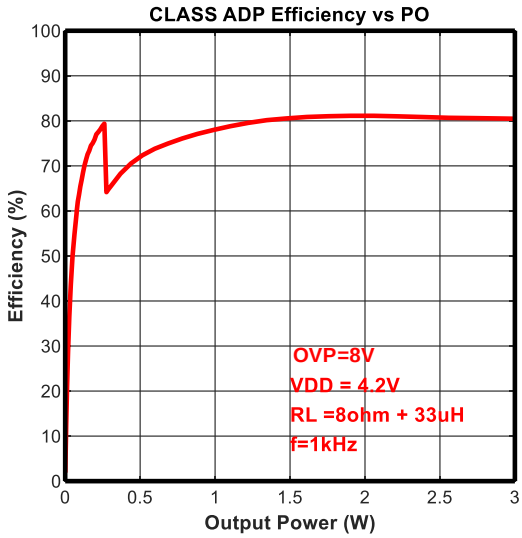


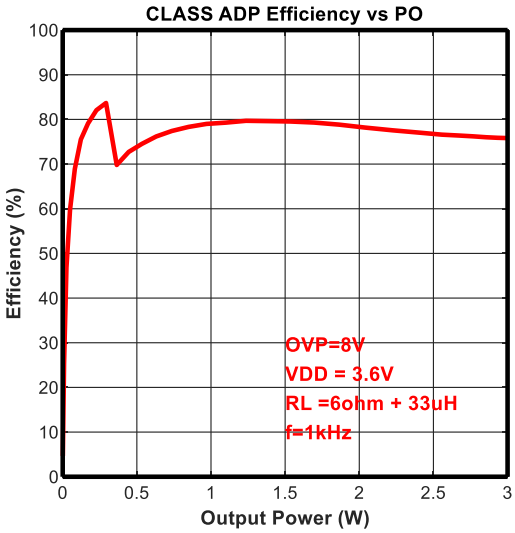


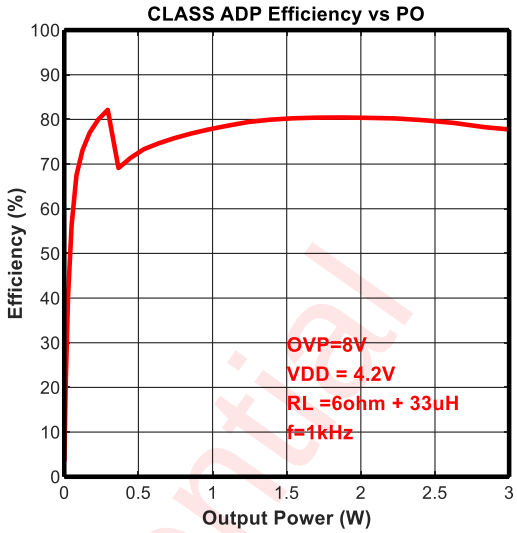


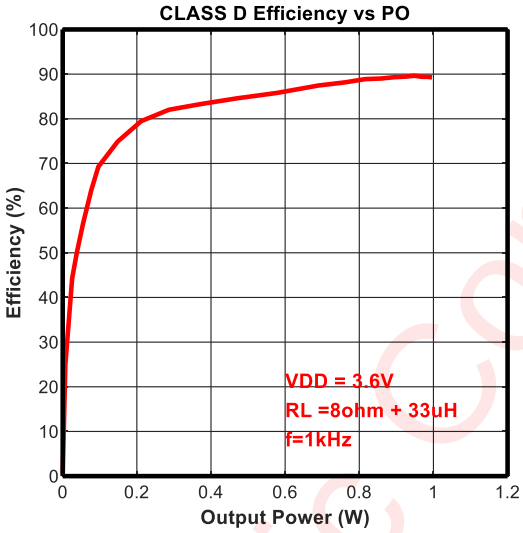


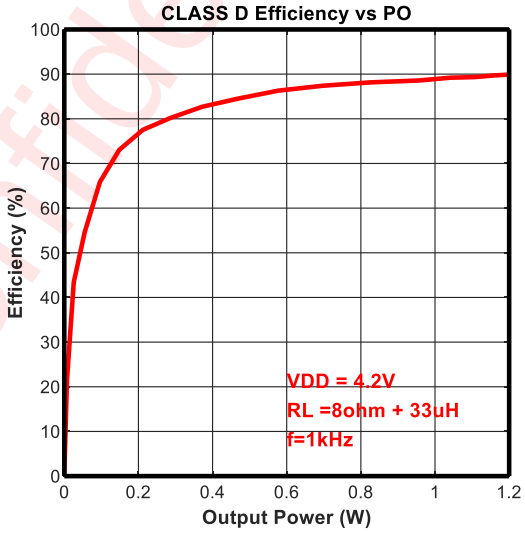


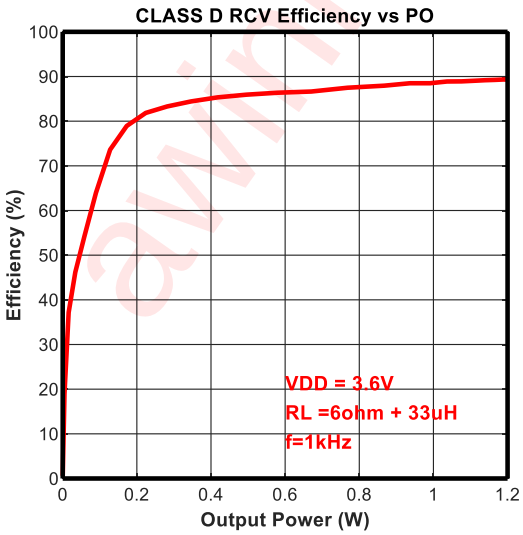


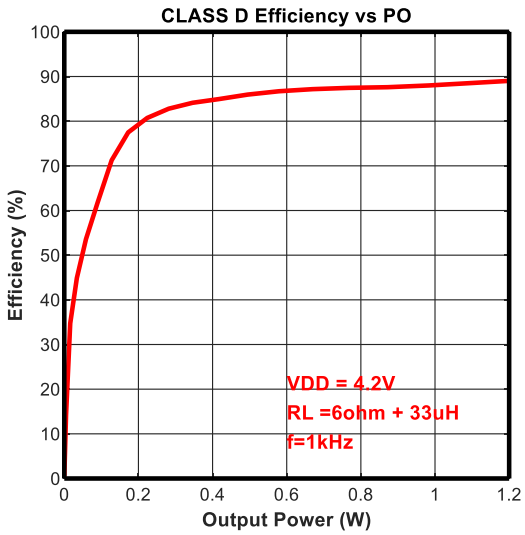


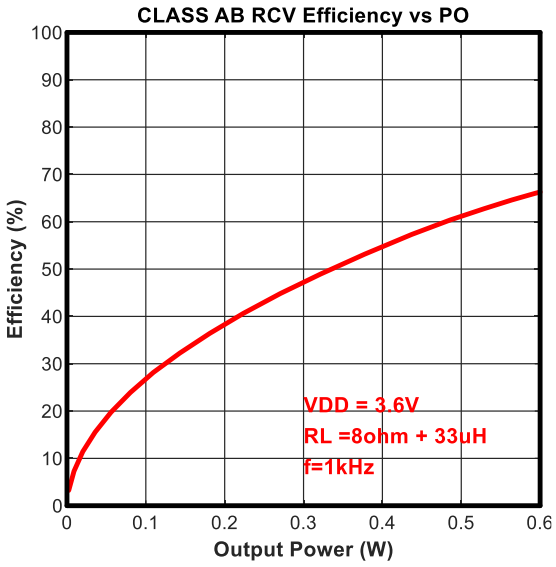


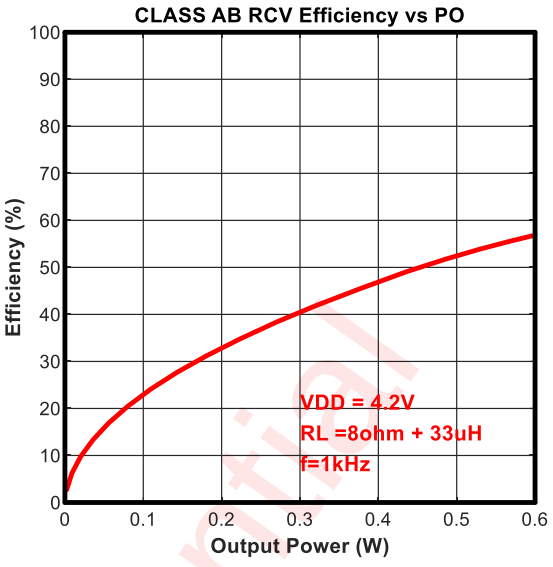


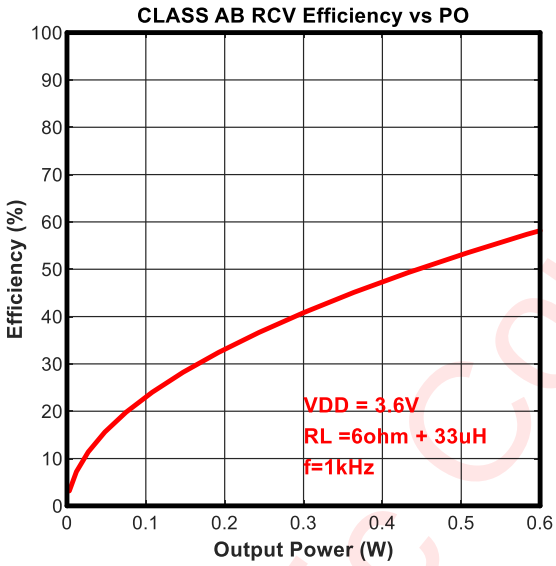


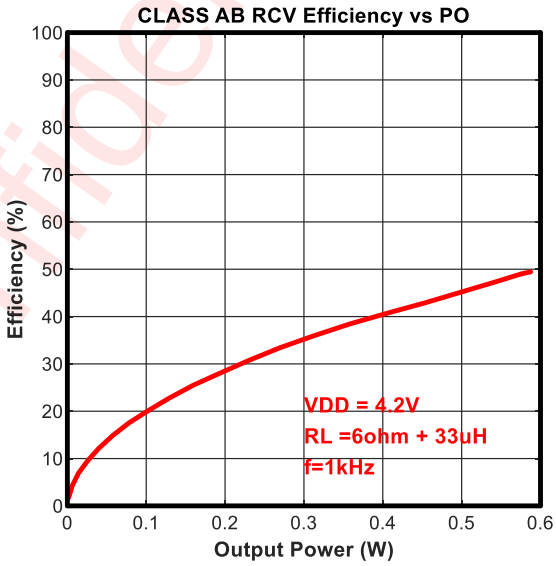


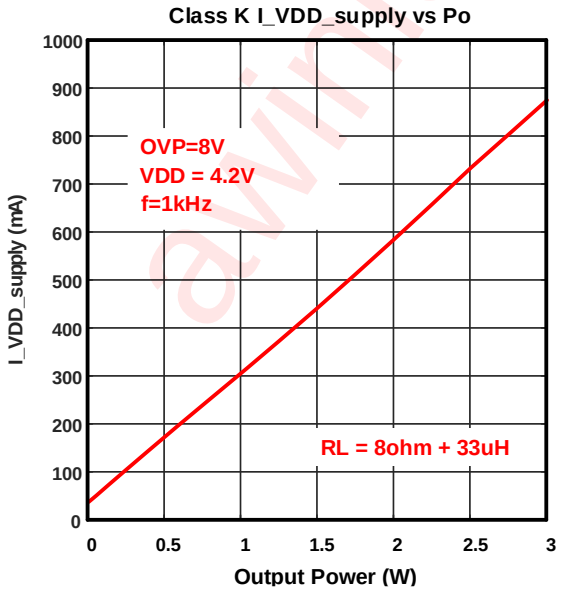


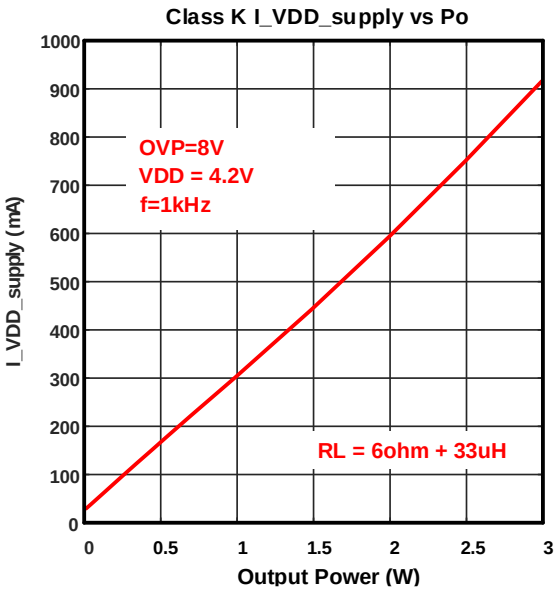


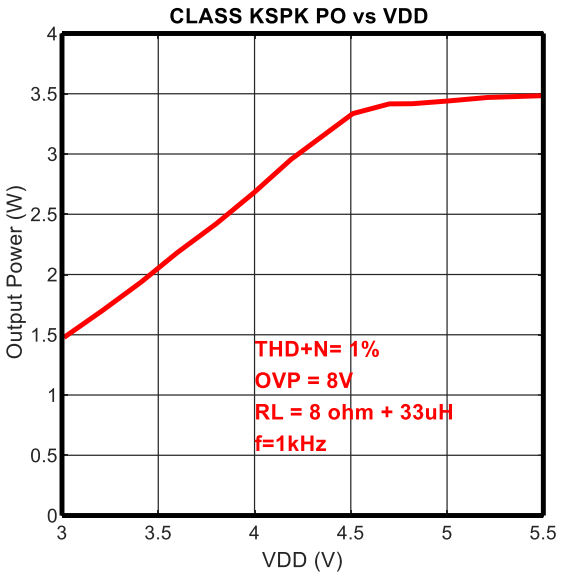


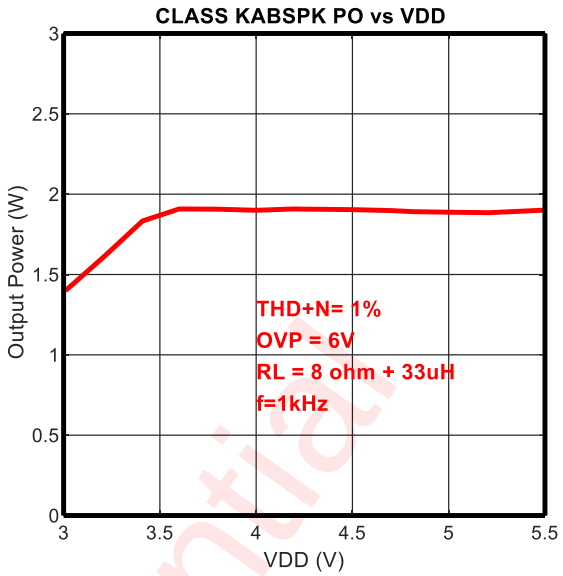


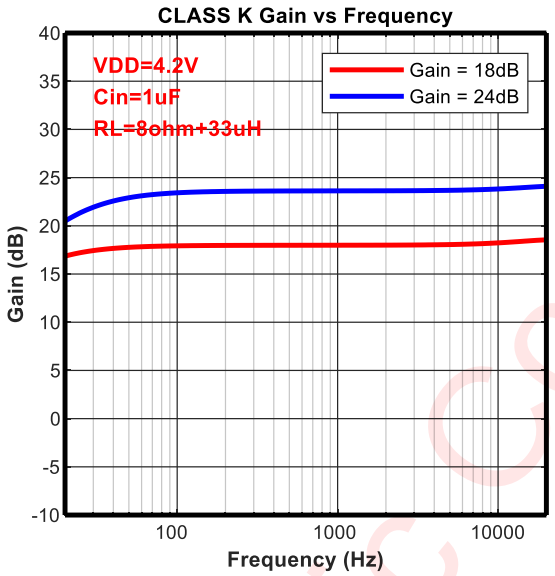


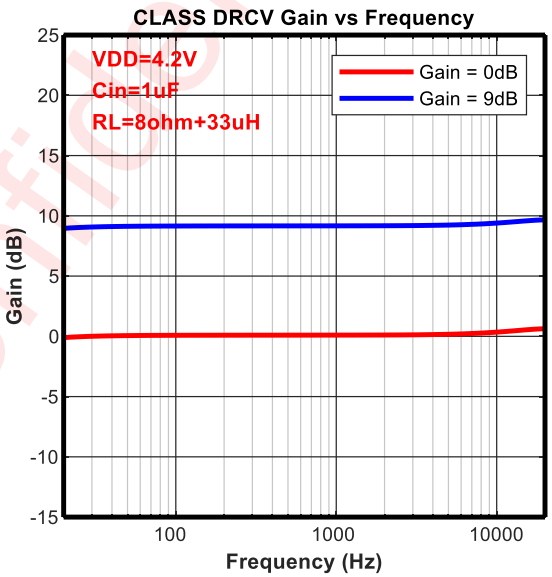


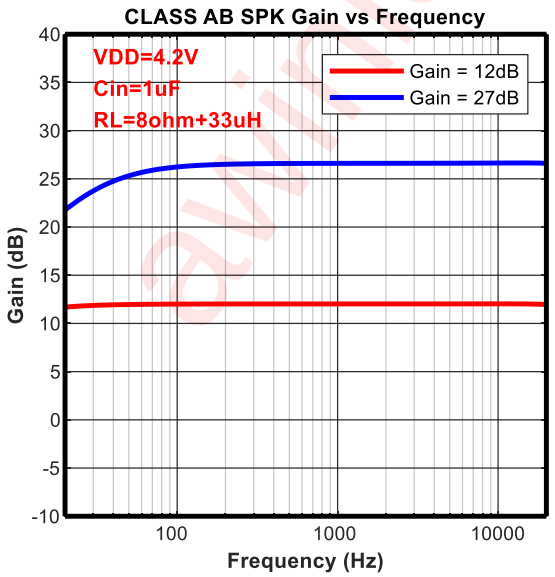


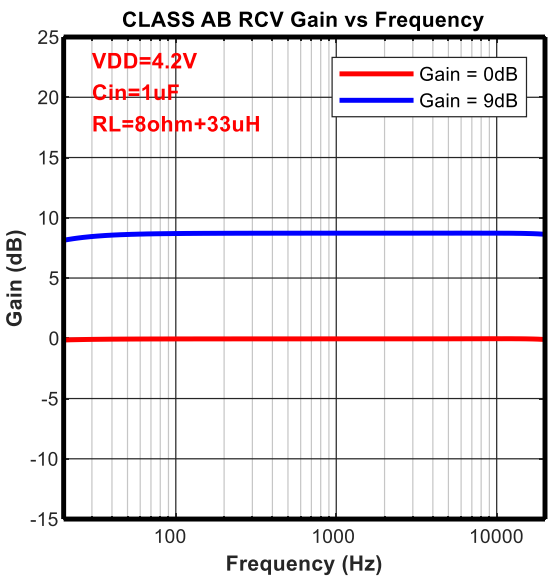


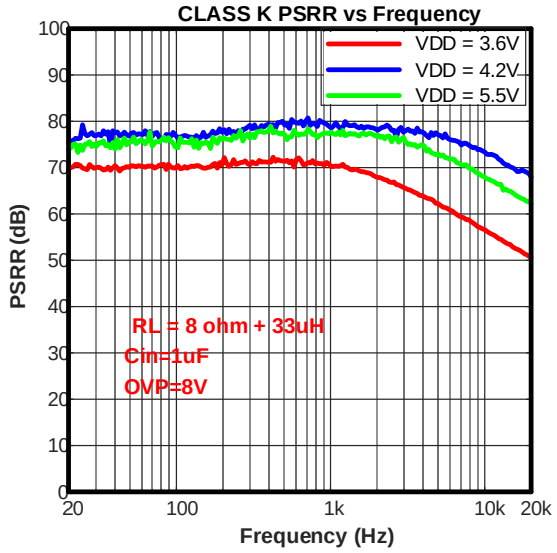


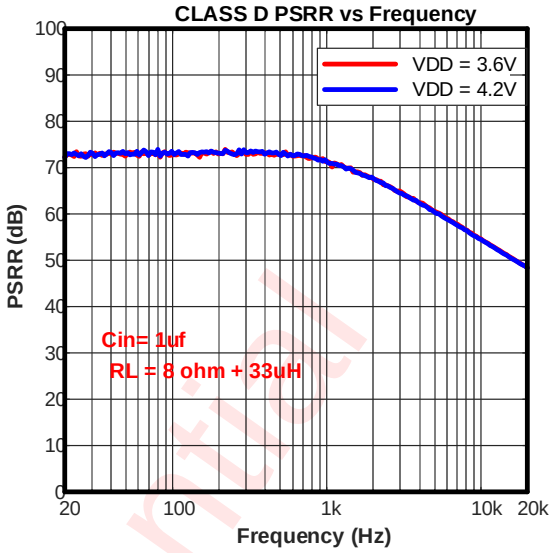


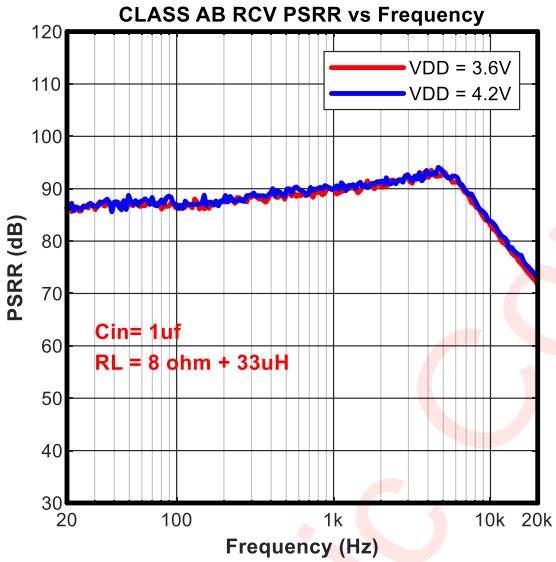


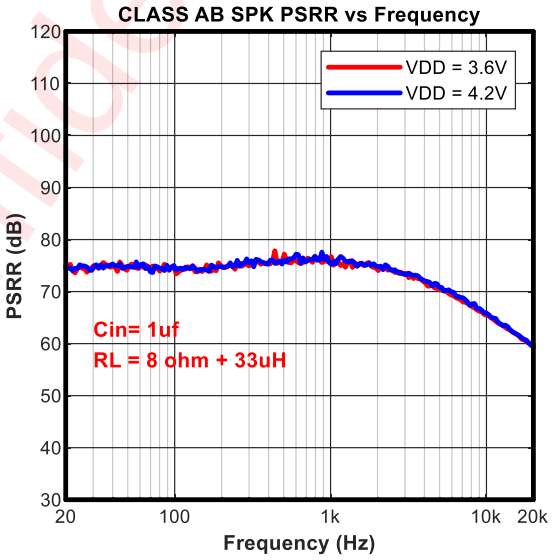


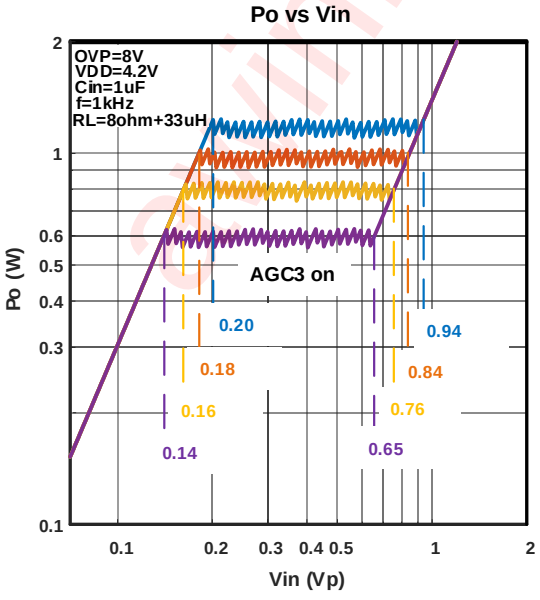


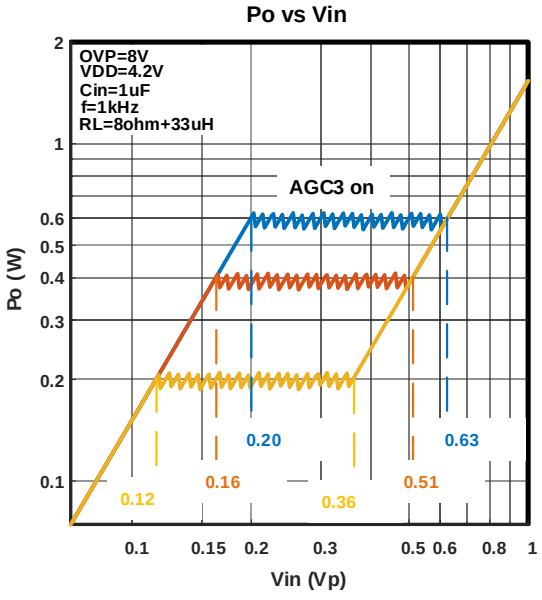


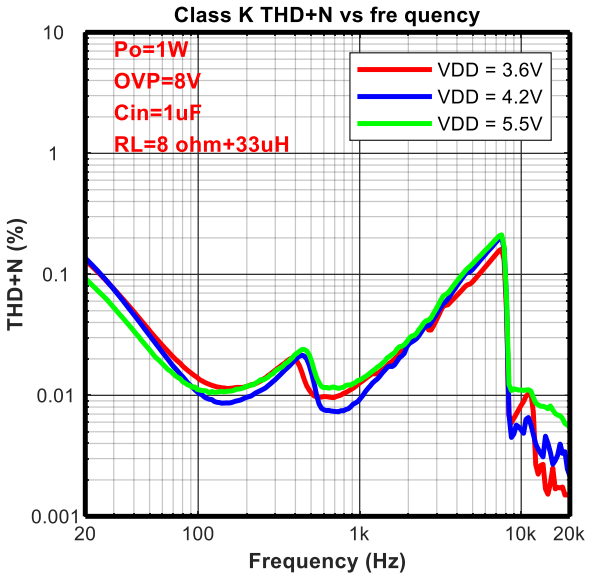


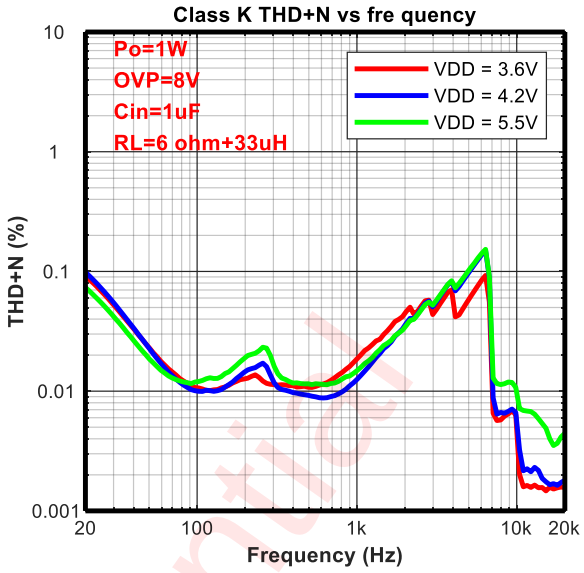


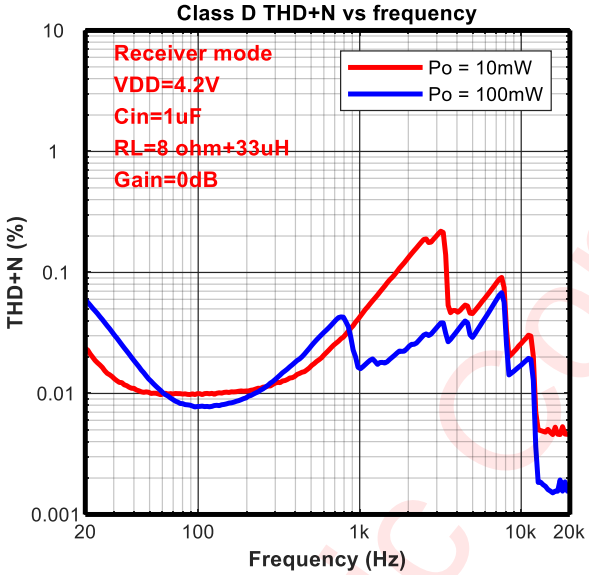


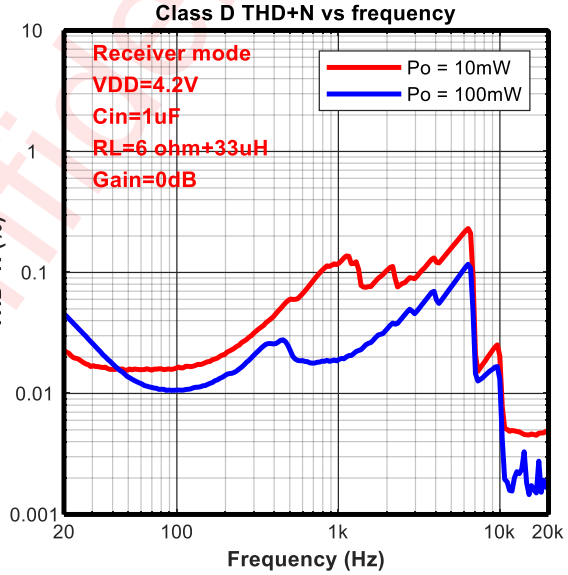


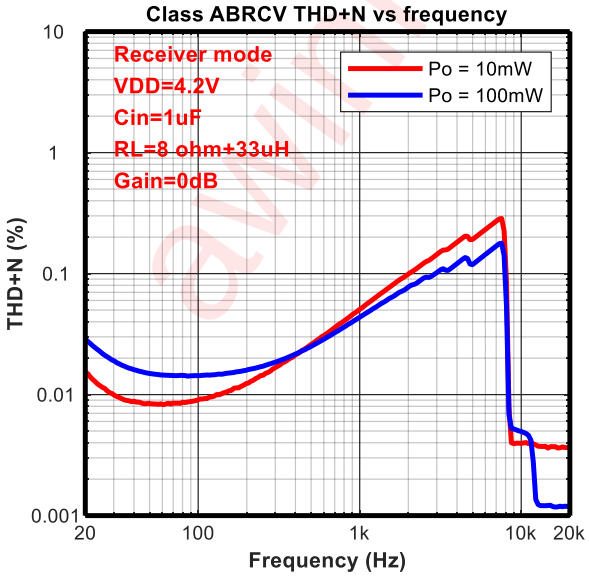


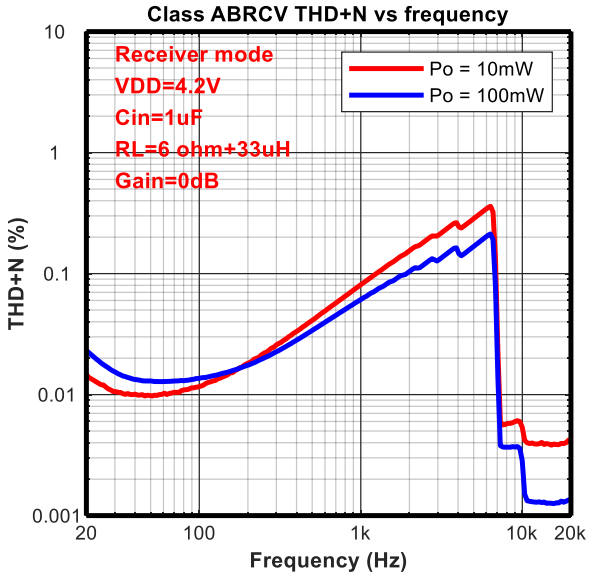




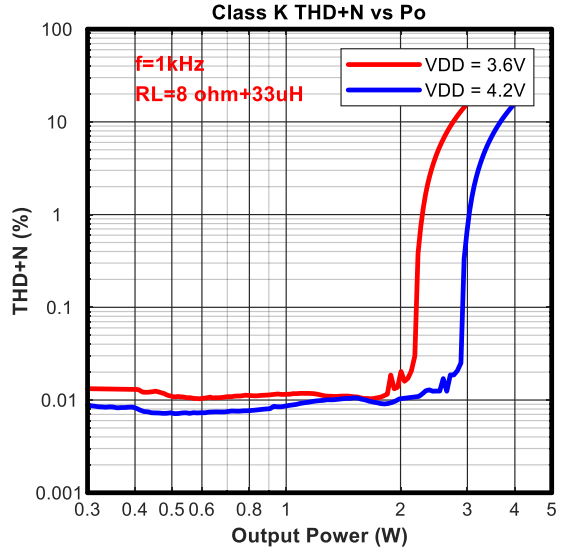




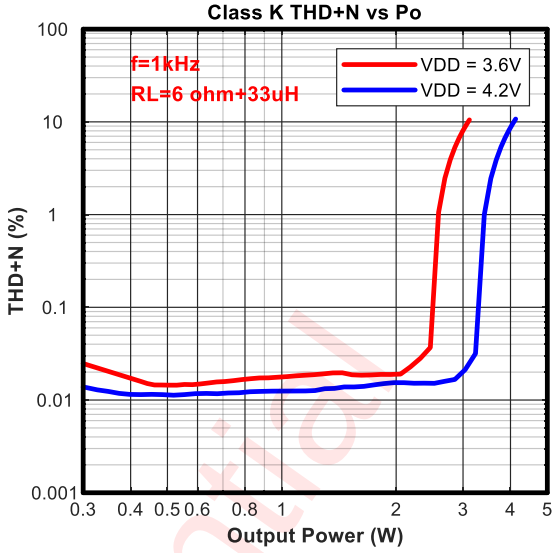




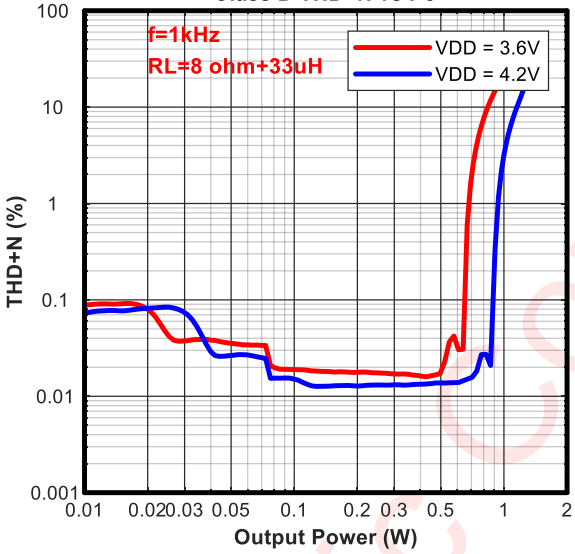
Class K THD+N vs Po



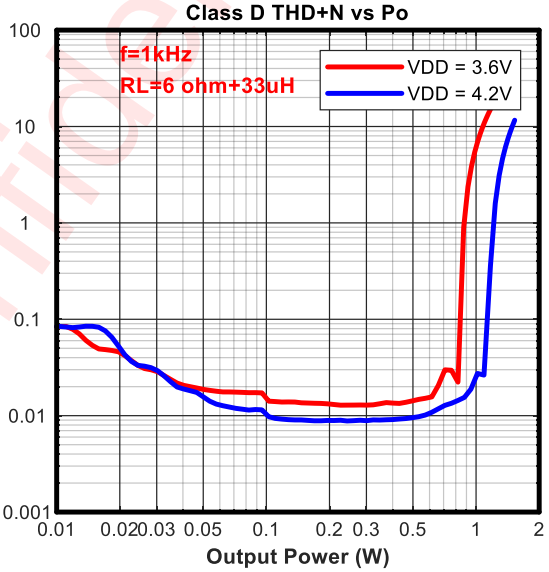
Class K THD+N vs Po



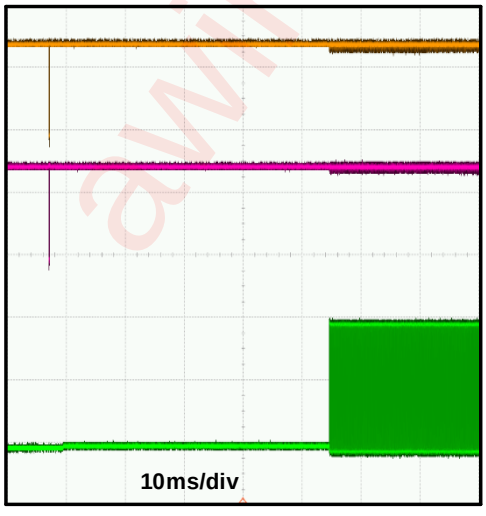
Class D THD+N vs Po



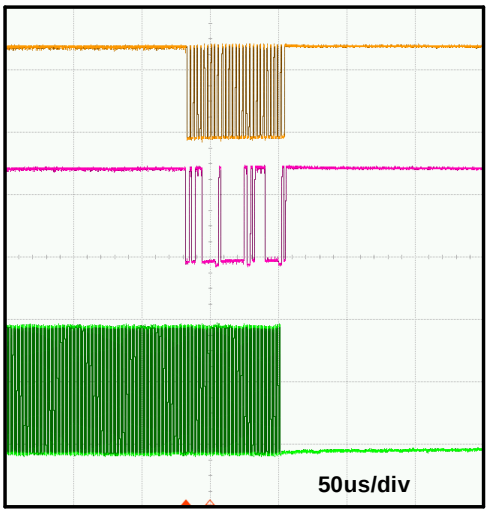
Class D THD+N vs Po



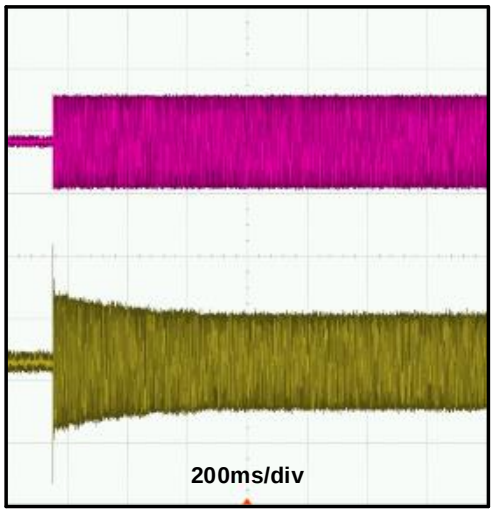
Start-up sequence



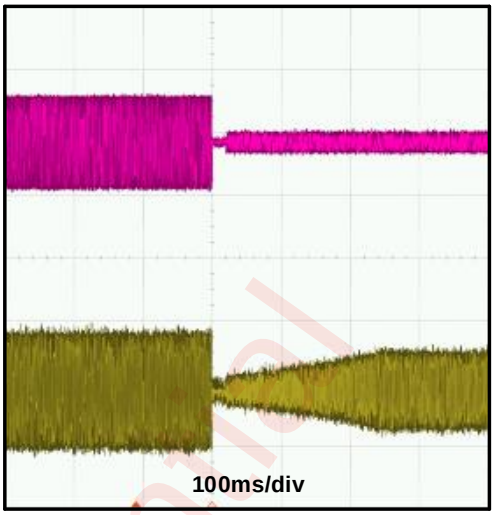
Shutdown sequence



Triple-Level Triple Rate AGC Attack Timing



Triple-Level Triple Rate AGC Release Timing



WORKING PRINCIPLE

AW87390G is specifically designed to improve the musical output dynamic range, enhance the overall sound quality, which is a new high efficiency, low noise, constant large volume, 6th Smart K audio amplifier. AW87390G integrates awinic's proprietary Triple-Level Triple-Rate AGC audio algorithm, effectively eliminating music noise and improving sound quality and volume. AW87390G integrated efficiency up to 90% of High voltage ADP DO-Chargepump boost technology, significantly improving the dynamic range of the music output。AW87390G noise floor is as low as to 38μV at speaker mode, with 102dB high signal-to-noise-ratio (SNR). The ultra-low distortion 0.02% and unique Triple-Level Triple-Rate AGC technology bring high quality music enjoyment.

AW87390G support Speaker and High power Receiver stereo applications；supports speaker and receiver 2-in-1 applications，class AB/D Receiver optional，ultra-low noise is 9.5uV.

AW87390G controls internal registers through the I2C interface. Register parameters include charge pump output Voltage, power amplifier gain, Triple-Level Triple-Rate AGC parameters etc.

AW87390G built-in over current protection, over temperature protection and short circuit protection function, effectively protect the chip. AW87390G features small FCQFN 2.0mmX2.5mmX0.55mm-16L package.

CONSTANT OUTPUT POWER

In the mobile phone audio applications, the AGC function to promote music volume and quality is very attractive, but as the lithium battery voltage drops, general power amplifier output power will reduce gradually. So, it is hard to provide high quality music within the battery voltage range. AW87390G uses unique Triple-Level Triple-Rate technology, within lithium battery voltage range (3.3V~4.35V), to guarantee that output power is constant, and the output power will not drop along with the decrease of lithium battery voltage. In the process of using the phone, even if the battery voltage drops, AW87390G can still provide high quality large volume music enjoyment. The output power of AW87390G can be configured from 0.1W to 2W via I^2C, matching general speakers. Unique Triple-Level Triple-Rate AGC technology can bring high-quality music enjoyment.

Triple-Level Triple-Rate AGC technology

AWINIC proprietary Triple-Level Triple-Rate AGC technology is designed for the protection of the high voltage power amplifier, which is divided into AGC1, AGC2 and AGC3 power levels, to obtain a large volume while maintaining excellent sound quality.

In practical applications, speaker can continuously work long hours at rated power, and also can work short-term at high power. For example, in the standard reliability of the loudspeaker experiment, the powder of peak power reached around four times of the rated power. For achieving larger volume and better sound quality, speakers need to work at high power for short periods of time, in order to improve the performance of the speaker. AW87390G Triple-Level Triple-Rate AGC technology can fit the speaker better and perform better overall performance. AGC1 prevents output signal clipping by detecting output voltage in a very short time after clipping, which can effectively restrain the noise clipping; AGC2 can improve the dynamic range of the music in a relatively short period of time; AGC3 can make the speaker work under rated power, which can effectively improve the volume and protect the speaker. Triple-Level Triple-Rate AGC can obtain more excellent overall performance.

Triple-Level Triple-Rate AGC detects the peak output voltage of the power amplifier, when the output peak voltage is higher than the compression threshold voltage, the amplifier gain decreases in 0.5dB step. When the output peak voltage is lower than the release threshold voltage, the amplifier gain is recovery to the initial gain in 0.5dB step. The detailed process can be described as follows:

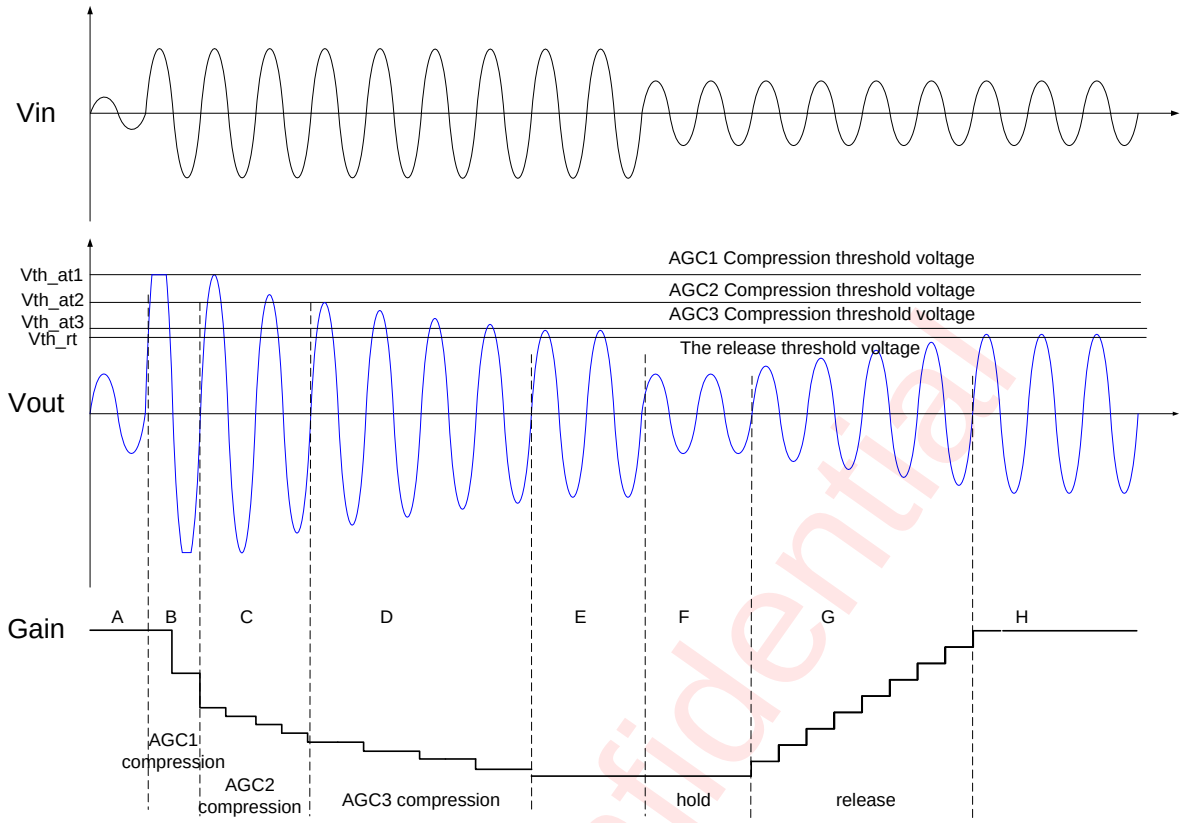


Figure 9 Triple-Level Triple-Rate AGC Operation Principle

A: Small input signal, the output voltage is lower than threshold voltage Vth of AGC, AGC don't work.

B: Input voltage becomes large. It leads to the output voltage clipping, AGC1 starts fast compression, the attack time is set through the I²C register 0x0Ah [2:1], when the output voltage is higher than Vth_at1, and gain register began to decrease. Gain decreases when the output signal passes through the zero. It eliminates the clipping noise as soon as possible.

C: When the output voltage is not clipping and higher than threshold voltage Vth_at2, AGC2 starts work, the attack time is set through the I²C register 0x09h [4:2], gain register begins to decrease at a certain rate. Gain register began to decrease. Gain decreases when the output signal passes through the zero. The output voltage gradually decreases to below the AGC2 attack threshold voltage Vth_at2, which can protect the speaker and enhance the sound.

D: When the output voltage is lower than the AGC2 attack threshold voltage Vth_at2 and higher than the AGC3 attack threshold voltage Vth_at3, AGC3 starts work, the attack time is set through the I²C register 0x07h [4:2], and gain register began to decrease at a certain rate. Gain decreases when the output signal passes through the zero, so the output voltage gradually decreases to below of the AGC3 attack threshold voltage Vth_at3, matching the speaker to achieve greater volume and better sound quality.

E: Triple-Level Triple-Rate AGC attack time ends, Amplifier output power is close to the speaker rated power.

F: Input voltage decreases, the output voltage becomes lower than the release threshold voltage Vth_rt, at this point, gain remains the same in the maintain time (10ms~20ms).

G: Gain increases when the time of output voltage lower than the release threshold voltage Vth_rt is longer than the holding time. The release time can be set through I²C register 0x07h [7:5].

H: Stop release when the output signal is larger than the release threshold or the gain is equal to the initial value. The output voltage remains constant.

Triple-Level Triple-Rate AGC can switch independently according to different application requirements. Such as close AGC1 and AGC2, retain only AGC3, this is the single-AGC mode, similar to AW8736 (AGC3 attack

time is set to 1.28ms/dB; release time is set to 41ms/dB); Close AGC2, open AGC1 and AGC3, this is Multi_level AGC. It can be set similar to AW8738 (AGC1 attack time is set to 80us/dB; AGC3 attack time is set to 0.64ms/dB; release time is set to 10.24ms/dB).

Zero-Crossing Adjustment Technology

Traditional AGC doesn't contain zero adjustment technology; AGC gain changes generally at the peak, the gain variation at the peak would generate a certain transient distortion, such distortions are audibly imperceptible. Such as individual songs have a slight click.

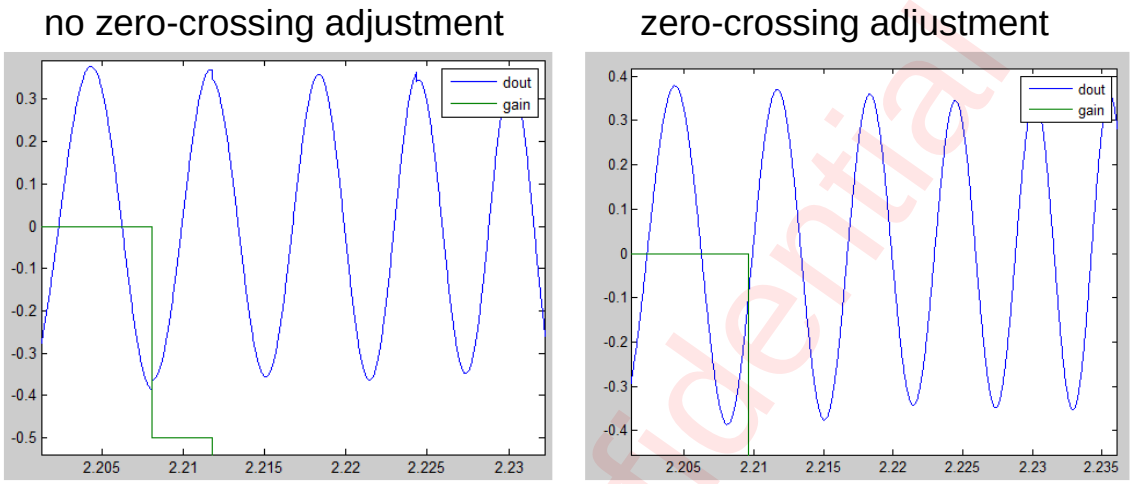


Figure 10 Zero-adjust Comparison

As shown above, when there is no zero-adjustment technology, it can be seen the obvious step change at the peak of large signal, the steps sound slightly perceived in special audio. Gain changes at zero. The steps disappear by using zero-crossing detection technology. Using zero detection technology can make the music pure and natural.

ADP DO-Chargepump

AW87390G features ADP DO-chargepump technology, with high efficiency and high drive capability, operating frequency 1.45MHz, built-in soft start circuit, current limiting control loop and over-voltage control loop to ensure circuit stable and reliable work.

High efficiency

AW87390G features ADP DO-chargepump architecture, the output voltage PVDD of which can be adjusted according to the output power. When the output power is less than Pth, the PVDD is equal to the input voltage VDD, and when the output power is greater than Pth, the PVDD is twice the VDD. Under ideal conditions, the efficiency of ADP DO-chargepump can reach 100%. The efficiency of the ADP DO-chargepump is the ratio of the output power to input power:

$$\eta = \frac{P_{OUT}}{P_{IN}} * 100\%$$

For example, in an ideal M times the ADP DO-chargepump, the input current I_{IN} is M times of I_{OUT}, the efficiency formula is:

$$\eta = \frac{P_{OUT}}{P_{IN}} * 100\% = \frac{V_{OUT} * I_{OUT}}{V_{IN} * M * I_{OUT}} * 100\% = \frac{V_{OUT}}{M * V_{IN}} * 100\%$$

Where M is the operating mode variable of the chargepump, V_{OUT} is the output voltage of chargepump,

I_{OUT} is the load current. For the ADP DO-chargepump, the output voltage is twice of the input voltage, can greatly improve the power efficiency, taking into account the chargepump internal switching losses and IC quiescent current loss, the actual efficiency is as high as 90%.

AW87390G ADP DO-chargepump can be set to pass-through mode and 2X chargepump mode via the register 0x02h [3] to supply power to the Class D output stage.

Chargepump structure

The basic diagram of the chargepump shows in Figure 11, the chargepump in AW87390G has four switches, the output voltage PVDD can reach twice of the input voltage through the four switches of the timing control.

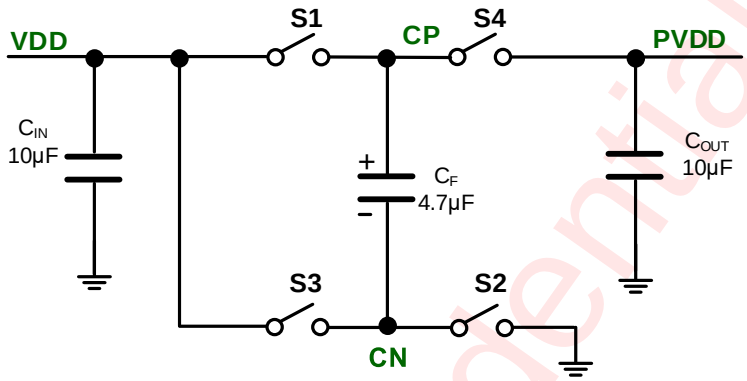


Figure 11 Chargepump Schematic Diagram

The chargepump works with two phases, in Φ1, as shown in the Figure 12：S1, S2 on, VDD charges the capacitor C_F.

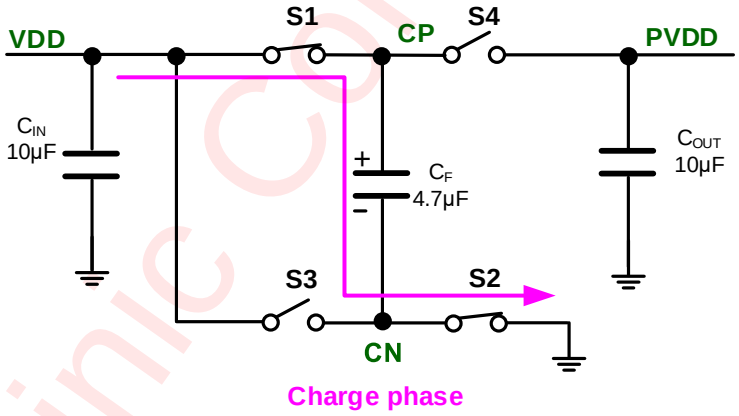


Figure 12 Φ1： Flying Capacitor Charging

In Φ2, as shown in the Figure 13：S1 and S2 off, S3 and S4 on, since the voltage across the capacitor cannot be changed abruptly, the capacitors C_F are superimposed on VDD, causing the PVDD to rise to a higher voltage.

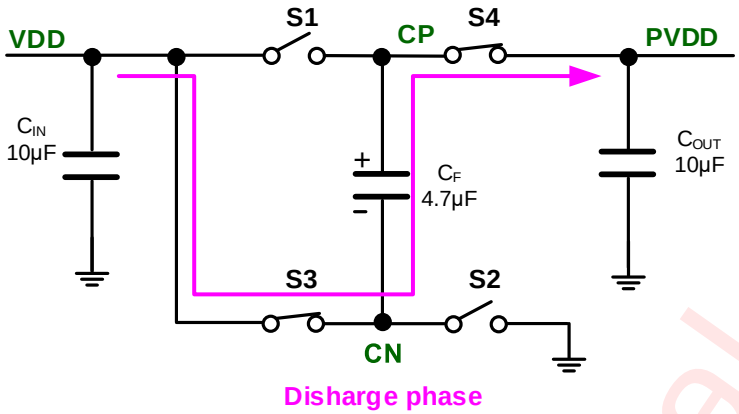


Figure 13 Φ2：Flying Capacitor Charge is Transferred to C_{OUT}

Soft start

In order to limit the inrush current of the power supply during the start of the chargepump, the chargepump has a soft start function. The current limit is 300mA during start-up.

Current limiting control

ADP DO-chargepump architecture integrates the current limiting control loop, in normal operation, the current limiting control loop controls the maximum output current capability of the chargepump when the load is too heavy or the chargepump flows through a large current.

Over-voltage protection(OVP) control

The output voltage PVDD is twice of the input voltage VDD in ADP DO-chargepump structure, providing high voltage rail for internal power amplifier circuits, allowing the amplifier in the lithium battery voltage range to provide greater output dynamic range, in order to achieve high volume, high-quality class K audio amplifier playback sound quality. ADP DO-chargepump integrated over-voltage protection control loop, when the input voltage VDD is greater than 4V, the output voltage PVDD is not twice of VDD, it is determined by the over-voltage control loop. And PVDD is stable at 8.0V.

Speaker & Receiver 2-in-1 application

AW87390G built-in speaker and receiver 2-in-1 application mode, through the register settings, there are class AB-type 2-in-1 receiver mode and class D-type 2-in-1 receiver mode can be selected, the gain can be adjusted through the I²C register 0x05, adjustable range of 0~9dB, the application is very flexible. The 2-in-1 receiver mode uses the signal path of the speaker, with ultra-low distortion and strong drive capability, and eliminates the need for additional peripheral components, saving system cost and PCB layout space.
In the typical application case of Figure 5, the input capacitance Cin=68nF, the gain is 24dB in the speaker application mode, the input high-pass cutoff frequency is 260Hz; In 4.5dB gain class D-type 2-in-1 receiver application mode, The output noise is 16μV, the input high-pass cut-off frequency is 34Hz; In 0dB gain class AB-type 2-in-1 receiver application mode, the output noise is as low as 9.5μV, the input high-pass cut-off frequency is 22Hz, which is very suitable for high-definition voice applications. AW87390G can achieve speaker and receiver's 2-in-1 application without changing any hardware in the case.

High Power Receiver Stereo Applications

AW87390G built-in high-power receiver stereo application mode, makes full use of the receiver, not only takes the voice calls into account and uses the receiver as speaker, but also combines the AWINIC's propriety TLTR-AGC technology, significantly enhancing the stereo sound quality and volume, enhancing the

dynamic music, therefore, high power receiver stereo application has gradually become a mainstream application in smart phone.

AW87390G is in the high-power receiver stereo application mode, when the register 0x02h [2] is set to 1. Gain adjustable range is 0~ 27dB by adjusting the I²C register 0x05h [4: 0], AGC3 power adjustable range is 0.1W~1.5W@8ohm receiver, 0.025W~0.375W@32ohm receiver through adjusting the I²C register 0x06h [3:0]. AW87390G can flexibly match a variety of high-power Receiver, combined with TLTR AGC technology, significantly enhance the stereo sound quality and volume, and enhance music dynamic listening.

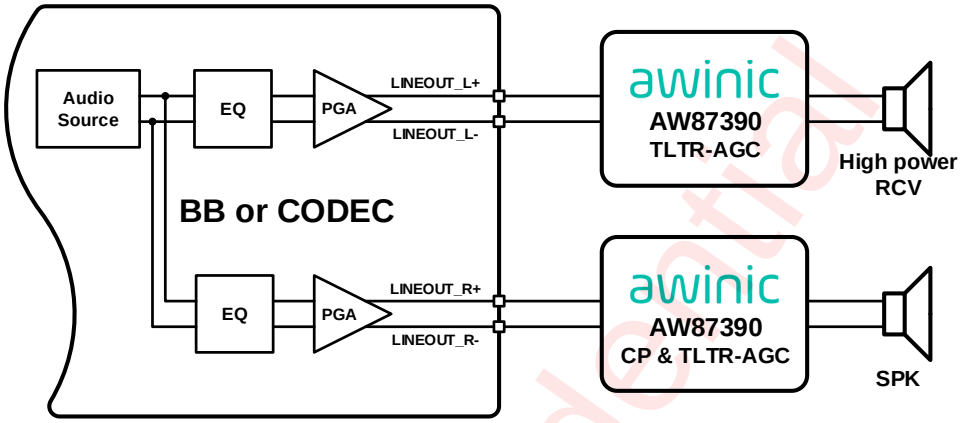


Figure 14 AW87390G High Power Receiver Stereo Mode Application

RNS(RF TDD Noise Suppression)

TDD Noise Causes

GSM cell phones use TDMA (Time Division Multiple Access) slot sharing technology. The time is divided into periodic frames in TDMA, and each frame is subdivided into a plurality of time slots. In order to transmit signals to the base station, the signals sent from the base stations to the plurality of mobile terminals are arranged in a predetermined time slot in the transmission. In this case, each TDMA frame contains 8 time slots, the entire frame is about 4.615ms long, and each slot time is 0.577ms.

With GSM handset, the RF power amplifier will transmit once every 4.615ms (217Hz), and the signal will produce intermittent Burst current and strong electromagnetic radiation. Intermittent Burst current will form a power fluctuation of 217 Hz; High frequency (900MHz and 1800MHz) RF signals form a 217Hz RF envelope signal. 217Hz power fluctuations will be conducted through the conduction to the audio signal path, 217Hz RF envelope signal will be coupled through the radiation into the audio signal path, if the protection is not good, it will produce an audible TDD Noise, which includes the 217Hz noise And a harmonic noise signal of 217 Hz.

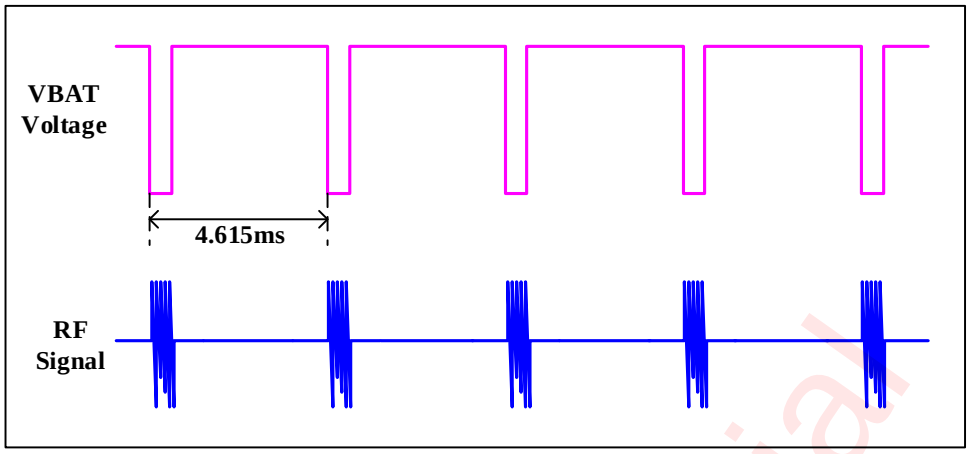


Figure 15 Schematic Diagram of Power Supply Voltage and RF Signal during GSM RF Operation

RNS fully inhibit the conduction and radiation interference by the AWINIC unique circuit architecture. Effectively improve the ability to suppress TDD Noise.

Conduction noise suppression

When the RF power amplifier is operating, it will draw the current from the battery by 217Hz frequency, Power supply will be introduced to 217Hz power ripple since the battery has a certain internal resistance, it will be coupled to the speaker through the audio power amplifier. The ability to suppress power fluctuations depends on the PSRR of the audio power amplifier.

$$PSRR = 20\log(\frac{vdd_{ac}}{vout_{ac}})$$

Due to the input and output of the fully differential amplifier is perfectly symmetrical, theoretically, the effect of the power supply fluctuation on the two outputs is exactly the same, and the differential output is completely unaffected by the power supply fluctuation. In practice, due to process bias and other factors, the amplifier will have a certain mismatch, PSRR is generally better than 60dB, it shows the output relative to the power fluctuations can be reduced by 1000 times, such as 500mVp power fluctuations, the differential output of 0.5 mV, which basically can meet the application requirements.

But in practical applications, the power amplifier may encounter conduction of TDD Noise problem even if its PSRR is 60dB or 80dB, why is this? Because we also need to consider the impact of peripheral power mismatches of audio power amplifiers

For conventional audio power amplifiers, when the input resistor Rin and the input capacitor Cin mismatch, will greatly affect the audio power amplifier PSRR indicators, in the case of 24V/V gain, PSRR will be weakened to 46dB or so if the input resistance and Capacitor with 1% mismatch. PSRR will be weakened to 28dB or so if the input resistance and input capacitance mismatch with 10% mismatch, when the power fluctuations, it is easy to produce audible TDD Noise.

In order to enhance the audio power amplifier PSRR in the input resistance and input capacitance mismatch case, AW87390G features a unique conduction noise suppression circuit, making the power amplifier to maintain a high PSRR value even in the input resistance, the input capacitance deviation of 10% or more, this greatly inhibits the generation of conducted noise.

Radiation noise suppression

Input traces, output traces, horn loops, and even power and ground loops are likely to be subject to RF radiation interference in the audio signal module, longer input traces and output traces similar to the antenna, especially vulnerable RF radiation effects.

The reasonable PCB layout can reduce the influence of RF radiation in the design, such as shorten the line length of input and output as much as possible; audio devices should be shielded and far away from the RF antenna, maintain the integrity of the device to audio signal pathway; to increase the small bypass capacitor RF signals in the sensitive nodes. However, in practical applications, PCB layout is difficult to fully consider the influence of RF radiation on the audio signal path, and some RF energy will still be coupled to the audio signal path to form audible TDD Noise. Therefore, AW87390G features a unique RF radiation suppression circuit, a shielding layer inside the chip, effectively prevent high frequency energy into RF chip, to ensure that the drive single of the amplifier provided to the speaker will not be affected by the antenna RF radiation, thus avoiding the antenna RF Radiation caused by TDD Noise.

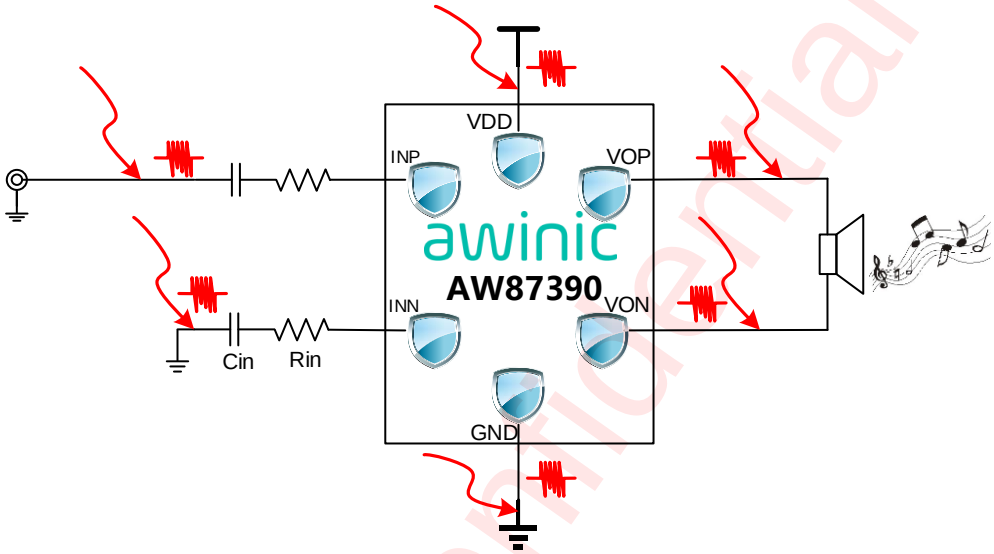


Figure 16 RF Radiation Coupling Graph

Class D amplifier without filter

When the traditional class D amplifier is in idle state of no input signal, the output will have the inverse square wave, it will directly above the load of the speaker, will form a large current power switch on the speaker, therefore we need to increase the LC filter to restore the analog audio signal at the amplifier output. The LC filter increase the cost and PCB layout area, while increase the power consumption, reduce the performance of THD+N.

The AW87390G features a Class D amplifier without a filter, eliminating the need for an output LC filter. In the idle state of no input signal, the two outputs (VOP, VON) of the amplifier are in-phase square waves and not generate idle switching currents on the speaker load. When the input signal is added to the input terminal, the duty ratio of the output is changed. The duty cycle of the VOP becomes larger and the duty cycle of the VON becomes smaller, and the difference value of the output forms the differential amplified signal on the speaker.

EEE

The AW87390G features a unique Enhanced Emission Elimination (EEE) technology, that controls fast transition on the output, greatly reduces EMI over the full bandwidth, fully meet FCC CLASS B specification requirements.

Pop-Click Suppression

The AW87390G features unique timing control circuit, that comprehensively suppresses pop-click noise, eliminates audible transients on shutdown, wakeup, and power-up/down.

Over temperature protection

When the AW87390G operates in a fault condition, the chip temperature is too high, up to a preset temperature protection temperature threshold (160°C), the system starts overheating protection, the chip will be turned off, restarts to resume normal work when the chip temperature returns to normal operating range (less than 130°C).

Automatic recovery of overcurrent protection

AW87390G with automatic recovery of the output overcurrent protection function, when the overcurrent occurs, AW87390G internal protection circuit will chip off to ensure that the chip is not damaged, when the short-circuit fault is eliminated, the chip will automatically resume working without restarting.

I²C Timing feature

Parameter			MIN	TYP	MAX	UNIT
No.	Sym	Name				
1	f_{SCL}	SCL Clock frequency			400	kHz
2	t_{LOW}	SCL Low level Duration	1.3			μs
3	t_{HIGH}	SCL High level Duration	0.6			μs
4	t_{RISE}	SCL, SDA rise time			0.3	μs
5	t_{FALL}	SCL, SDA fall time			0.3	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			μs
7	$t_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			μs
9	t_{BUF}	the Bus idle time START state to STOP state	1.3			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			μs
11	$t_{HD:DAT}$	SDA hold time	10			ns

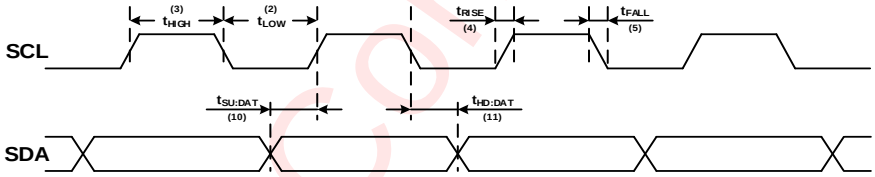


Figure 17 SCL and SDA timing relationships in the data transmission process

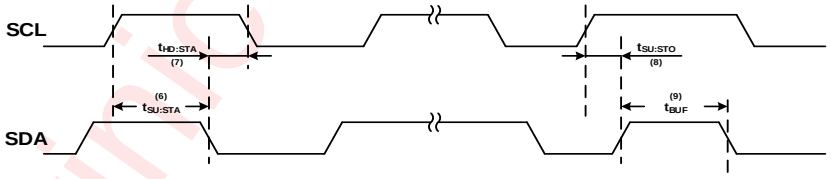


Figure 18 the Timing Relationship between START and STOP State

General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The device is addressed by a unique 7-bit address; the same device can send and receive data. In addition, Communications equipment has distinguish master from slave device: In the communication process, only the master device can initiate a transfer and terminate data and generate a corresponding clock signal. The devices using the address access during transmission can be seen as a slave device.

SDA and SCL connect to the power supply through the current source or pull-up resistor. SDA and SCL default is a high level. All data to start transmission and end of transmission requires the main device to

issue START state and STOP status:

START state：The SCL maintain a high level, SDA from high to low level

STOP state：The SCL maintain a high level, SDA pulled low to high level

Start and Stop states can be only generated by the master device. In addition, if the device does not produce STOP state after the data transmission is completed, instead re-generate a START state (Repeated START, Sr), and it is believed that this bus is still in the process of data transmission. Functionally, Sr state and START state is the same. As shown in Figure 19.

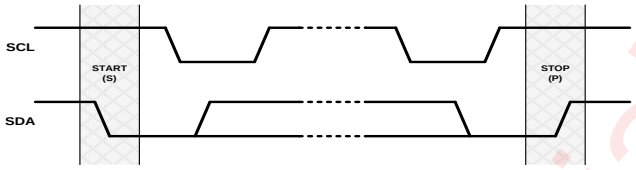


Figure 19 START and STOP State Generation Process

In the data transmission process, when the clock line SCL maintains a high level, the data line SDA must remain the same. Only when the SCL maintain a low level, the data line SDA can be changed, as shown in Figure 20. Each transmission of information on the SDA is 9 bits as a unit. The first eight bits are the data to be transmitted, and the first one is the most significant bit (Most Significant Bit, MSB), the ninth bit is an confirmation bit (Acknowledge, ACK or A), as shown in Figure 21. When the SDA transmits a low level in ninth clock pulse, it means the acknowledgment bit is 1, namely the current transmission of 8 bits data are confirmed, otherwise it means that the data transmission has not been confirmed. Any amount of data can be transferred between START and STOP state.

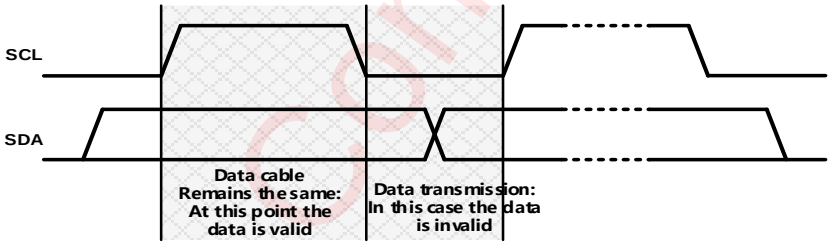


Figure 20 The Data Transfer Rules on the I²C Bus

The whole process of actual data transmission is shown in Figure 21. When generating a START condition, the master device sends an 8-bit data, including a 7-bit slave addresses (Slave Address), and followed by a "read / write" flag ($R/\overline{W}$). The flag is used to specify the direction of transmission of subsequent data. The master device will produce the STOP state to end the process after the data transmission is completed. However, if the master device intends to continue data transmission, you can directly send a Repeated START state, without the need to use the STOP state to end transmission.

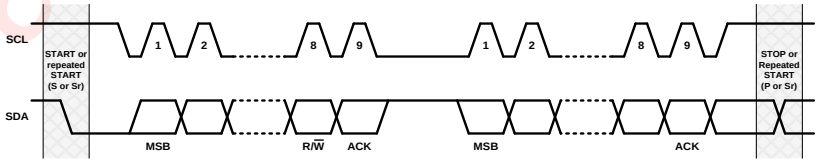


Figure 21 Data Transmission on the I²C Bus

I²C Read/Write Processes

The following describes two kinds of ways of the I²C bus data transmission:

Write Process

Writing process refers to the master device write data into the slave device. In this process, the transfer direction of the data is always unchanged from the master device to the slave device. All acknowledge bits are transferred by the slave device, in particular, AW87390G as the slave device, the transmission process in accordance with the following steps, as shown in Figure 22:

Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.

Master device transmits the 7-bits device address of the slave device, followed by the "read / write" flag (flag $R/\overline{W} = 0$);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device transmits the 8-bit AW87390G register address to which the first data byte will written;

The slave device asserts an acknowledgment (ACK) bit to confirm the register address is correct;

Master sends 8 bits of data to register which needs to be written;

The slave device asserts an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

If the master device needs to continue transmitting data, it does not need further to send the register address for AW87390G, within AW87390G each send confirmation bit(ACK) regret automatic accumulation register address then only need to repeat the sixth step and seven step:

The master device generates the STOP state to end the data transmission.

Figure 22 Writing Process (Data Transmission Direction Remains the Same)

Read Process

Reading process refers to the slave device reading data back to the master device. In this process, the direction of data transmission will change. Before and after the change, the master device sends START state and slave address twice, and sends the opposite "read/write" flag. In particular, AW87390G as the slave device, the transmission process carried out by following steps listed in Figure 23:

(1) Master device asserts a start condition;

(2) Master device transmits the 7 bits address of AW87390G, and followed by a "read / write" flag ($R/\overline{W} = 0$);

(3) The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

(4) The master device sends the 8bit address that the AW87390G register needs to read the data;

(5) The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;

(6) The master device restarts the data transfer process by continuously generating STOP state and START state or a separate Repeated START;

(7) Master sends 7-bits address of the slave device and followed by a read / write flag (flag $R/\overline{W}$ = 1) again;
(8) The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;
(9) The slave transmits 8 bits of data to register which needs to be read;
(10) The master device sends an acknowledgment bit (ACK) to confirm whether the data is sent successfully;
(11) AW87390G automatically increment register address once after the slave sent each acknowledge bit (ACK);
(12) The master device generates the STOP state to end the data transmission;

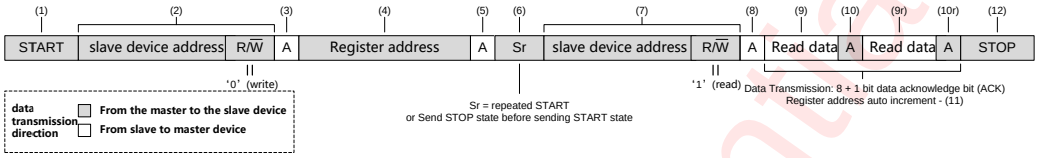
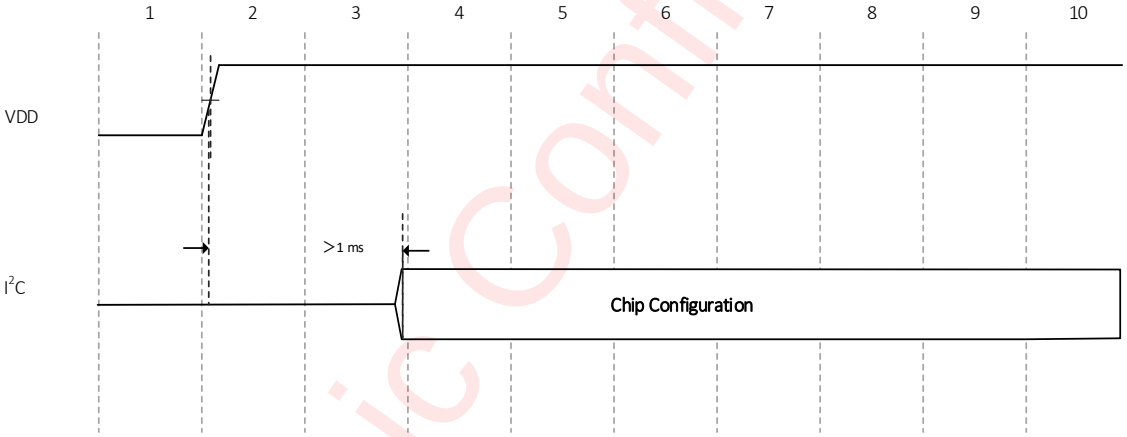


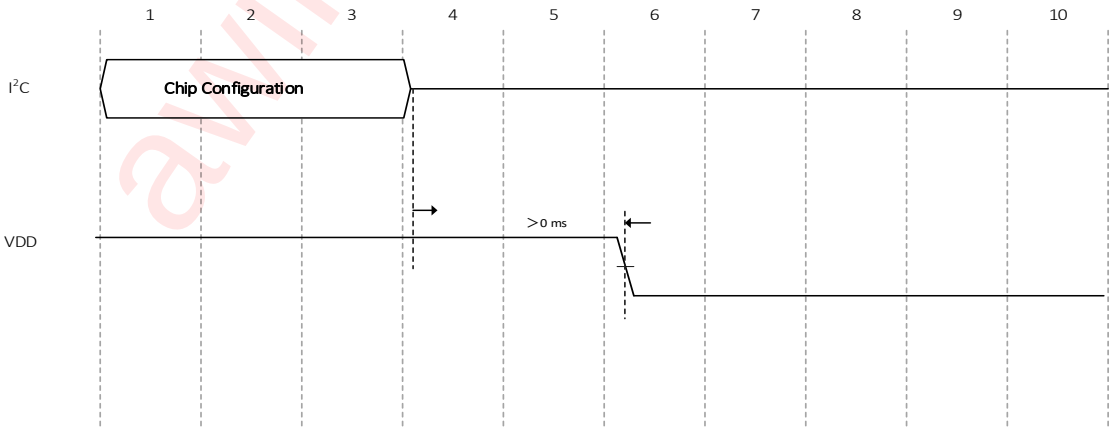
Figure 23 Reading Process (Data Transmission Direction Remains the Same)

Power Up and Power Down Sequence

Power up sequence considering I²C timing shows as below:



Power down sequence considering I²C timing shows as below:



Register List

Write AA to the 00 register of the AW87390G to reset the register

name	address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
Chip ID	0x00	IDCODE								0X76
SYSCTRL	0x01	-					EN_PA	EN_CP	EN_CCPA	0X06
MODECTRL	0x02	-			EN_ADP	EN_2X	EN_SPK(1)	-	EN_AB(2)	0X0C
CPOVP	0x03	-				CP_OVP(3)				0X08
CPP	0x04	-								0X05
Gain	0x05	-			Gain					0X0C
AGC3_Po	0x06	-				AGC3_Po				0X07
AGC3	0x07	AGC3_RT			AGC3_AT			AGC3FAST		0X4E
AGC2_Po	0x08	-				AGC2_Po				0X06
AGC2	0x09	-			AGC2_AT			AGC2FAST		0X08
AGC1	0x0A	-	AGC1THVTH				AGC1_AT		PD_AGC1	0X4A
ADPVTH	0x63	-				ADPVTH		-		0X05
AGC1MD	0x64	-				AGC1MD		-		0X28

(1) EN_SPK: enable speaker application
(2) EN_AB: enable class AB application
(3) CP_OVP: chargepump OVP voltage

Any register address which is more than 0x0A and all reserved bits are reserved for debugging and testing purposes. Changing their values may affect the normal function of the power amplifier; Reading them will get any possible values. AW87390G's I²C address is 10110A2A1, as shown in**Table 2** , in order to avoid conflict with other I²C devices address, you can pull up or pull-down AW87390G of AD2 and AD1 pins to set the value of A2 and A1, respectively. The following lists specific information about all visible registers, including default values and programmable ranges.

AD2/A2	AD1/A1	I²C address
0	0	0x58
0	1	0x59
1	0	0x5A
1	1	0x5B

Table 2 AW87390G Address Byte

CHIP ID* Register *(address: 0x00 Default:0x76)

I²C Bit	Name	R/W	Default	Description
7:0	IDCODE	RO	0x76	Chip ID will be returned after read.

SYSTEM CONTROL (SYSCTRL)* Register *(address: 0x01 Default:0x06)

I²C Bit	Name	R/W	Default	Description
7:3	--	--	00000	Reserved and Unused
2	EN_PA	R/W	1	Power Amplifier enable 0: Power Amplifier disable 1: Power Amplifier enable, the PA working mode depends on EN_AB

1	EN_CP	R/W	1	Chargepump Enable 0: Charge Pump disable, PVDD=0 1: Charge Pump enable, the CP working mode depends on EN_2X
0	PU_CPPA	R/W	0	CP and PA software power-up. If EN_PA=EN_CP=1, when change EN_CP from 1 to 0, only set PU_CPPA=0. 0: CP and PA software power-down 1: CP and PA software power-up

MODE CONTROL (MODECTRL)* Register *(address: 0x02 Default:0x0C)

I²C Bit	Name	R/W	Default	Description
7:5	--	--	000	Reserved and Unused
4	EN_ADP	R/W	0	ADP Function setting 0: disable(default) 1: enable
3	EN_2X	R/W	1	2X Charge Pump Mode enable 0: 1X Direct Through Mode enable 1: 2X Charge Pump Mode enable
2	EN_SPK	R/W	1	SPK Mode or RCV Mode enable 0: SPK Mode disable 1: SPK Mode enable
1	--	--	0	Reserved and Unused
0	EN_AB	R/W	0	Class AB enable, Class D disable 00: Class AB disable, Class D enable 01: Class AB enable, Class D disable

CHARGEPUMP OUTPUT VOLTAGE (CPOVP)* Register *(address: 0x03 Default:0x08)

I²C Bit	Name	R/W	Default	Description
7:4	--	--	0000	Reserved and Unused
3:0	CP_OVP	R/W	1000	Setting Chargepump OVP Voltage 1011~1111: reserved. If set, turns to default. 0000: 6.0V 0001: 6.25V 0010: 6.5V 0011: 6.75V 0100: 7V 0101: 7.25V 0110: 7.5V 0111: 7.75V 1000: 8V 1001: 8.25V 1010: 8.5V 1011~1111: reserved.

CHAREPUMP PARAMETER (CPP)* Register *(address: 0x04 Default:0x05)

I²C Bit	Name	R/W	Default	Description
7:0	--	--	00000101	Reserved and Unused

GAIN CONTROL (*Gain*) Register *(address: 0x05 Default:0x0C)*

For EN_SPK=1 :

I²C Bit	Name	R/W	Default	Description
7:5	--	--	000	Reserved and Unused
4:0	Gain	R/W	01100	Power Amplifier Gain setting

				00000~00111, 10011~11111: reserved. If set, turns to default.
				01000: 12dB
				01001: 13.5dB
				01010: 15dB
				01011: 16.5dB
				01100: 18dB
				01101: 19.5dB
				01110: 21dB
				01111: 22.5dB
				10000: 24dB
				10001: 25.5dB
				10010: 27dB

For EN_SPK=0，EN_AB=0:

I²C Bit	Name	R/W	Default	Description
7:5	--	--	000	Reserved and Unused
4:0	Gain	R/W	01100	Power Amplifier Gain setting
				11011~11111: reserved. If set, turns to default. 00000~10010: reserved. If set, turns to default.
				10011: 0dB
				10100: 1.5dB
				10101: 3dB
				10110: 4.5dB
				10111: 6dB
				11000: 7.5dB
				11001: 9dB
				11010: 10.5dB

For EN_SPK=0，EN_AB=1:

I²C Bit	Name	R/W	Default	Description
7:5	--	--	000	Reserved and Unused
4:0	Gain	R/W	01100	Power Amplifier Gain setting
				11001: 0dB
				11010: 1.5dB
				11011: 3dB
				11100: 4.5dB
				11101: 6dB
				11110: 7.5dB
				11111: 9dB
				00000~11000: reserved. If set, turns to default.

AGC3 OUTPUT POWER (AGC3_Po)* Register *(address: 0x06 Default:0x07)

For EN_SPK=1 :

I²C Bit	Name	R/W	Default	Description
7:4	--	--	0000	Reserved and Unused
3:0	AGC3_PO	R/W	0111	AGC3 Output Power setting
				0000~0011: reserved. If set, turns to default.
				0100: 0.5W@8Ω;0.67W@6Ω;
				0101: 0.6W@8Ω;0.80W@6Ω;
				0110: 0.7W@8Ω;0.93W@6Ω;
				0111: 0.8W@8Ω;1.06W@6Ω;
				1000: 0.9W@8Ω;1.20W@6Ω;

				1001: 1.0W@8Ω;1.33W@6Ω;
				1010: 1.1W@8Ω;1.47W@6Ω;
				1011: 1.2W@8Ω;1.60W@6Ω;
				1100: 1.3W@8Ω;1.73W@6Ω;
				1101: 1.4W@8Ω;1.87W@6Ω;
				1110: 1.5W@8Ω;2.00W@6Ω;
				1111: AGC3 OFF

For EN_SPK=0:

I²C Bit	Name	R/W	Default	Description
7:4	--	--	0000	Reserved and Unused
3:0	AGC3_PO	R/W	0111	AGC3 Output Power setting
				0000~1110: reserved. If set, turns to default.
				1111: AGC3 OFF

AGC3 PARAMETER (AGC3)* Register *(address: 0x07 Default:0x4E)

I²C Bit	Name	R/W	Default	Description
7:5	AGC3_RT	R/W	010	AGC3 Release Time setting
				000: 5.12ms/dB
				001: 10.24ms/dB
				010: 20.48ms/dB
				011: 41ms/dB
				100: 82ms/dB
				101: 164ms/dB
				110: 328ms/dB
				111: 656ms/dB
4:2	AGC3_AT	R/W	011	AGC3 Attack Time setting
				000: 1.28ms/dB
				001: 2.56ms/dB
				010: 10.24ms/dB
				011: 41ms/dB
				100: 82ms/dB
				101: 164ms/dB
				110: 328ms/dB
				111: 656ms/dB
1:0	AGC3FAST	R/W	10	AGC3 First Attack Time setting
				00: 10.24ms/dB
				01: 20.48ms/dB
				10: 41ms/dB
				11: 82ms/dB

AGC2 OUTPUT POWER(AGC2_Po)* Register *(address: 0x08 Default:0x06)

For EN_SPK=1:

I²C Bit	Name	R/W	Default	Description
7:4	--	--	0000	Reserved and Unused
3:0	AGC2_PO	R/W	0110	AGC2 Output Power setting
				1010~1111: reserved. If set, turns to default.
				0000: 0.4W@8Ω;0.53W@6Ω;
				0001: 0.6W@8Ω;0.80W@6Ω;
				0010: 0.8W@8Ω;1.06W@6Ω;
				0011: 1.0W@8Ω;1.33W@6Ω;
				0100: 1.2W@8Ω;1.60W@6Ω;
				0101: 1.4W@8Ω;1.87W@6Ω;
				0110: 1.6W@8Ω;2.17W@6Ω;
				0111: 1.8W@8Ω;2.40W@6Ω;

				1000: 2.0W@8Ω;2.67W@6Ω;
				1001: AGC2 OFF

For EN_SPK=0:

I²C Bit	Name	R/W	Default	Description
7:4	--	--	0000	Reserved and Unused
3:0	AGC2_PO	R/W	0110	AGC2 Output Power setting
				0000~1000, 1010~1111: reserved. If set, turns to default.
				1001: AGC2 OFF

AGC2 PARAMETER (AGC2)* Register *(address: 0x09 Default:0x08)

I²C Bit	Name	R/W	Default	Description
7:5	--	--	000	Reserved and Unused
4:2	AGC2_AT	R/W	010	AGC2 Attack Time setting
				000: 0.16ms/dB
				001: 0.32ms/dB
				010: 0.64ms/dB
				011: 2.56ms/dB
				100: 10.24ms/dB
				101: 41ms/dB
				110: 82ms/dB
				111: 164ms/dB
1:0	AGC2FAST	R/W	00	AGC2 First Attack Time setting
				00: 0.16ms/dB
				01: 0.64ms/dB
				10: 2.56ms/dB
				11: 10.24ms/dB

AGC1 PARAMETER (AGC1)* Register *(address: 0x0A Default:0x4A)

I²C Bit	Name	R/W	Default	Description
7:3	--	--	01001	Reserved and Unused
2:1	AGC1AT	R/W	01	AGC2 First Attack Time setting
				00: 0.04ms/dB
				01: 0.08ms/dB
				10: 0.16ms/dB
				11: 0.32ms/dB
0	PD_AGC1	R/W	0	AGC1 function power-down
				0: AGC1 function power-up
				1: AGC1 function power-down

ADPVTH PARAMETER (ADPVTH)* Register *(address: 0x63 Default:0x05)

I²C Bit	Name	R/W	Default	Description
7:4	--	--	0000	Reserved and Unused
3:2	ADPVTH	R/W	01	ADP Po Detect setting
				00:0.1W
				01:0.2W
				10:0.3W
1:0	-	-	01	Reserved and Unused

AGC1MD PARAMETER (AGC1MD)* Register *(address: 0x64 Default:0x28)

I²C Bit	Name	R/W	Default	Description
7:4	--	--	0010	Reserved and Unused
3:2	AGC1MD	R/W	10	AGC1 Working Mode setting 00:RAMP_GEN 01:THGEN 10:RAMP_GEN and THGEN 11:reserved，if set，turns to default
1:0	-	-	00	Reserved and Unused

APPLICATION INFORMATION

Capacitor Selection

The output capacitor of chargepump is usually within the range 0.1μF~47μF, It needs to use Class II type (EIA) multilayer ceramic capacitors (MLCC). Its internal dielectric is ferroelectric material (typically BaTiO3), a high the dielectric constant in order to achieve smaller size, but at the same Class II type (EIA) multilayer ceramic capacitors has poor temperature stability and voltage stability as compared to the Class I type (EIA) capacitance. Capacitor is selected based on the requirements of temperature stability and voltage stability, considering the capacitance material, capacitor voltage, and capacitor size and capacitance values.

a) temperature stability

Class II capacitance have different temperature stability in different materials, usually choose X5R type in order to ensure enough temperature stability, and X7R type capacitance has better properties, the price is relatively more expensive. X5R capacitance change within ±15% in temperature range of 55°C to 85°C, X7R capacitance change within ±15% in temperature range of -55°C~125°C. The output capacitance of the AW87390G's chargepump recommends X5R ceramic capacitors.

b) Voltage Stability

Class II type capacitor has poor voltage stability ——Capacitance values falling fast along with the DC bias voltage applied across the capacitor increasing. The rate of decline is related to capacitance material, capacitors rated voltage, capacitance volume. Take for TDK C series X5R for example, its pressure voltage value is 16V or 25V, the package size is 0805, 1206 or 0603, the capacitance value is 10μF. The capacitor's voltage stability of different types of capacitor is as shown below:

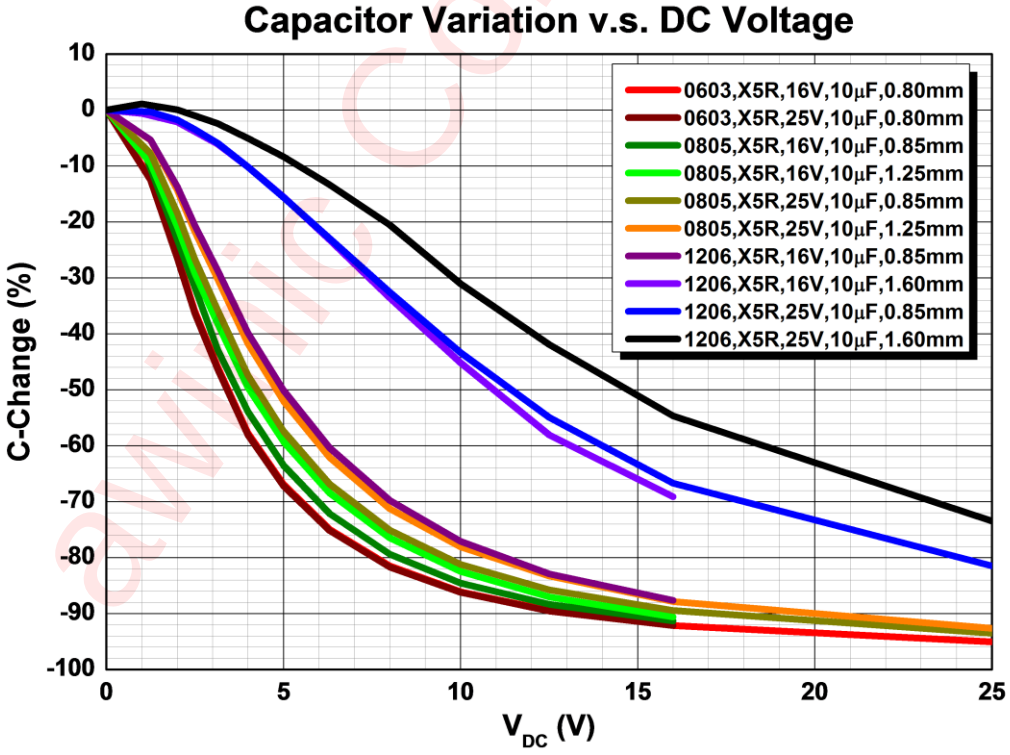


Figure 24 Different Types of Capacitive Voltage Stability

Among them, the space remaining value of different types of capacitors at VDC = 8.0V as shown below：

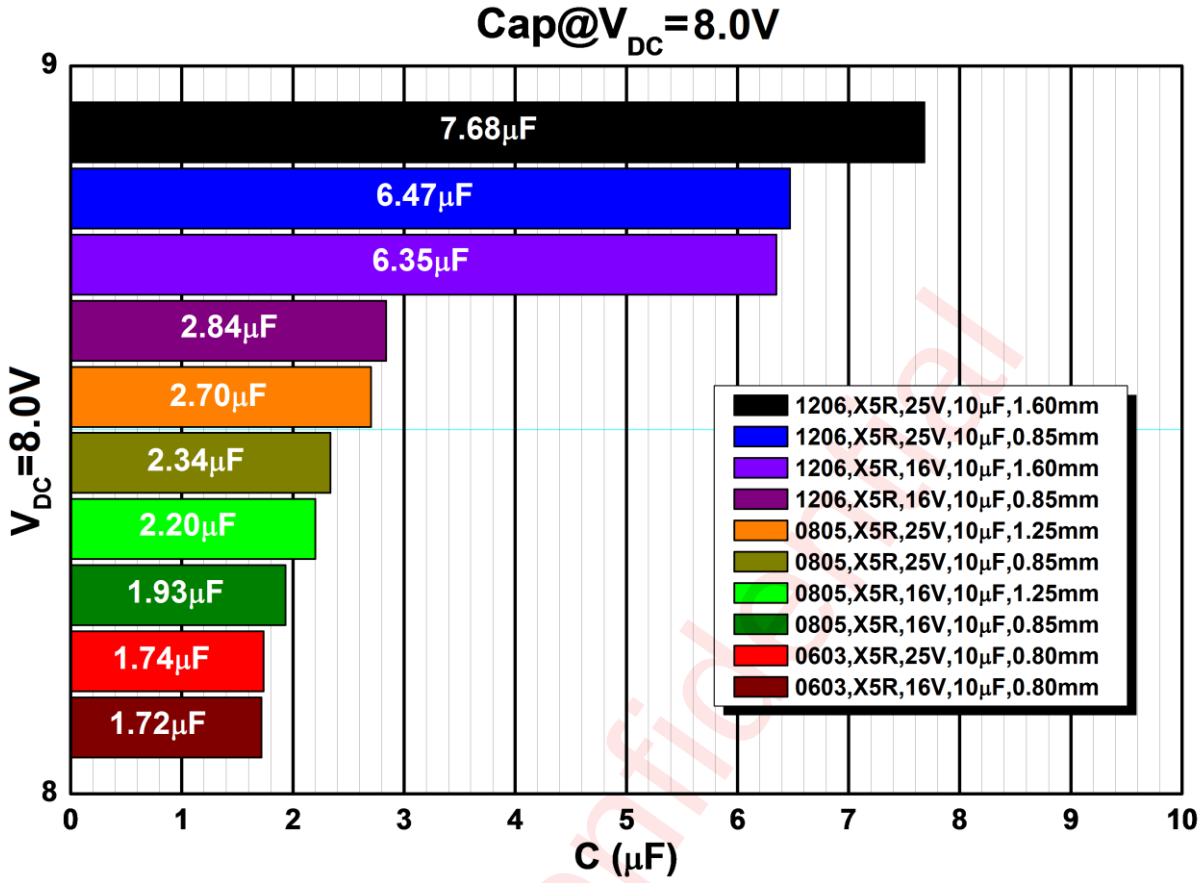


Figure 25 The Space Remaining Value of Different Types of Capacitors at V_{DC} = 8.0V

It can be found that the rate of capacitance capacity value descent becomes slow along with "large capacitor size, capacitance pressure voltage rise". The larger the package size, the better voltage stability. the higher the height, the better voltage stability with the same length and width of the capacitance. Voltage stability of smaller package size (0603) capacitor change affected by the pressure value is very small.

In AW87390G typical applications, it is necessary to ensure the output value of the PVDD capacitor ≥3μF when PVDD=8.0V.

Input Capacitor-C_{in}（input high-pass cutoff frequency）

The input capacitors and input resistors form a high-pass filter to filter out the DC component of the input signal. The -3dB frequency points of the high pass filter is shown below：

$$f_H(-3dB)=\frac{1}{2*\pi*R_{intotal}*C_{in}}(Hz)$$

The selection of a smaller Cin capacitor in the application helps to filter out 217Hz noise, which comes from the input coupling, and the smaller capacitor is advantageous to reduce the pop-click noise when the power amplifier turn on.Better matching of the input capacitors improves performance of the circuit and also helps to suppress pop-click noise. A capacitor value deviation of 10% or better capacitance is recommended.

Take typical application as an example, the input high-pass cutoff frequency is calculated as below:

$$f_H(-3dB) = \frac{1}{2 * \pi * R_{intotal} * C_{in}} = \frac{1}{2 * \pi * 9k\Omega * 68nF}(Hz) = 260Hz$$

Class D-type speaker & receiver 2-in-1 application (Gain=1), the input high pass frequency is as follows:

$$f_H(-3dB) = \frac{1}{2 * \pi * R_{intotal} * C_{in}} = \frac{1}{2 * \pi * 48k\Omega * 100nF}(Hz) = 34Hz$$

Class AB-type speaker & receiver 2-in-1 (Gain=1), the input high pass frequency is as follows:

$$f_H(-3dB) = \frac{1}{2 * \pi * R_{intotal} * C_{in}} = \frac{1}{2 * \pi * 72k\Omega * 100nF}(Hz) = 22Hz$$

Supply Decoupling Capacitor（C_S）

A good decoupling capacitor can improve the efficiency and the best performance of the power amplifier. At the same time, in order to get good high frequency transient performance, the ESR value of the capacitor should be as small as possible. In AW87390G applications, low ESR (equivalent-series-resistance) X7R or X5R ceramic capacitors are recommended. Generally, 10μF ceramic capacitors are used to bypass the VDD to the ground, and the decoupling capacitor should be placed as close to the VDD chip as possible in the layout. If you want to filter out low-frequency noise better, you need to add a 10μF or greater decoupling capacitor depending on your application. Meanwhile, a 33pF~0.1μF ceramic capacitor is placed on the pin of the power supply to filter the high frequency interference on the power supply. The capacitor should be placed as close as possible to the D4 pin and inductor.

Chargepump Flying capacitor (C_F)

The Flying capacitor is used to transfer energy between the power supply and the chargepump load, the value of the Flying capacitor directly affects the load regulation rate and the output drive capability of the chargepump. If flying capacitor is too small, it will affect the chargepump load adjustment rate and output drive capability, thereby affecting the power output of the amplifier, and the larger the Flying capacitor, the better the load regulation ability, driving ability is also stronger. Recommended use of 4.7μF, low ESR X7R, X5R ceramic capacitors, it is recommended to use more than 10V pressure capacitor.

Output capacitance of chargepump（C_{OUT}）

The output capacitance of the chargepump and the ESR directly affect the ripple of the output, thus affecting the performance of the power amplifier. Recommended use of 10μF, low ESR X7R or X5R ceramic capacitors, you need to select the 25V voltage resistance capacitor.

Output beads, capacitors, TVS

Using EEE technology, in the class K mode, the AW87390G can also meet the FCC CLASS B specification requirements. It is recommended to Use ferrite chip beads and capacitors if device near the EMI sensitive circuits, there are long leads from amplifier to speaker, placed as close as possible to the output pin.

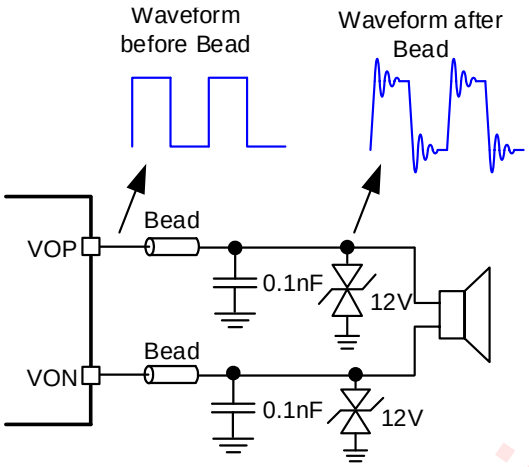


Figure 26 Ferrite Chip Bead and Capacitor

Amplifier output is a square wave signal. The voltage across the capacitor will be much larger than the PVDD voltage after increasing the bead capacitor. It suggested the use of rated voltage above 16V capacitor. At the same time a square wave signal at the output capacitor switching current form, the static power consumption increases, so the output capacitance should not be too much which is recommended 0.1nF ceramic capacitor rated voltage of 16V. If you want to get better EMI suppression performance, can use 1nF, rated voltage 16V capacitor, but quiescent current will increase.

Power amplifier output PWM signals of high voltage to PVDD voltage, voltage to 8.5 V, will produce some ringing after bead capacitor, resulting in higher peak voltage. Recommended choose the operating voltage of 12V TVS.

PCB AND DEVICE LAYOUT CONSIDERATION

EXTERNAL COMPONENTS PLACEMENT

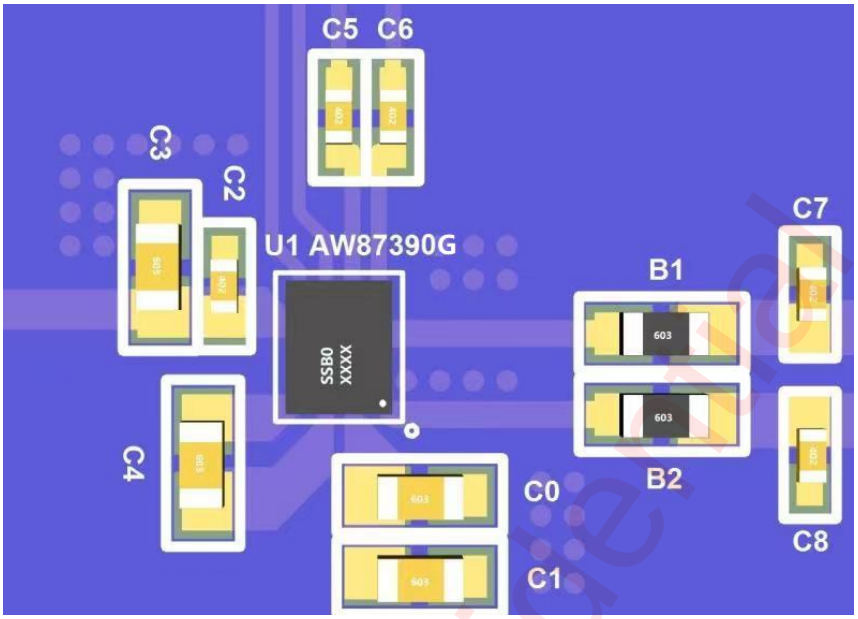


Figure 27 AW87390G External Components Placement

LAYOUT CONSIDERATIONS

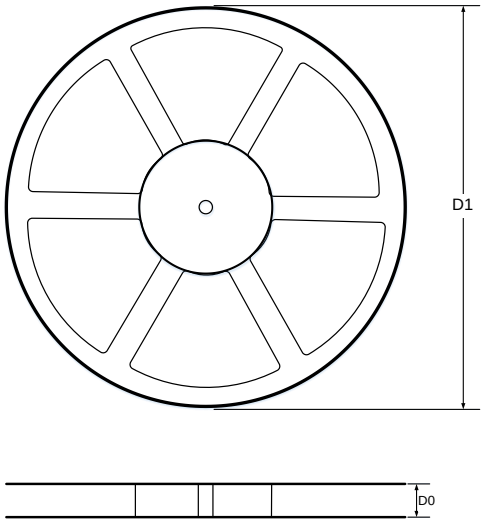
This device is a power amplifier chip. To obtain the optimal performance, PCB layout should be considered carefully.

In order to obtain excellent performance of AW87390G, PCB layout must be carefully considered. The design consideration should follow the following principles:

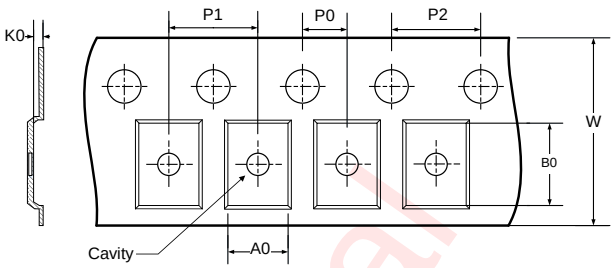
1. In AW87390G peripheral device layout, you first need to guarantee the chargepump output capacitance close to PVDD pin and the VDD capacitance close to VDD pin.
2. Try to provide a separate short and thick power line to AW87390G, the copper width is recommended to be larger than 0.75mm. The decoupling capacitors should be placed as close as possible to boost power supply pin.
3. The input capacitors should be close to AW87390G INN and INP input pin, the input line should be parallel to suppress noise coupling.
4. The beads and capacitor should be placed near to AW87390G VON and VOP pin. The output line from AW87390G to speaker should be as short and thick as possible. The width is recommended to be larger than 0.5mm.

TAPE & REEL DESCRIPTION

REEL DIMENSIONS

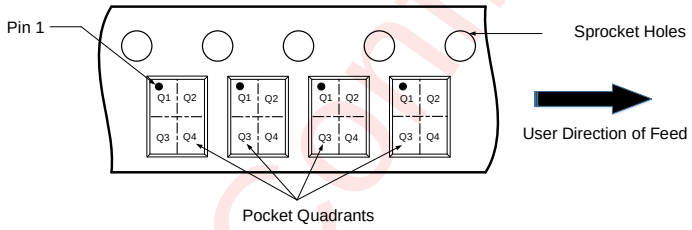


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

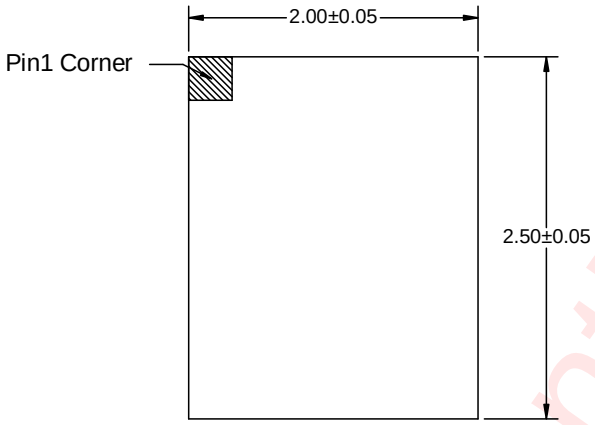


Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

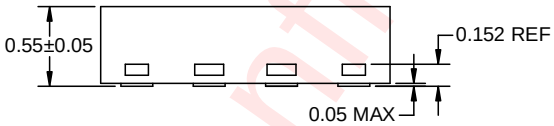
All Dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330.00	12.40	2.20	2.67	0.83	2.00	8.00	4.00	12.00	Q1

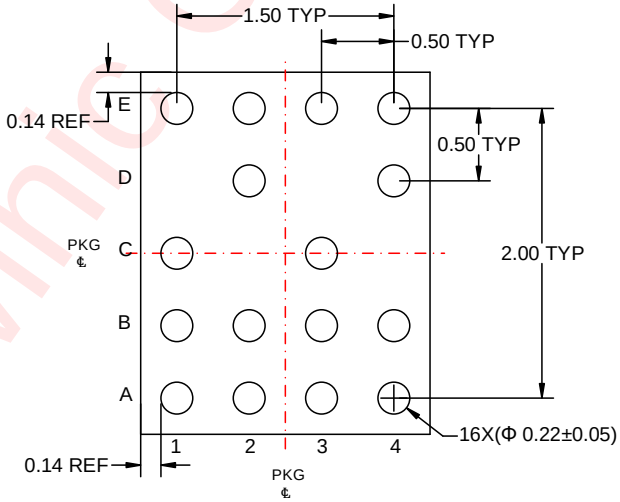
PACKAGE DESCRIPTION



Top View



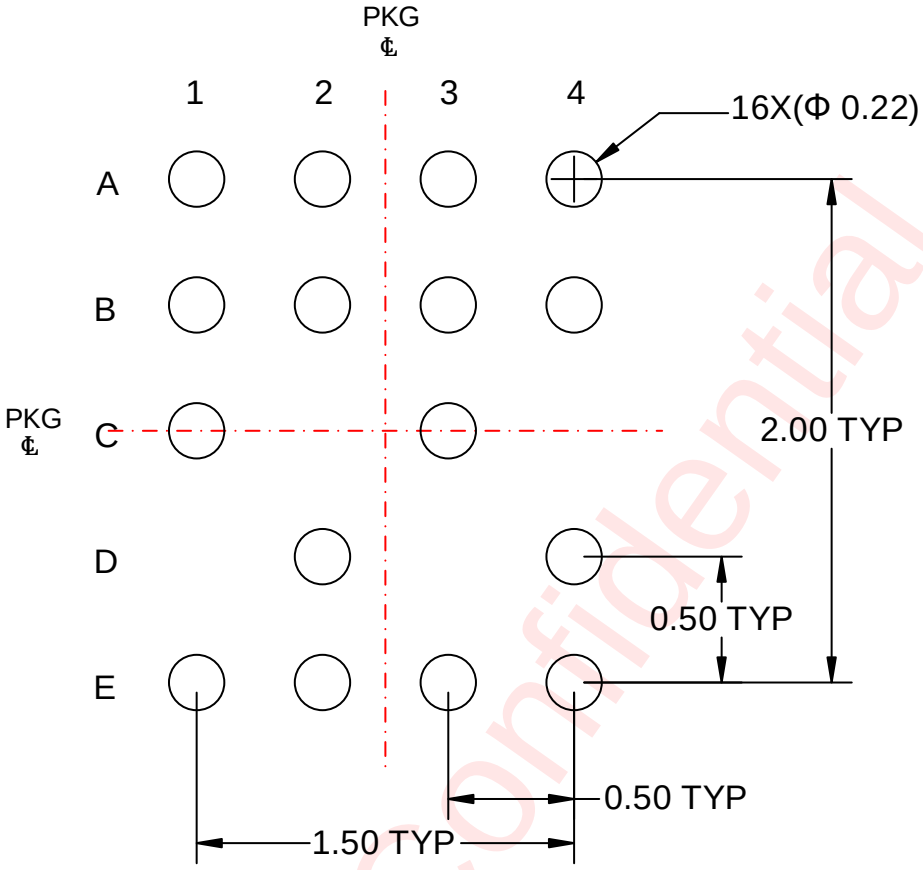
Side View

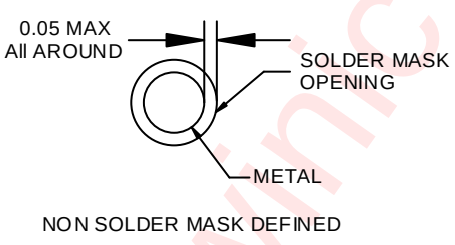


Bottom View

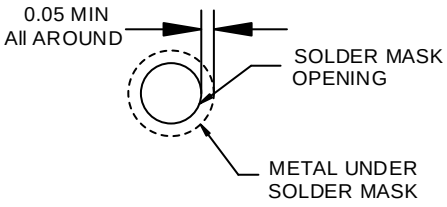
Unit: mm

LAND PATTERN





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

VERSION INFORMATION

Version	Date	Description
V1.0	2023-02-28	AW87390GFCR datasheet V1.0

DISCLAIMER

Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.