Overvoltage Protection Load Switch with Bidirectional Blocking and Surge Protection

Features

- Integrated ultra-low Ron switch: typical 20mΩ
- Bidirectional blocking between IN and OUT
- Pin-selectable overvoltage protection threshold V_{OVP}=13V/17V
- Fast overvoltage protection turn-off response: typical 50ns
- Surge protection compliant with IEC61000−4−5 up to ±100V
- Wide input voltage range from 3.1V to 28V
- 3A DC nominal and 5A maximum current capability
- Autonomous mode and slave mode operation
- WLCSP 2.105mm X1.565mm-20B, 0.4mm pitch package

Applications

- Smartphones and Tablets
- Portable Devices
- Charging Ports

General Description

The AW32101 is a high input voltage, large current and ultra-low Ron load switch with bidirectional blocking.

The AW32101 is turned off very fast once the input voltage exceeds the OVP threshold to prevent damage to the protected downstream devices. The IN pin is capable of withstanding fault voltages up to 28VDC. The AW32101 provides a selectable OVP threshold of 13V or 17V typical.

The AW32101 features reverse−blocking of output voltage. When the switch is open, the IN and OUT ports are completely cut off, preventing leakage current from IN to OUT and from OUT to IN.

The AW32101 OVP load switch features surge protection, an internal clamp circuit protects the device from surge voltages up to +/-100V. It also features over-temperature protection that prevents itself from thermal damaging.

Autonomous mode allows manual operation. Slave mode operation allows the device be controlled by a system controller.

Typical Application Circuit

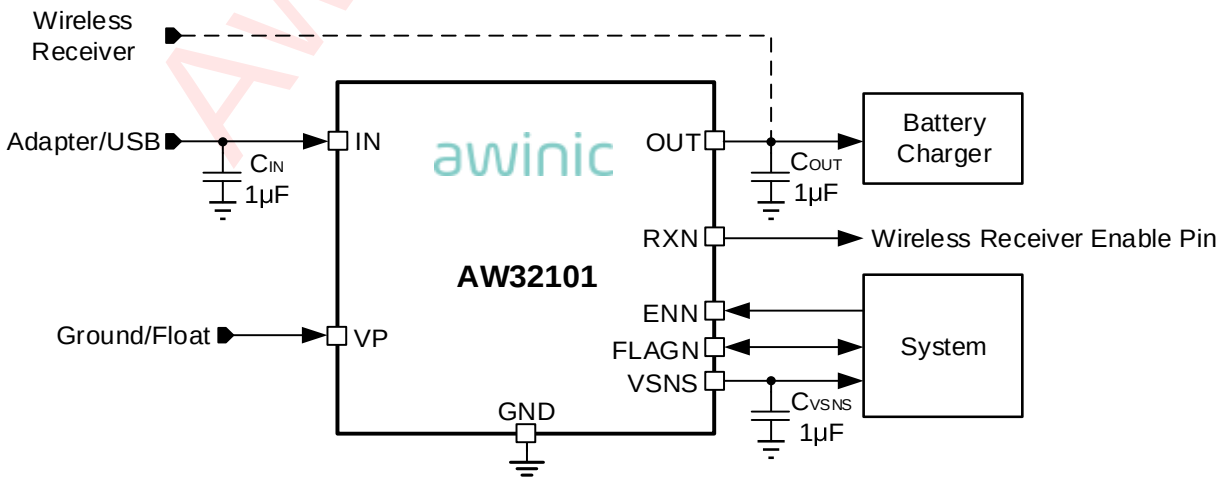
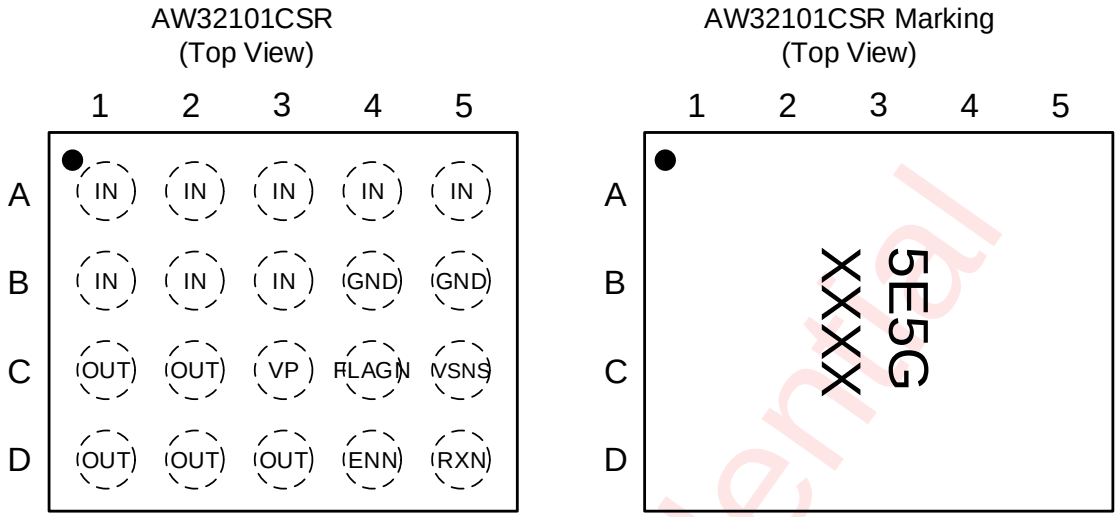


Figure 1 Typical Application Circuit of AW32101

Pin Configuration And Top Mark



5E5G – AW32101CSR
XXXX– Production Tracing Code

Figure 2 Pin Configuration And Top Mark

Pin Definition

PIN	NAME	DESCRIPTION
A1,A2,A3,A4,A5	IN	Switch input and power supply.
B1,B2,B3		
B4,B5	GND	Device ground.
C1,C2,D1,D2,D3	OUT	Switch output.
C3	VP	Overvoltage protection threshold setting and VSNS clamp voltage. VP=Low, setting V_{OVP}=17V and V_{CLAMP_VSNS}=18V; VP=High or floating, setting V_{OVP}=13V and V_{CLAMP_VSNS}=14V. The VP is connected to the 1.8V LDO output via an internal 120kΩ resistor.
C4	FLAGN	OTG enable input, or V_{IN} validation flag output. In autonomous mode OTG application, pull FLAGN logic low to enter OTG mode and turn on switch, toggle high to turn off switch. The FLAGN is open drain output and connected to the 1.8V LDO output via an internal 120kΩ resistor.
C5	VSNS	Sensing V_{IN} with output clamp capability.
D4	ENN	Mode selection and switch control input. Keep ENN logic Low or connect to GND, select autonomous mode. Once pulling ENN to logic High, select slave mode or exit from autonomous mode to slave mode. In slave mode, toggle ENN to open or close switch. The ENN is pull down to GND via an internal 530kΩ resistor.
D5	RXN	Active Low logic enable. The RXN is open drain output and connected to the 1.8V LDO output via an internal 60kΩ resistor.

Functional Block Diagram

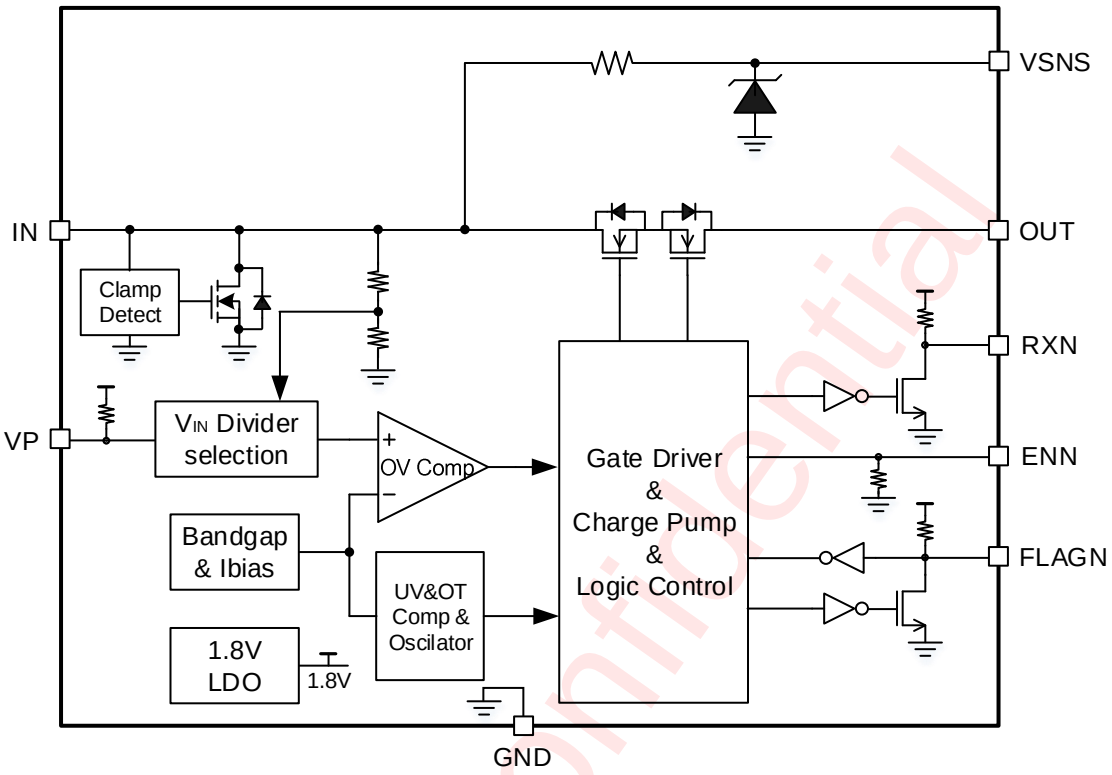


Figure 3 Functional Block Diagram

Typical Application Circuits

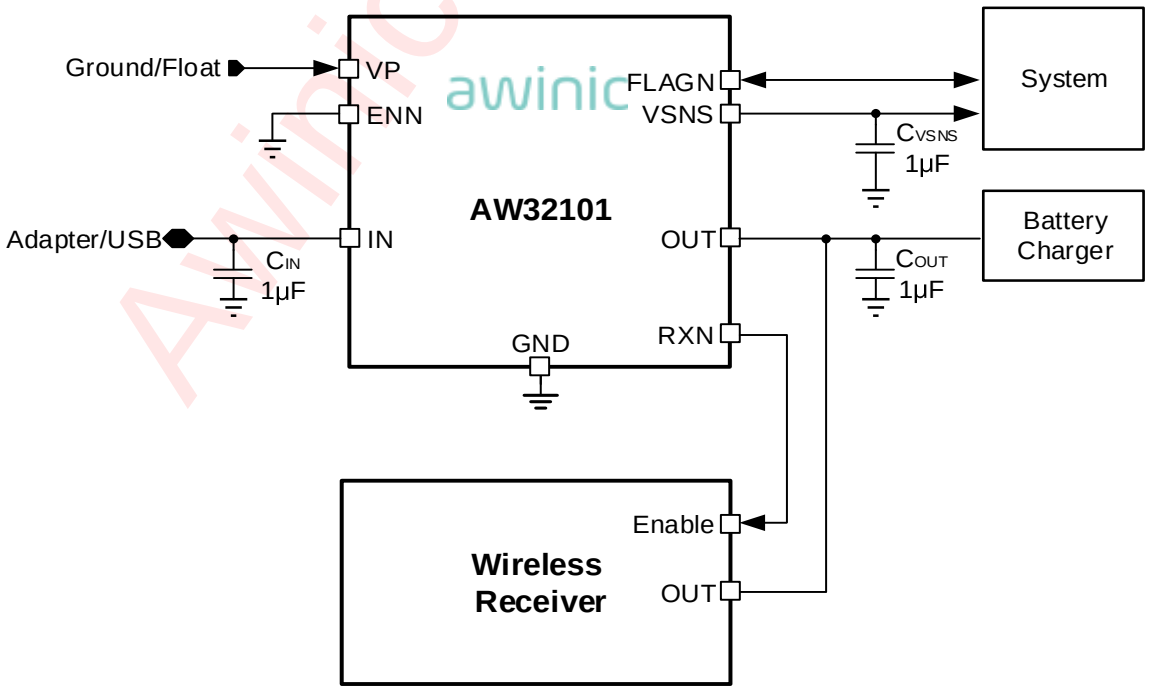


Figure 4 Dual Input Device (Autonomous Mode)

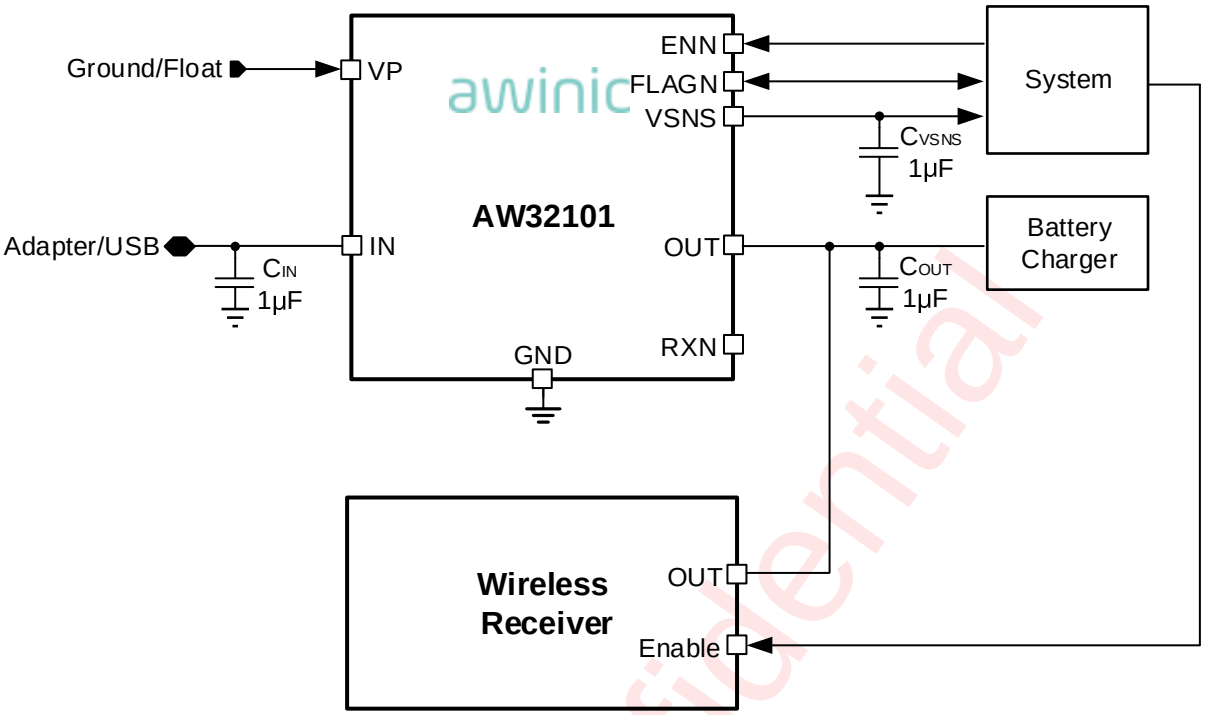


Figure 5 Dual Input Device (Slave mode)

Notice for Typical Application Circuits:

1. Both scheme are just examples, not only apply to Wireless Recevier.
2. The AW32101 has an internal 120kΩ pull up resistor on VP, so it can be left floating and pulled up to internal 1.8V LDO output voltage.
3. FLANG and RXN are pulled up to 1.8V via 120kΩ and 60kΩ respectively.
4. Connecting ENN to GND, the device is set autonomous mode. If ENN is connected to the system digital I/O port and toggled, the device works as a slaver of the system, what is so-called slave mode.
5. V_{IN} is sensed through the VSNS port, which can help the system make decision. C_{VSNS} is not necessary for the device.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW32101CSR	-40°C～85°C	WLCSP 2.105mmX1.565 mm-20B	5E5G	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS	RANGE
Input voltage range V_{IN}	-0.3V to 28V
Output voltage range V_{OUT}	-0.3V to 20V
Output voltage range V_{VSNS}	-0.3V to 20V
Input/Output DC voltage(ENN, VP, RXN, FLAGN)	-0.3V to 6V
Continuous current of switch IN-OUT(NOTE2)	5A
Peak switch current on IN and OUT pin(10ms) (NOTE2)	8A
Continuous current of switch OUT-IN(NOTE2)	5A
Junction-to-ambient thermal resistance θ_{JA}	55°C/W
Maximum operating junction temperature T_{JMAX}	150°C
Operating free-air temperature range	-40°C to 85°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD	
Human Body Model (All pins, per ANSI/ESDA/JEDEC JS-001)	±2kV
Charged Device Model (All pins, per JESD22-C101)	±1kV
Latch-Up	
Test condition: JEDEC78	±200mA
Surge	
Test condition: IEC61000-4-5 test with 2Ω equivalent series resistance.	±100V

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: *Limited by thermal design.*

Electrical Characteristics

T_A = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V_{IN}=5V, C_{IN}=1μF, C_{OUT}=1μF, C_{VSNS}=1μF, T_A = 25°C.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input operating supply voltage		3.1		28	V
V_{CLAMP_IN}	IN input clamp voltage	I_{IN}=10mA, T_A=+25°C	30			V
V_{OUT}	Output operating supply voltage		3.1		20	V
V_{LK_IN}	OUT float voltage	ENN=High, V_{IN}=4.5V to 28V, OUT no load			0.4	V
V_{LK_OUT}	IN float voltage	ENN=High, V_{OUT}=4.5V to 16V, IN no load			0.4	V
I_{Q_IN}	Input quiescent current, standby state	ENN=High, VP float, V_{IN}=5.0V		200		μA
I_{DD_IN}	Input operating current	ENN=Low, VP float, V_{IN}=5.0V, OUT no load		240		μA
I_{Q_OUT}	Input quiescent current, standby state	ENN=High, VP and FLAGN float, V_{OUT}=5.0V		138		μA
I_{DD_OUT}	Input operating current	ENN=Low, VP float, V_{OUT}=5.0V, FLAGN=Low, IN no load		210		μA
$R_{ON(IN-OUT)}$	Switch ON resistance from IN to OUT	T_A=25℃, ENN=Low, I_{OUT}=0.5A		20	31	mΩ
I_{OUT}, I_{OTG}	Continuous output current		0	3.0		A
Protection						
V_{UVLO_IN}	IN UVLO trip level	V_{IN} rising	2.83	2.93	3.03	V
		Hysteresis		0.1		V
V_{UVLO_OUT}	OUT UVLO trip level	V_{OUT} rising	2.80	2.90	3.00	V
		Hysteresis		0.1		V
V_{OVP}	V_{IN} OVP threshold	VP to ground, V_{IN} rising	16	17	18	V
		VP to ground, Hysteresis		0.4		V
		VP left floating V_{IN} rising	12	13	14	V
		VP left floating, Hysteresis		0.34		V
V_{CLAMP_VSNS}	VSNS pin clamping voltage	VP to ground, I_{VSNS}=0	16.0	18.0	20.0	V
		VP left floating, I_{VSNS}=0	12.0	14.0	16.0	V
V_{DROP_VSNS}	Sense pin voltage drop when loaded	I_{VSNS}=10mA		102		mV
R_{DIS_IN}	IN discharge resistance	ENN=Low, V_{IN}=V_{OUT}=5V		470		Ω
R_{DIS_OUT}	OUT discharge resistance	ENN=Low, V_{IN}=V_{OUT}=5V		470		Ω

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
T_{SD}	Thermal shutdown	Enter the shutdown state		140		℃
T_{SD_HYS}	Thermal shutdown hysteresis			20		℃
Digital Characteristics						
V_{IL}	Digital Input low level				0.5	V
V_{IH}	Digital Input high level		1.2			V
V_{OL}	Digital output low level	Isink=2mA			0.2	V
V_{OH}	Digital output high level	Output logic high, no load	1.65	1.8		V
R_{FLAGN}	FLAGN pull-up resistance	FLAGN logic high pull-up	100	120	140	kΩ
R_{RXN}	RXN pull-up resistance	RXN logic high pull-up	50	60	70	kΩ
R_{VP}	VP pull-up resistance	VP logic high pull-up	100	120	140	kΩ
I_{LEAK_ENN}	ENN Input leakage current	ENN=5V, V_{IN}=5V			12	μA
R_{ENN}	ENN pull-down resistance	ENN=5V, V_{IN}=5V		530		kΩ
T_{DEB_IL}	Input logic debounce time	ENN/FLAGN toggle		40		μs
Timing Characteristics						
T_{DEB_IN}	IN input debounce time	V_{UVLO_IN}<V_{IN}<V_{OVP}, ENN=Low, time delay between V_{IN} rising and RXN rising		50		ms
T_{DEB_OUT}	OUT input debounce time	Debounce time of OUT		40		μs
T_{SSTART}	Switch soft-start time	Switch on, IN or OUT output rising time, no load			0.5	ms
T_{DIS}	Supply discharge time	Discharge time of IN and OUT on discharge state		50		ms
T_{INIT}	Power up and initialization time	The time from V_{IN} or V_{OUT} crossing V_{UVLO} to ENN active		100		μs
T_{SS_VSNS}	Soft startup time of V_{VSNS}	V_{IN}=5V, V_{VSNS} from 0V to 4.5V, no load			500	μs
T_{OFF_DLY}	Disable the switch delay time	Time delay from ENN, FLAGN or UVLO trigger to disable the load switch		15		μs
T_{OVP_DLY}	The delay time between V_{IN} over voltage and switch turn-off	V_{IN}>V_{OVP} to V_{OUT} stop rising		50		ns
Capacitance						
C_{IN}	Input capacitance			1	10	μF
C_{VSNS}	VSNS output capacitance			1		μF
C_{OTG}	OTG hot swap capacitance			1	200	μF
C_{OUT}	Output capacitance			1		μF

Typical Characteristics

Ambient temperature is 25°C, V_{IN}/V_{OUT}=5V, C_{IN} = C_{OUT}= C_{VSNS}=1μF, VP floating(V_{OVP}=13V), unless otherwise noted.

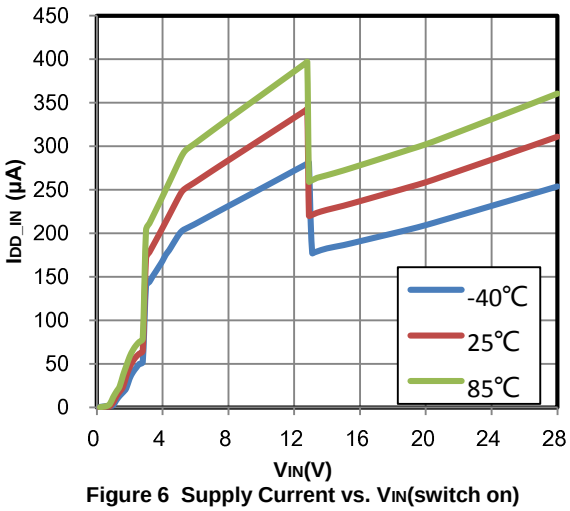


Figure 6 Supply Current vs. V_{IN}(switch on)

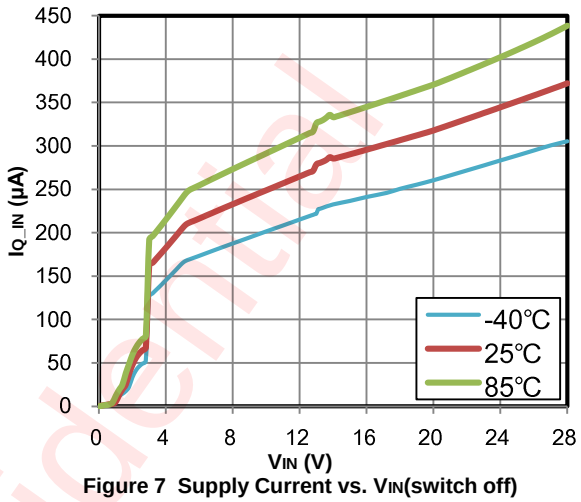


Figure 7 Supply Current vs. V_{IN}(switch off)

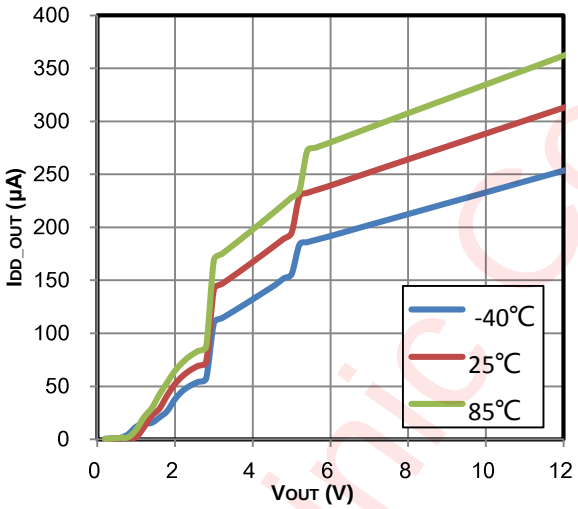


Figure 8 Supply Current vs. V_{OUT}(switch on)

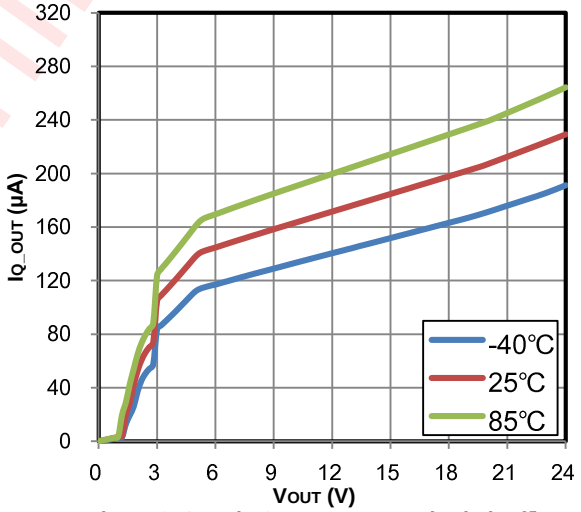


Figure 9 Supply Current vs. V_{OUT}(switch off)

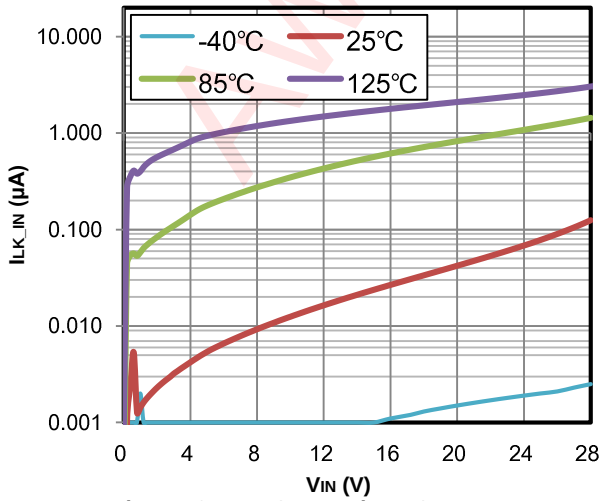


Figure 10 IN to OUT Leakage Current vs. V_{IN}

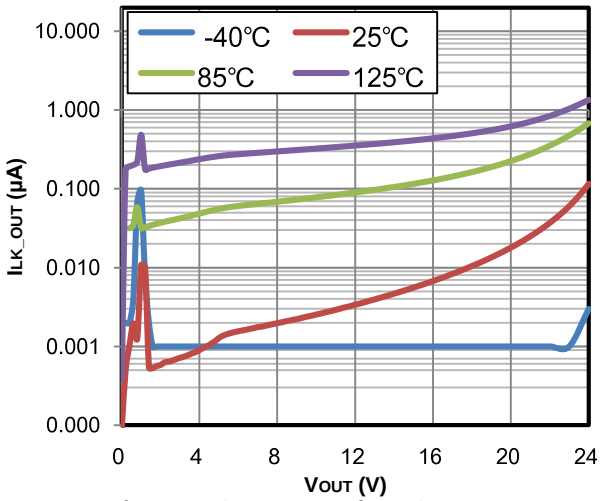


Figure 11 OUT to IN Leakage Current vs. V_{OUT}

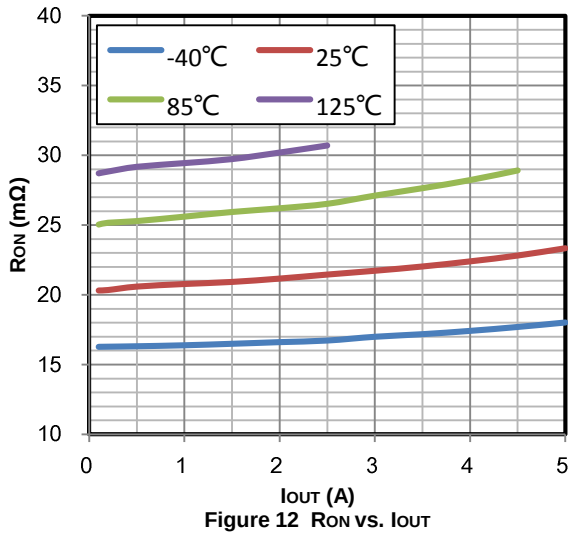


Figure 12 RON vs. IOUT

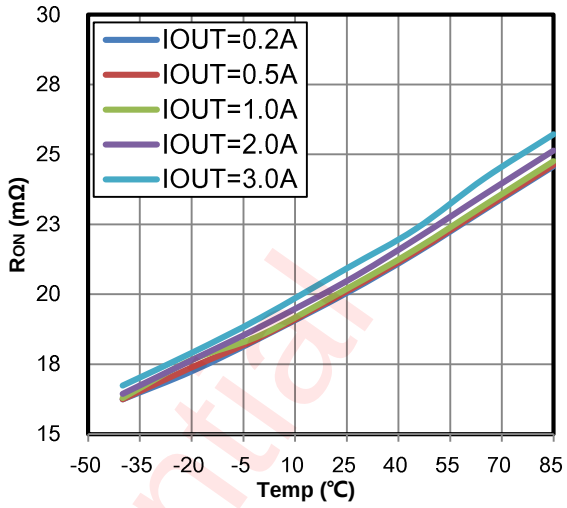


Figure 13 RON vs. Temperature

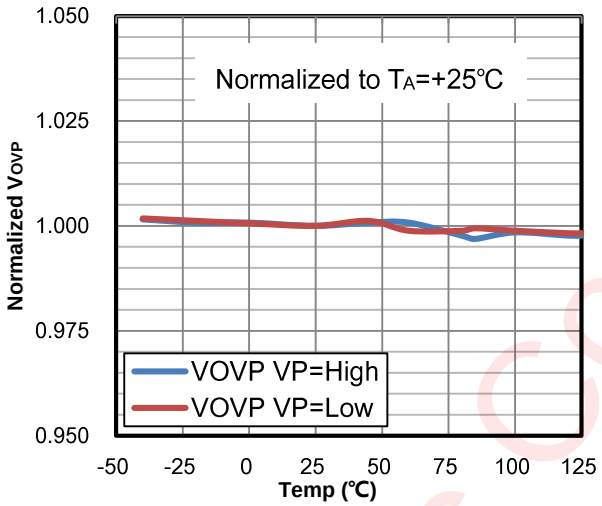


Figure 14 OVP Voltage vs. Temperature

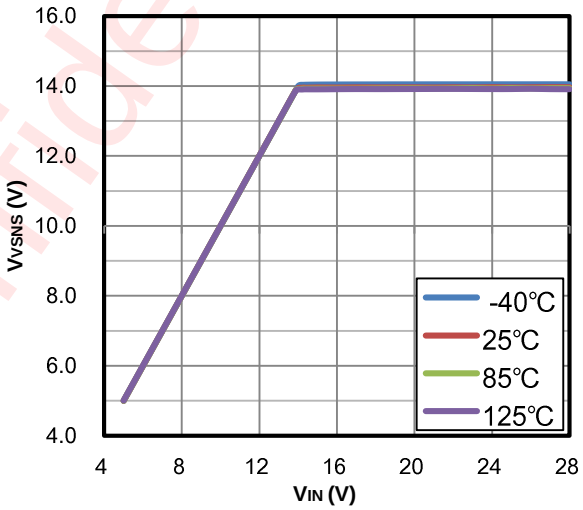


Figure 15 VSNS Clamp Voltage vs. VIN

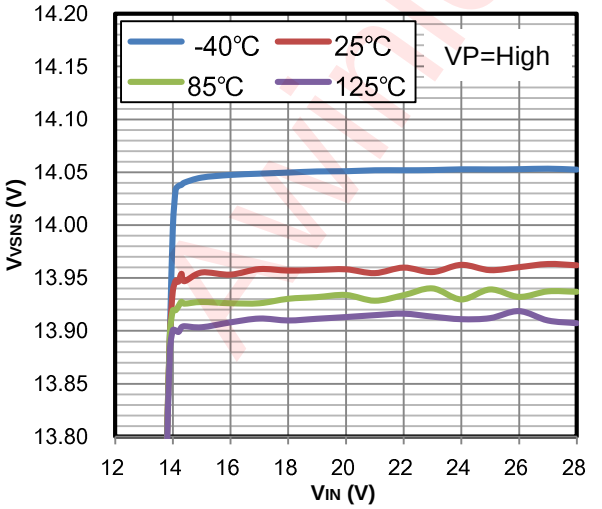


Figure 16 VSNS Clamp Voltage vs. VIN

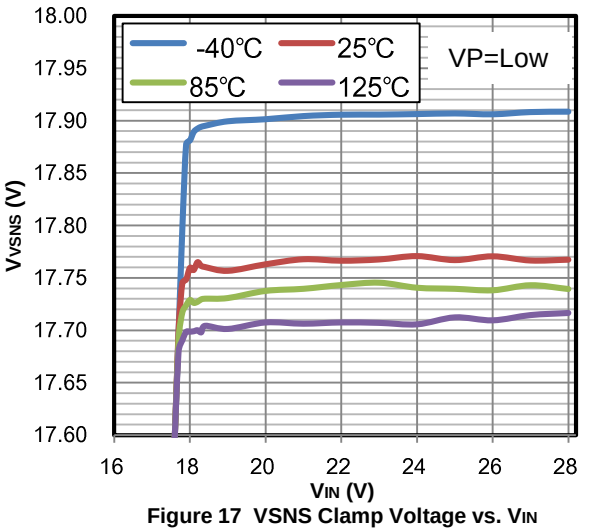


Figure 17 VSNS Clamp Voltage vs. VIN

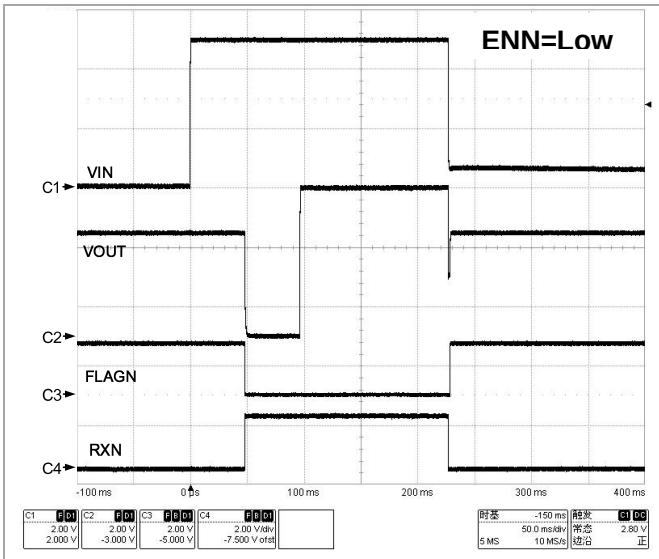


Figure 18 VIN=5V Insert and Remove

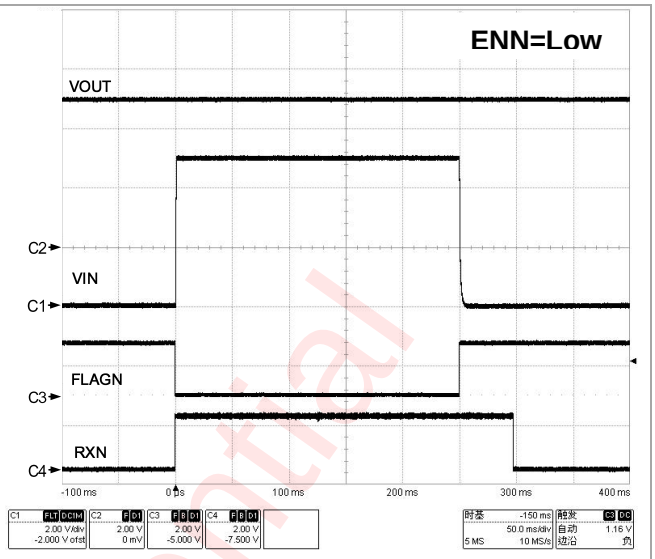


Figure 19 VOUT=5V Switch Turn On-Off by FLAGN

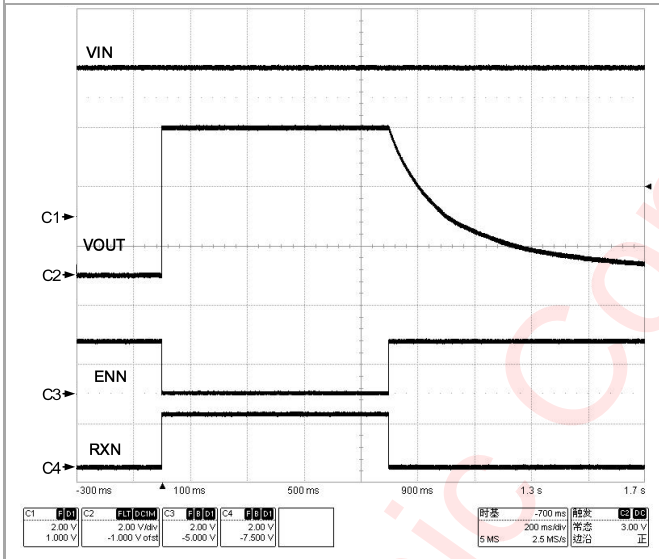


Figure 20 VIN=5V Switch Turn On-Off by ENN

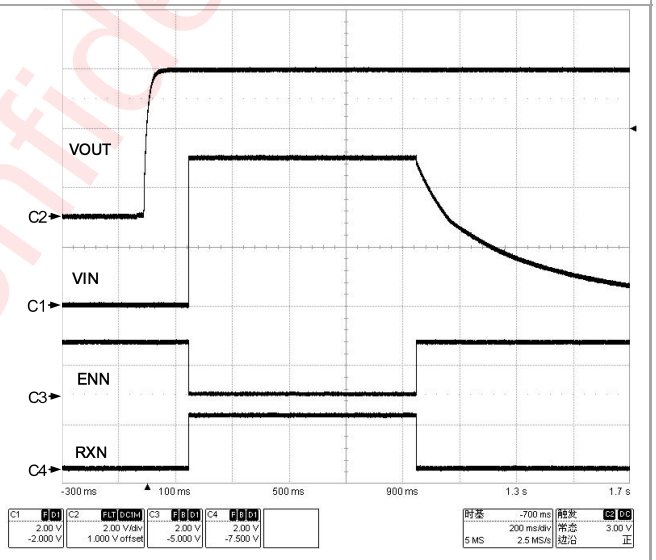


Figure 21 VOUT=5V Switch Turn On-Off by ENN

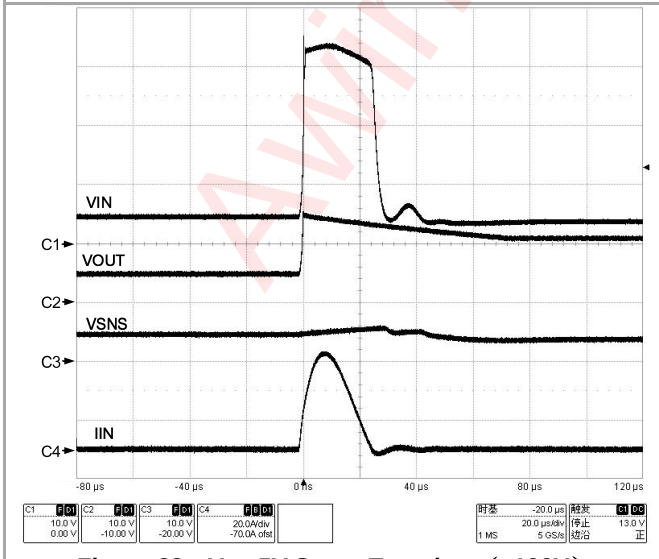


Figure 22 VIN=5V Surge Transient（+100V）

Detailed Functional Description

When a wirelessly charging mobile phone suddenly encounters an USB charging access, dual power sources wired-and will be happened, which may cause permanent damage to the power supply sources. Because of two internal integrated back-to-back switches and the break before make mechanism, AW32101 can achieve effective bidirectional blocking between input and output.

In the dual-source power supply system, the AW32101 is inserted on one of the supply paths, and the aforementioned dual power wired-and problems can be effectively solved under the control logic. The AW32101 switch consists of two back-to-back series MOSFETs with on-resistance as low as 20mΩ, and can transmit up to 5A DC current. Its IN port features overvoltage protection and surge protection to provide effective protection for the rear system. In addition, the system can also detect V_{IN} in real time through VSNS.

Surge Protection

The AW32101 integrates a clamp circuit to suppress input surge voltage. For surge voltages between V_{OVP} and V_{CLAMP_IN}, the switch will be turned off but the clamp circuit will not work. For surge voltages greater than V_{CLAMP_IN}, the internal clamp circuit will detect surge voltage level and discharge the surge energy to ground. The device can suppress surge voltages up to 100V.

Over-Voltage Protection

If the IN input voltage exceeds the OVP rising trip level, the switch will be turned off in about 50ns. The switch will remain off until V_{IN} falls below the OVP falling trip level. The voltage at the IN port is to be sensed by the device and outputs to VSNS port, which will have to be clamped to protect the downstream components. The overvoltage trip level and the VSNS clamp voltage are selectable by the VP port. Connecting VP to ground, selects the V_{OVP} of typical 17V and the maximum V_{CLAMP_VSNS} of 20V. With the VP left floating,. selects the V_{OVP} of typical 13V and the maximum V_{CLAMP_VSNS} of 16V.

Bidirectional Blocking

The AW32101 integrates two back-to-back MOSFETs, when the load switch between IN and OUT is open, IN and OUT is bidirectional blocking, thereby blocking any reverse current.

Break Before Make Mechanism

A break before make mechanism will ensure the safety of the dual input sources. In autonomous mode, the IN 50ms debounce period is followed by at least 50ms break-before-make delay that allows time to discharging OUT until the V_{OUT} invalid. The device keeps the switch open and the wireless receiver disable through pulling RXN high during the break-before-make delay.

A 10mA (or 470Ω) pull-down at OUT is active during the break-before-make delay. The break-before-make delay is inactive when the IN is removed since UVLO is active and the load-switch is not powered. So the RXN goes low, and the wireless receiver will automatically be enabled again.

Mode Configure

In application, the AW32101 can operate autonomously or be used as a slaver. At the end of the initialization of the device, if ENN is detected to be low, it is recognized as working in autonomous mode, otherwise in slave mode. Once ENN is pulled high in autonomous mode, it will transfer to slave mode.

Autonomous Mode

In autonomous mode, the device has a higher priority than the wireless receiver to power the output. The device is automatically turned on and off according to the presence of IN input. If V_{IN} is valid (V_{IN}>V_{UVLO_IN}), after the debounce time of 50ms, RXN is pulled high by the internal resistor, which disables the wireless charging path. And then, the device discharges to IN and OUT ports until the 50ms full and V_{OUT} invalid on the AUTO DISCH state. The switch is closed to provide the voltage from IN to OUT; Otherwise the switch is open and the discharge state is continued.

In OTG applications, if V_{OUT} is valid (V_{OUT} >V_{UVLO_OUT}), after the debounce time of 40μs and the initialization process, FLAGN will be released and pulled up through an internal pull-up resistor. So the system can close the switch by forcing FLAGN low which will provide the voltage from OUT to IN, and output RXN high. The system releases the FLAGN, and the internal pull-up resistor again pulls the FLAGN up and the RXN returns to low after the 50ms discharge time. If the RXN is connected to a wireless receiver, RXN=High can be used to turn off the wireless receiver.

Slave Mode

In slave mode, the switch's state is controlled via the ENN pin, RXN and FLAGN work as output pins. In the case of V_{IN} keep valid in the debounce time of 50ms, the switch can be turned on through pulling low ENN, and the RXN goes high. The turn off process is opposite. In slave mode, the priority of the input power source between dual input devices is assigned by the system.

Concurrent OTG Mode

The wireless receiver can provide a regulated 5V to OUT, not only for supplying the system but also to support OTG operation. This is referred to as concurrent OTG mode.

FLAGN Logic

The FLAGN pin is a bidirectional input/output pin that controls the transition to and from OTG modes while in autonomous mode. When IN is disconnected (floating) and a valid OUT voltage is detected, the FLAGN pin serves as an output signal and FLAGN is logic high. Subsequently, the load switch can be activated by toggling the FLAGN to low, which triggers OTG mode by transitioning into the ON-state.

Softstart

Both the switch between IN and OUT and the MOSFET between IN and VSNS turn on about 0.5ms soft start time which is designed to limit the peak inrush currents.

VSNS Short Protection

When VSNS is short to ground, the IN to VSNS current is limited to prevent the device burning.

Thermal Shutdown Protection

When the junction temperature rises to approximately 140℃, thermal shutdown(TSD) protection turns off the load switch for cooling the device until the junction temperature falls to approximately 120℃.

If the current mode is autonomous mode, once TSD happened, the device will enter TSD AUTO state, and if it is in temperature, the device will exit to AUTO READY state. Similarly in slave mode, the device enters TSD SLAVE state and exits to SLAVE READY state.

Flow Diagram

The operation of the state machine of the AW32101 exhibits in the below flow diagram. In combination with the label definitions as listed in the table afterwards, it provides more details on the above described behavior. The state machine can only operate if the AW32101 is sufficiently supplied from either IN or OUT. In both cases, the voltage will have to be above the under voltage lockout threshold. In case the internal circuit is not or no longer supplied, the state machine is in the OFF state.

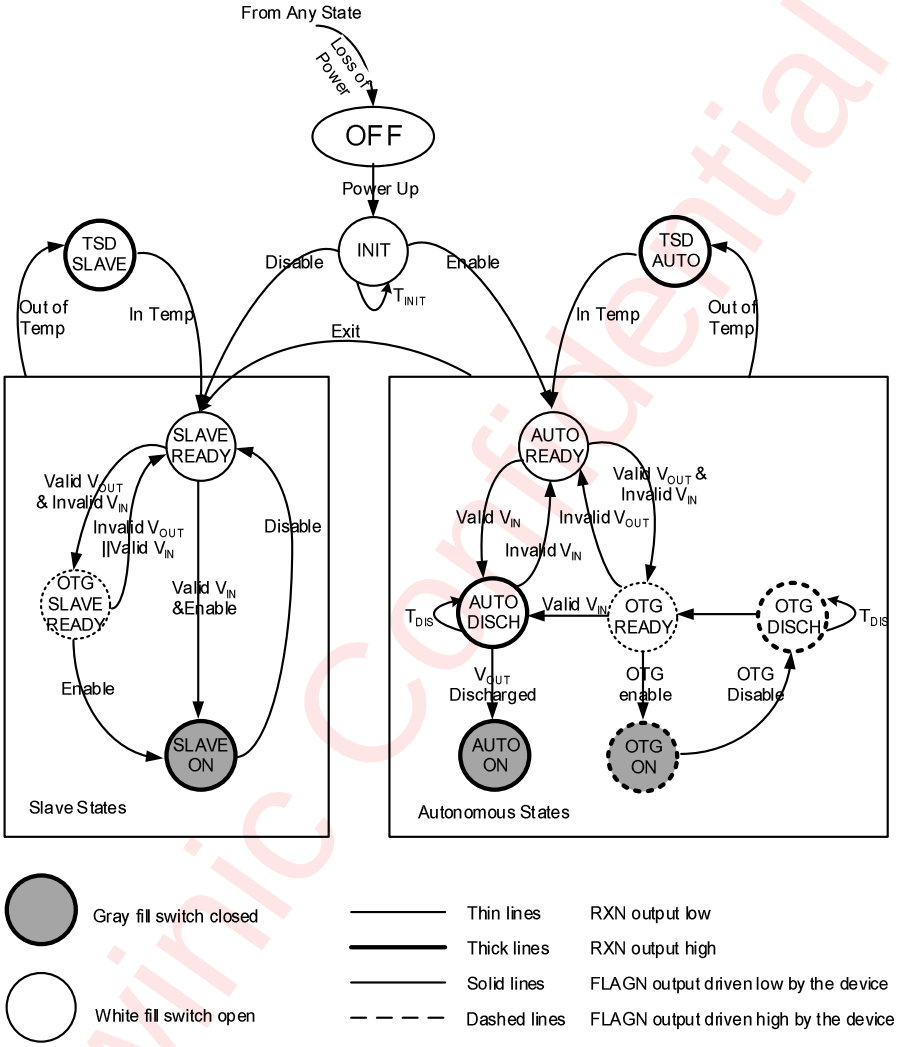


Figure 23 Logic State Diagram

Table1 The Description of The Labels

Label	Description
Loss of Power	Both IN and OUT below the UVLO threshold.
Power Up	IN and/or OUT above the UVLO threshold.
Enable	ENN pin is low, debounced for T_{DEB_IL}.
Disable	ENN pin is high, debounced for T_{DEB_IL}.
Valid V_{IN}	IN above the V_{UVLO_IN} debounced for T_{DEB_IN}, the voltage at OUT is a don't care.
Invalid V_{IN}	Inverted signal of 'Valid V_{IN}'.
Valid V_{OUT}	OUT above the V_{UVLO_OUT} debounced for T_{DEB_OUT}.

Invalid V_{OUT}	Inverted signal of 'Valid V_{OUT}'.
V_{OUT} Discharged	OUT below the UVLO threshold, no debounce.
OTG Enable	FLAGN pin is forced low by the system while FLAGN was pulled high by the device, debounced for T_{DEB_IL}.
OTG Disable	FLAGN pin is released by the system and FLAGN is pulled up by the device, debounced for T_{DEB_IL}.
Out of Temp	Die temperature exceeds thermal shutdown threshold.
In Temp	Die temperature falls below thermal shutdown threshold.
T_{INIT}	Power up and initialization duration.
T_{DIS}	Discharge duration.
OFF	Device is not powered.
INIT	ENN don't care, switch open, RXN and FLAGN low. Startup of the device including analog and digital blocks and reading of OTP fuses. Duration T_{IINIT}.
TSD SLAVE	ENN don't care, switch open, RXN high, FLAGN low. Entered from any slave state at out of Temp condition.
TSD AUTO	ENN low, switch open, RXN high, FLAGN low. Entered from any autonomous state at out of Temp condition.
AUTO READY	ENN low, switch open, RXN and FLAGN low. Autonomous mode is detected during INIT state. Can also be entered from AUTO DISCH (if invalid V_{IN}).
AUTO DISCH	ENN low, switch open, RXN high, FLAGN low. A 'Valid V_{IN}' is detected, discharge load activated on OUT and IN, minimum duration T_{DIS}. The 'V_{OUT} Discharged' condition must be met before exiting for AUTO ON (verification done for safety reasons).
AUTO ON	ENN low, switch closed, RXN high, FLAGN low. Under normal conditions this state is only exited upon loss of power (eg. USB removal).
OTG READY	ENN low, switch open, RXN low, FLAGN high. A 'Valid V_{OUT}' is detected.
OTG ON	ENN low, switch closed, RXN high, FLAGN forced low by the system. An 'OTG enable' condition is detected.
OTG DISCH	ENN low, switch open, RXN high, FLAGN high (no longer forced low by the system). Discharge load activated on OUT and IN duration T_{DIS}, exited for OTG READY.
SLAVE READY	ENN high, switch open, RXN and FLAGN low. Slave mode is detected during INIT state. Can also be entered from certain autonomous states if ENN toggled high after the INIT state.
OTG SLAVE READY	ENN high, switch open, RXN low, FLAGN high. A 'Valid V_{OUT}' is detected.
SLAVE ON	ENN low, switch closed, RXN high, FLAGN low.
Exit	While in one of the autonomous states, ENN is toggled to high, which leads to an Exit to a slave state. The device will enter the SLAVE READY state at first.

Timing Diagrams

Figure 24 through Figure 29 show autonomous mode and slave mode timing diagrams.

In autonomous mode (ENN=Low), a T_{DEB_IN}=50ms debounce time followed by 50ms discharge time, and T_{SSTART} soft-start delay are applied when the V_{IN}>V_{UVLO_IN} is detected. If the V_{OUT}>V_{UVLO_OUT} is detected, V_{OUT} is valid and a debounce delay of T_{DEB_OUT}=40μs begins.

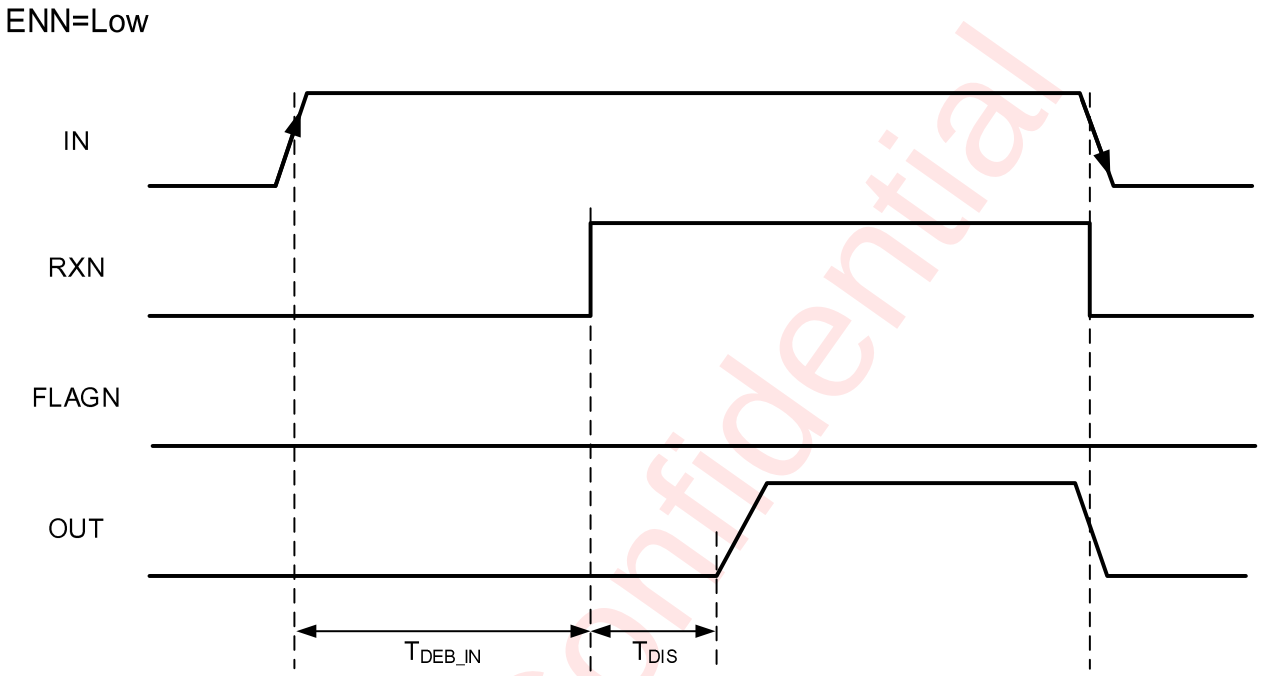


Figure 24 Autonomous Mode Timing: Insertion and Removal of IN Input

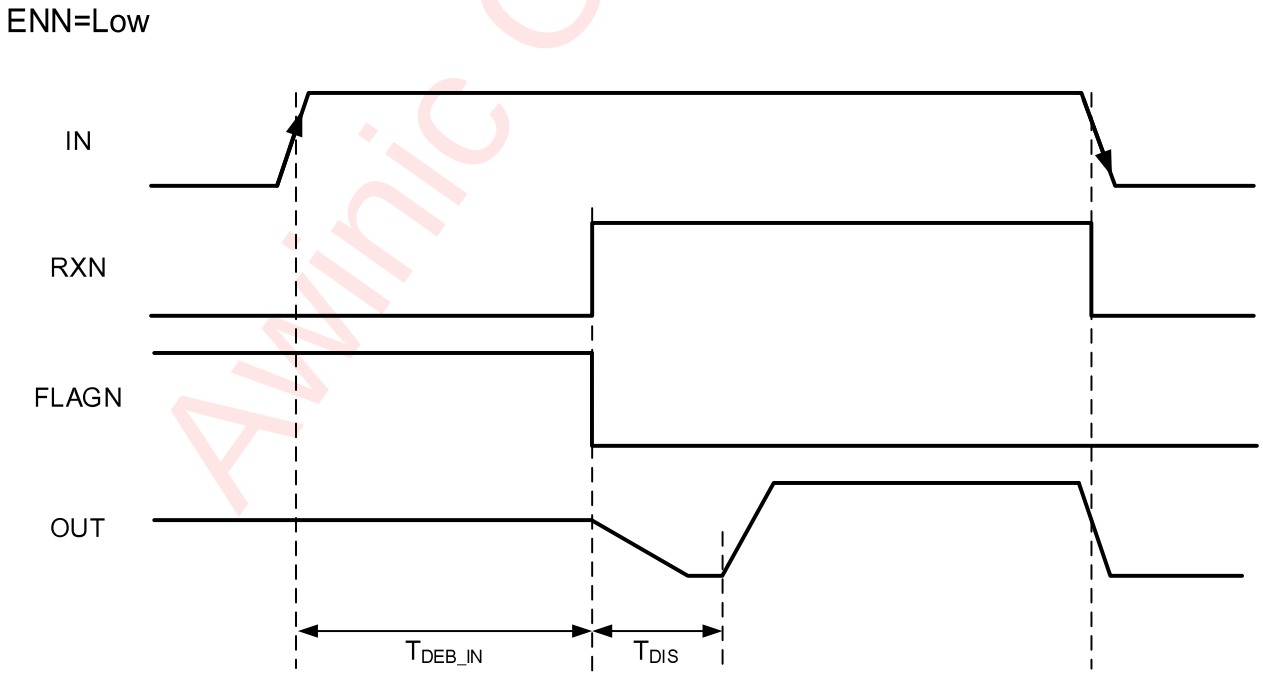


Figure 25 Autonomous Mode Timing: Dual Input with IN Insertion and Removal

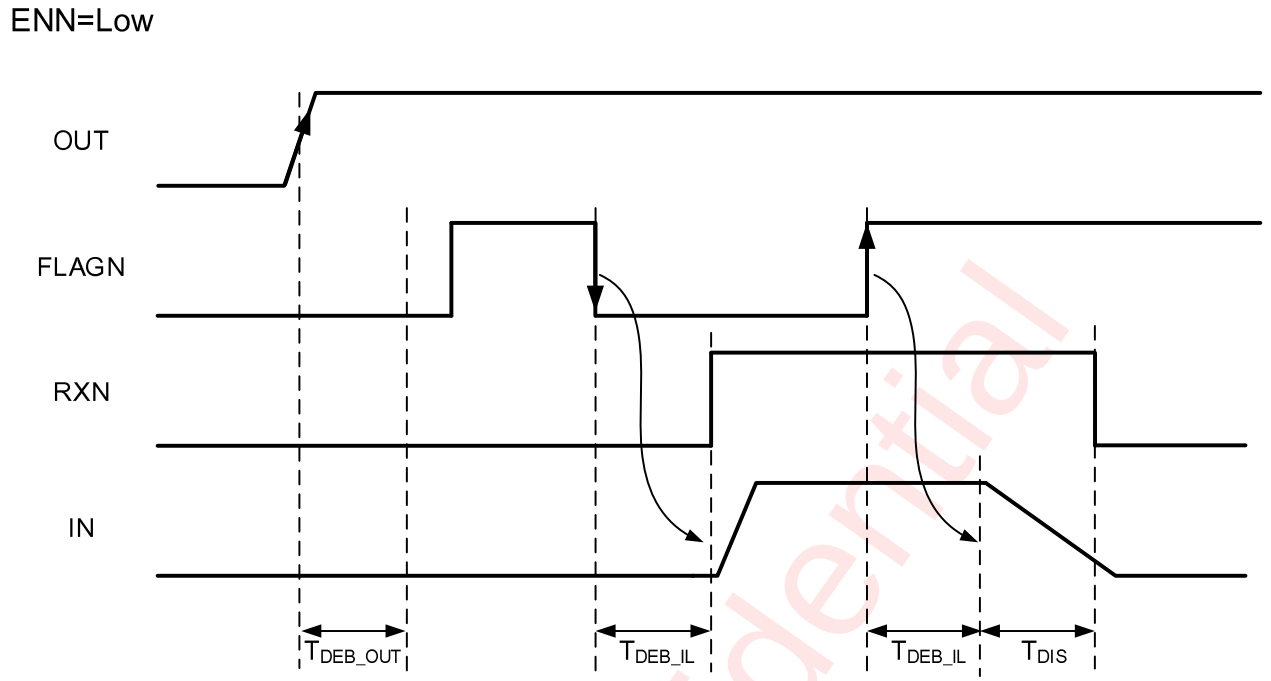


Figure 26 Autonomous Mode Timing: Application of OTG, Enable and Disable

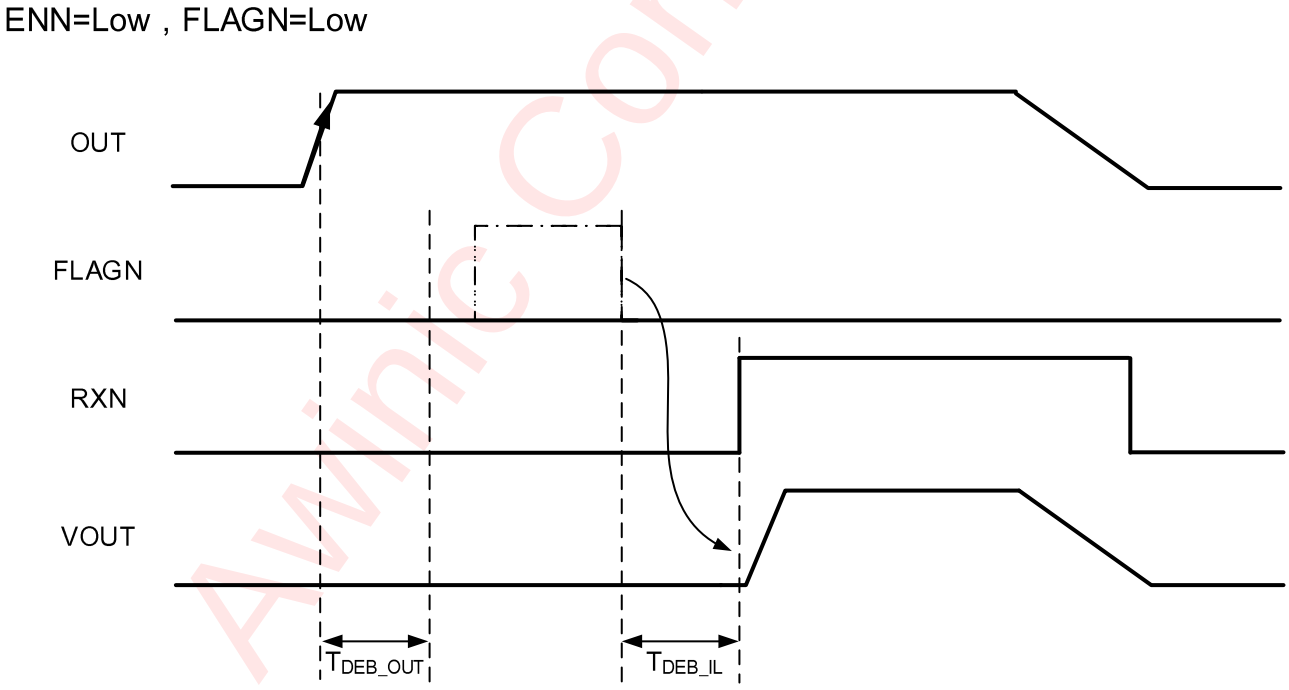


Figure 27 Autonomous Mode Timing: Application of OTG (Defualt)

In slave mode, the on/off state of the load switch is determined by the ENN logic input pin that is tied to the system logic I/O.

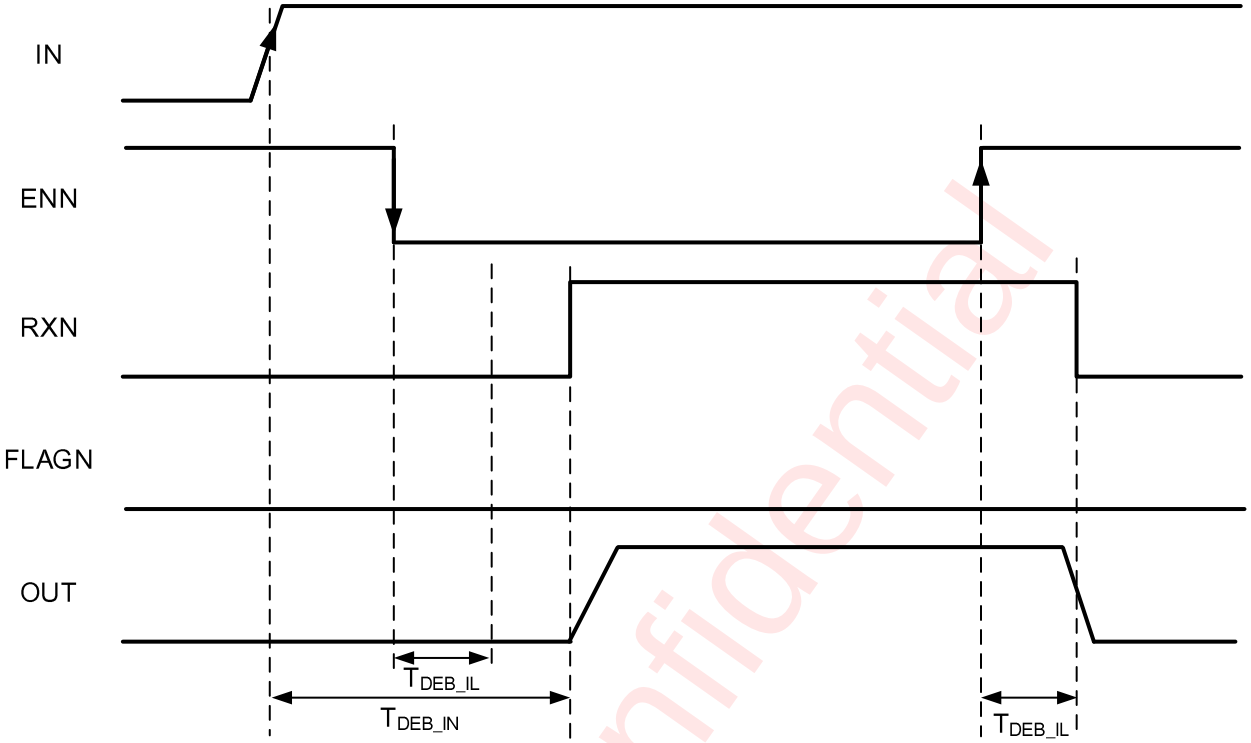


Figure 28 Slave Mode Timing: Application of IN input, Enable and Disable

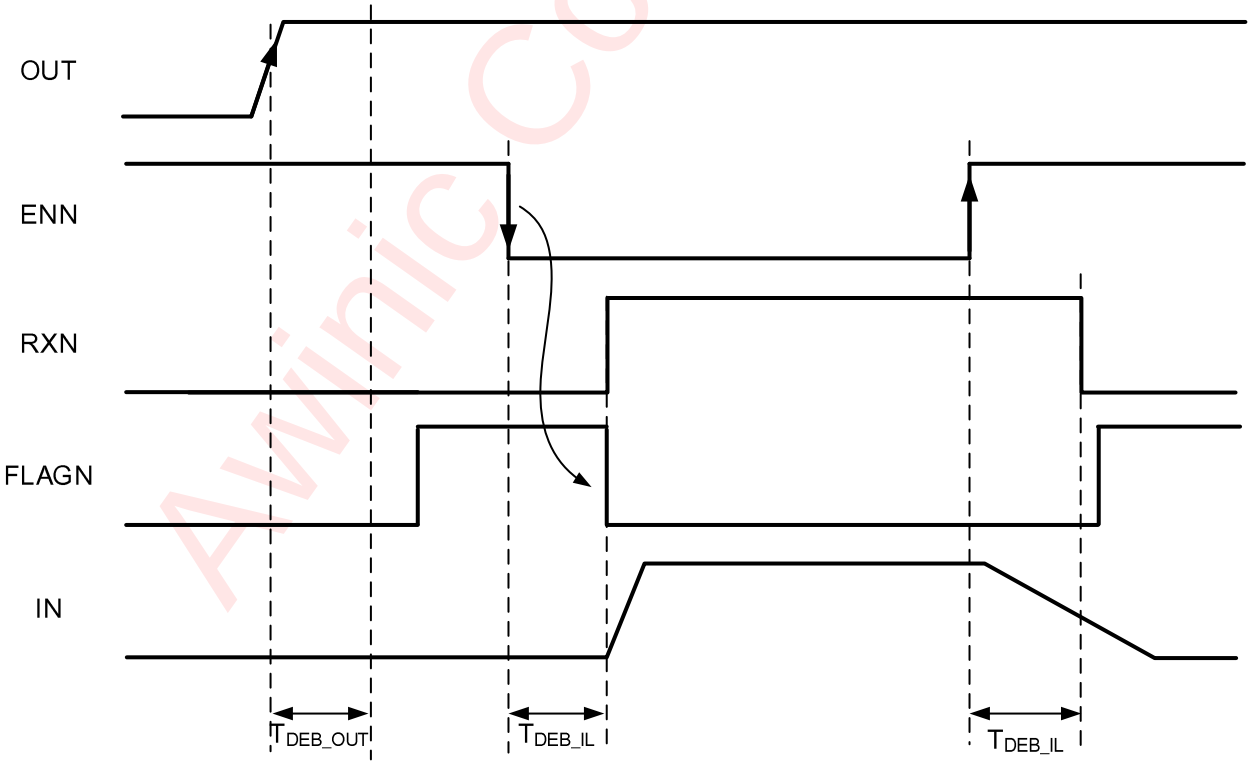


Figure 29 Slave Mode Timing: Application of OTG, Enable and Disable

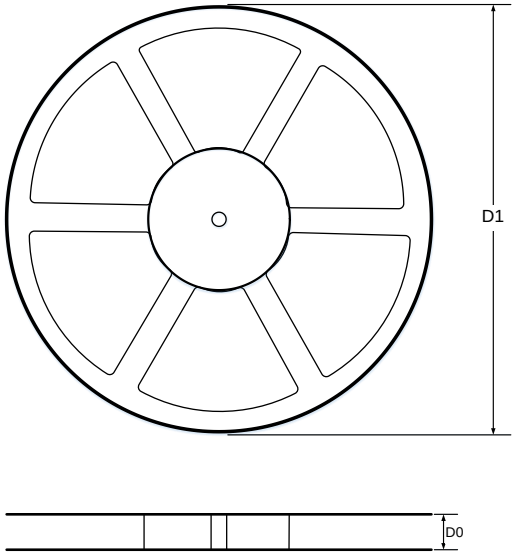
PCB Layout Consideration

To obtain the optimal performance of AW32101, PCB layout should be considered carefully. Here are some guidelines:

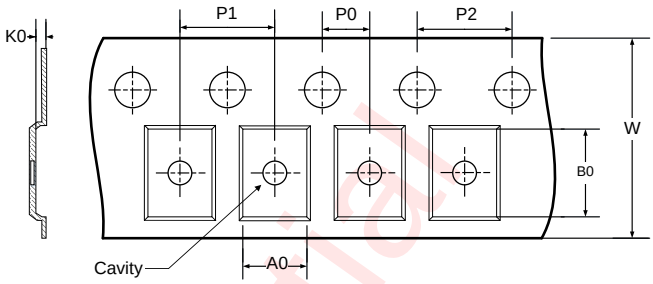
1. All the peripherals should be placed as close to the device as possible, especially C_{IN}, C_{OUT} and C_{VSNS}. For example, Place the input capacitor C_{IN} on the top layer (same layer as the AW32101) and close to IN pin.
2. The AW32101 integrate an up to 5A rated MOSFET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation.
3. Use rounded corners on the power trace from the power supply connector to AW32101 to decrease EMI coupling.

Tape And Reel Information

REEL DIMENSIONS

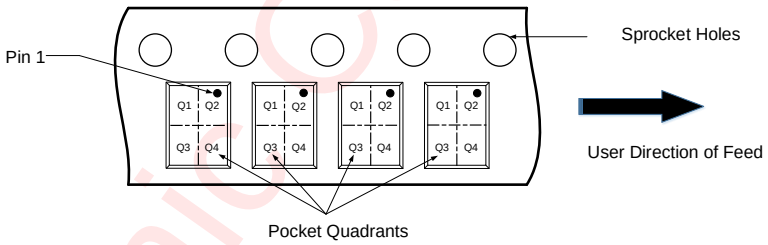


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

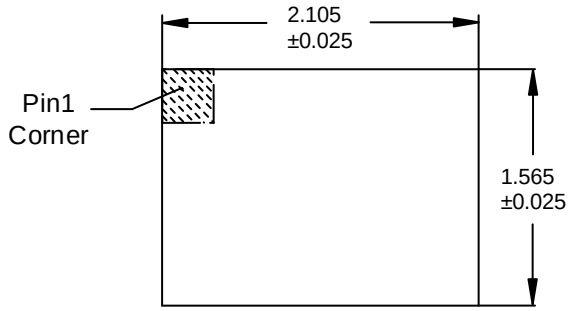
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



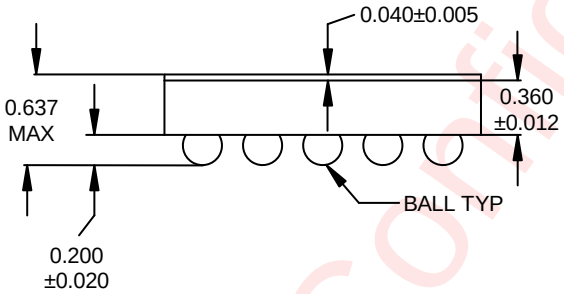
All dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	1.75	2.30	0.75	2.00	4.00	4.00	8.00	Q2

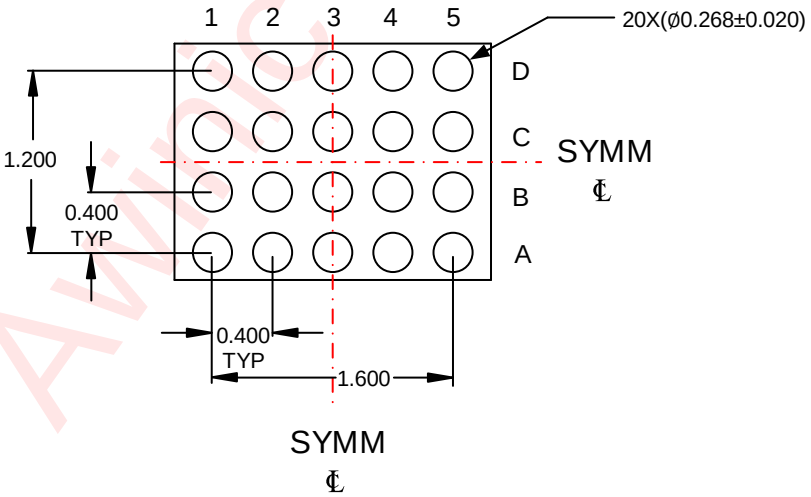
Package Description



Top View



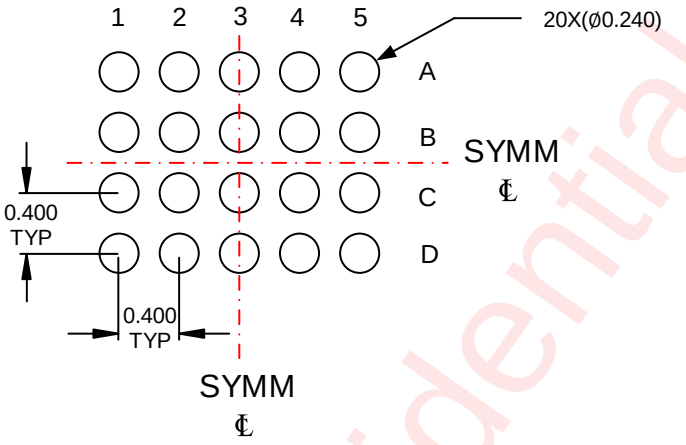
Side View

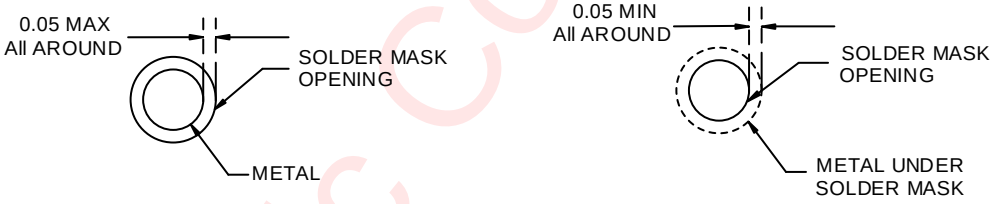


Bottom View

Unit: mm

Land Pattern Data





NON-SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	January 2019	Datasheet V1.0 released.
V1.1	August 2019	1、 Updated the T_{OVP_DLY} in the Features description and Electrical Characteristics table. 2、 Changed the test condition of V_{UVLO_OUT} "V_{IN} rising" to "V_{OUT} rising" 3、 Changed the I_{LEAK_ENN} maximum value from 1μA to 12μA. 4、 Changed the test condition of R_{ENN} from "ENN=5V" to "ENN=5V, V_{IN}=5V", and updated R_{ENN}=600kΩ to R_{ENN}=530kΩ. 5、 Updated the Figure 22.
V1.2	December 2019	1、 Updated the T_{OVP_DLY} in the Features description and Electrical Characteristics table. 2、 Changed the I_{DD_IN} and I_{DD_OUT} in the Electrical Characteristics table, and updated the Figure 6, 8, 12 and 13.

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