SP4T Switch with MIPI for 5G TRX

Features

- Broadband frequency range: 0.1 to 6.0 GHz
- Low insertion loss: 0.89dB typical @ 6GHz
- High isolation: 23dB typical @ 6GHz
- High power handling capability of up to 40dBm
- MIPI RFFE V2.1 compatible Interface
- 50-Ohm termination enabling at isolation mode
- FCLGA 1.1mm X1.1mm X0.47mm-9L package

Applications

- Cellular 2G/3G/4G/5G TRX
- Cellular modems, tablets and USB Devices
- Other RF front-end modules

General Description

The AW13504HFLR is a SP4T switch with low insertion loss and high isolation. It can be used to 2G/3G/4G/5G applications, such as 5G SRS and High Power User Equipment.

The symmetrical design of internal ports makes it convenient for PCB routing and adjustment of receiving and transmitting signals. The band switching is realized by the MIPI RFFE 2.1 Interface.

Typical Application Circuit

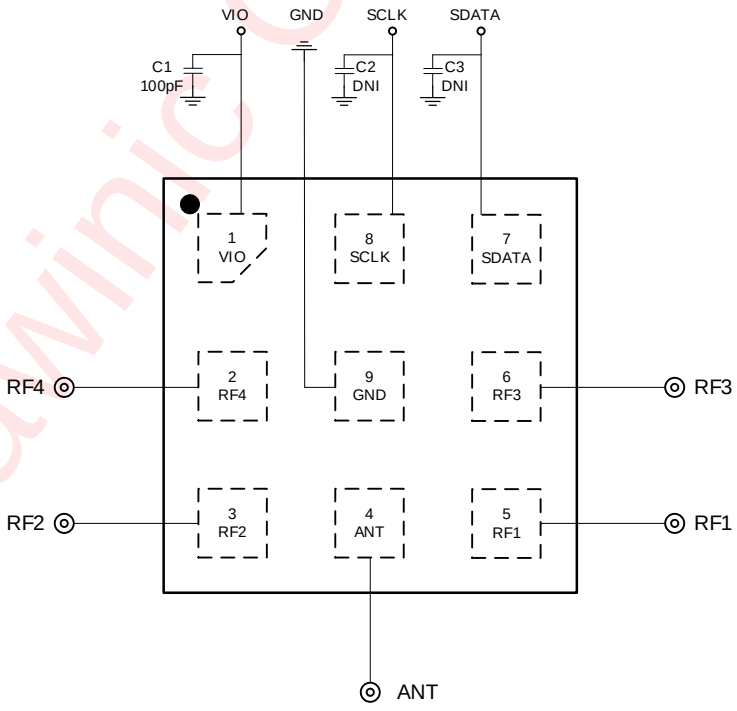
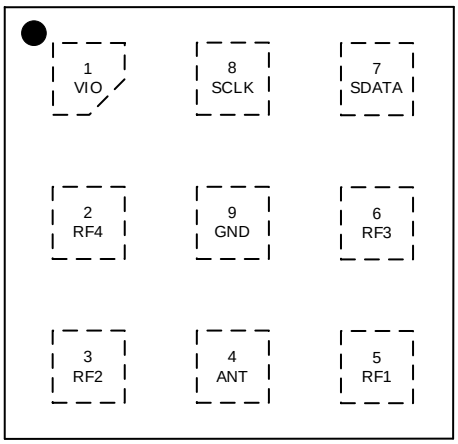


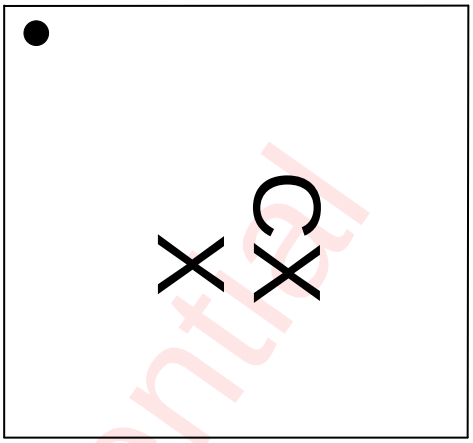
Figure 1 Typical Application Circuit

Pin Configuration and Top Mark

AW13504HFLR
(Top View)



AW13504HFLR Marking
(Top View)



CX - AW13504HFLR
X - Production Tracing Code

Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	VIO	Voltage Supply
2	RF4	RF Port4
3	RF2	RF Port2
4	ANT	Antenna
5	RF1	RF Port1
6	RF3	RF Port3
7	SDATA	RFFE Data Signal
8	SCLK	RFFE Clock Signal
9	GND	Ground

Functional Block Diagram

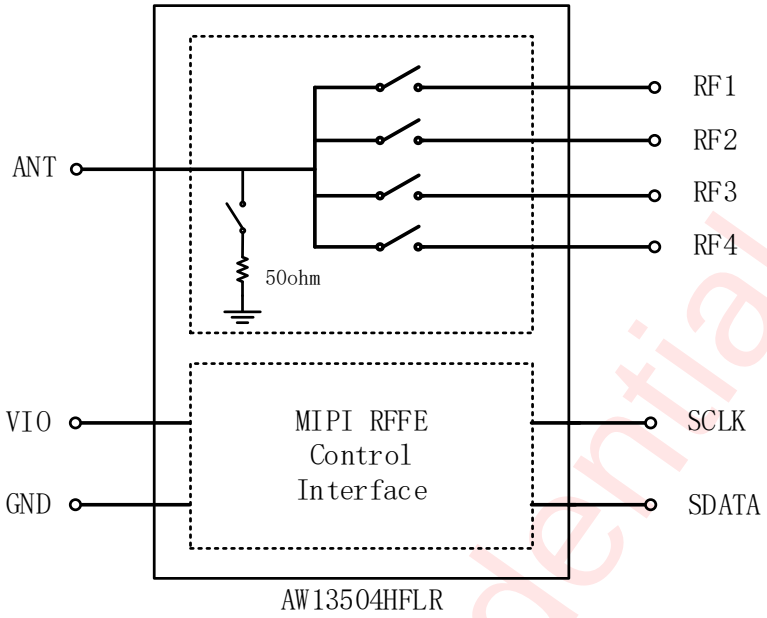


Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW13504HFLR	-40°C～90°C	FCLGA 1.1mmX1.1mm X0.47mm-9L	CX	MSL3	RoHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings(*NOTE1*)

PARAMETERS	RANGE
Supply Voltage Range V_{IO}	-0.3V to +2.5 V
RRFFE Bus Voltage (SDATA, SCLK)	-0.3V to +2.5 V
Max input power(RF1/RF2/RF3/RF4/ANT) 900MHz&1900MHz, 25% DC VSWR=1:1	40dBm
Operating Free-air Temperature Range	-40°C to 90°C
Storage Temperature T_{STG}	-65°C to 150°C
Maximum Junction temperature T_{JMAX}	125 °C
ESD (*NOTE 2*)	
HBM	±2000V
CDM	±1000V

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017. CDM test method is ESDA/JEDEC JS-002-2018.*

Electrical Characteristics

V_{IO}=1.8V, P_{IN}=0dBm, Temp=+25℃, Z_0=50Ω. Unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC Specifications						
V_{IO}	Supply Voltage		1.65	1.8	1.95	V
I_{IO}	Supply Current	Active Mode		53	100	μA
		Low Power Mode		2	10	μA
V_{IH}	SDATA,SCLK Control Voltage High		0.7*V_{IO}	V_{IO}	V_{IO}	V
V_{IL}	SDATA,SCLK Control Voltage Low		0	0	0.3*V_{IO}	V
T_{WK}	Wakeup Time	From end of Low Power State 50% SCLK to 90% of final RF amplitude		4	8	μs
T_{SW}	Switching Time (One RF port to another)	From end of RFFE Sequence to 90%/10% of final RF amplitude		1.5	2	μs
RF Specifications						
IL	Insertion loss (ANT to RFx)	617-960MHz		0.34	0.45	dB
		960-2170 MHz		0.39	0.50	dB
		2170-2700 MHz		0.43	0.60	dB
		3300-3800 MHz		0.52	0.75	dB
		3800-4200 MHz		0.56	0.80	dB
		4400-5000 MHz		0.68	0.85	dB
		5150-5925 MHz		0.89	1.10	dB
ISO	Isolation (ANT to RFy)&(RFx to RFy)	617-960MHz	35	47		dB
		960-2170 MHz	26	37		dB
		2170-2700 MHz	24	34		dB
		3300-3800 MHz	22	29		dB
		3800-4200 MHz	20	28		dB
		4400-5000 MHz	19	26		dB
		5150-5925 MHz	16	23		dB
RL	Return Loss (ANT/RF1/RF2/RF3/RF4)	617-960MHz	22	27		dB
		960-2170 MHz	18	22		dB
		2170-2700 MHz	17	21		dB
		3300-3800 MHz	15	19		dB
		3800-4200 MHz	13	18		dB
		4400-5000 MHz	12	16		dB
		5150-5925 MHz	10	13		dB
$2F_0$	Second harmonics	PIN=+26dBm, 900MHz VSWR=1:1		-79	-69	dBm
		PIN=+35dBm, 900MHz VSWR=1:1		-60	-50	dBm

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
		PIN=+26dBm, 1900MHz VSWR=1:1		-75	-65	dBm
		PIN=+33dBm, 1900MHz VSWR=1:1		-60	-50	dBm
$3F_0$	Third harmonics	PIN=+26dBm, 900MHz VSWR=1:1		-80	-70	dBm
		PIN=+35dBm, 900MHz VSWR=1:1		-55	-45	dBm
		PIN=+26dBm, 1900MHz VSWR=1:1		-77	-67	dBm
		PIN=+33dBm, 1900MHz VSWR=1:1		-55	-50	dBm
IIP2	2nd order intercept point	f1=26dBm, 1950MHz f2=-20dBm,4090MHz	114	124		dBm
IIP3	3nd order intercept point	f1=26dBm, 2560MHz f2=-10dBm,3310MHz	62	72		dBm
$P_{0.1dB}$	0.1dB Compression Point	900MHz&1900MHz, 25% DC VSWR=1:1		40		dBm

Timing Requirements

1. Once V_{IO} is powered down to 0 V, wait at least 10 μs to reapply power to V_{IO}.

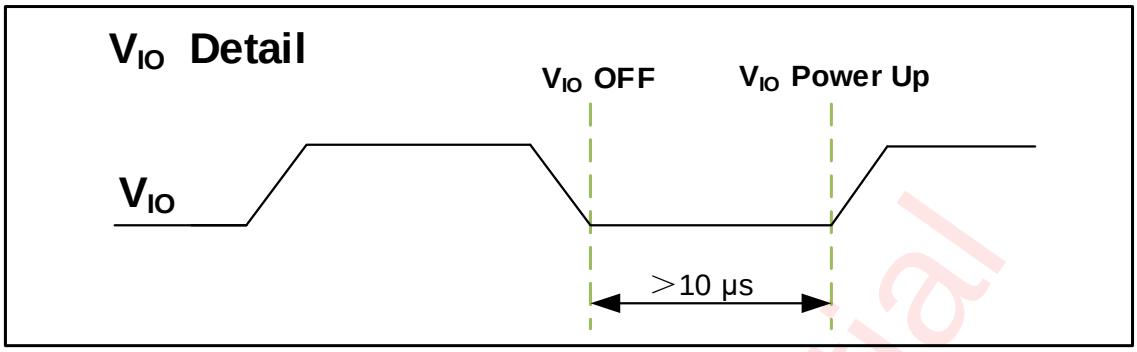


Figure 4 Digital Supply Detail

2. Before applying RF power , V_{IO} must be turned on for at least 20 μs.

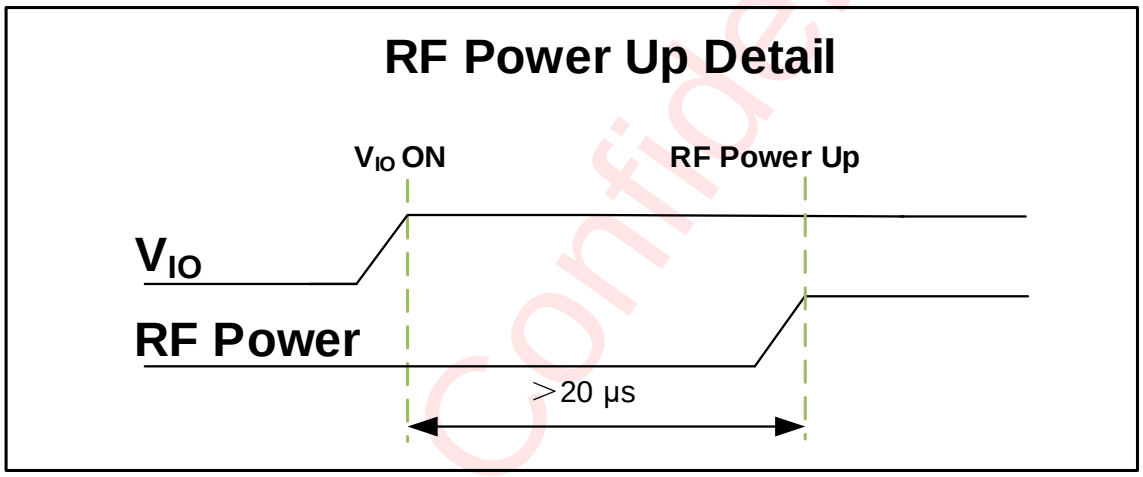


Figure 5 RF Power-Up Detail

3. Before sending SDATA/SCLK , V_{IO} must be applied for at least 120 ns to ensure correct data transmission. And after the RFFE bus is idle, wait at least 10 μs to apply the RF signal.

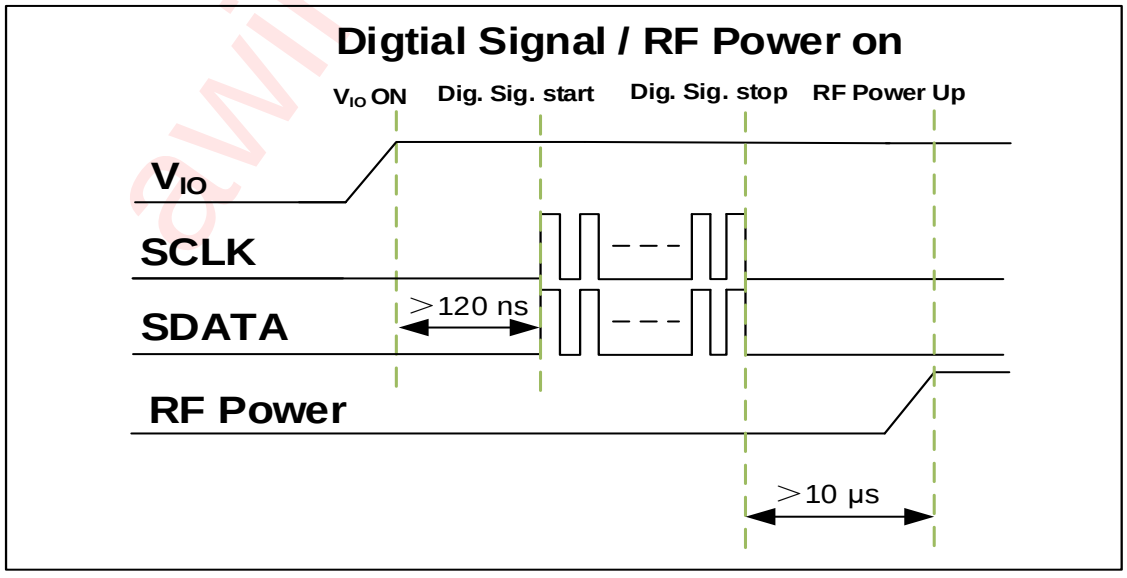


Figure 6 Digital Signal / RF Power-On Detail

4. There shall be no RFFE bus operations during RF Signal active to protect the device. So RF input signal shall be applied after RFFE bus operations being finished and be removed before RFFE bus operations being started.

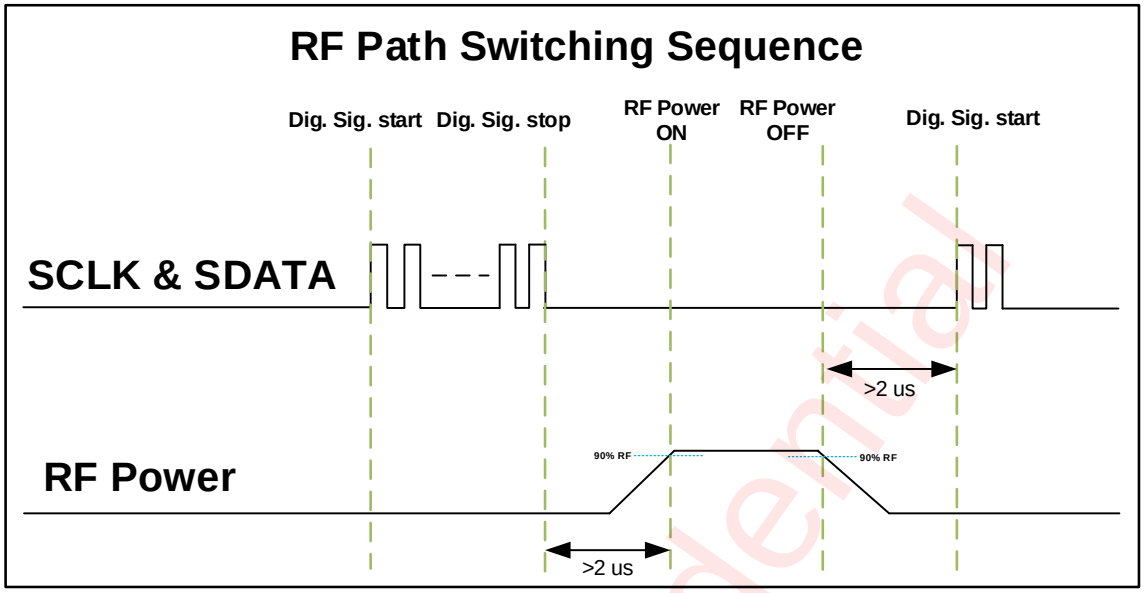


Figure 7 RF Path Switching Sequence

MIPI RFFE Specification

The MIPI RFFE interface is working in systems following the MIPI Alliance Specification for RF Front-End Control Interface version 2.1.

TABLE1: MIPI FEATURES

Feature	Supported	Comment
MIPI RFFE 2.1 standard	Yes	
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Masked write command sequence	Yes	Indicated as MW in below register mapping tables
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz for read and write
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz for write
Half speed read	Yes	
Full speed read/Full speed write	Yes	
Longer Reach RFFE Bus Length Feature	Yes	
Programmable driver strength	Yes	
Programmable Group SID	Yes	
Programmable USID	Yes	Support for three registers write and extended write sequences
Trigger functionality	Yes	
Extended Triggers and Trigger Masks	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID select pin	No	

TABLE2: Start-up Behavior

Feature	State	Comment
Power status	Low power mode	Low power mode after start-up
Trigger function	Enable	Enable after start-up. Programmable via register

MIPI Read and Write Timing

Register 0 write:

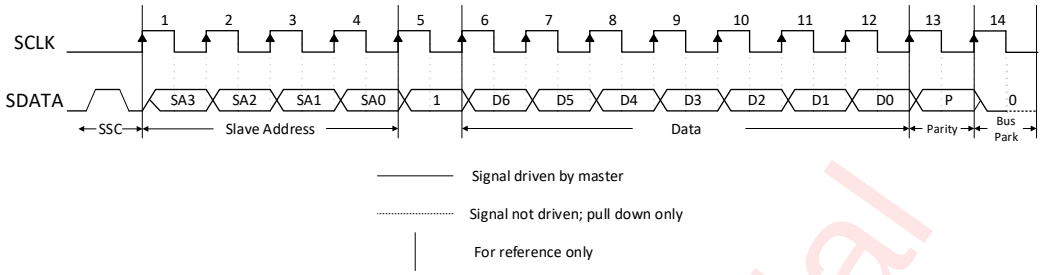


Figure 8 Register 0 Write Command Sequence

Register write:

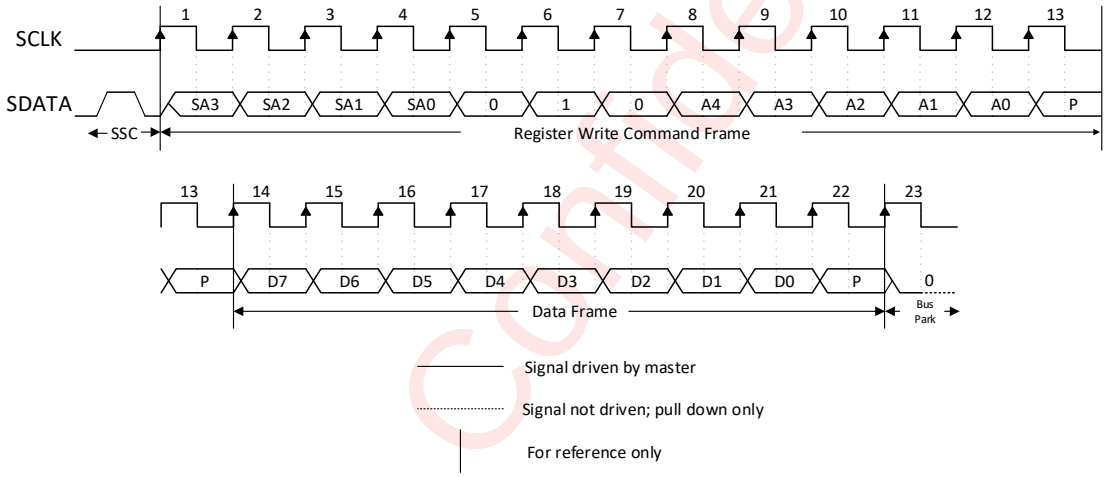


Figure 9 Register Write Command Sequence

Register read:

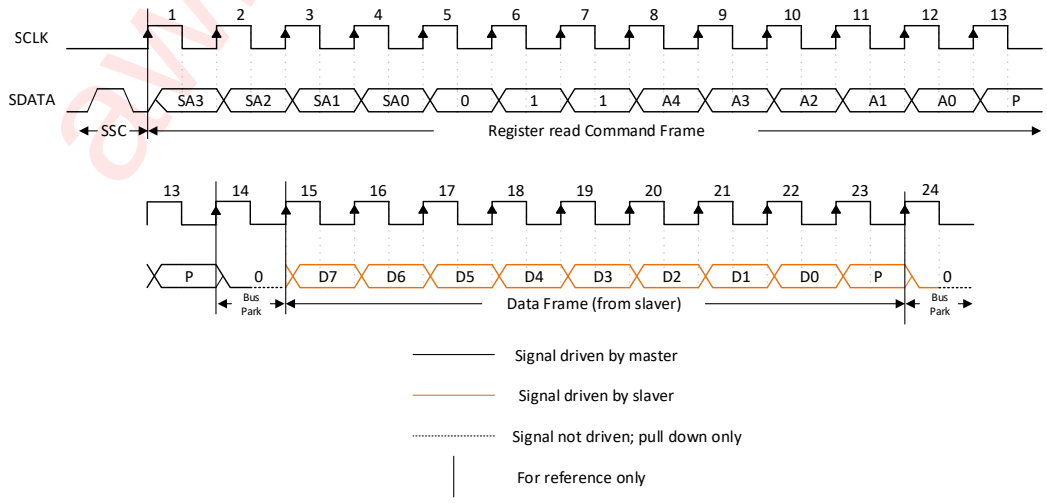


Figure 10 Register Read Command Sequence

Extended Register write:

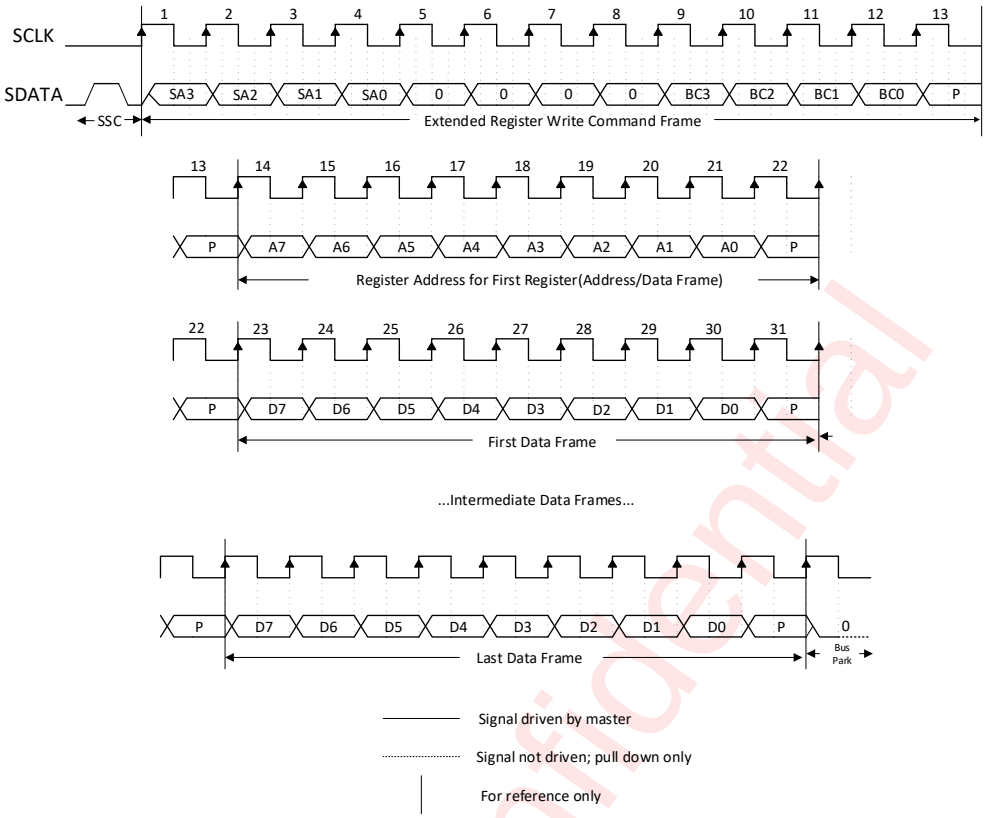


Figure 11 Extended Register Write Command Sequence

Extended Register read:

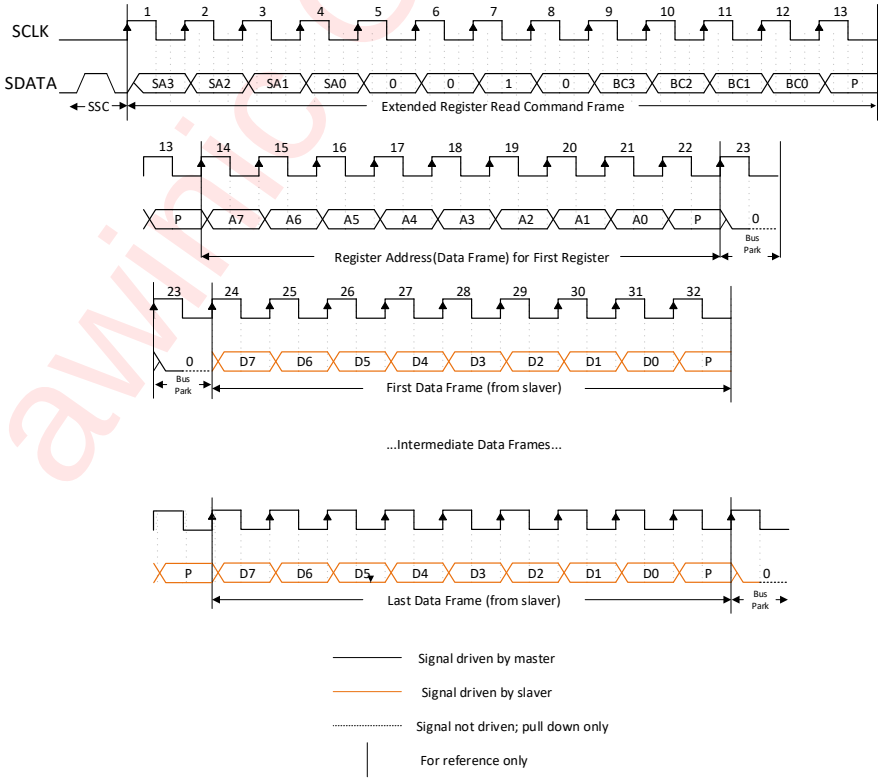


Figure 12 Extended Register Read Command Sequence

Masked write:

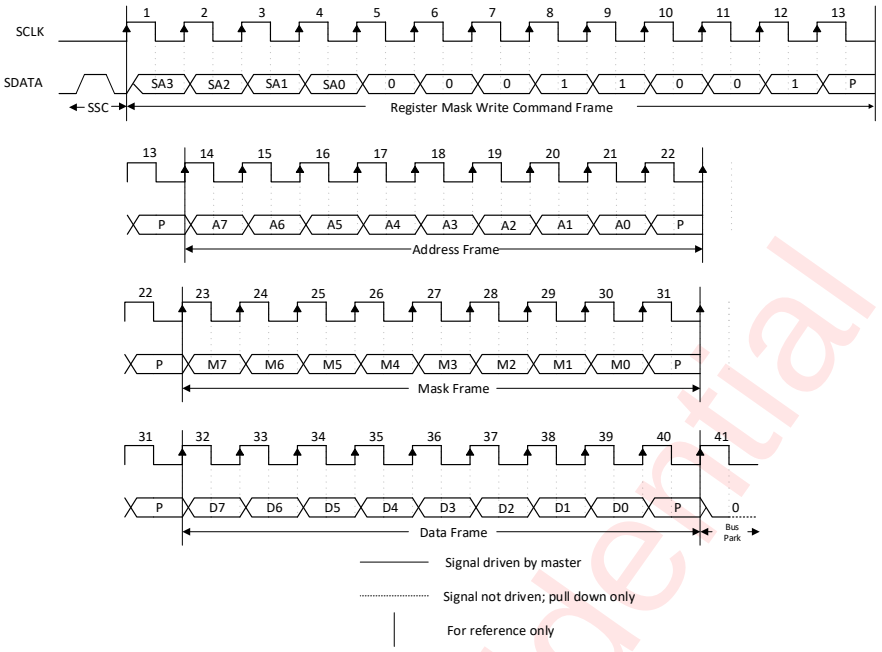


Figure 13 Masked Write Command Sequence

Register Configuration

Register Detailed Description

REGISTER_0：Mode Control Register(Address 0000h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	MODE_CTRL	xxx00000: ALL OFF (ANT float) xxxxxxx1: RF1 on xxxxxx1x: RF2 on xxxxx1xx: RF3 on xxxx1xxx: RF4 on xxx1xxxx: ANT connected to a 50Ω (x—either 0 or 1)	RW MW	No	Yes 0-10	0x00

-This device supports multi-channel on simultaneously, when multi bit=1 at [D3~D0].

- It's not recommended to open both ANT connected to a 50Ω and RFx on at the same time.

RFFE_STATUS：RFFE Status Register(Address 001Ah)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7	UDR_RST	Reset all configurable non-RFFE reserved register to default values 0: normal operation 1: software reset	W	No	No	0
6	CMD_FR_P_ERR	Command Frame received with a parity error	RW	No	No	0
5	CMD_LEN ERR	Command Sequence received with an incorrect length	RW	No	No	0
4	ADDR_FR_P_ERR	Address Frame received with a parity error	RW	No	No	0
3	DATA_FR_P_ERR	Data Frame received with a parity error	RW	No	No	0
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	RW	No	No	0
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	RW	No	No	0
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	RW	No	No	0

GSID0_1：Group ID 0-1 Register(Address 001Bh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:4	GSID0	Group Slave ID0	RW	No	No	0000

3:0	GSID1	Group Slave ID1	RW	No	No	0000

PM_TRIG：Pwr_mode and Trig Register(Address 001Ch)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7	PWR_MODE[1]	0: Normal Operation 1: Low Power - Antenna in isolation	RW	Yes	No	1
6	PWR_MODE[0]	0: active 1: start up – Reset all register to default	RW	Yes	No	0
5:3	Trigger Mask[2:0]	Setting bit Trigger Mask[N] disables Trigger[N] Trigger Mask[N] updates before Trigger[N] is processed *Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register. If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.*	RW	No	No	000
2:0	Trigger[2:0]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[0], [1], and [2] will always read as 0.*	W	Yes	No	000

PRODUCT_ID：Product ID Register(Address 001Dh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	PROD_ID	Lower eight bits of Product ID	R	No	No	0x08

MANUFACTURER_ID：Manufacture ID Register(Address 001Eh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	MFG_ID	Lower eight bits of Manufacturer ID	R	No	No	0x49

MAN_USID：User ID Register(Address 001Fh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:4	MFG_ID	Upper four bits of Manufacturer ID	R	No	No	0000

3:0	USID	Unique Slave ID	RW	No	No	1000

EXT_PRODUCT_ID：Extend Product ID Register(Address 0020h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	PROD_ID	Upper eight bits of Product ID	R	No	No	0x00

REVISION_ID：Revision ID Register(Address 0021h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	REV_ID	Revision ID	R	No	No	0x01

GSID2_3：Group ID 2-3 Register(Address 0022h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:4	GSID2	Group Slave ID2	R/W	No	No	0000
3:0	GSID3	Group Slave ID3	R/W	No	No	0000

UDR_RST：UDR Reset Register(Address 0023h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7	UDR_RST	Reset all configurable non-RFFE reserved register to default values 0: normal 1: software reset	R/W	Yes	No	0
6:0	RESERVED	Reserved	R/W	No	No	0x00

ERR_SUM：Error Command Status Register(Address 0024h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7	SPARE	Reserved for future use	R/W	No	No	0
6	COM_FR_P_ERR	Command Frame received with a parity error	R/W	No	No	0
5	COM_LEN_ERR	Command Sequence received with an incorrect length	R/W	No	No	0
4	ADDR_FR_P_ERR	Address Frame received with a parity error	R/W	No	No	0
3	DATA_FR_P_ERR	Data Frame received with a parity error	R/W	No	No	0

2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	R/W	No	No	0
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	R/W	No	No	0
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	R/W	No	No	0

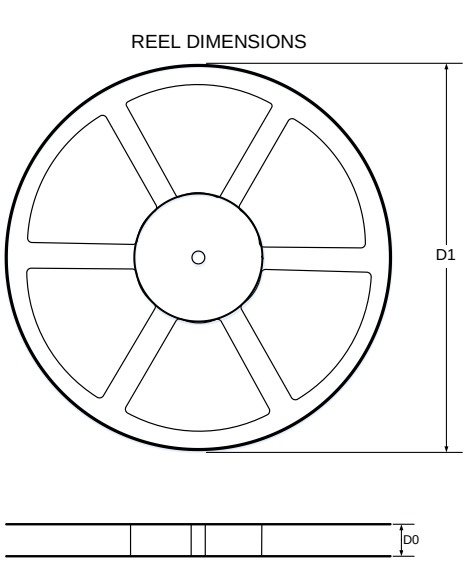
EXT_TRIG_MASK：Extend Trig Mask Register(Address 002Dh)

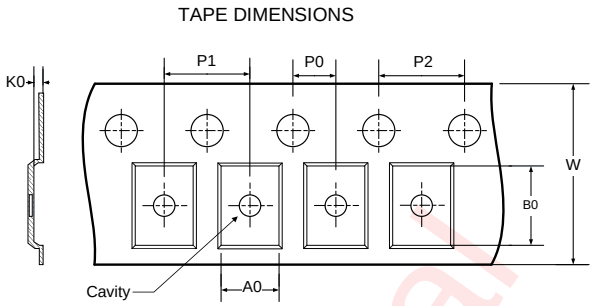
Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	Trigger Mask[10:3]	Setting bit Trigger Mask[N] disables Trigger[N] If using an Extended Write to update both Trigger Mask and Trigger, than Trigger Mask[N] updates before Trigger[N] is processed *Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register. If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.*	RW	No	No	0xFF

EXT_TRIG：Extend Trig Register(Address 002Eh)

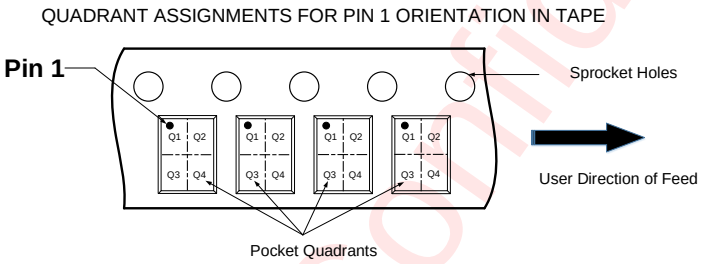
Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	Trigger[10:3]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[10 - 3] will always read as 0.*	W	Yes	No	0x00

Tape and Reel Information





A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

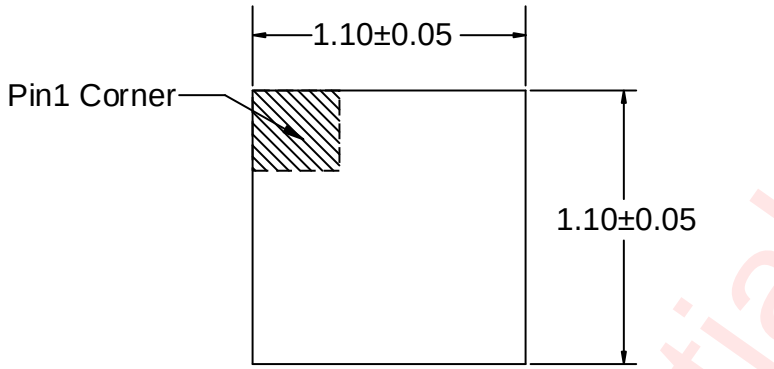
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
180	8.4	1.25	1.25	0.6	2	4	4	8	Q1

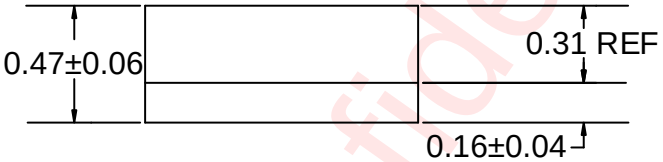
All dimensions are nominal

Figure 14 Tape and Reel

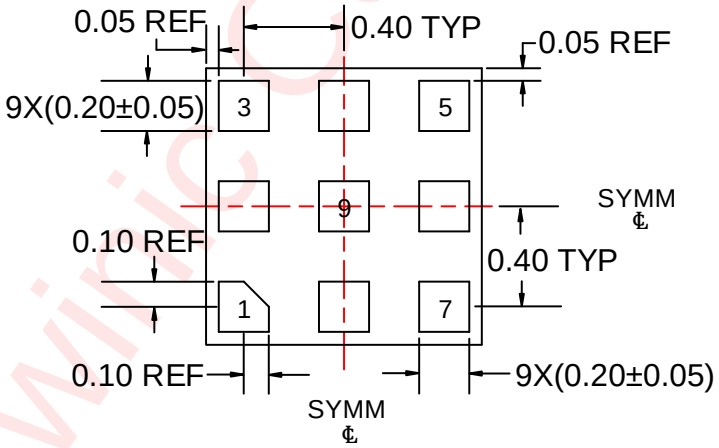
Package outline dimensions



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Unit:mm

Figure 15 Package Outline

Land Pattern Data

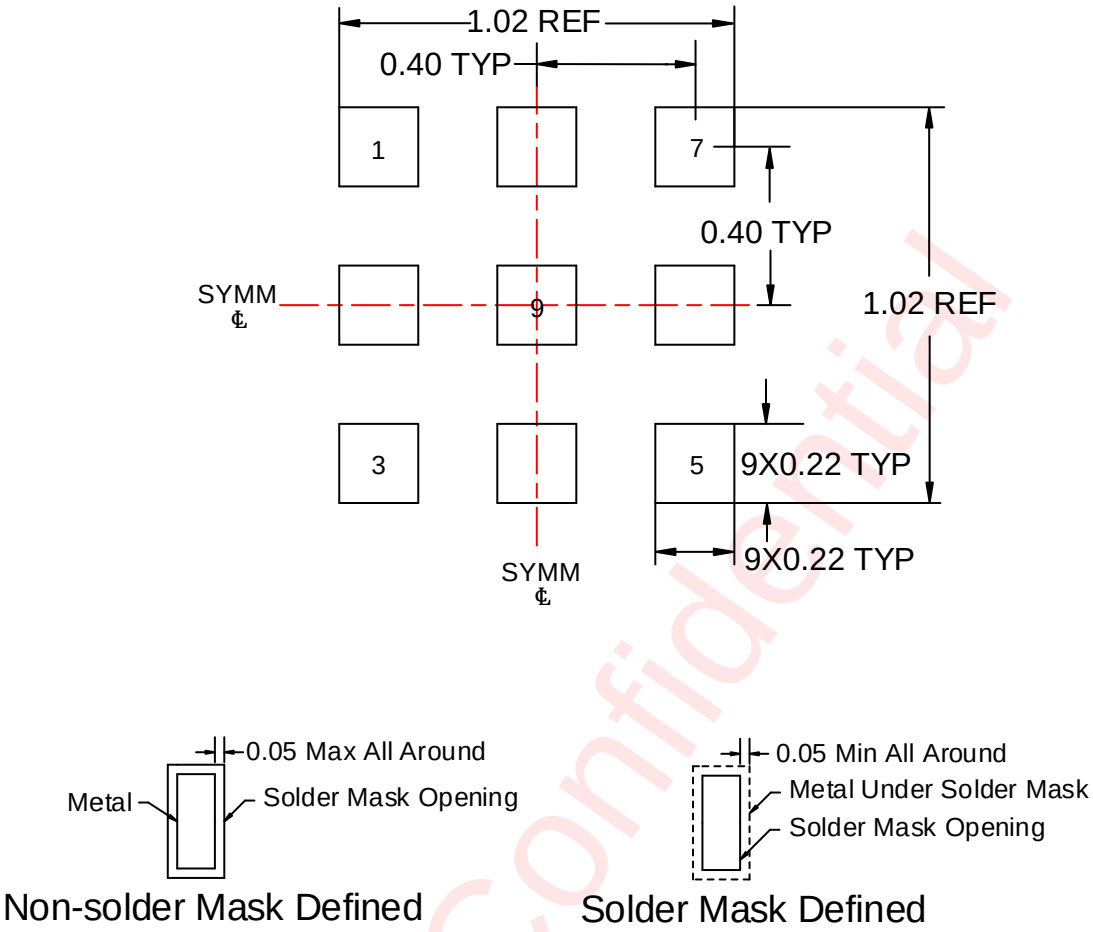


Figure 16 Land Pattern Data

Revision History

Version	Date	Change Record
V1.0	Oct. 2022	Officially Released
V1.1	Aug. 2023	Optimize S parameter and add 0x21 register
V1.2	Dec. 2023	Optimize 0x00 register

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