AW9546 4-Channel I²C-bus Switch With Reset

Features

- 1-to-4 bidirectional translating switches
- I²C bus and SMBus compatible
- Active-low reset input
- Three address pins, allowing up to eight devices on the I²C bus
- Channel selection through an I²C bus, in any combination
- Power up with all switch channels deselected
- Low R_{ON} switches
- 400kHz I²C interface
- Allows voltage-level translation between 1.8V, 2.5V, 3.3V and 5V buses
- 1.65V~5.5V power supply
- 5.5V tolerant inputs
- No glitch on power up
- Supports hot insertion
- Low standby current
- TSSOP-16L package

Applications

- Servers
- Routers (telecom switching equipment)
- Factory Automation
- Products with I²C slave address conflicts (such as multiple, identical temperature sensors)

General Description

The AW9546 is an 4-channel, bidirectional translating switch that can be controlled through the I²C bus. The SCL/SDA upstream pair fans out to 4 downstream pairs, or channels. Any individual SCn/SDn channel or combination of channels can be selected, determined by the contents of the programmable control register.

The device offers an active-low RESETN input which resets the state machine and allows the AW9546 to recover from a situation where one of the downstream I²C buses get stuck in a low state. The state machine of the device can also be reset by cycling the power supply, V_{CC}, also known as a power-on reset (POR). Both the RESETN function and a POR cause all channels to be deselected and initializes the I²C/SMBus state machine.

The pass-gate transistors of the AW9546 are constructed so that the V_{CC} pin can be used to limit the maximum high voltage which is passed by the AW9546. Limiting the maximum high voltage allows the use of different bus voltages on each pair, so that 1.8V or 2.5V or 3.3V parts can communicate with 5V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5.5V tolerant.

Typical Application Circuit

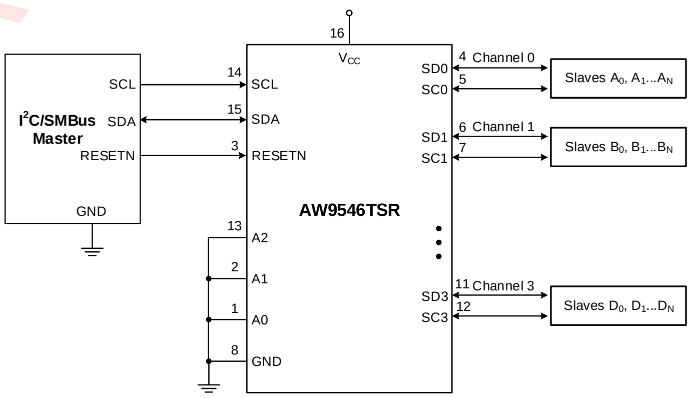
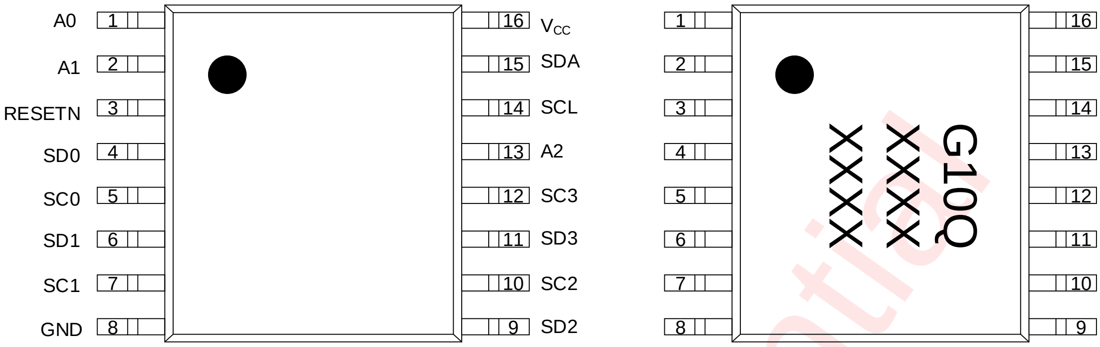


Figure 1 AW9546TSR Simplified Application Circuit

Pin Configuration And Top Mark

AW9546TSR (Top View) **AW9546TSR Marking (Top View)**



G10Q - AW9546TSR
XXXX/XXXX - Production Tracing Code

Figure 2 Pin Configuration and Marking

Pin Definition

NO.	NAME	DESCRIPTION
1	A0	Address input 0. Connect directly to V_{CC} or ground.
2	A1	Address input 1. Connect directly to V_{CC} or ground.
3	RESETN	Active-low reset input. Connect to V_{CC} or V_{DPUM}(NOTE1) through a pull-up resistor, if not used.
4	SD0	Serial data 0. Connect to V_{DPU0}(NOTE1) through a pull-up resistor.
5	SC0	Serial clock 0. Connect to V_{DPU0}(NOTE1) through a pull-up resistor.
6	SD1	Serial data 1. Connect to V_{DPU1}(NOTE1) through a pull-up resistor.
7	SC1	Serial clock 1. Connect to V_{DPU1}(NOTE1) through a pull-up resistor.
8	GND	Ground.
9	SD2	Serial data 2. Connect to V_{DPU2}(NOTE1) through a pull-up resistor.
10	SC2	Serial clock 2. Connect to V_{DPU2}(NOTE1) through a pull-up resistor.
11	SD3	Serial data 3. Connect to V_{DPU3}(NOTE1) through a pull-up resistor.
12	SC3	Serial clock 3. Connect to V_{DPU3}(NOTE1) through a pull-up resistor.
13	A2	Address input 2. Connect directly to V_{CC} or ground.
14	SCL	Serial clock bus. Connect to V_{DPUM}(NOTE1) through a pull-up resistor.
15	SDA	Serial data bus. Connect to V_{DPUM}(NOTE1) through a pull-up resistor.
16	V_{CC}	Supply voltage.

NOTE1: V_{DPUX} is the pull-up reference voltage for the associated data line. V_{DPUM} is the master I^2C reference voltage and V_{DPU0}~V_{DPU3} are the slave channel reference voltages.

Functional Block Diagram

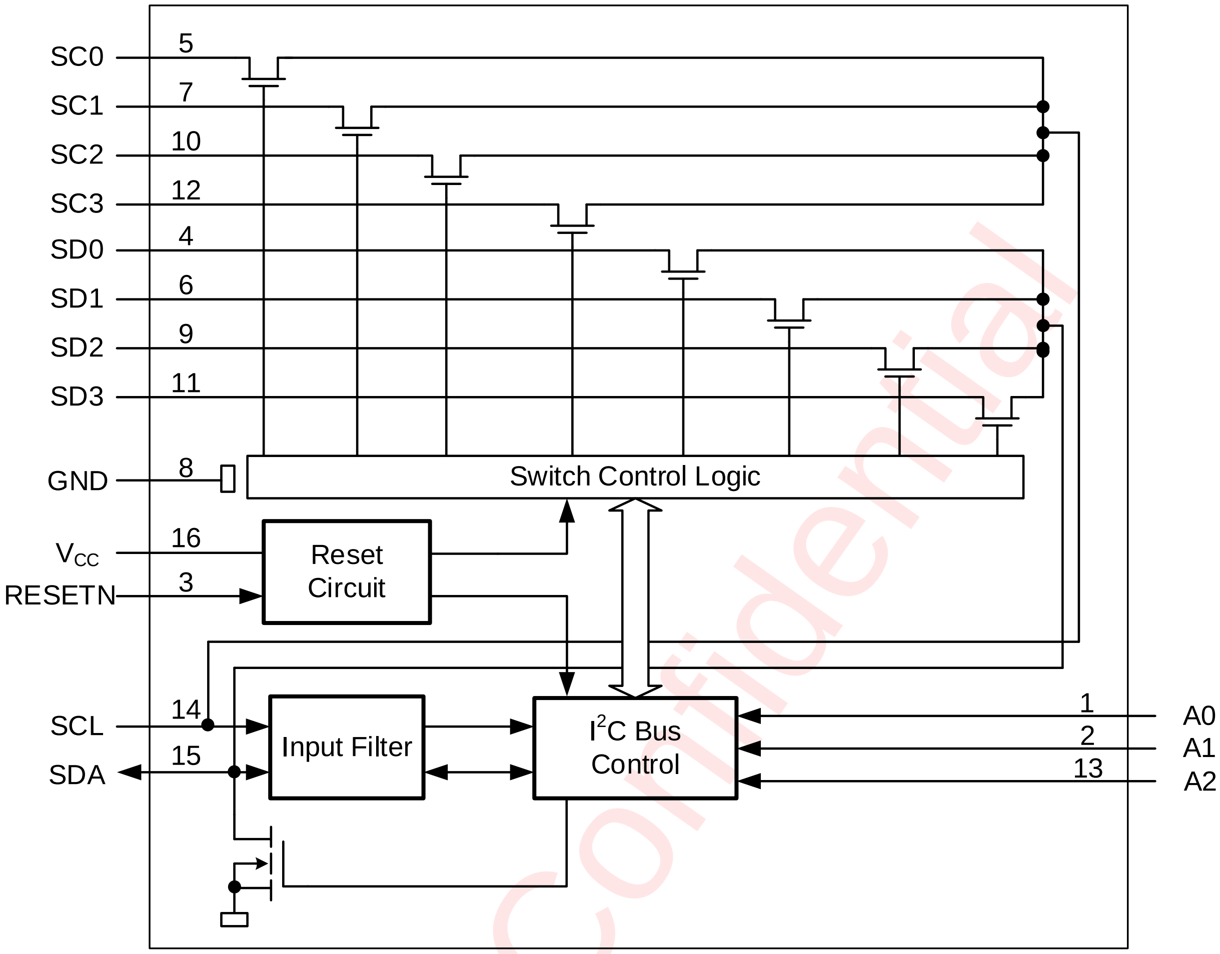


Figure 3 AW9546TSR Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW9546TSR	-40°C~125°C	TSSOP-16L	G10Q	MSL2	RoHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE2)

PARAMETERS	RANGE
Supply voltage V_{CC}	-0.5V to 7.0V
Input voltage V_I	-0.5V to 7.0V
Input current I_I	-20mA to 20mA
Output current I_O	-25mA to 25mA
Supply current I_{CC}	-100mA to 100mA
Operating free-air temperature range T_A	-40°C to 125°C

Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
Maximum operating junction temperature T_{JMAX}	150°C
ESD(Including HBM CDM)(NOTE3)	
HBM	±4kV
CDM	±1.5kV
Latch-Up	
Test condition: according to JEDEC78E	+IT: 300mA -IT: -300mA

NOTE2: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE3: The HBM test method: ESDA/JEDEC JS-001-2017, the CDM test method: ESDA/JEDEC JS-002-2018.

Recommended Operating Conditions

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		1.65		5.5	V
V_{IH}	High-level input voltage	SCL, SDA	0.7×V_{CC}		6	V
		A2-A0, RESETN	0.7×V_{CC}		6	V
V_{IL}	Low-level input voltage	SCL, SDA	-0.5		0.3×V_{CC}	V
		A2-A0, RESETN	-0.5		0.3×V_{CC}	V
T_A	Operating free-air temperature	V_{CC}=1.65V to 5.5V	-40		125	°C

Electrical Characteristics

V_{CC}=1.65V to 5.5V, T_A=25°C for typical values (unless otherwise noted).

Parameters		Test Condition	V_{CC}	Min.	Typ.	Max.	Unit
V_{PORR}	Power-on reset voltage, V_{CC} rising	No load, V_I=V_{CC} or GND(NOTE4)	1.65V to 5.5V		1.25	1.5	V
V_{PORF}	Power-on reset voltage, V_{CC} falling	No load, V_I=V_{CC} or GND(NOTE4)		0.8	1.05		V
$V_{O(SW)}$	Switch output voltage	$V_{i(SW)}$=V_{CC}, I_{SWout}=-100μA	5V		3.2		V
			4.5V to 5.5V	2.6		4	V
			3.3V		1.9		V
			3V to 3.6V	1.5		2.3	V
			2.5V		1.3		V

Parameters			Test Condition	V_{CC}	Min.	Typ.	Max.	Unit
				2.3V to 2.7V	1		1.6	V
				1.8V		0.7		V
				1.65V to 1.95V	0.5		1	V
I_{OL}	SDA		V_{OL}=0.4V	1.65V to 2V	15			mA
				2V to 5.5V	20			mA
I_I	SCL, SDA		V_I=V_{CC} or GND(NOTE4)	1.65V to 5.5V	-1		1	μA
	A2-A0, RESETN				-1		1	μA
	SC3-SC0, SD3-SD0				-1		1	μA
I_{CC}	Active mode	f_{SCL}=400kHz	V_I=V_{CC} or GND(NOTE4), I_O=0	1.65V		3.9	8	μA
				2.7V		8	15	μA
				3.6V		13	25	μA
				5.5V		26	50	μA
		f_{SCL}=100kHz	V_I=V_{CC} or GND(NOTE4), I_O=0	1.65V		1.2	3	μA
				2.7V		2.5	5	μA
				3.6V		4	10	μA
				5.5V		8	20	μA
	Standby mode	Low and high inputs	V_I=V_{CC} or GND(NOTE4), I_O=0	1.65V		0.4	1	μA
				2.7V		0.7	1.5	μA
				3.6V		1	2	μA
				5.5V		1.5	3	μA
ΔI_{CC}	Supply-current change		SCL or SDA input at 0.6V, other inputs at V_{CC} or GND(NOTE4)	1.65V to 5.5V		1.5	15	μA
			SCL or SDA input at V_{CC}-0.6V, other inputs at V_{CC} or GND(NOTE4)			1.5	15	μA
R_{ON}	Switch-on resistance		V_O=0.4V, I_O=15mA	4.5V to 5.5V	4	8	20	Ω
				3V to 3.6V	5	10	25	Ω
			V_O=0.4V, I_O=10mA	2.3V to 2.7V	8	15	30	Ω
				1.65V to 1.95V	14	25	50	Ω
C_i	A2-A0		V_I=V_{CC} or GND(NOTE4)	1.65V to 5.5V		4	5	pF
	RESETN					4	5	pF
$C_{io(off)}$	SCL, SDA		V_I=V_{CC} or GND(NOTE4), Switch OFF	1.65V to 5.5V		26	34	pF
	SC3-SC0, SD3-SD0					5.5	7.5	pF

NOTE4: RESETN=V_{CC} (held high) when all other input voltages, V_I = GND.

I²C Interface Timing Requirements

<table>
<tr><th colspan="3" rowspan="2">Parameters</th><th colspan="2">Standard Mode</th><th colspan="2">Fast Mode</th><th rowspan="2">Unit</th></tr>
<tr><th>Min</th><th>Max</th><th>Min</th><th>Max</th></tr>
<tr><td>f_{SCL}</td><td colspan="2">Interface clock frequency</td><td>0</td><td>100</td><td>-</td><td>400</td><td>kHz</td></tr>
<tr><td>$t_{HD:STA}$</td><td colspan="2">(Repeat-start) START condition hold time</td><td>4</td><td></td><td>0.6</td><td>-</td><td>μs</td></tr>
<tr><td>t_{LOW}</td><td colspan="2">Low level width of SCL</td><td>4.7</td><td></td><td>1.3</td><td>-</td><td>μs</td></tr>
<tr><td>t_{HIGH}</td><td colspan="2">High level width of SCL</td><td>4</td><td></td><td>0.6</td><td>-</td><td>μs</td></tr>
<tr><td>$t_{SU:STA}$</td><td colspan="2">(Repeat-start) START condition setup time</td><td>4.7</td><td></td><td>0.6</td><td>-</td><td>μs</td></tr>
<tr><td>$t_{HD:DAT}$</td><td colspan="2">Data hold time</td><td>0</td><td></td><td>0</td><td>-</td><td>μs</td></tr>
<tr><td>$t_{SU:DAT}$</td><td colspan="2">Data setup time</td><td>0.25</td><td></td><td>0.1</td><td>-</td><td>μs</td></tr>
<tr><td>t_R</td><td colspan="2">Rising time of SDA and SCL</td><td></td><td>1000</td><td>$20+0.1C_b$</td><td>300</td><td>ns</td></tr>
<tr><td>t_F</td><td colspan="2">Falling time of SDA and SCL</td><td></td><td>300</td><td>$20+0.1C_b$</td><td>300</td><td>ns</td></tr>
<tr><td>$t_{SU:STO}$</td><td colspan="2">STOP condition setup time</td><td>4</td><td></td><td>0.6</td><td>-</td><td>μs</td></tr>
<tr><td>t_{BUF}</td><td colspan="2">Time between start and stop condition</td><td>4.7</td><td></td><td>1.3</td><td>-</td><td>μs</td></tr>
<tr><td>t_{SP}</td><td colspan="2">Pulse width of spikes that must be suppressed by the input filter</td><td></td><td>50</td><td></td><td>50</td><td>ns</td></tr>
<tr><td rowspan="2">$t_{VD:DAT}$</td><td>Valid-data time (high to low) (NOTE5)</td><td>SCL low to SDA output low valid</td><td></td><td>1</td><td></td><td>1</td><td>μs</td></tr>
<tr><td>Valid-data time (low to high) (NOTE5)</td><td>SCL low to SDA output high valid</td><td></td><td>0.6</td><td></td><td>0.6</td><td>μs</td></tr>
<tr><td>$t_{VD:ACK}$</td><td>Valid-data time of ACK condition</td><td>ACK signal from SCL low to SDA output low</td><td></td><td>1</td><td></td><td>1</td><td>μs</td></tr>
<tr><td>C_b</td><td colspan="2">Capacitive load for each bus line</td><td></td><td>400</td><td></td><td>400</td><td>pF</td></tr>
</table>

NOTE5: Data taken using a 1kΩ pull-up resistor and 50pF load.

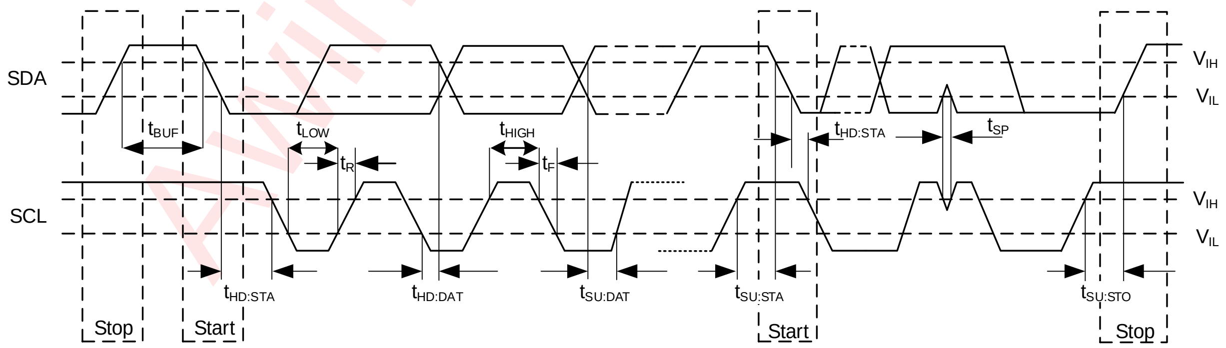


Figure 4 Definition of Timing on The I2C-bus

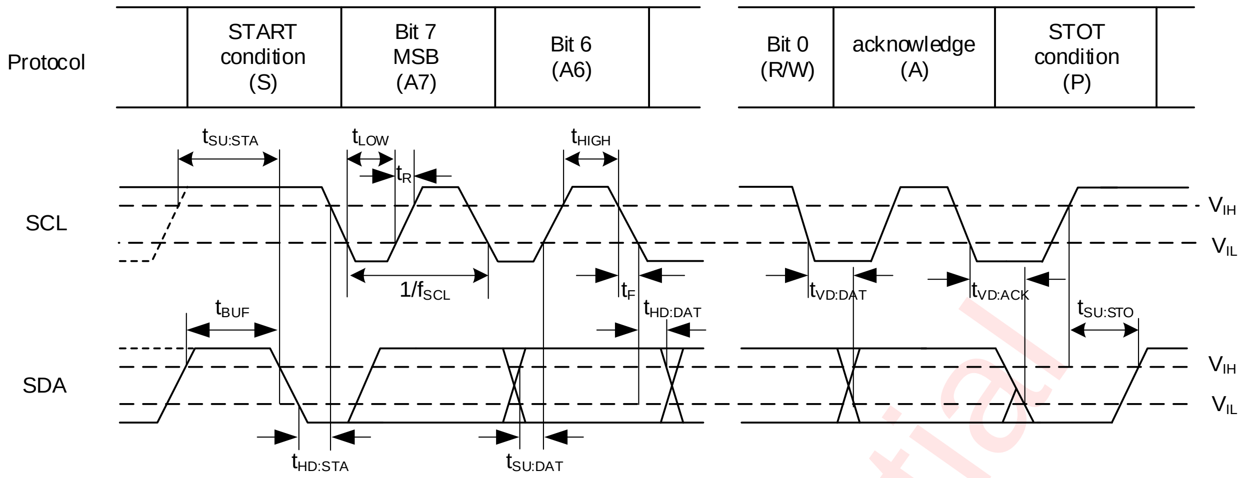


Figure 5 I²C-bus Timing Diagram

Reset Timing Requirements

Symbol	Parameter	Min.	Max.	Unit
$t_{W(rst)L}$	Low-level reset time	6		ns
$T_{REC:STA}$	Recovery time from RESETN to start	0		ns

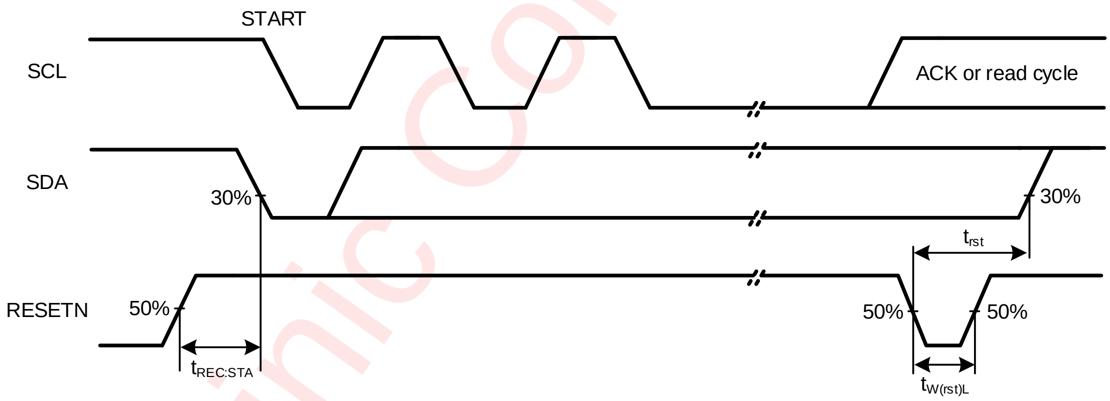


Figure 6 Definition of RESETN Timing

Switching Characteristics

Symbol	Parameter		From (Input)	To (Output)	Min.	Max.	Unit
t_{pd}(NOTE6)	Propagation delay time	R_{ON}=20Ω C_L=15pF	SDA or SCL	SDn or SCn		0.3	ns
		R_{ON}=20Ω C_L=50pF				1	ns
t_{rst}(NOTE7)	RESETN time (SDA clear)		RESETN	SDA		500	ns

NOTE6: The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

NOTE7: t_{rst} is the propagation delay measured from the time the RESET pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of $t_{W(rst)L}$.

Typical Characteristics

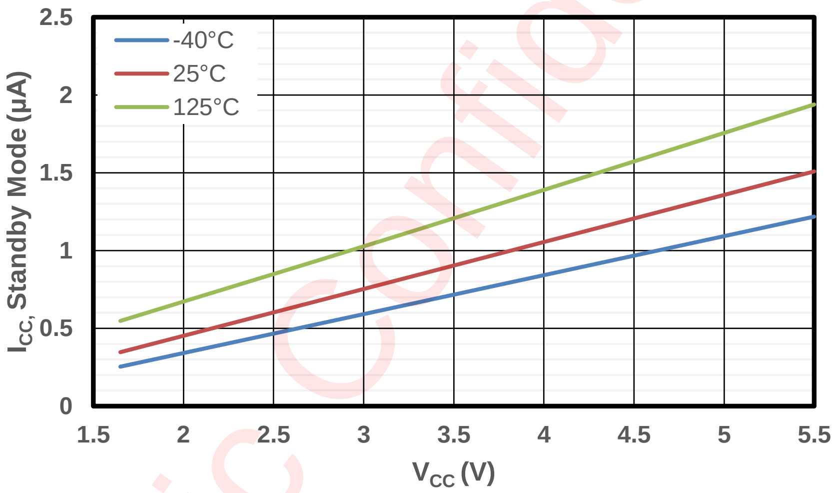


Figure 7 Standby Current (I_{CC}) vs Supply Voltage (V_{CC}) at Three Temperature Points

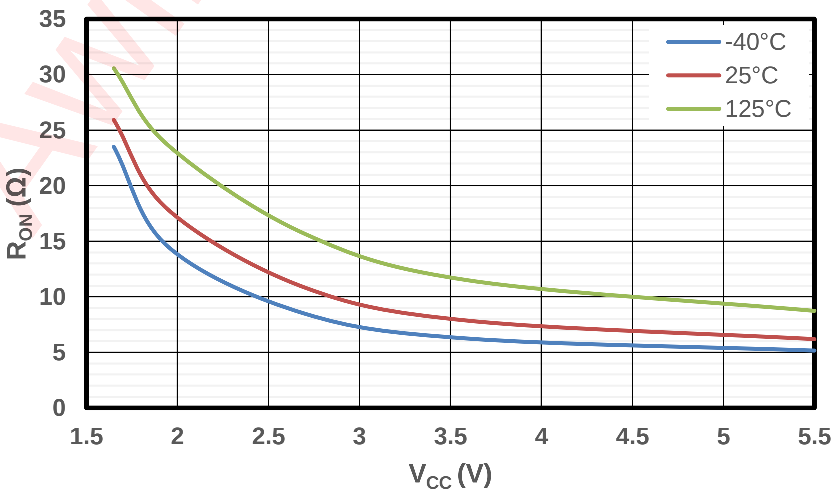


Figure 8 On-Resistance (R_{ON}) vs Supply Voltage (V_{CC}) at Three Temperatures

Detailed Functional Description

The AW9546 is a 4-channel bidirectional transfer switch used for I^{2}C bus that supports standard mode (100kHz) and fast mode (400kHz). The AW9546 has I^{2}C control function and uses a single 8-bit control register, in which each bit controls the enable and disable of the corresponding switch channel for I^{2}C data flow.

The connections of the I^{2}C data path are controlled by the same I^{2}C master device that is switched to communicate with multiple I^{2}C slaves. After the successful acknowledgment of the slave address (hardware selectable by A0, A1 and A2 pins), a single 8-bit control register is written to or read from to determine the selected channels.

AW9546 can also be used for voltage conversion of the I^{2}C bus, allowing 1.8V, 2.5V or 3.3V devices to communicate with 5V devices. In addition, if the communication on the I^{2}C bus enters the fault state, the AW9546 can be resumed to normal operation through the RESETN pin or by a power-on reset which results from cycling power to the device.

RESETN Input

The RESETN input is an active-low signal that may be used to recover from a bus-fault condition. When this signal is asserted low for a minimum of $t_{W(rst)L}$, the AW9546 resets its registers and I^{2}C state machine and deselects all channels. The RESETN input must be connected to V_{CC} through a pull-up resistor.

Power On Reset

When power is applied to V_{CC}, an internal power-on reset circuit holds the AW9546 in a reset condition until V_{CC} has reached V_{PORR}. At that time, the reset condition is released, and the AW9546 registers and I^{2}C/SMBus state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. After that, V_{CC} must be lowered to below V_{PORF} to reset the device .

Device Address

The AW9546 features 3 hardware address pins (A0, A1 and A2) to allow the user to program the device's I^{2}C address by pulling each pin to either V_{CC} or GND to signify the bit value in the address. This allows up to eight AW9546 devices to be on the same bus without address conflicts. The voltage on the pins must not change while the device is powered up in order to prevent possible I^{2}C glitches as a result of the device address changing during a transmission. All of the pins must be tied either to V_{CC} or GND and cannot be left floating.

The permitted I^{2}C addresses are 0x70 (7-bit) through 0x77 (7-bit). The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

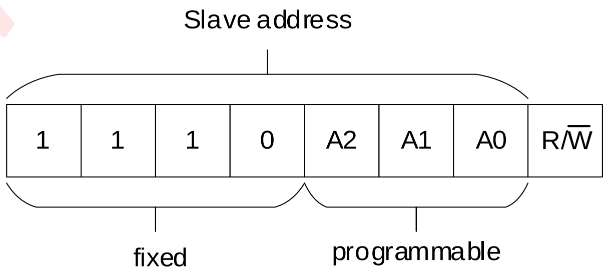


Figure 9 AW9546 Device Address

Control Register

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the AW9546 (see figure 10). This register can be written and read via the I^{2}C bus. Each bit in the command byte corresponds to a SCn/SDn channel and a high (or 1) selects this channel. Multiple SCn/SDn channels may be selected at the same time. When a channel is selected, the channel becomes active after a stop condition has been placed on the I²C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition always must occur immediately after the acknowledge cycle. If multiple bytes are received by the AW9546, it saves the last byte received.

Channel Selection Bits (Read/Write)

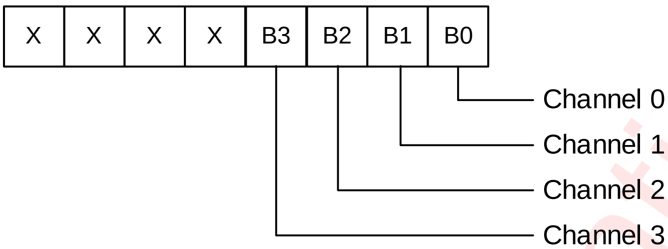


Figure 10 AW9546TSR Control Register

Table 1 shows the AW9546 command byte definition.

Table 1 AW9546 Command Byte Definition

Control register bits								Command
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
x	x	x	x	x	x	x	0	Channel 0 disabled
x	x	x	x	x	x	x	1	Channel 0 enabled
x	x	x	x	x	x	0	x	Channel 1 disabled
x	x	x	x	x	x	1	x	Channel 1 enabled
x	x	x	x	x	0	x	x	Channel 2 disabled
x	x	x	x	x	1	x	x	Channel 2 enabled
x	x	x	x	0	x	x	x	Channel 3 disabled
x	x	x	x	1	x	x	x	Channel 3 enabled
0	0	0	0	0	0	0	0	No channel selected, power-up/reset default state

NOTE: Multiple channels can be enabled at the same time. Example: B3=1, B2=1, B1=0, B0=0, means that channels 1 and 0 are disabled and channels 3 and 2 are enabled. Care should be taken not to exceed the maximum bus capacitance. Default condition is all zeroes.

I²C Interface

The AW9546 has a standard bidirectional I²C interface that is controlled by a master device in order to be configured or read the status of this device. Each slave on the I²C bus has a specific device address to differentiate between other slave devices that are on the same I²C bus. Many slave devices require configuration upon startup to set the behavior of the device. This is typically done when the master accesses internal register maps of the slave, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read.

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. The size of the pull-up resistor is determined by the amount of capacitance on the I²C lines. Data transfer may be initiated only when the bus is not busy and a bus is considered idle if both SDA and SCL lines are high after a STOP condition.

Data Validation

When SCL is high level, SDA level must be stable. SDA can be changed only when SCL is low level.

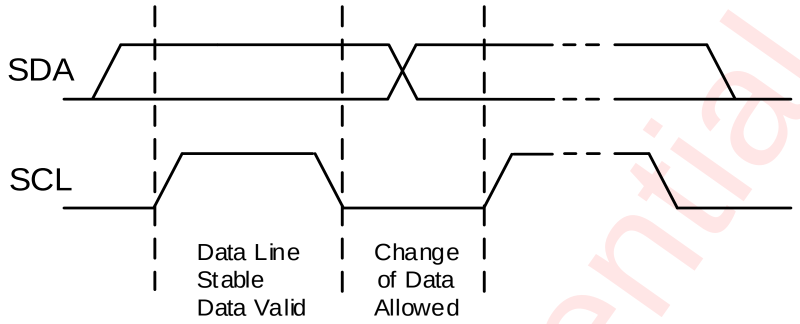


Figure 11 Data Validation Diagram

I²C Start/Stop

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

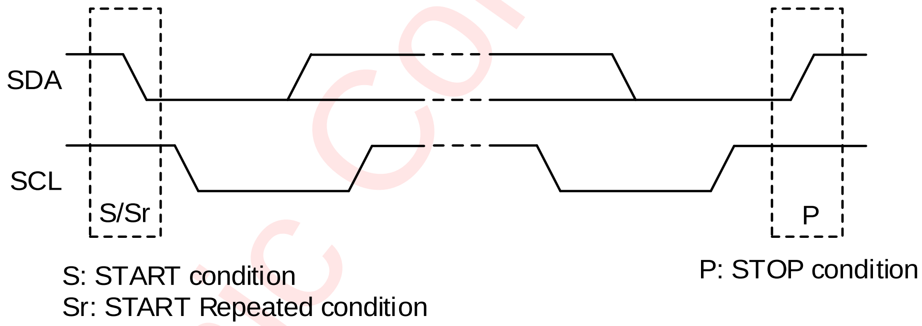


Figure 12 I²C Start/Stop Condition Timing

Acknowledge(ACK)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is sent and I²C stop is not sent by master, slave device sends the next data. If ACK is not sent by master, slave device stops to send data and waits for I²C stop.

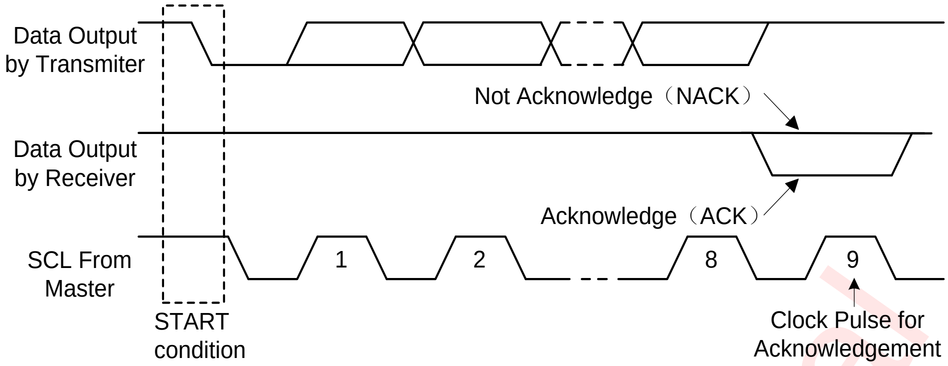


Figure 13 I²C ACK Timing

Bus Transactions

Data must be sent to and received from the slave devices, and this is accomplished by reading from or writing to registers in the slave device.

Registers are locations in the memory of the slave which contain information, whether it be the configuration information or some sampled data to send back to the master. The master must write information to these registers in order to instruct the slave device to perform a task.

While it is common to have registers in I²C slaves, note that not all slave devices have registers. Some devices are simple and contain only one register, which may be written to directly by sending the register data immediately after the slave address, instead of addressing a register. The AW9546 is example of a single-register device, which is controlled via I²C commands. Since it has 1 bit to enable or disable a channel, there is only one register needed, and the master merely writes the register data after the slave address, skipping the register number.

Writes

To write on the I²C bus, the master sends a START condition on the bus with the address of the slave, as well as the last bit (the R/W bit) set to 0, which signifies a write. The slave acknowledges, letting the master know it is ready. After this, the master starts sending the control register data to the slave until the master has sent all the data necessary (which is sometimes only a single byte), and the master terminates the transmission with a STOP condition.

There is no limit to the number of bytes sent, but the last byte sent is what is in the register.

Figure 14 shows an example of AW9546 writing a single byte to a slave register.

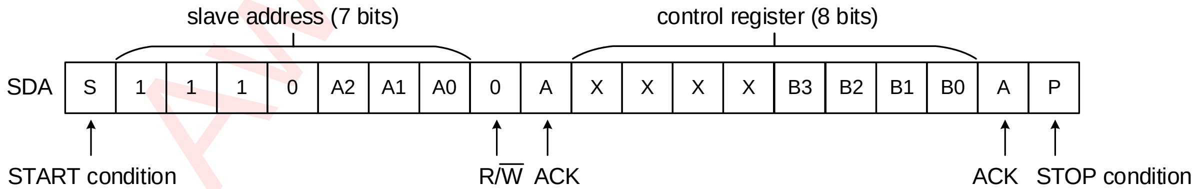


Figure 14 AW9546 Write To Control Register

Reads

Reading from a slave is very similar to writing, but the master sends a START condition, followed by the slave address with the R/W bit set to 1 (signifying a read). The slave acknowledges the read request, and the master releases the SDA bus but continues supplying the clock to the slave. During this part of the transaction, the master becomes the master-receiver, and the slave becomes the slave-transmitter.

The master continues to send out the clock pulses, but releases the SDA line so that the slave can transmit data. At the end of every byte of data, the master sends an ACK to the slave, letting the slave know that it is ready for more data. Once the master has received the number of bytes it is expecting, it sends a NACK, signaling to the slave to halt communications and release the bus. The master follows this up with a STOP condition.

Figure 15 shows an example of AW9546 reading a single byte from a slave register.

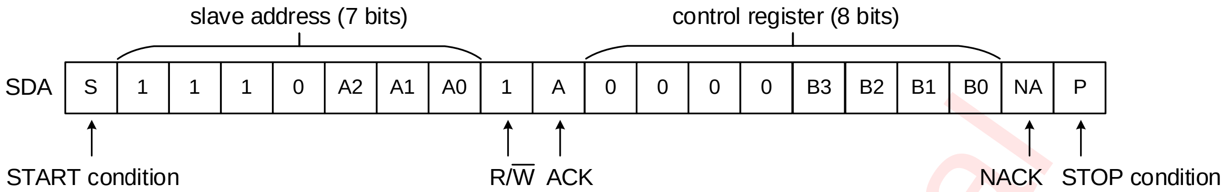


Figure 15 AW9546 Read From Control Register

Application Information

Applications of the AW9546 contain an I²C (or SMBus) master device and up to four I²C slave devices. The downstream channels are ideally used to resolve I²C slave address conflicts. For example, if four identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0-3. When the temperature at a specific location needs to be read, the appropriate channel can be enabled and all other channels switched off, the data can be retrieved, and the I²C master can move on and read the next channel.

In an application where the I²C bus contains many additional slave devices that do not result in I²C slave address conflicts, these slave devices can be connected to any desired channel to distribute the total bus capacitance across multiple channels. If multiple switches are enabled simultaneously, additional design requirements must be considered (see the Design Requirements section and Pull-up Resistor Calculation section). Figure 16 shows an application in which the AW9546 can be used.

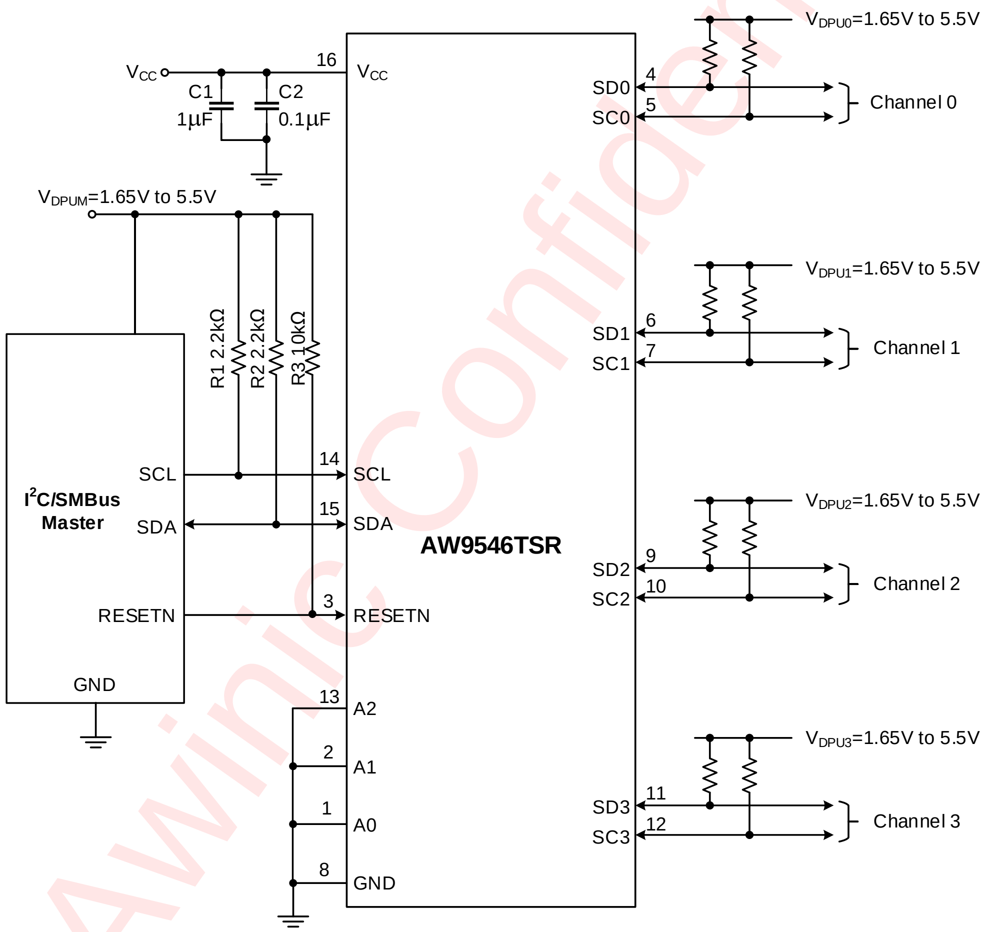


Figure 16 AW9546TSR Application Circuit

Design Requirements

A typical application of the AW9546 contains one or more data pull-up voltages, V_{DPUX}, one for the master device (V_{DPUM}) , and one for each of the selectable slave channels (V_{DPU0}~V_{DPU3}). In the event where the master device and all slave devices operate at the same voltage, then V_{DPUM}=V_{DPUX}=V_{CC}. In an application where voltage translation is necessary, additional design requirements must be considered to determine an appropriate V_{CC} voltage.

The A0, A1 and A2 pins are hardware selectable to control the slave address of the AW9546. These pins may be tied directly to GND or V_{CC} in the application.

If multiple slave channels are activated simultaneously in the application, then the total I_{OL} from SCL/SDA to GND on the master side is the sum of the currents through all pull-up resistors R_p.

The pass-gate transistors of the AW9546 are constructed such that the V_{CC} voltage can be used to limit the maximum voltage that is passed from one I²C bus to another.

Figure 17 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the Electrical Characteristics table). In order for the AW9546 to act as a voltage translator, the $V_{O(SW)}$ voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5V and the downstream buses are 3.3V and 2.7V, $V_{O(SW)}$ must be equal to or below 2.7V to effectively clamp the downstream bus voltages. As shown in figure 17, $V_{O(SW)}$(max) is 2.7V when the AW9546 supply voltage is 4V or lower, so the AW9546 supply voltage could be set to 3.3V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see figure 16).

Pull-up Resistor Calculation

Once all the slaves are assigned to the appropriate slave channels and bus voltages are identified. The pull-up resistors, R_p, for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of V_{DPUX}, V_{OL}(max), and I_{OL} as shown in Equation 1.

$$R_{p(min)}=\frac{V_{DPUX}-V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300ns for fast-mode operation, f_{SCL} =400kHz) and bus capacitance, C_b as shown in Equation 2.

$$R_{p(max)}=\frac{t_r}{0.8473\times C_b} \quad (2)$$

The maximum bus capacitance for an I²C bus must not exceed 400pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the AW9546, $C_{io(off)}$, the capacitance of wires, connections and traces, and the capacitance of additional slaves on the bus. If multiple channels are activated simultaneously, each of the slaves on all channels contribute to total bus capacitance.

Application Curves

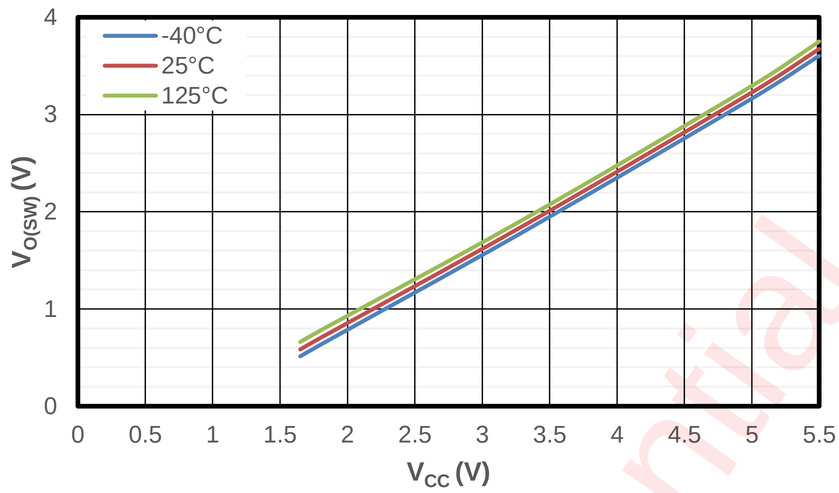
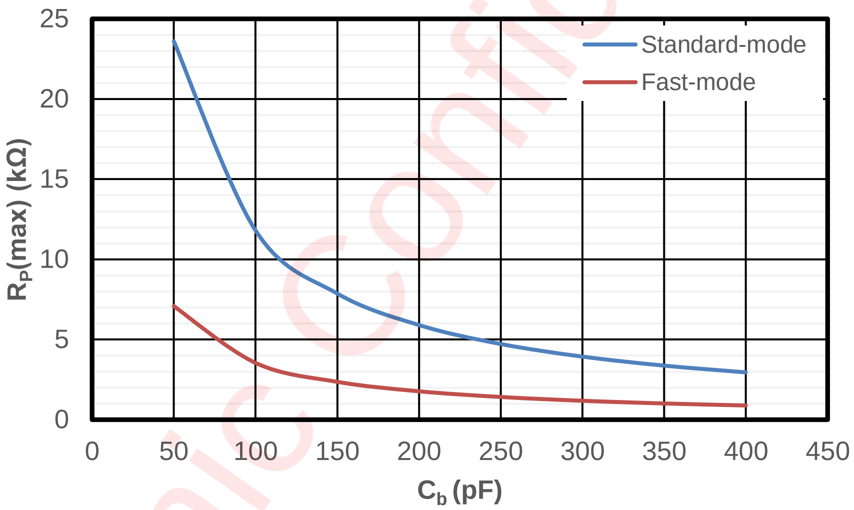


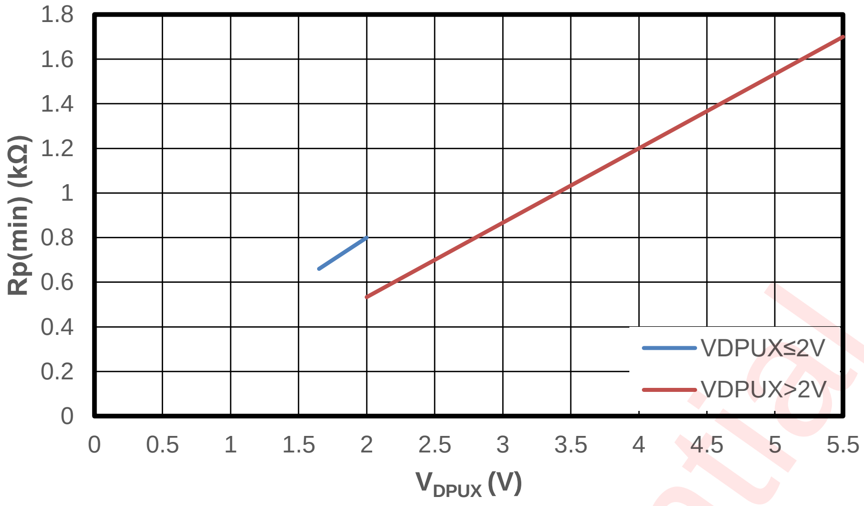
Figure 17 Pass-Gate Voltage ($V_{O(SW)}$) vs Supply Voltage (V_{CC})



Standard-mode (f_{SCL}=100kHz, t_r=1μs)

Fast-mode (f_{SCL}=400kHz, t_r=300ns)

Figure 18 Maximum Pull-Up Resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL}=0.2*V_{DPUX}, I_{OL}=2mA when V_{DPUX}≤2V

V_{OL}=0.4V, I_{OL}=3mA when V_{DPUX}>2V

Figure 19 Minimum Pull-up Resistance (Rp(min)) vs Pull-up Reference Voltage (V_{DPUX})

Power Supply Recommendations

The operating power-supply voltage range of the AW9546 is 1.65V to 5.5V applied at the V_{CC} pin. When the AW9546 is powered on for the first time or anytime the device must be reset by cycling the power supply, the power-on reset requirements must be followed to ensure the I²C bus logic is initialized properly.

Power-On Reset Requirements

In the event of a glitch (data output or input or even power) or data corruption, the AW9546 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.
A power-on reset is shown in the following figure.

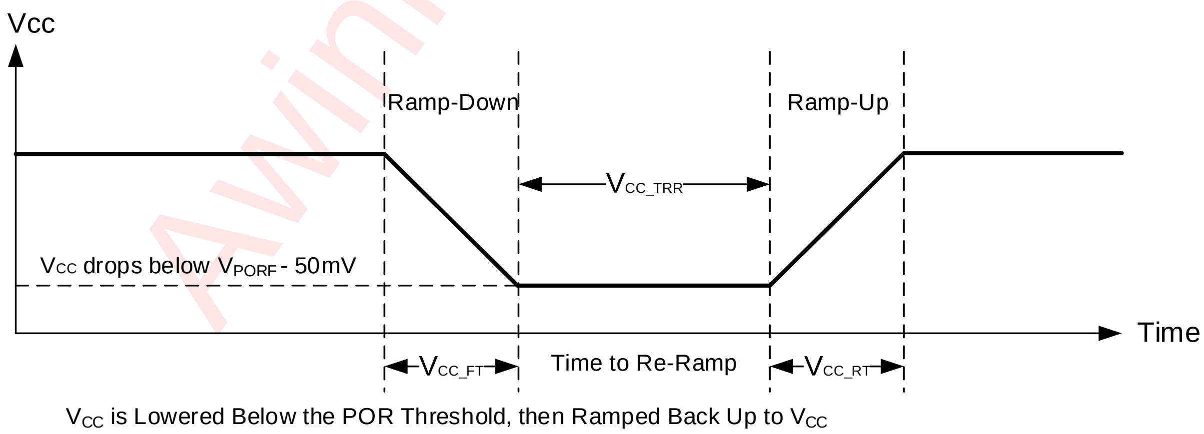


Figure 20 Power-On Reset Waveform

The following table specifies the performance of the power-on reset feature for AW9546 for both types of power-on reset.

Table 2 Recommended Supply Sequencing and Ramp Rates

Parameters			Min.	Max.	Unit
V_{CC_FT}	Fall rate	See Figure 20	1	100	ms
V_{CC_RT}	Rise rate	See Figure 20	0.1	100	ms
V_{CC_TRR}	Time to re-ramp (V_{CC} drops to V_{PORF}(min) – 50 mV or when V_{CC} drops to GND)	See Figure 20	40		μs
V_{CC_GH}	Level that V_{CC} can glitch down to, but not cause a functional disruption when V_{CC_GW}=1μs	See Figure 21		1.2	V
V_{CC_GW}	Glitch width that does not cause a functional disruption when V_{CC_GH}=0.5×V_{CC}	See Figure 21		10	μs

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. figure 21 and table 2 provide more information on how to measure these specifications.

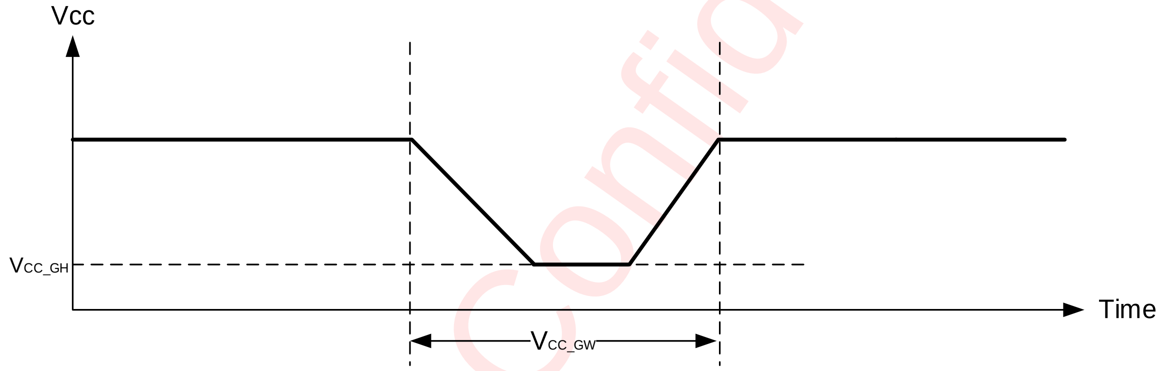


Figure 21 Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 22 and table 2 provide more details on this specification.

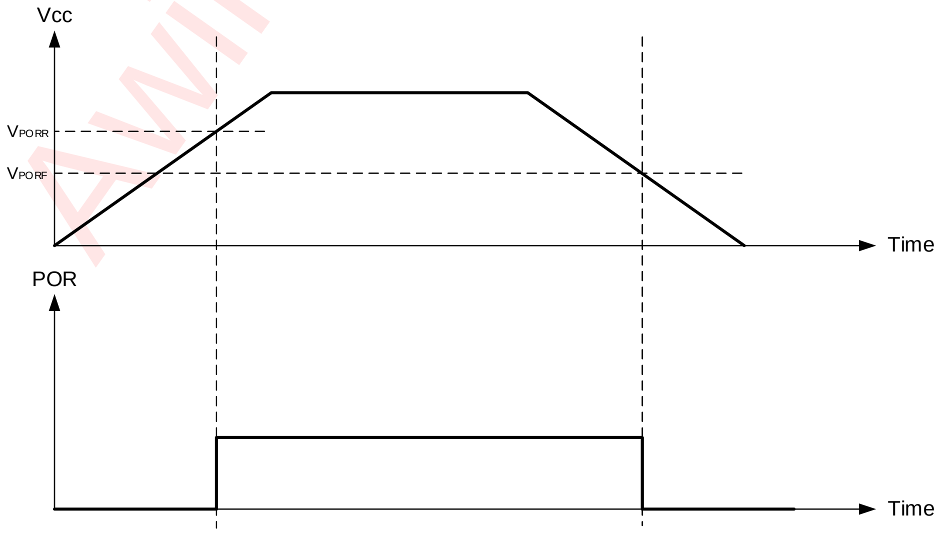


Figure 22 V_{POR}

PCB Layout Consideration

To obtain the good thermal performance, PCB layout should be considered carefully. Here are some guidelines:

1. The C1, C2 should be placed as close to the chip as possible.
2. To reduce the total I²C bus capacitance added by PCB parasitics, data lines (SCn and SDn) must be as short as possible and the widths of the traces must also be minimized.
3. In an application where voltage translation is not required, all V_{DPUX} voltages and V_{CC} could be at the same potential and a single copper plane could connect all of pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required, V_{DPUM}, V_{DPU0}~V_{DPU3}, may all be on the same layer of the board with split planes to isolate different voltage potentials.

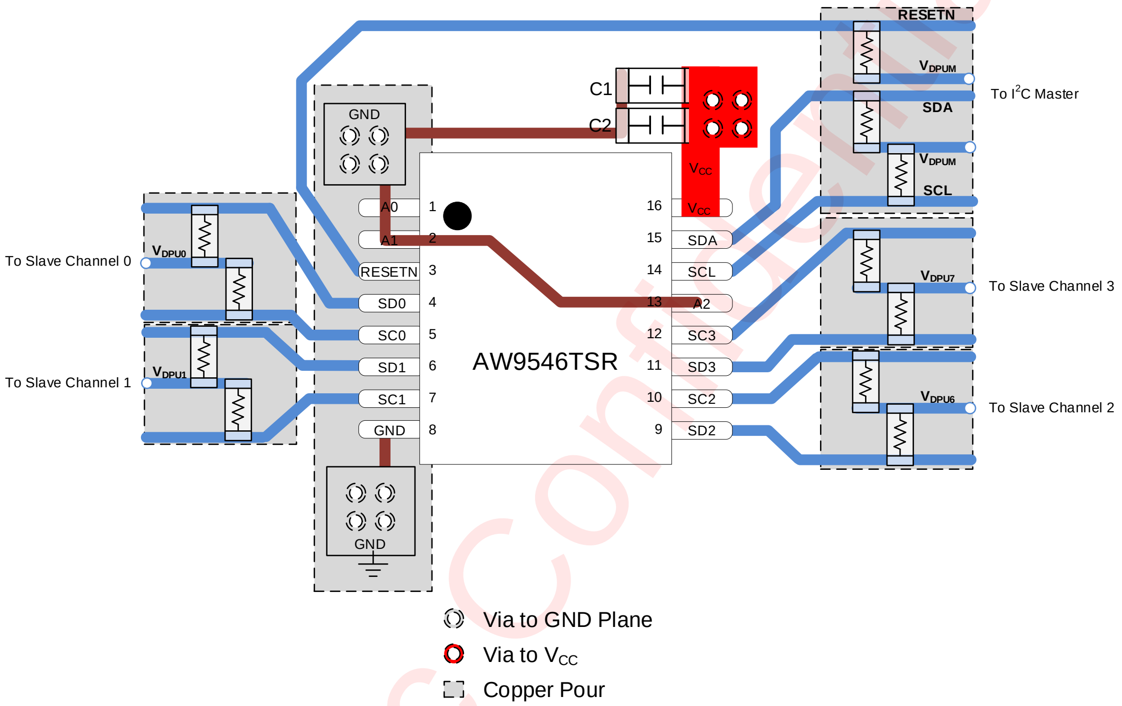
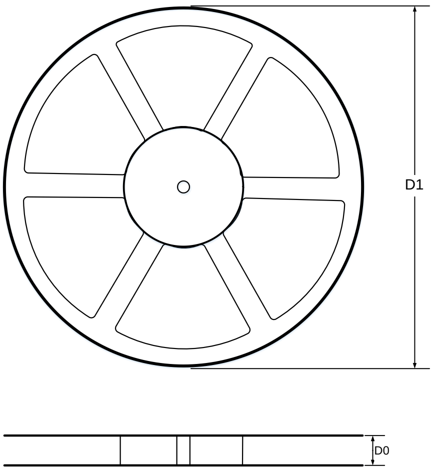


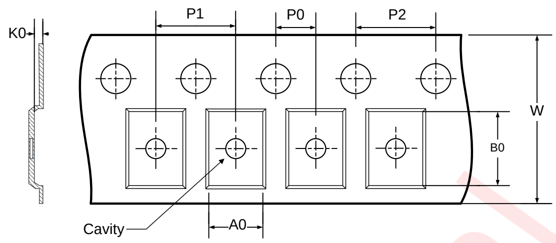
Figure 23 AW9546TSR Layout Example

Tape And Reel Information

REEL DIMENSIONS

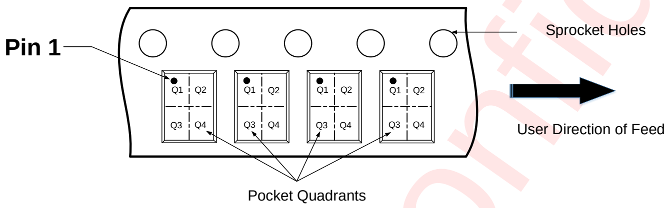


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



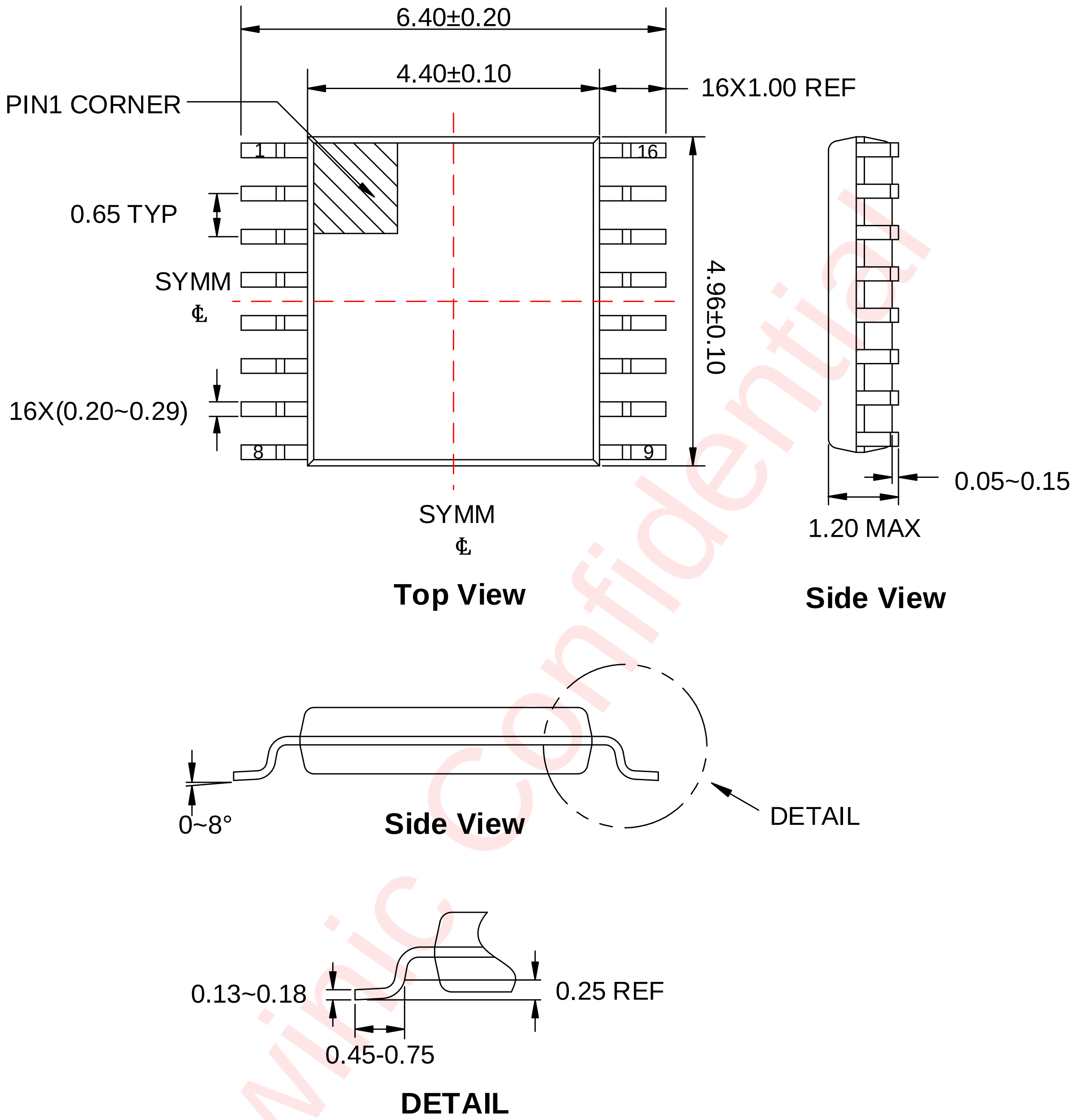
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330.0	12.40	6.80	5.40	1.30	2.00	8.00	4.00	12.00	Q1

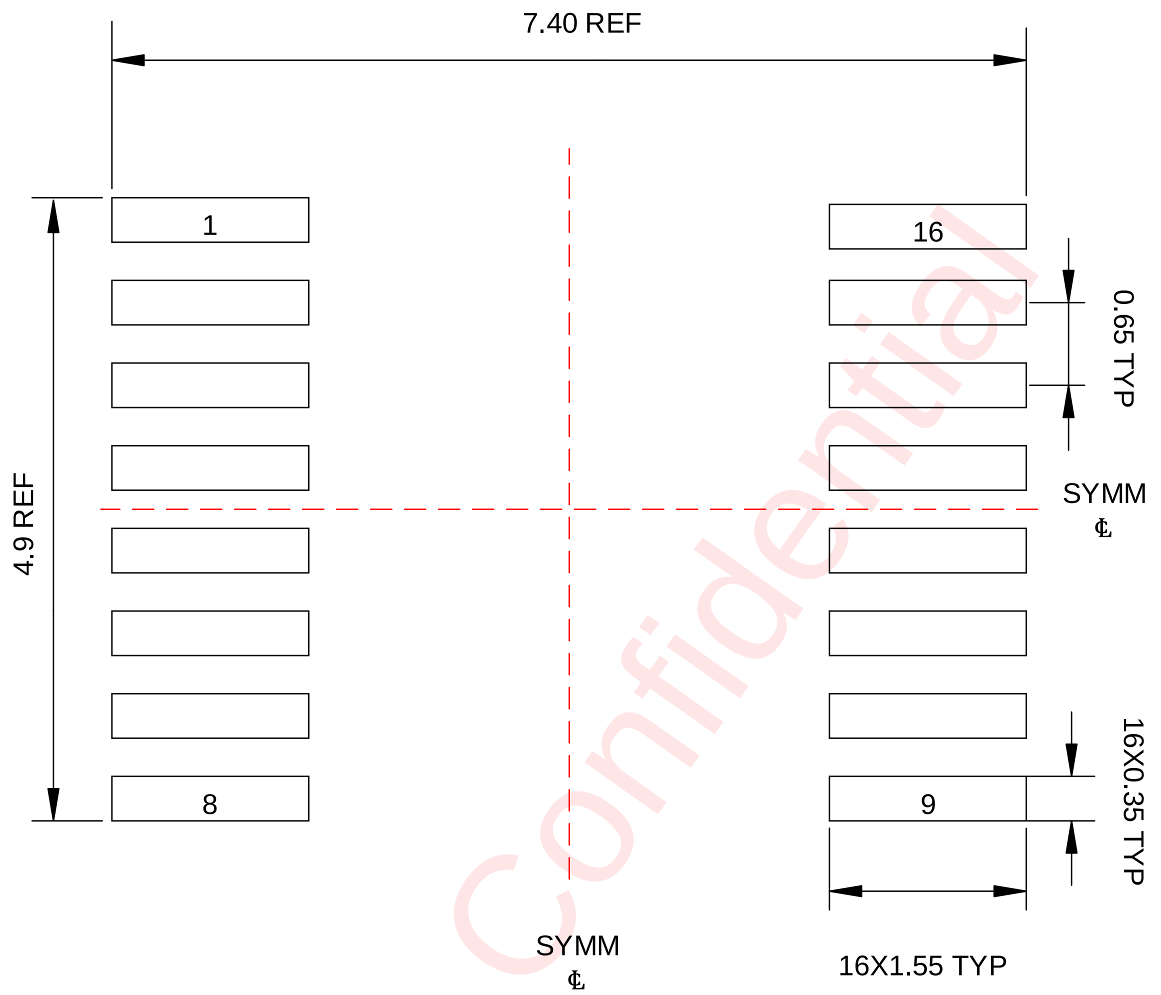
All dimensions are nominal

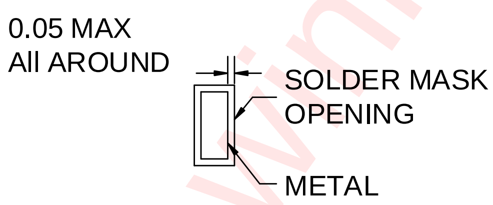
Package Description



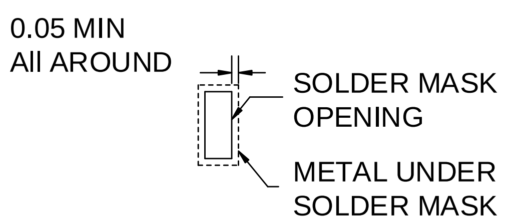
Unit： mm

Land Pattern Data





NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit： mm

Revision History

Version	Date	Change Record
V1.0	Jul. 2024	Officially released

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