

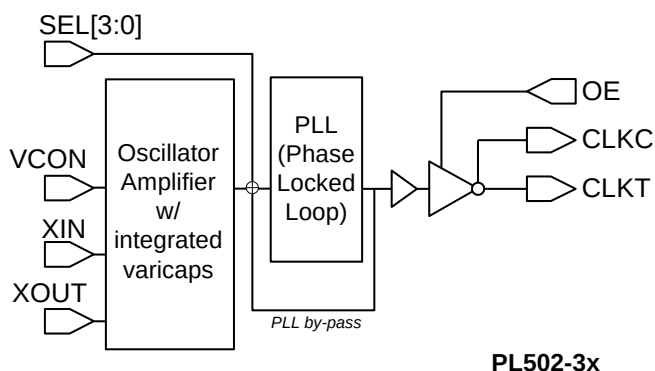
### FEATURES

- Selectable 750kHz to 800MHz range
- Low phase noise output (@ 10kHz frequency offset, -142dBc/Hz for 19.44MHz, -125dBc/Hz for 155.52MHz, -115dBc/Hz for 622.08MHz)
- LVCMOS (PL502-37), LVPECL (PL502-35 and PL502-38) or LVDS (PL502-39) output
- 12MHz to 25MHz crystal input
- No external load capacitor or varicap required.
- Output Enable selector
- Wide pull range ( $\pm 200$  ppm)
- Selectable /16 to x32 frequency divider/multiplier
- 3.3V operation
- Available in 16-Pin TSSOP or 16-pin 3x3mm QFN GREEN/RoHS compliant packages

### DESCRIPTION

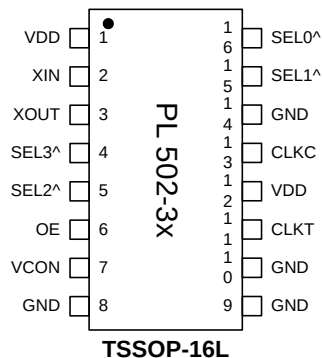
The PL502-35 (LVPECL with inverted OE), PL502-37 (LVCMOS), PL502-38 (LVPECL), and PL502-39 (LVDS) are high performance and low phase noise VCXO IC chips. They provide phase noise performance as low as -125dBc at 10kHz offset (at 155MHz), by multiplying the input crystal frequency up to 32x. The wide pull range ( $\pm 200$  ppm) and very low jitter make them ideal for a wide range of applications, including SONET/SDH and FEC. They accept fundamental parallel resonant mode crystals from 12MHz to 25MHz.

### BLOCK DIAGRAM



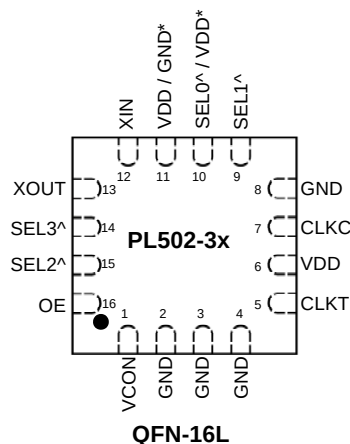
### PIN CONFIGURATION

(Top View)



^: Internal pull-up

\*: On 3x3 package, PL502-35/-38 do not have SEL0 available: Pin 10 is VDD, pin 11 is GND. However, PL502-37/-39 have SEL0 (pin 10), and pin11 is VDD. See pin assignment table for details.



### OUTPUT ENABLE LOGICAL LEVELS

| Part #                           | OE          | State          |
|----------------------------------|-------------|----------------|
| PL502-38                         | 0 (Default) | Output enabled |
|                                  | 1           | Tri-state      |
| PL502-35<br>PL502-37<br>PL502-39 | 0           | Tri-state      |
|                                  | 1 (Default) | Output enabled |

OE input: Logical states defined by LVPECL levels for PL502-38  
Logical states defined by LVCMOS levels for PL502-37/-39



# PL502-35/-37/-38/-39

## 750kHz – 800MHz Low Phase Noise Multiplier VCXO

Universal Low Phase Noise ICs

### FREQUENCY SELECTION TABLE

| SEL3 | SEL2 | SEL1 | SEL0 | Selected Multiplier |
|------|------|------|------|---------------------|
| 0    | 0    | 1    | 1    | Fin x 32            |
| 0    | 1    | 1    | 0    | Fin / 8             |
| 0    | 1    | 1    | 1    | Fin x 2             |
| 1    | 0    | 0    | 1    | Fin / 2             |
| 1    | 0    | 1    | 0    | Fin / 16            |
| 1    | 0    | 1    | 1    | Fin x 4             |
| 1    | 1    | 0    | 0    | Fin / 4             |
| 1    | 1    | 0    | 1    | Fin x 8             |
| 1    | 1    | 1    | 0    | Fin x 16            |
| 1    | 1    | 1    | 1    | No multiplication   |

**Note:** SEL0 is not available (always "1") for PL502-35 and PL502-38 in 3x3mm package

### PIN DESCRIPTIONS PL502-35 and PL502-38 (see next page for PL502-37/-39)

| Name | TSSOP<br>Pin number | 3x3mm QFN<br>Pin number | Type | Description                                                                                                           |
|------|---------------------|-------------------------|------|-----------------------------------------------------------------------------------------------------------------------|
| XIN  | 2                   | 12                      | I    | Crystal input (See Crystal Specification on page 4)                                                                   |
| XOUT | 3                   | 13                      | I    | Crystal output (See Crystal Specification on page 4)                                                                  |
| OE   | 6                   | 16                      | I    | Output enable pin (See OE logic state table on page 1)                                                                |
| VCON | 7                   | 1                       | I    | Voltage Control input                                                                                                 |
| GND  | 8,9,10,14           | 2,3,4,8,11              | P    | Ground connection                                                                                                     |
| CLKT | 11                  | 5                       | O    | LVPECL True output                                                                                                    |
| CLKC | 13                  | 7                       | O    | LVPECL Complementary output                                                                                           |
| SEL0 | 16                  | Not available           | I    | Multiplier selector pins. These pins have an internal pull-up that will default SEL to '1' when not connected to GND. |
| SEL1 | 15                  | 9                       | I    |                                                                                                                       |
| SEL2 | 5                   | 15                      | I    |                                                                                                                       |
| SEL3 | 4                   | 14                      | I    |                                                                                                                       |
| VDD  | 1, 12               | 6,10                    | P    | +3.3V power supply.                                                                                                   |



# PL502-35/-37/-38/-39

## 750kHz – 800MHz Low Phase Noise Multiplier VCXO

Universal Low Phase Noise ICs

### PIN DESCRIPTIONS PL502-37/-39 (see previous page for PL502-35/-38)

| Name | TSSOP<br>Pin number | 3x3mm QFN<br>Pin number | Type | Description                                                                                                            |
|------|---------------------|-------------------------|------|------------------------------------------------------------------------------------------------------------------------|
| XIN  | 2                   | 12                      | I    | Crystal input. See Crystal Specification on page 4.                                                                    |
| XOUT | 3                   | 13                      | I    | Crystal output. See Crystal Specification on page 4.                                                                   |
| OE   | 6                   | 16                      | I    | Output enable pin (see OE logic state table on page 1).                                                                |
| VCON | 7                   | 1                       | I    | Voltage Control input.                                                                                                 |
| GND  | 8,9,10,14           | 2,3,4,8                 | P    | Ground.                                                                                                                |
| CLKT | 11                  | 5                       | O    | LVDS True output for PL502-39<br>No Connect for PL502-37                                                               |
| CLKC | 13                  | 7                       | O    | LVDS Complementary output for PL502-39<br>LVCMOS out for PL502-37                                                      |
| SEL0 | 16                  | 10                      | I    | Multiplier selector pins. These pins have an internal pull-up that will default SELx to '1' when not connected to GND. |
| SEL1 | 15                  | 9                       | I    |                                                                                                                        |
| SEL2 | 5                   | 15                      | I    |                                                                                                                        |
| SEL3 | 4                   | 14                      | I    |                                                                                                                        |
| VDD  | 1, 12               | 6,11                    | P    | +3.3V power supply.                                                                                                    |

## ELECTRICAL SPECIFICATIONS

### 1. Absolute Maximum Ratings

| PARAMETERS                        | SYMBOL   | MIN. | MAX.         | UNITS |
|-----------------------------------|----------|------|--------------|-------|
| Supply Voltage                    | $V_{DD}$ |      | 4.6          | V     |
| Input Voltage, dc                 | $V_I$    | -0.5 | $V_{DD}+0.5$ | V     |
| Output Voltage, dc                | $V_O$    | -0.5 | $V_{DD}+0.5$ | V     |
| Storage Temperature               | $T_S$    | -65  | 150          | °C    |
| Ambient Operating Temperature*    | $T_A$    | -40  | 85           | °C    |
| Junction Temperature              | $T_J$    |      | 125          | °C    |
| Lead Temperature (soldering, 10s) |          |      | 260          | °C    |
| ESD Protection, Human Body Model  |          |      | 2.5          | kV    |

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

\* **Note:** Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

## 750kHz – 800MHz Low Phase Noise Multiplier VCXO

Universal Low Phase Noise ICs

### 2. Crystal Specifications

| PARAMETERS                  | SYMBOL          | CONDITIONS                | MIN. | TYP. | MAX. | UNITS    |
|-----------------------------|-----------------|---------------------------|------|------|------|----------|
| Crystal Resonator Frequency | $F_{XIN}$       | Parallel Fundamental Mode | 12   |      | 25   | MHz      |
| Crystal Loading Rating      | $C_{L(xtal)}$   | At $V_{CON} = 1.65V$      |      | 9.5  |      | pF       |
| Crystal Pullability         | $C_0/C_1(xtal)$ | AT cut                    |      |      | 250  | -        |
| Recommended ESR             | $R_E$           | AT cut                    |      |      | 30   | $\Omega$ |

**Note:** Crystal Loading rating: 9.5pF is the loading the crystal sees from the VCXO chip at  $V_{CON} = 1.65V$ . It is assumed that the crystal will be at nominal frequency at this load. If the crystal requires more load to be at nominal frequency, the additional load must be added externally. This however may reduce the pull range.

### 3. Voltage Control Crystal Oscillator

| PARAMETERS                    | SYMBOL        | CONDITIONS                                                                      | MIN.      | TYP. | MAX. | UNITS      |
|-------------------------------|---------------|---------------------------------------------------------------------------------|-----------|------|------|------------|
| VCXO Stabilization Time *     | $T_{VCXOSTB}$ | From power valid                                                                |           |      | 10   | ms         |
| VCXO Tuning Range             |               | $F_{XIN} = 12 - 25MHz$ ;<br>$XTAL C_0/C_1 < 250$<br>$0V \leq V_{CON} \leq 3.3V$ |           | 500  |      | ppm        |
| CLK output pullability        |               | $V_{CON} = 1.65V, \pm 1.65V$                                                    | $\pm 200$ |      |      | ppm        |
| VCXO Tuning Characteristic    |               |                                                                                 |           | 150  |      | ppm/V      |
| Pull range linearity          |               |                                                                                 |           |      | 10   | %          |
| $V_{CON}$ pin input impedance |               |                                                                                 | 2000      |      |      | k $\Omega$ |
| $V_{CON}$ modulation BW       |               | $0V \leq V_{CON} \leq 3.3V, -3dB$                                               | 10        |      |      | kHz        |

**Note:** Parameters denoted with an asterisk (\*) represent nominal characterization data and are not production tested to any specific limits.

### 4. General Electrical Specifications

| PARAMETERS                                    | SYMBOL   | CONDITIONS                 | MIN.                       | TYP.     | MAX.      | UNITS |
|-----------------------------------------------|----------|----------------------------|----------------------------|----------|-----------|-------|
| Supply Current, Dynamic (with Loaded Outputs) | $I_{DD}$ | LVPECL/LVDS/LVCMOS         | $F_{OUT} < 24MHz$          |          | 60/28/15  | mA    |
|                                               |          |                            | $24MHz < F_{OUT} < 96MHz$  |          | 65/45/30  |       |
|                                               |          |                            | $96MHz < F_{OUT} < 800MHz$ |          | 100/80/40 |       |
| Operating Voltage                             | $V_{DD}$ |                            | 2.97                       |          | 3.63      | V     |
| Output Clock Duty Cycle                       |          | @ 50% $V_{DD}$ (LVCMOS)    | 45                         | 50       | 55        | %     |
|                                               |          | @ 1.25V (LVDS)             | 45                         | 50       | 55        |       |
|                                               |          | @ $V_{DD} - 1.3V$ (LVPECL) | 45                         | 50       | 55        |       |
| Short Circuit Current                         |          |                            |                            | $\pm 50$ |           | mA    |

## 750kHz – 800MHz Low Phase Noise Multiplier VCXO

Universal Low Phase Noise ICs

### 5. Jitter Specifications

| PARAMETERS                 | CONDITIONS                                                               | FREQUENCY | MIN. | TYP. | MAX. | UNITS |
|----------------------------|--------------------------------------------------------------------------|-----------|------|------|------|-------|
| Period jitter RMS          | With capacitive decoupling between $V_{DD}$ and GND. Over 10,000 cycles. | 19.44MHz  |      | 2.2  |      | ps    |
|                            |                                                                          | 77.76MHz  |      | 4.5  |      |       |
|                            |                                                                          | 155.52MHz |      | 4.5  |      |       |
|                            |                                                                          | 622.08MHz |      | 5.0  |      |       |
| Period jitter Peak-to-Peak | With capacitive decoupling between $V_{DD}$ and GND. Over 10,000 cycles. | 19.44MHz  |      | 17   |      | ps    |
|                            |                                                                          | 77.76MHz  |      | 25   |      |       |
|                            |                                                                          | 155.52MHz |      | 27   |      |       |
|                            |                                                                          | 622.08MHz |      | 35   |      |       |
| Integrated jitter RMS      | Integrated 12kHz to 20MHz                                                | 155.52MHz |      | 2.5  | 4    | ps    |
|                            |                                                                          | 622.08MHz |      | 2.5  | 4    |       |

### 6. Phase Noise Specifications

| PARAMETERS                                | FREQUENCY | @10Hz | @100Hz | @1kHz | @10kHz | @100kHz | UNITS  |
|-------------------------------------------|-----------|-------|--------|-------|--------|---------|--------|
| Phase Noise relative to carrier (typical) | 19.44MHz  | -80   | -108   | -132  | -142   | -150    | dBc/Hz |
|                                           | 77.76MHz  | -72   | -103   | -122  | -130   | -125    |        |
|                                           | 155.52MHz | -65   | -95    | -120  | -125   | -121    |        |
|                                           | 622.08MHz | -55   | -85    | -109  | -115   | -110    |        |

Note: Phase Noise measured at  $V_{CON} = 0V$

### 7. LVCMOS Electrical Characteristics

| PARAMETERS                  | SYMBOL   | CONDITIONS                                 | MIN. | TYP. | MAX. | UNITS |
|-----------------------------|----------|--------------------------------------------|------|------|------|-------|
| Output drive current        | $I_{OH}$ | $V_{OH} = V_{DD} - 0.4V$ , $V_{DD} = 3.3V$ | 10   |      |      | mA    |
|                             | $I_{OL}$ | $V_{OL} = 0.4V$ , $V_{DD} = 3.3V$          | 10   |      |      | mA    |
| Output Clock Rise/Fall Time |          | 0.3V ~ 3.0V with 15 pF load                |      | 2.4  |      | ns    |

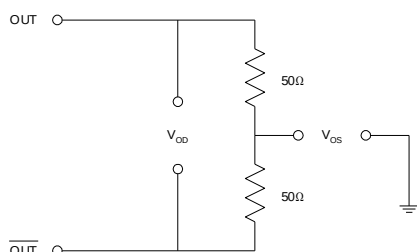
### 8. LVDS Electrical Characteristics

| PARAMETERS                   | SYMBOL          | CONDITIONS                                 | MIN.  | TYP.    | MAX.     | UNITS   |
|------------------------------|-----------------|--------------------------------------------|-------|---------|----------|---------|
| Output Differential Voltage  | $V_{OD}$        | $R_L = 100\Omega$<br>(see figure)          | 247   | 355     | 454      | mV      |
| $V_{DD}$ Magnitude Change    | $\Delta V_{OD}$ |                                            | -50   |         | 50       | mV      |
| Output High Voltage          | $V_{OH}$        |                                            |       | 1.4     | 1.6      | V       |
| Output Low Voltage           | $V_{OL}$        |                                            | 0.9   | 1.1     |          | V       |
| Offset Voltage               | $V_{OS}$        |                                            | 1.125 | 1.2     | 1.375    | V       |
| Offset Magnitude Change      | $\Delta V_{OS}$ |                                            | 0     | 3       | 25       | mV      |
| Power-off Leakage            | $I_{OXD}$       | $V_{out} = V_{DD}$ or GND<br>$V_{DD} = 0V$ |       | $\pm 1$ | $\pm 10$ | $\mu A$ |
| Output Short Circuit Current | $I_{OSD}$       |                                            |       | -5.7    | -8       | mA      |

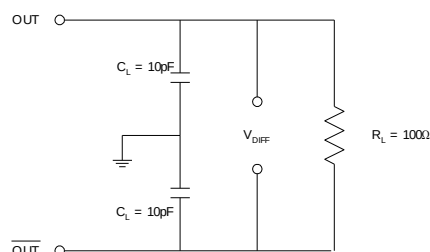
### 9. LVDS Switching Characteristics

| PARAMETERS                   | SYMBOL | CONDITIONS                                                | MIN. | TYP. | MAX. | UNITS |
|------------------------------|--------|-----------------------------------------------------------|------|------|------|-------|
| Differential Clock Rise Time | $t_r$  | $R_L = 100\Omega$<br>$C_L = 10\text{ pF}$<br>(see figure) | 0.2  | 0.7  | 1.0  | ns    |
| Differential Clock Fall Time | $t_f$  |                                                           | 0.2  | 0.7  | 1.0  | ns    |

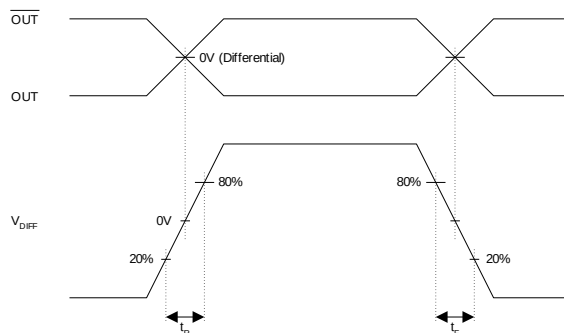
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transistion Time Waveform



## 750kHz – 800MHz Low Phase Noise Multiplier VCXO

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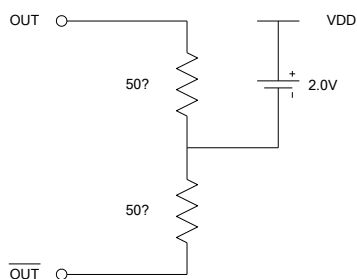
### 10. LVPECL Electrical Characteristics

| PARAMETERS          | SYMBOL   | CONDITIONS                                          | MIN.             | MAX.             | UNITS |
|---------------------|----------|-----------------------------------------------------|------------------|------------------|-------|
| Output High Voltage | $V_{OH}$ | $R_L = 50\Omega$ to $(V_{DD} - 2V)$<br>(see figure) | $V_{DD} - 1.025$ |                  | V     |
| Output Low Voltage  | $V_{OL}$ |                                                     |                  | $V_{DD} - 1.620$ | V     |

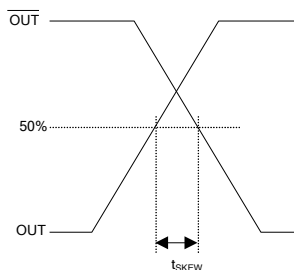
### 11. LVPECL Switching Characteristics

| PARAMETERS      | SYMBOL | CONDITIONS          | MIN. | TYP. | MAX. | UNITS |
|-----------------|--------|---------------------|------|------|------|-------|
| Clock Rise Time | $t_r$  | 20%~80% of Waveform |      | 0.6  | 1.5  | ns    |
| Clock Fall Time | $t_f$  |                     |      | 0.6  | 1.5  | ns    |

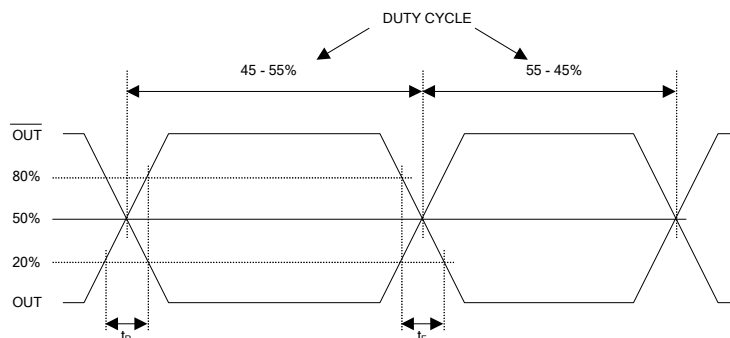
LVPECL Levels Test Circuit



LVPECL Output Skew



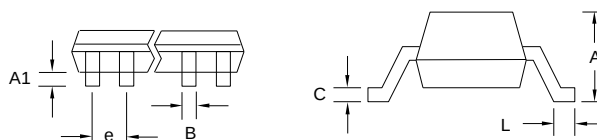
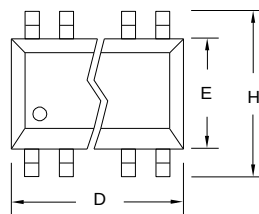
LVPECL Transition Time Waveform



### PACKAGE INFORMATION (GREEN PACKAGE COMPLIANT)

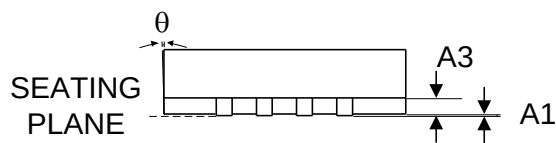
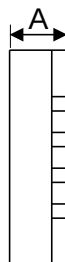
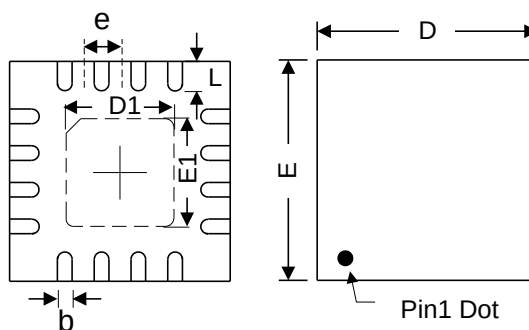
#### TSSOP-16L

| Symbol | Dimension in MM |      |
|--------|-----------------|------|
|        | Min.            | Max. |
| A      | -               | 1.20 |
| A1     | 0.05            | 0.15 |
| b      | 0.19            | 0.30 |
| C      | 0.09            | 0.20 |
| D      | 4.90            | 5.10 |
| E      | 4.30            | 4.50 |
| H      | 6.20            | 6.60 |
| L      | 0.45            | 0.75 |
| e      | 0.65 BSC        |      |



#### QFN-16L

| Symbol | Dimension (mm) |       |       |
|--------|----------------|-------|-------|
|        | Min            | Nom   | Max   |
| A      | 0.70           | 0.75  | 0.80  |
| A1     | 0.00           | -     | 0.05  |
| A3     | 0.203          |       |       |
| b      | 0.20           | 0.25  | 0.30  |
| D      | 2.95           | 3.00  | 3.05  |
| E      | 2.95           | 3.00  | 3.05  |
| D1     | 1.65           | 1.70  | 1.75  |
| E1     | 1.65           | 1.70  | 1.75  |
| L      | 0.250          | 0.300 | 0.350 |
| e      | 0.50BSC        |       |       |





### ORDERING INFORMATION

**For part ordering, please contact our Sales Department:**

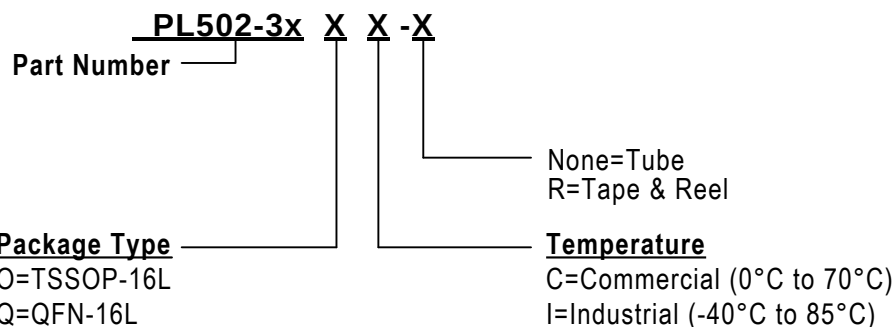
2180 Fortune Drive, San Jose, CA 95131, USA

Tel: (408) 944-0800 Fax: (408) 474-1000

#### PART NUMBER

The order number for this device is a combination of the following:

Part number, Package type, Operating temperature range, shipping method



| Part/Order Number* | Marking**              |                        | Package Option                    |
|--------------------|------------------------|------------------------|-----------------------------------|
|                    | Commercial             | Industrial             |                                   |
| PL502-35OC         | P502-35<br>OC<br>LLLLL | P502-35<br>OI<br>LLLLL | 8-pin TSSOP-16L – (Tube)          |
| PL502-35OC-R       |                        |                        | 8-pin TSSOP-16L – (Tape and Reel) |
| PL502-35QC-R       | P502<br>35<br>LLL      | P502<br>35I<br>LLL     | 16-pin QFN-16L - (Tape and Reel)  |
| PL502-37OC         | P502-37<br>OC<br>LLLLL | P502-37<br>OI<br>LLLLL | 8-pin TSSOP-16L – (Tube)          |
| PL502-37OC-R       |                        |                        | 8-pin TSSOP-16L – (Tape and Reel) |
| PL502-37QC-R       | P502<br>37<br>LLL      | P502<br>37I<br>LLL     | 16-pin QFN-16L - (Tape and Reel)  |
| PL502-38OC         | P502-38<br>OC<br>LLLLL | P502-38<br>OI<br>LLLLL | 8-pin TSSOP-16L – (Tube)          |
| PL502-38OC-R       |                        |                        | 8-pin TSSOP-16L – (Tape and Reel) |
| PL502-38QC-R       | P502<br>38<br>LLL      | P502<br>38I<br>LLL     | 16-pin QFN-16L - (Tape and Reel)  |
| PL502-39OC         | P502-39<br>OC<br>LLLLL | P502-39<br>OI<br>LLLLL | 8-pin TSSOP-16L – (Tube)          |
| PL502-39OC-R       |                        |                        | 8-pin TSSOP-16L – (Tape and Reel) |
| PL502-39QC-R       | P502<br>39<br>LLL      | P502<br>39I<br>LLL     | 16-pin QFN-16L - (Tape and Reel)  |

\*Note: For Industrial use "I" instead of "C" in the Part/Order number.

\*\*Note: "LLL" or "LLLLL" are designates lot number



## PL502-35/-37/-38/-39

### 750kHz – 800MHz Low Phase Noise Multiplier VCXO

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