

3.6A High Voltage H-Bridge DC Motor Driver

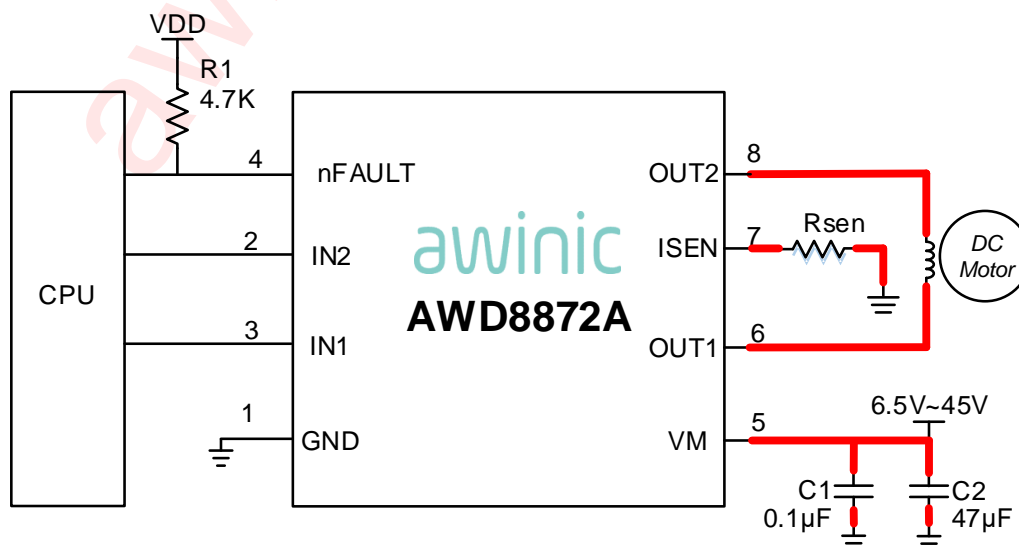
Features

- Drives a DC Motor or Other Loads
- $R_{dson\ HS + LS}$: 460m Ω
- 3.6-A Maximum Drive Current
- VM: 6.5V to 45V Operating Voltage Range
- PWM Control Interface
- Low-Power Sleep Mode
- Small Package and Footprint
 - 8-Pin SOP With Power PAD
 - WBESOP-8L
- Over-Circuit Protection (OCP)
- Over-Temperature Protection(OTP)
- Under-Voltage Protection(UVLO)
- Automatic Fault Recovery

Applications

- Printers
- Appliances
- Industrial Equipment
- Other Mechatronic Applications

Typical Application Circuit



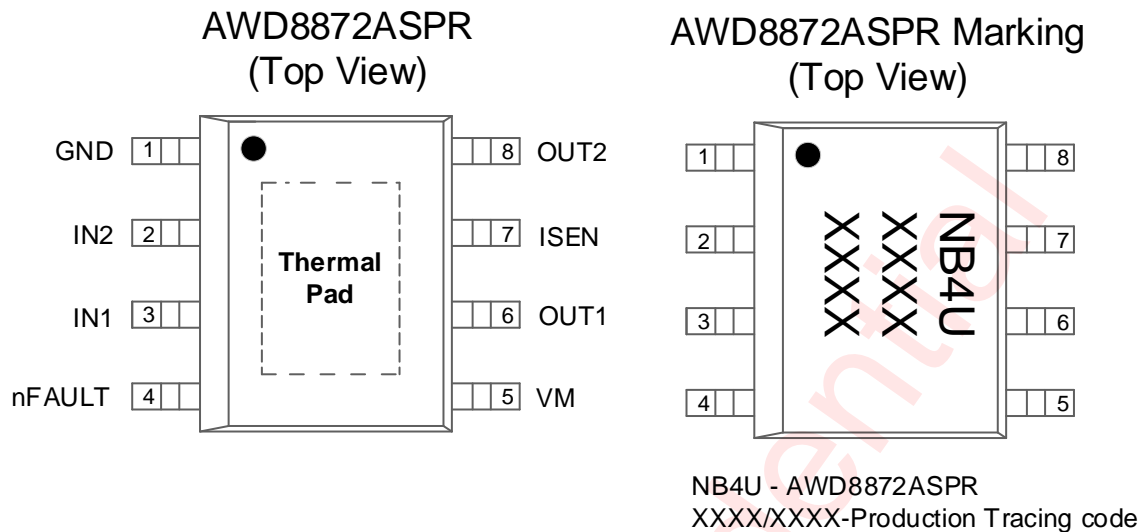
General Description

The AWD8872A provides an integrated motor driver solution for printers, appliances, industrial equipment, and other small machines. The device can supply up to 3.6A of output current. It operates on a motor power supply voltage from 6.5V to 45V. The output driver block consists of N-channel power MOSFETs configured as an H-bridge to drive the motor winding. The inputs can be pulse width modulated (PWM) to control motor speed, using a choice of current-decay modes. Setting both inputs low enters a low-power sleep mode.

The AWD8872A device features integrated current regulation, based on an internal reference voltage and the voltage on the ISEN pin, which is proportional to motor current through an external sense resistor. The ability to limit current to a known level can significantly reduce the system power requirements and bulk capacitance needed to maintain stable voltage, especially for motor startup and stall conditions.

Internal shutdown functions are provided for Over-current protection (OCP), Short-circuit protection, Under-voltage lockout (UVLO), and Over-temperature protection (OTP). When the fault condition is removed, the device automatically resumes normal operation.

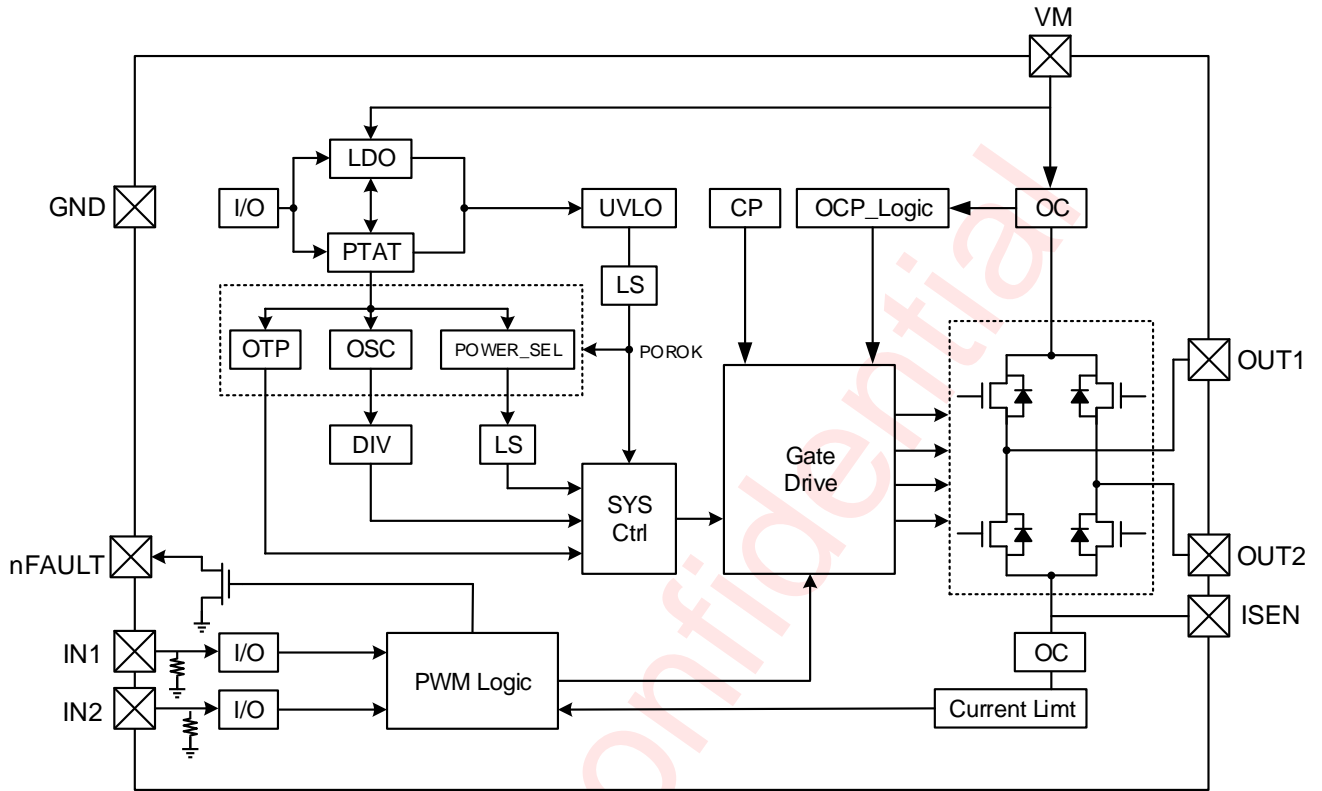
Pin Configuration And Top Mark



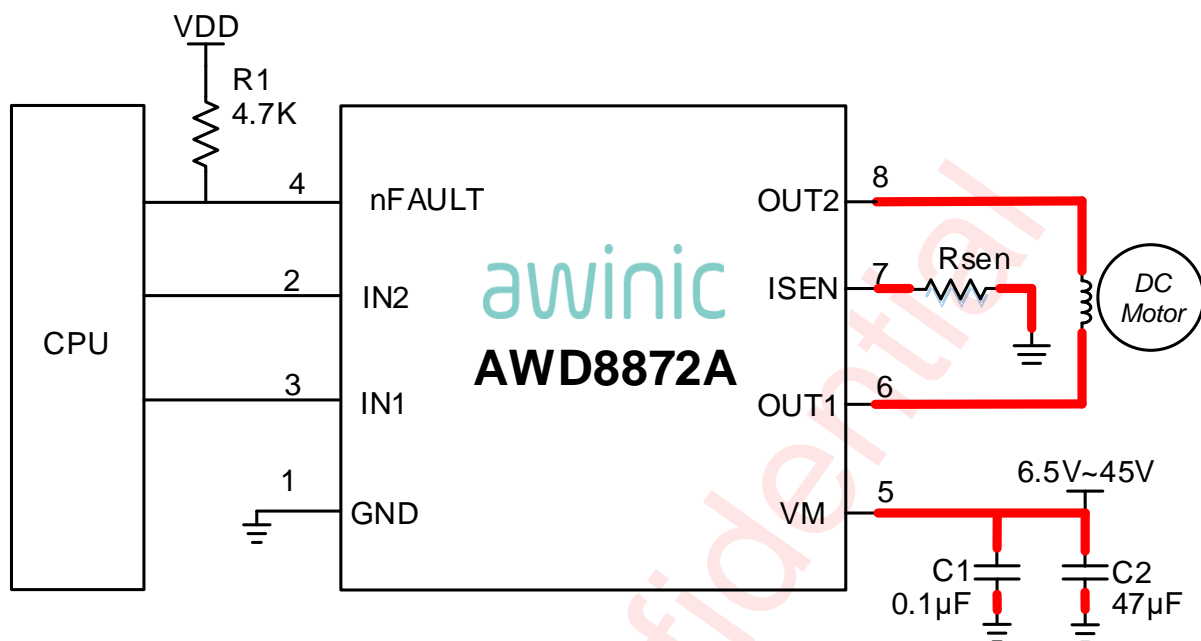
Pin Definition

NAME	PIN	DESCRIPTION
GND	1	Device ground. This pin must be connected to ground.
IN2	2	Logic inputs Controls the H-bridge output. Has internal pulldowns.
IN1	3	Logic inputs Controls the H-bridge output. Has internal pulldowns.
nFAULT	4	Fault status(open-drain). Low-level indicates UVLO, OTP, or OCP fault. Connect to a pullup resistor.
VM	5	Connect a 0.1- μ F bypass capacitor to ground, as well as sufficient bulk capacitance, rated for the VM voltage.
OUT1	6	H-bridge output Connect directly to the motor or other inductive load.
ISEN	7	If using current regulation, connect ISEN to a resistor (low-value, high-power-rating) to ground.If not using current regulation, connect ISEN directly to ground
OUT2	8	H-bridge output Connect directly to the motor or other inductive load.
Thermal PAD	-	Connect to board ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes.

Functional Block Diagram



Typical Application Circuits



Notice for Typical Application Circuits:

- 1: Please place C1, C2 as close to the chip as possible. The capacitors should be placed in the same layer with the AWD8872ASPR chip.
- 2: For the sake of driving capability, the power lines and output lines should be short and wide as possible.
- 3: The power path marked in red as shown in the figures above, please traces according to **5A** power line alignment rules.
- 4: **Table 1** lists the recommended external components for the device.

Table 1 External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C1	VM	GND	0.1µF ceramic capacitor rated for VM
C2	VM	GND	47µF bulk capacitor rated for VM
R1	nFAULT	VDD	4.7K

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWD8872ASPR	-40°C~125°C	WBESOP-8L	NB4U	MSL3	RoHS + HF	3000units/ Tape and Reel

Absolute Maximum Ratings^(NOTE1)

PARAMETERS	RANGE
Motor power-supply voltage (VM)	-0.3V to 50V
Control pin voltage (IN1, IN2)	-0.3V to 5.5V
Fault pin (nFAULT)	-0.3V to 5.5V
Continuous phase node pin voltage (OUT1,OUT2)	-0.7V to VM+0.7V
Current sense input pin voltage (ISEN)	-0.5V to 1V
Output current (100% duty cycle)	0A to 3.6A
Maximum operating junction temperature T _{JMAX}	160°C
Storage temperature T _{STG}	-65°C to 150°C
ESD(Including CDM HBM MM) ^(NOTE 2)	
HBM(Human Body Model)	±2kV
CDM(Charge Device Model)	±1.5KV
Latch-Up	
Test Condition: JEDEC STANDARD NO.78E	+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ANSI/ESDA/JEDEC JS-001.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		Range	Unit
VM	Power supply voltage	6.5 to 45	V
V _I	Logic input voltage (IN1, IN2)	0 to 5	V
f _{PWM}	Logic input PWM frequency (IN1, IN2)	0 to 200 ⁽¹⁾	kHz
I _{peak}	Peak output current ⁽²⁾	0 to 3.6	A
T _A	Operating ambient temperature	-40 to 125	°C

(1) The voltages applied to the inputs should have at least 2500ns of pulse width to ensure detection.

(2) Power dissipation and thermal limits must be observed.

Thermal Information

PARAMETERS		Range	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.25	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	59.75	$^{\circ}\text{C}/\text{W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	2.43	$^{\circ}\text{C}/\text{W}$
ψ_{JT}	Junction-to-top characterization parameter	5.94	$^{\circ}\text{C}/\text{W}$
ψ_{JB}	Junction-to-board characterization parameter	2.15	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	1.65	$^{\circ}\text{C}/\text{W}$

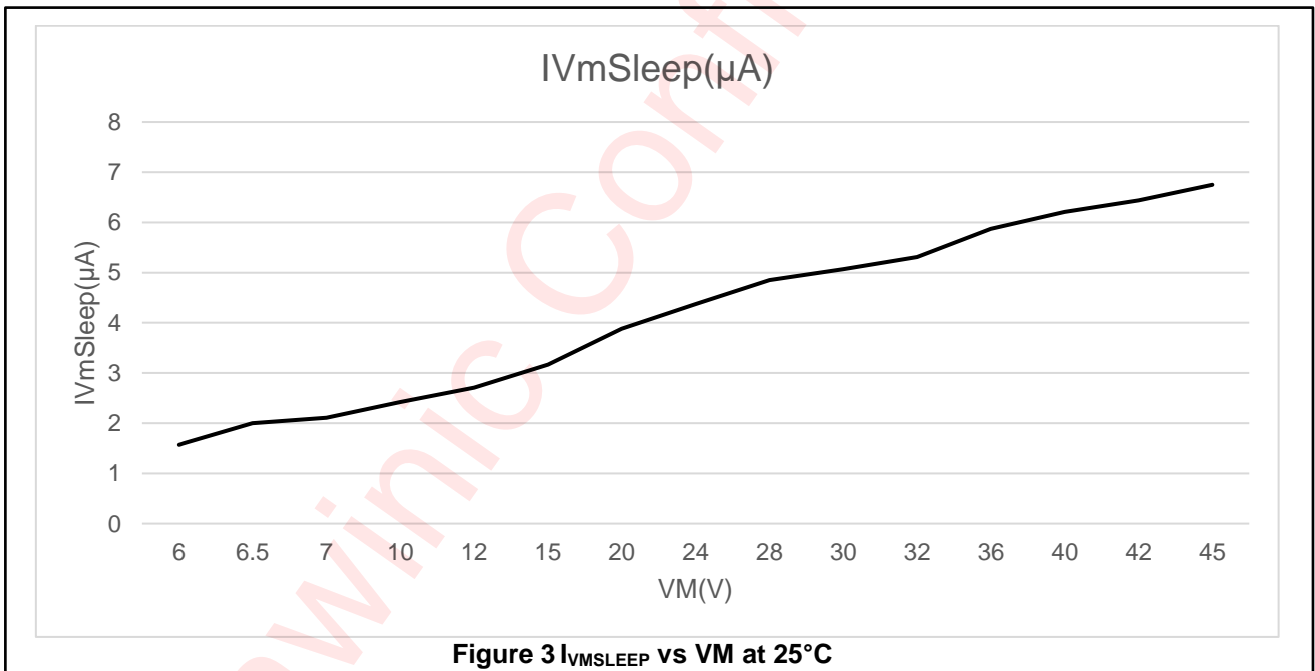
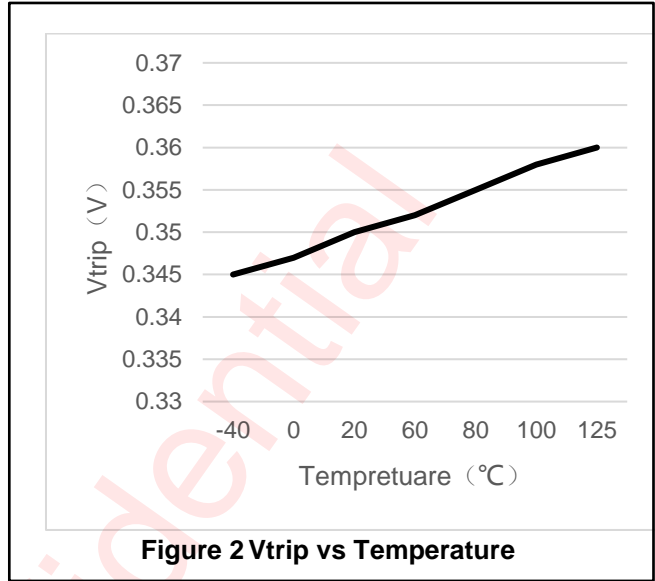
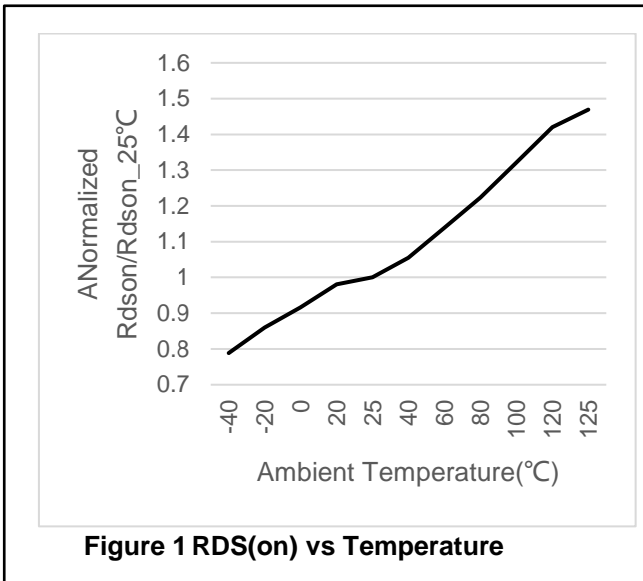
Electrical Characteristics

$T_A=25^{\circ}\text{C}$ for typical values (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM)					
VM	VM operating voltage	6.5		45	V
I_{VM}	VM operating supply current	VM = 12 V	3	10	mA
I_{VMQ}	VM sleep mode supply current	VM = 12 V		10	μA
t_{ON}	Turn-on time	VM > V_{UVLO} with IN1 or IN2 high	45	65	μs
LOGIC-LEVEL INPUTS (IN1, IN2)					
VIL	Input logic low voltage			0.50	V
VIH	Input logic high voltage	1.5			V
VHYS	Input logic hysteresis		0.15		V
IIL	Input logic low current	VIN = 0 V	-1	1	μA
IIH	Input logic high current	VIN = 3.3 V	33	100	μA
R_{PD}	Pulldown resistance	To GND	100		k Ω
t_{PD1}	Propagation delay	INx to OUTx change (see Figure 6)	0.3	1	μs
t_{PD2}	Propagation delay	INx to OUTx change (see Figure 6)	0.4	1	μs
t_{sleep}	Time to sleep	Inputs low to sleep	1.5	2	ms

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOTOR DRIVER OUTPUTS (VO1, VO2)						
R _{DSON}	High-side FET on-resistance	VM = 24 V; IO=1000mA;		270		mΩ
R _{DSON}	Low-side FET on-resistance	VM = 24 V; IO=1000mA;		190		mΩ
t _{DEAD1}	Output dead time	INx to VOx change (see Figure 6)		210		ns
t _{DEAD2}	Output dead time			110		ns
V _d	Body diode forward voltage	I _{OUT} =1A		0.93		V
CURRENT REGULATION						
V _{TRIP}	ISEN voltage for current chopping		0.32	0.35	0.38	V
t _{OFF}	PWM off-time			25		μs
t _{BLANK}	PWM blanking time			2.4		μs
PROTECTION CIRCUITS						
V _{UVLO}	VM undervoltage lockout	VM falls until UVLO triggers		6.1	6.4	V
		VM rises until operation recovers		6.3	6.5	
V _{UV,HYS}	VM undervoltage hysteresis	Rising to falling threshold	100	270		mV
I _{OCP}	Overcurrent protection trip level		3.7	4.1	6.4	A
t _{OCP}	Overcurrent deglitch time			2		μs
t _{RETRY}	Overcurrent retry time			3		ms
T _{SD}	Thermal shutdown temperature	Die temperature T _J		175		°C
T _{HYS}	Thermal shutdown hysteresis			30		°C
nFAULT OPEN DRAIN OUTPUT						
V _{OL}	Output low voltage	I _o =5mA			0.5	V
I _{OH}	Output high leakage current	V _o =3.3V			1	μA

Typical Characteristics



Detailed Functional Description

OVERVIEW

The AWD8872A device is a conventional 8-pin chip used to drive one brushed DC motors, with a maximum peak current of 3.6A. The H-bridge driver is controlled using a PWM interface (IN1 and IN2), which has a typical R_{dson} of 460 m Ω (including one high-side and one low-side FET). PWM input can adjust the motor speed by changing the duty cycle and frequency. When the inputs are all low, the chip enters sleep mode after 1.5ms. The integrated charge pump of the device boosts VM internally and fully enhances the high-side FETs. In addition, the AWD8872A adds protection features beyond traditional discrete implementations: under-voltage lockout, overcurrent protection, and thermal shutdown.

FEATURE DESCRIPTION

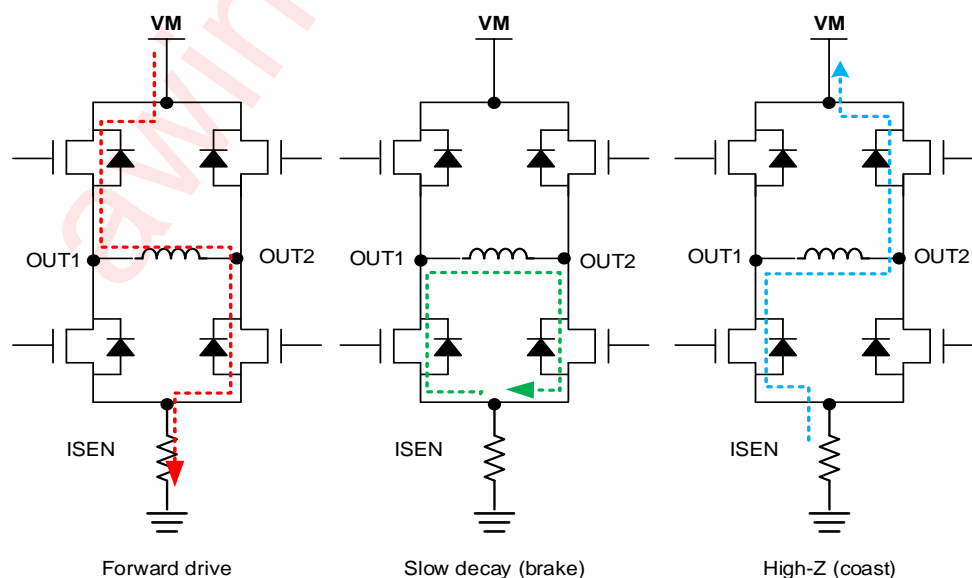
BRIDGE CONTROL

The AWD8872A is controlled using a PWM input interface. Each output is controlled by a corresponding input pin. **Table 2** shows the logic for the AWD8872A device.

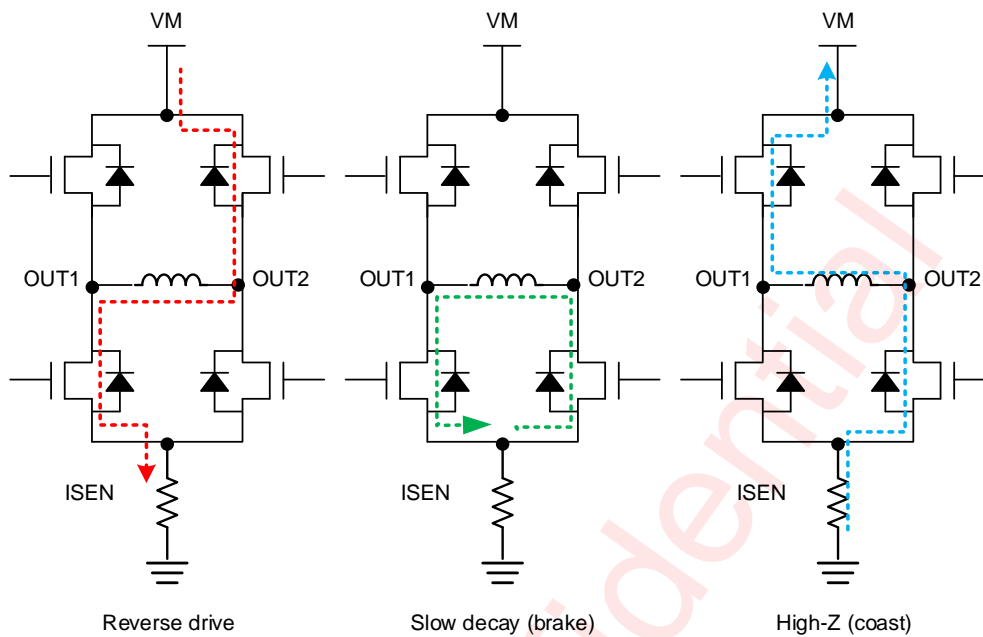
Table 2 AWD8872A Device Logic

IN1	IN2	OUT1	OUT2	FUNCTION (DC MOTOR)
0	0	Z	Z	Coast , sleep entered after 1.5ms
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake, low-side slow decay

The input pins can be powered before VM is applied. The H-bridge driver is controlled using a PWM interface (IN1 and IN2), and PWM input can adjust the motor speed by changing the duty cycle and frequency. The H-bridge current paths can be controlled by setting IN1 and IN2. Alternatively, the coast mode (IN1 = 0, IN2 = 0) for fast current.



H-Bridge Forward drive Paths



H-Bridge Reverse drive Paths

Figure 4 H-Bridge Current Paths

SLEEP MODE

If the IN1 or IN2 pins are all low, the outputs remain High-Z (the coast mode) and discharge quickly. After time t_{SLEEP} 1.5ms, the AWD8872A enters a low-power sleep mode. When the IN1 or IN2 pins are high for at least $5\mu s$, the device is operational $45\mu s$ (t_{ON}) later.

CURRENT REGULATION

The AWD8872A device can adjust the output current by changing R_{ISEN} according to Equation 1:

$$I_{TRIP}(A) = \frac{V_{TRIP}(V)}{R_{ISEN}(\Omega)} = \frac{0.35(V)}{R_{ISEN}(\Omega)}$$

Where

- R_{ISEN} is the resistance of an external sense resistor on the ISEN pin
- I_{TRIP} is the threshold current

For example, if $R_{ISEN} = 0.2\Omega$, the threshold current I_{TRIP} is 1.75 A. The AWD8872A device limits motor current to 1.75A no matter how much load torque is applied. For guidelines on selecting a sense resistor, see the Sense Resistor section.

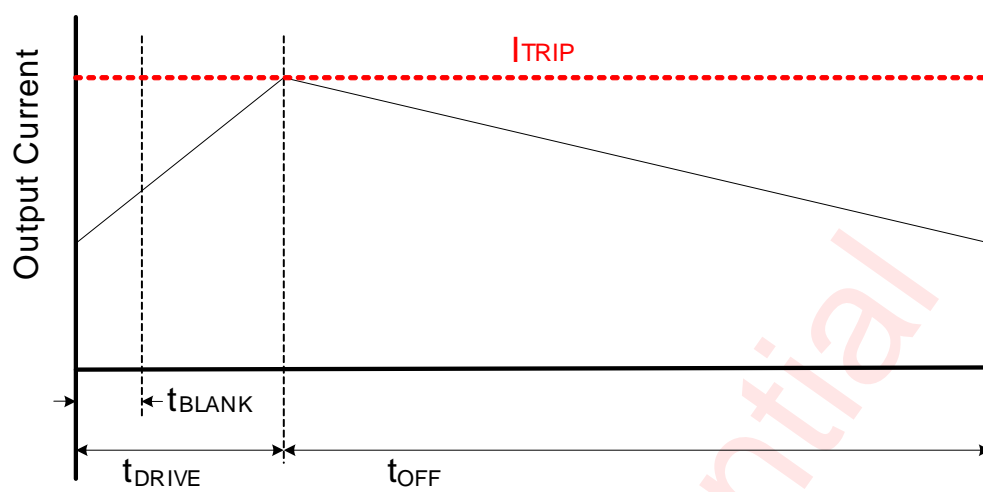


Figure 5 Current Regulation Time Periods

TIMING REQUIREMENTS

When the input signal changes, the output signal will change after time t_{PD} (typically 400ns). In order to prevent the H-bridge from generating shoot-through current, dead time is necessary. The t_{DEAD} time is the time in the middle when the output is High-Z. If the output pin is measured during t_{DEAD} , the voltage depends on the direction of current. If the current is leaving the pin, the voltage is a diode drop below ground. If the current is entering the pin, the voltage is a diode drop above V_M . This diode is the body diode of the high-side or low-side FET.

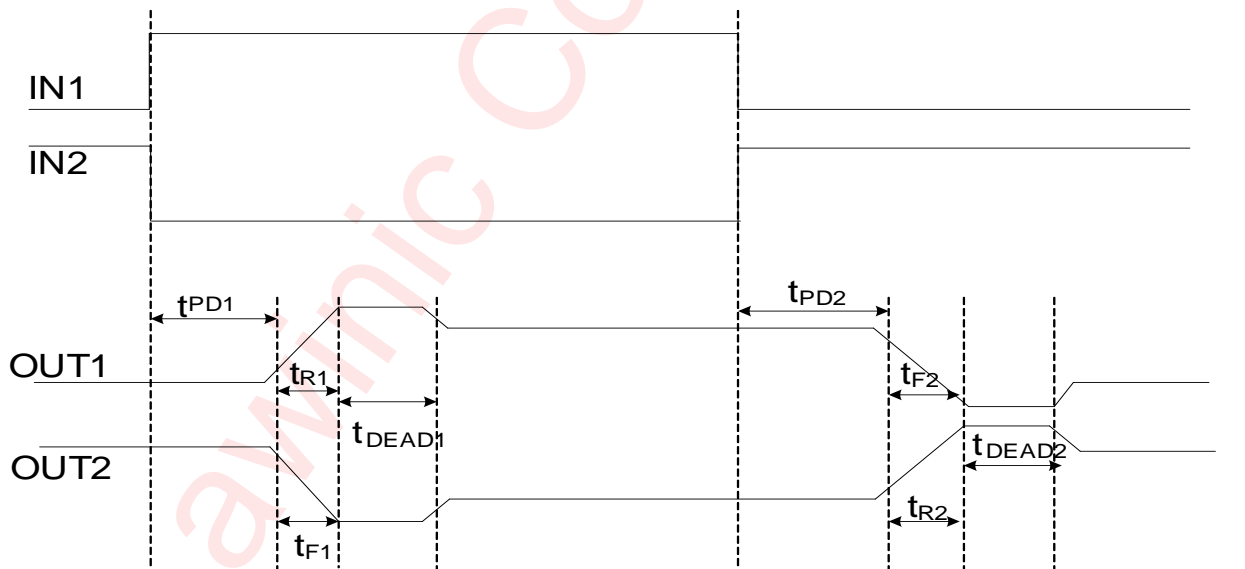


Figure 6 Propagation Delay Time

POWER SUPPLIE AND INPUT PINS

A single-power input, V_M , serves as both device power and the motor winding bias voltage. No leakage current path will exist to the supply. Each input pin has a weak pulldown resistor (approximately 100 k Ω) to ground.

VM UNDERVOLTAGE LOCKOUT

If at any time the voltage on the V_M pin falls below the under-voltage lockout threshold voltage, all FETs in the H-bridge are disabled. Operation resumes when the V_M pin voltage rises above the UVLO threshold.

OVERCURRENT PROTECTION

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than t_{DEG} , all FETs in the H-bridge are disabled. Operation resumes automatically after t_{RETRY} has elapsed. Overcurrent conditions are detected on both the high-side and low side FETs. A short to the VM pin, GND, or from the OUT1 pin to the OUT 2 pin results in an overcurrent condition.

THERMAL SHUTDOWN

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature falls to a safe level, operation automatically resumes.

Table 2 Fault Behavior

FAULT	CONDITION	H-BRIDGE	RECOVERY
VM under-voltage (UVLO)	$VM < V_{UVLO}$	Disabled	$VM > V_{UVLO} + V_{HS}$
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$	Disabled	t_{RETRY} elapses
Thermal Shutdown (TSD)	$T_J > T_{SD}$	Disabled	$T_J < T_{SD} - T_{HS}$

DEVICE FUNCTIONAL MODES

The AWD8872A is active unless the IN1 and IN2 are both logic low for time t_{SLEEP} (typically 1.5ms). In sleep mode, the H-bridge FETs are disabled Hi-Z. The AWD8872A is brought out of sleep mode automatically if the IN1 or IN2 pins are high for at least 5 μ s. The H-bridge outputs are disabled during under-voltage lockout, overcurrent, and over-temperature fault conditions.

PWM WITH CURRENT REGULATION

This scheme uses all of the capabilities of the device. The I_{TRIP} current is set above the normal operating current, and high enough to achieve an adequate spin-up time, but low enough to constrain current to a desired level. Motor speed is controlled by the duty cycle of one of the inputs, while the other input is static. Brake or slow decay is typically used during the off-time.

PWM WITHOUT CURRENT REGULATION

If current regulation is not needed, the ISEN pin should be directly connected to the PCB ground plane. This mode provides the highest possible peak current: up to 3.6 A for a few hundred milliseconds (depending on PCB characteristics and the ambient temperature). If current exceeds 3.6 A, the device might reach over current protection (OCP) or over-temperature shutdown (TSD). If that occurs, the device disables and protects itself for about 3 ms (t_{RETRY}) and then resumes normal operation.

STATIC INPUTS WITH CURRENT REGULATION

The IN1 and IN2 pins can be set high and low for 100% duty cycle drive, and ITRIP can be used to control the current of the motor, speed, and torque capability.

Application Information

The AWD8872A is used to drive one brushed dc motor. The following design procedure can be used to configure the AWD8872A device.

DESIGN REQUIREMENTS

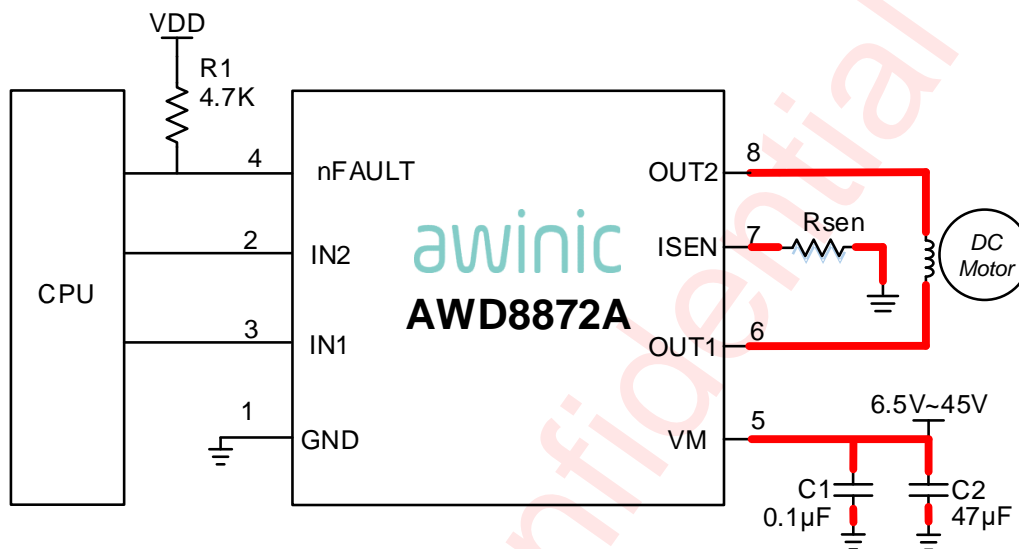


Table lists the required parameters for a typical usage case.

Table 3 Design Requirements

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	VM	16.5V
Motor RMS current	I _{RMS}	0.8 A
Motor startup current	I _{START}	1.5 A
Motor current trip point	I _{TRIP}	1.75 A
Sense resistance	R _{ISEN}	0.15Ω
PWM frequency	f _{PWM}	5 kHz

Note: Customers should validate and test their design implementation to confirm system functionality.

MOTOR VOLTAGE

The appropriate motor voltage depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed dc motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

DRIVE CURRENT

The current path is through the high-side sourcing NMOS power driver, motor winding, and low-side sinking NMOS power driver. Power dissipation losses in one source and sink NMOS power driver are shown in Equation 2:

$$P_D(W) = I^2(R_{DS(on)(HS)} + R_{DS(on)(LS)})$$

The AWD8872A device has been measured to be capable of 2A RMS current at 25°C on standard FR-4 PCBs. The maximum RMS current varies based on the PCB design, ambient temperature, and PWM frequency.

SENSE RESISTOR

For optimal performance, the sense resistor must have the following characteristics:

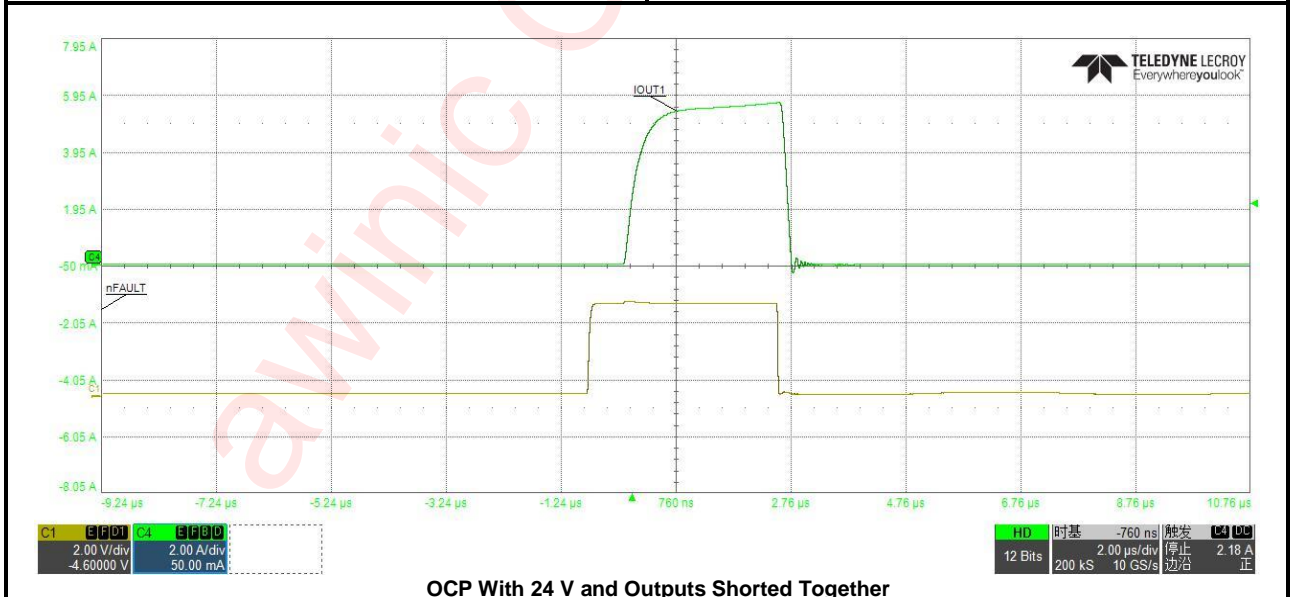
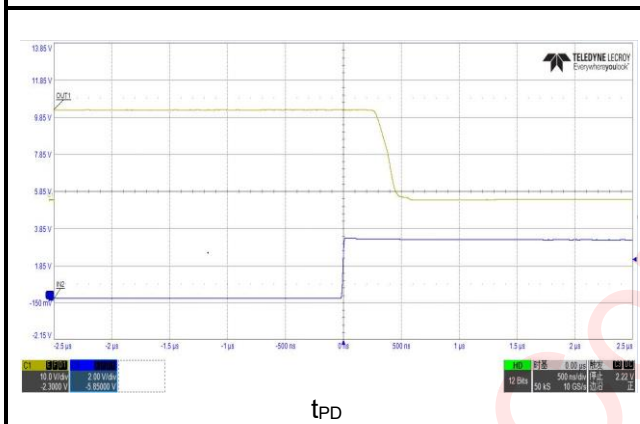
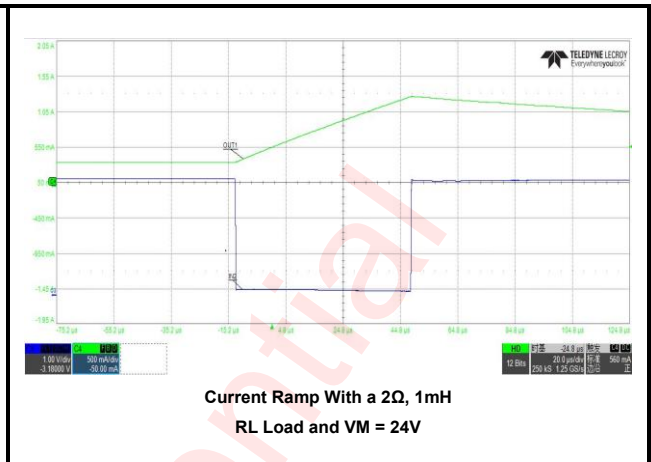
- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $I_{RMS}^2 \times R$. For example, if peak motor current is 3A, RMS motor current is 1.5A, and a 0.2Ω sense resistor is used, the resistor dissipates $(1.5A)^2 \times 0.2\Omega = 0.45W$. The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, the system designer should add margin. Measuring the actual sense resistor temperature in a final system is always best.

Because power resistors are larger and more expensive than standard resistors, using multiple standard resistors in parallel, between the sense node and ground, is common and distributes the current and heat dissipation.

APPLICATION CURVES



POWER SUPPLY RECOMMENDATIONS

BULK CAPACITANCE

Having appropriate local bulk capacitance is an important factor in motor-drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power-supply capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless dc, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The datasheet generally provides a recommended value, but system-level testing is required to determine the appropriate size of bulk capacitor.

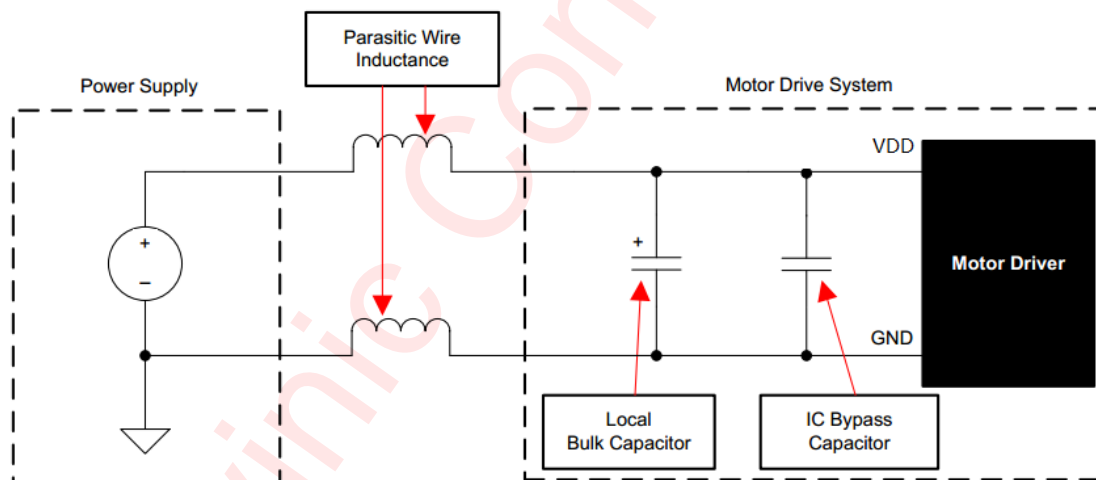


Figure 7 Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

PCB Layout Consideration

EXTERNAL COMPONENTS PLACEMENT

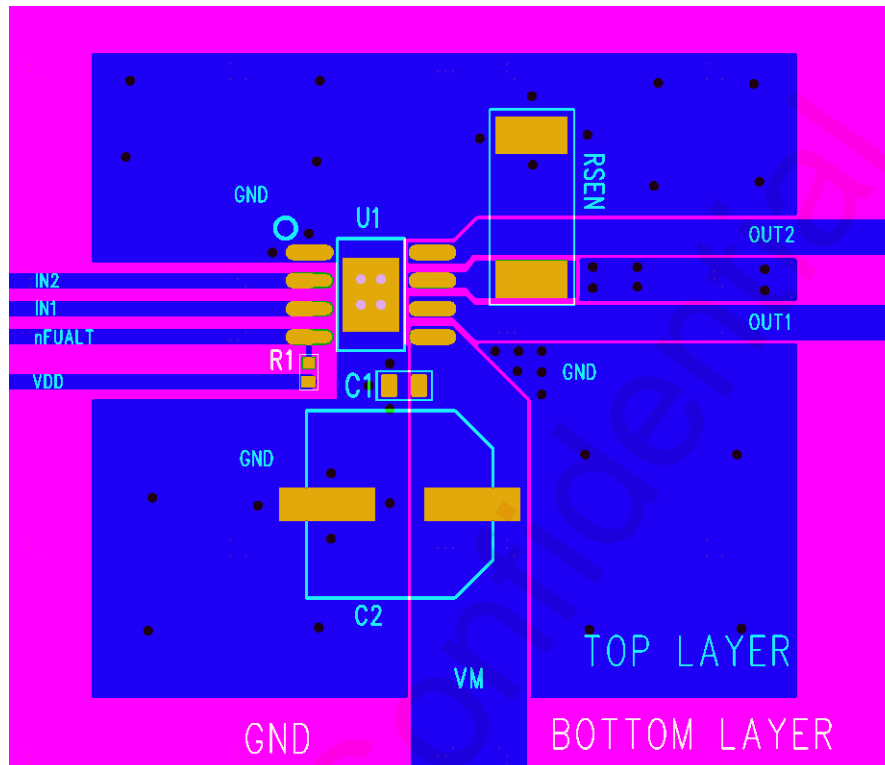


Figure 8 AWD8872A External Components Placement

LAYOUT CONSIDERATIONS

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

THERMAL CONSIDERATIONS

The AWD8872ASPR device has thermal shutdown (TSD) as described in the Thermal Shutdown (TSD) section. If the die temperature exceeds approximately 175°C, the device is disabled until the temperature drops below the temperature hysteresis level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high of an ambient temperature.

POWER DISSIPATION

Power dissipation in the AWD8872ASPR is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Use Equation to estimate the average power dissipation when running a stepper motor.

$$P_D(W) = I^2(R_{DS(ON)(HS)} + R_{DS(ON)(LS)})$$

Where

- P_D is the total power dissipation
- $I_{OUT(rms)}$ is the rms or dc output current being supplied to the load

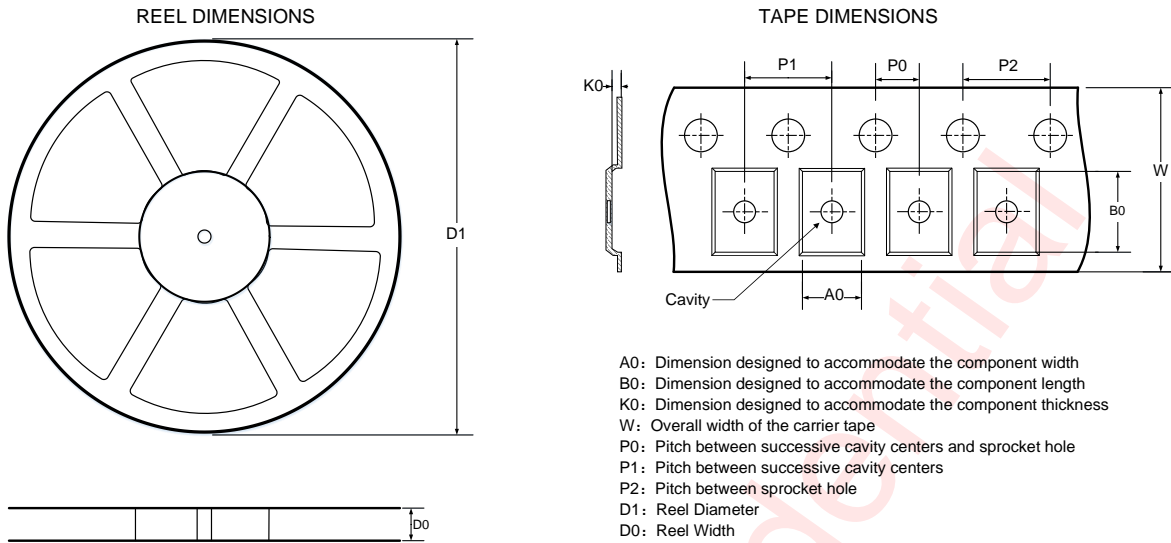
The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking. Note that at startup, the current is much higher than normal running current; this peak current and its duration must be also be considered.

For this example, the ambient temperature is 58°C, and the junction temperature reaches 80°C. At 58°C, the sum of $R_{DS(ON)}$ is about 0.53 Ω. With an example motor current of 0.8 A, the dissipated power in the form of heat is $(0.8A)^2 \times 0.53\Omega = 0.34W$.

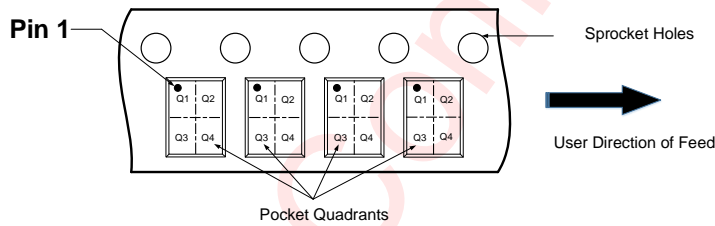
The temperature that the AWD8872ASPR reaches will depend on the thermal resistance to the air and PCB. It is important to solder the device PowerPAD to the PCB ground plane, with vias to the top and bottom board layers, in order dissipate heat into the PCB and reduce the device temperature. In the example used here, the AWD8872A device had an effective thermal resistance $R_{\theta JA}$ of 55.25°C/W, and:

$$T_j = T_A + (P_D \times R_{\theta JA}) = 58^\circ C + (0.34W \times 55.25^\circ C/W) = 77^\circ C$$

Tape And Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



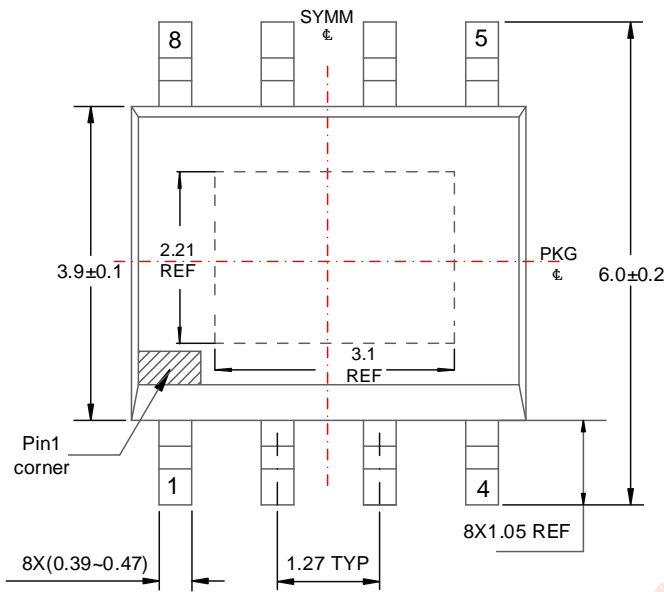
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

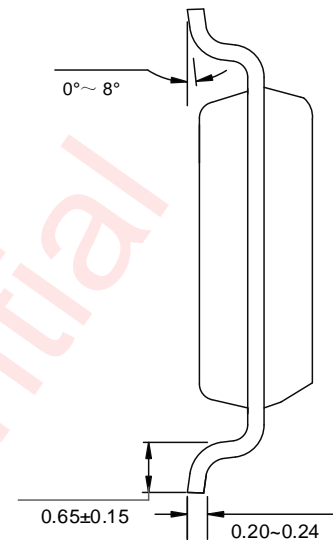
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	6.55	5.3	2	2	8	4	12	Q1

All dimensions are nominal

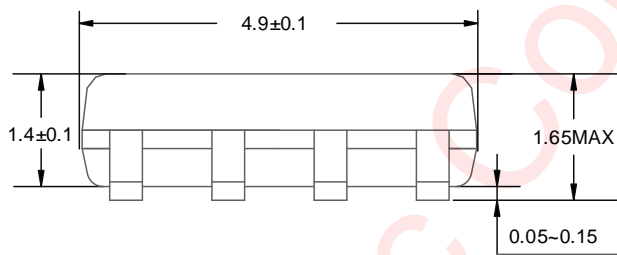
Package Description



Top View



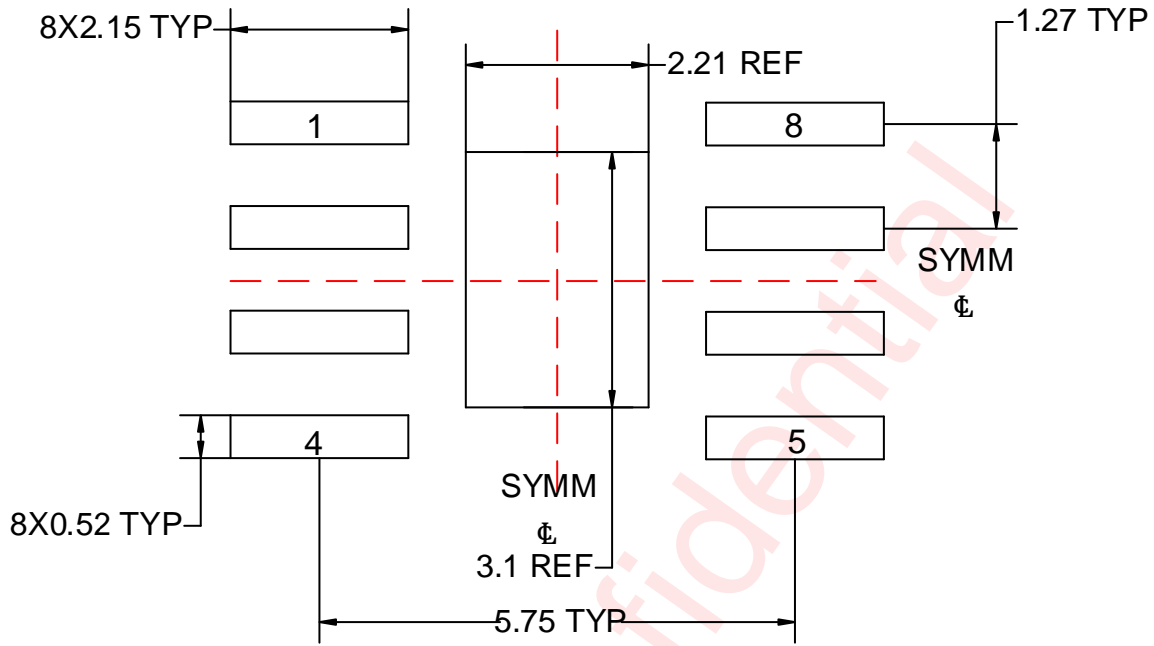
Side View



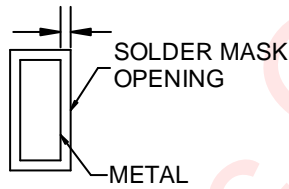
Side View

Unit: mm

Land Pattern Data

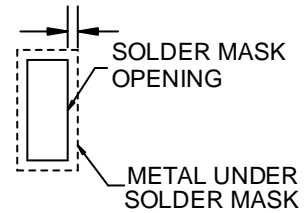


0.05 MAX
All AROUND



NON SOLDER MASK DEFINED

0.05 MIN
All AROUND



SOLDER MASK DEFINED

Unit: mm

REVISION HISTORY

Version	Date	Change Record
V1.0	Sep. 2023	Initial released

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