XPM6233

5.5-V Input 3-A Step-Down Power Module with Integrated Inductor

FEATURES

- 2.5-mm × 2.0-mm × 1.1-mm LGA package
- Up to 95% efficiency
- 2.7-V to 5.5-V input voltage range
- 0.6-V to 4-V adjustable output voltage
- 3-A continuous output current
- Advanced CoT control topology
- FCCM mode for low ripple voltage
- Hiccup short circuit protection
- Output discharge
- Power-good output with window comparator
- Integrated soft start-up
- Overtemperature protection

APPLICATIONS

- Optical modules
- Industrial PCs
- Wired Networking

DESCRIPTION

The XPM6233 is a 5.5-V input 3-A step-down power module optimized for small solution size and high efficiency. The module integrates a synchronous step-down converter and an inductor to simplify design, reduce external components, and save PCB area.

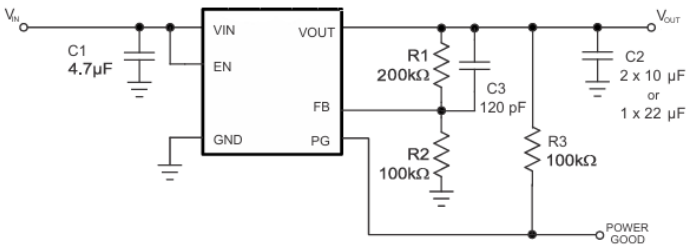
The low profile and compact solution is suitable for automated assembly by standard surface mount equipment.

The XPM6233 operates in PWM mode with a nominal 4MHz switching frequency across the whole load current range for low ripple voltage.

Using the Advanced CoT control topology, the XPM6233 achieves excellent load transient performance and accurate output voltage regulation.

The EN and PG pins, which support sequencing configurations, bring a flexible system design. An integrated soft start-up reduces the inrush current required from the input supply. Overtemperature protection and hiccup short circuit protection deliver a robust and reliable solution.

TYPICAL APPLICATION



REVISION HISTORY

Release	Rev	Changes	Date
Released			2/15/2025

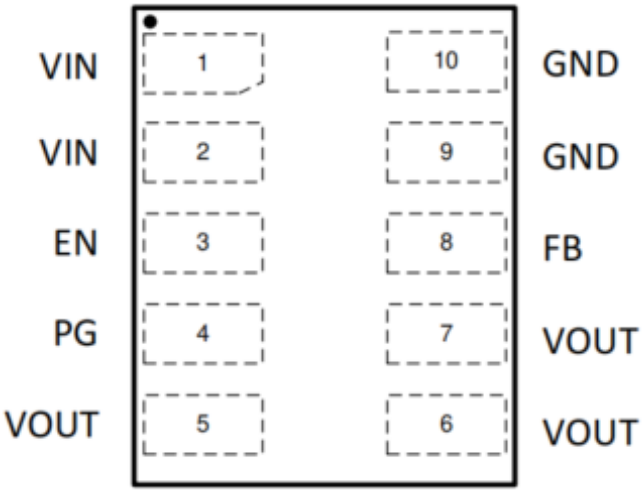
ORDERING INFORMATION

Part Number	Output Current (A)	VOUT (V)	Top Marking	MPQ
XPM6233G10R	3	Adjustable	Tracing code	3,000

MPQ = Minimum Packaging Quantity.
For production orders greater than MPQ, the order must be a multiple of MPQ per package size above.

PIN CONFIGURATION AND DESCRIPTION

10-Pin LGA Package
(Top View)



Pin Configuration

Pin	Name	Description
1,2	VIN	Input pin.
3	EN	Device enable pin. To enable the device, this pin needs to be pulled high. Pulling this pin low disables the device. Do not leave floating.
4	PG	Power-good open-drain output pin. The pullup resistor can be connected to voltages up to 5.5 V. If unused, leave it floating.
5,6,7	VOUT	Output pin.
8	FB	Feedback pin. This pin must be connected to the center of the output voltage resistor divider.
9,10	GND	Ground pin.

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
VIN ,VOUT, FB, EN, PG	-0.3	6	V
Operating junction temperature	-40	+125	°C
Storage temperature	-55	+125	°C
Electrostatic Discharge (HBM)	-2000	+2000	V
Electrostatic Discharge (CDM)	-1000	+1000	V

(1) Operation of the device outside of these parameters may cause permanent damage.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{IN}	2.7		5.5	V
Output voltage range	V_{OUT}	0.6		4.0	V
Output Current	I_{OUT}	0		3	A
Pullup resistor voltage	V_{PG}			5.5	V
Operating Temperature, Junction	T_{OJ}	-40		+125	°C

Thermal Information

Junction to ambient thermal resistance is a function of board layout and ambient air flow condition. This data is based on four layers PCB (30mm x 30mm; 70µm Cu top signal layer) in still air box in accordance with JEDEC standard JESD51 on natural convection.

Parameter	Symbol	Typ	Units
Junction-to-Ambient Thermal Resistance	θ_{JA}	TBD	°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	TBD	°C/W

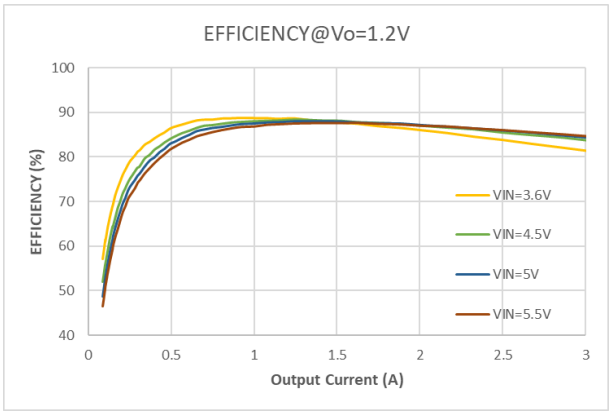
ELECTRICAL SPECIFICATIONS

T_J = -40˚C to 125˚C and V_{IN} = 2.7V to 5.5V. Typical values are at T_J = 25°C and V_{IN} = 3.3V, unless otherwise noted.

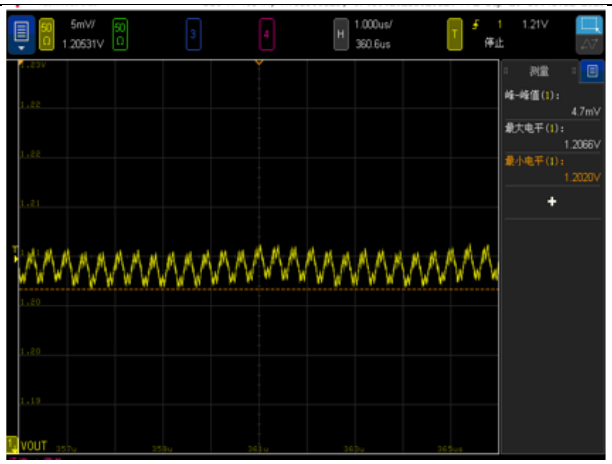
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
SUPPLY						
Supply Voltage	V_{IN}		2.7		5.5	V
Quiescent Current	I_Q	No Load, Not Switching		80		µA
Quiescent Current	I_Q	No Load, PWM mode		8		mA
Shutdown Current	I_{SHDN}	EN = LOW			0.5	µA
Under-Voltage Lockout Threshold	V_{UVLO}	Falling V_{IN}	2.4	2.5	2.6	V
Under-Voltage Lockout Hysteresis	$V_{UVLOHYST}$	Rising V_{IN}		160		mV
Thermal Shutdown	T_{TSD}			150		˚C
Thermal Shutdown Hysteresis	T_{HYST}			25		˚C
LOGIC INTERFACE EN						
EN High Threshold	VIH		1.0			V
EN Low Threshold	VIL				0.4	V
Input leakage current into EN pin	I_{EN_LKG}				0.1	uA
SOFT START, POWER GOOD						
Internal Soft-Start Time	t_{SS}	Time from EN high to 95% of V_{OUT} nominal		1.2		ms
PG UV Threshold Rising	PGTH_Hi		92%	95%	98%	VFB
PG UV Threshold Falling	PGTH_Lo		88%	91%	94%	VFB
PG OV Threshold Rising	PGTH_Hi		102%	105%	108%	VFB
PG OV Threshold Falling	PGTH_Lo		107%	110%	113%	VFB
Low-level output voltage	$V_{PG,OL}$	Isink = 1 mA			0.4	V
Input leakage current into PG pin	$I_{PG,LKG}$	VPG = 5.0 V			0.1	uA
OUTPUT						
Output voltage range	V_{OUT}		0.6		4	V
Regulated FB Voltage	V_{FB}	PWM mode	594	600	606	mV
Feedback input leakage current	$I_{FB,LKG}$	V_{FB} = 0.6V			0.05	uA
Output discharge current	I_{DIS}	V_{SW} = 0.4V; EN = LOW		100		mA
POWER SWITCH						
High-Side Switch On-Resistance	R_{DSONP}			90		mΩ
Low-Side Switch On-Resistance	R_{DSONN}			30		mΩ
High-Side Switch Current Limit		Sourcing		4.3	5	A
Low-Side Switch Current Limit		Sinking		-1.6		A
PWM switching frequency	f_{SW}	I_{OUT} = 1 A, V_{OUT} = 1.8 V		4		MHz

TYPICAL PERFORMANCE AND OPERATING CHARACTERISTICS

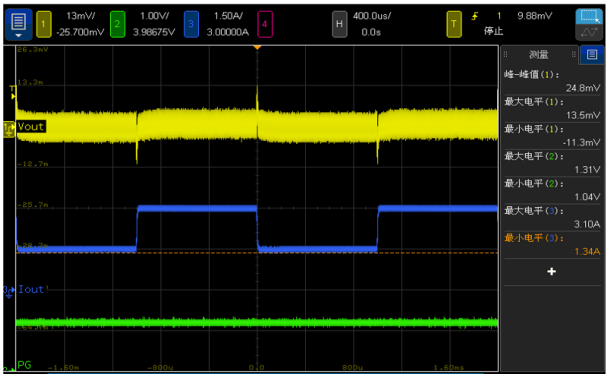
Test conditions unless otherwise noted: V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{IN} = 10uF, C_{OUT} = 2 x 10uF and T_A = +25°C.



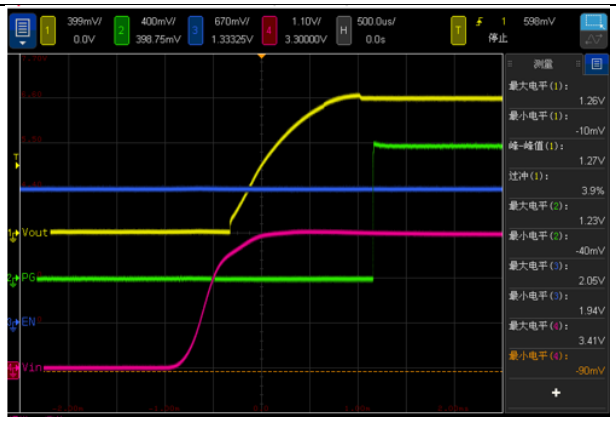
Efficiency vs. Load Current



Voltage Ripple (IOUT=3A)



Load Transient, IOUT= 1.5A to 3A

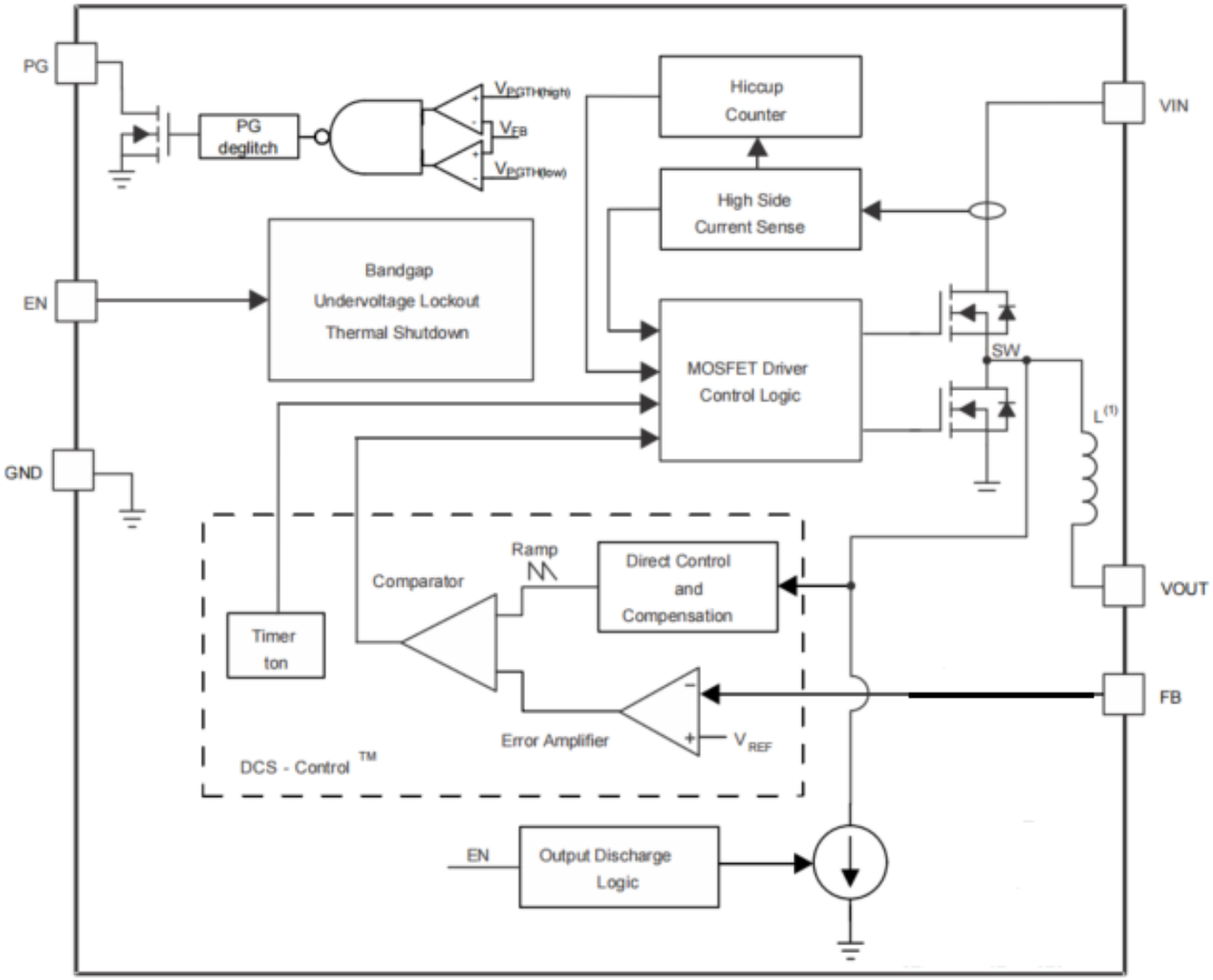


Start-Up, IOUT=0A

Shut-Down, IOUT=0A

Short Circuit Protection

FUNCTIONAL DESCRIPTION



Block Diagram

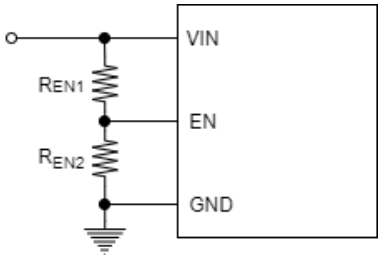
Overview

The XPM6233 is a synchronous step-down DC-DC voltage regulator available with switching frequency of 4MHz. Operating from an input voltage between 2.7V and 5.5V, the regulator can deliver up to 3A of load current.

Enable

Setting the EN pin to logic High enables the device. Alternatively, the device is disabled when the EN voltage is set to logic Low or floating. In this state the IC draws less than 0.5μA of current.

The EN pin can also be applied to adjust XPM6233 Under-Voltage Lockout (UVLO) threshold with two external resistors divider from VIN to ground, please refer to the following graph for application structure.



Soft-Start

After enabling the device, there is a 250-µs delay before switching starts. Then, an internal soft start-up circuitry ramps up the output voltage which reaches nominal output voltage during the start-up time of 1ms. This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance. The device is able to start into a pre-biased output capacitor. It starts with the applied bias voltage and ramps the output voltage to its nominal value.

Under-voltage Lockout (UVLO)

The under-voltage lockout feature prevents the device from turning on if V_{IN} is below the UVLO level of 4.2V. If the device is enabled under UVLO conditions, the circuitry will not turn on until the input voltage is increased. Once active, the UVLO circuit has 400mV of hysteresis and the device will turn off if V_{IN} drops below 3.8V.

Thermal Shutdown

The device thermal shutdown protection is enabled if the chip temperature exceeds 150°C. Once the temperature drops below 125°C, the device will be re-enabled, and a new soft-start cycle will begin.

Over current Protection

The device has over current protection to prevent damage to the device and inductor during over current conditions.

Peak current protection occurs at 4.3A. After V_{OUT} drops to about 60%, the output will be disabled. After being disabled for 10ms, the device will be re-enabled, and a new soft-start cycle will begin.

Power Good Indicator

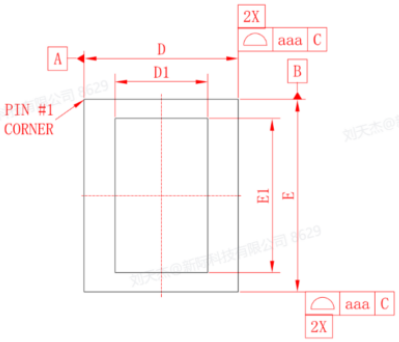
The device has a power-good output. The PG pin goes high impedance once the FB pin voltage is above 95% and less than 105% of the nominal voltage, and is driven low once the voltage falls below typically 91% or higher than 110% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power-good output requires a pullup resistor connecting to any voltage rail less than 5.5 V.
The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used. The PG rising edge has a 100-µs blanking time and the PG falling edge has a deglitch delay of 20 µs.

Output Discharge

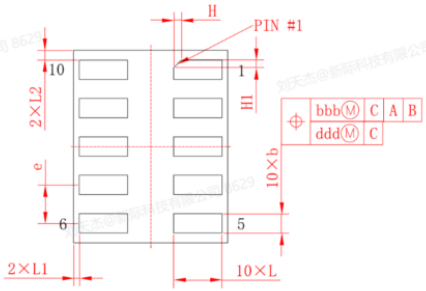
The purpose of the output discharge function is to ensure a defined down-ramp of the output voltage when the device is disabled and to keep the output voltage close to 0 V. The output discharge is active when the EN pin is set to a logic low and during thermal shutdown. The discharge is not active in UVLO.

PHYSICAL DIMENSIONS

Table: Chip Dimensions

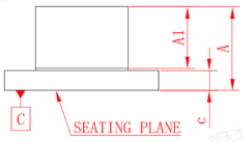


Top View



Bottom View

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.125	---	---	0.044
A1	---	---	0.800	---	---	0.031
c	0.225	0.255	0.285	0.009	0.010	0.011
D	1.950	2.000	2.050	0.077	0.079	0.081
E	2.450	2.500	2.550	0.096	0.098	0.100
D1	1.000	1.200	1.400	0.039	0.047	0.055
E1	1.800	2.000	2.200	0.071	0.079	0.087
H	---	0.100	---	---	0.004	---
H1	---	0.100	---	---	0.004	---
L	0.550	0.625	0.700	0.022	0.025	0.028
L1	0.000	0.075	0.150	0.000	0.003	0.006
L2	0.050	0.125	0.200	0.002	0.005	0.008
e	---	0.500	---	---	0.020	---
b	0.200	0.250	0.300	0.008	0.010	0.012
aaa		0.100			0.004	
bbb		0.150			0.006	
ddd		0.050			0.002	



Side View