

TPIC5421L H-BRIDGE GATE-PROTECTED LOGIC-LEVEL POWER DMOS ARRAY

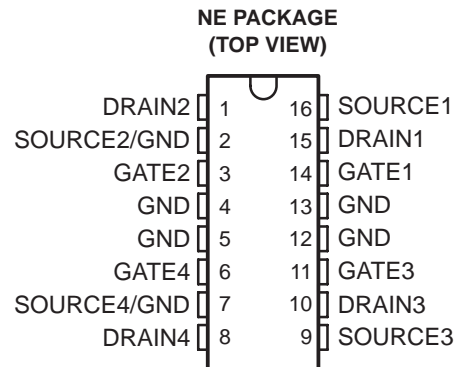
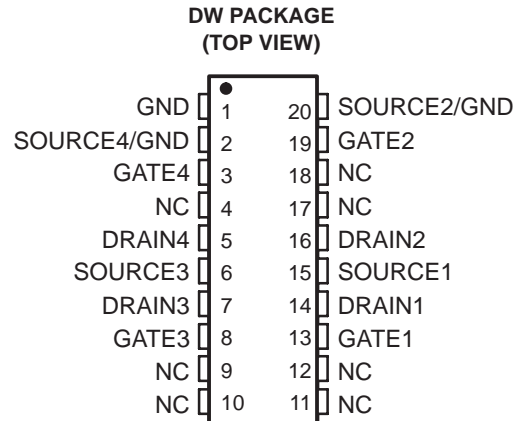
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- Low $r_{DS(on)}$. . . 0.4 Ω Typ
- Voltage Output . . . 60 V
- Input Protection Circuitry . . . 18 V
- Pulsed Current . . . 3 A Per Channel
- Extended ESD Capability . . . 4000 V
- Direct Logic-Level Interface

description

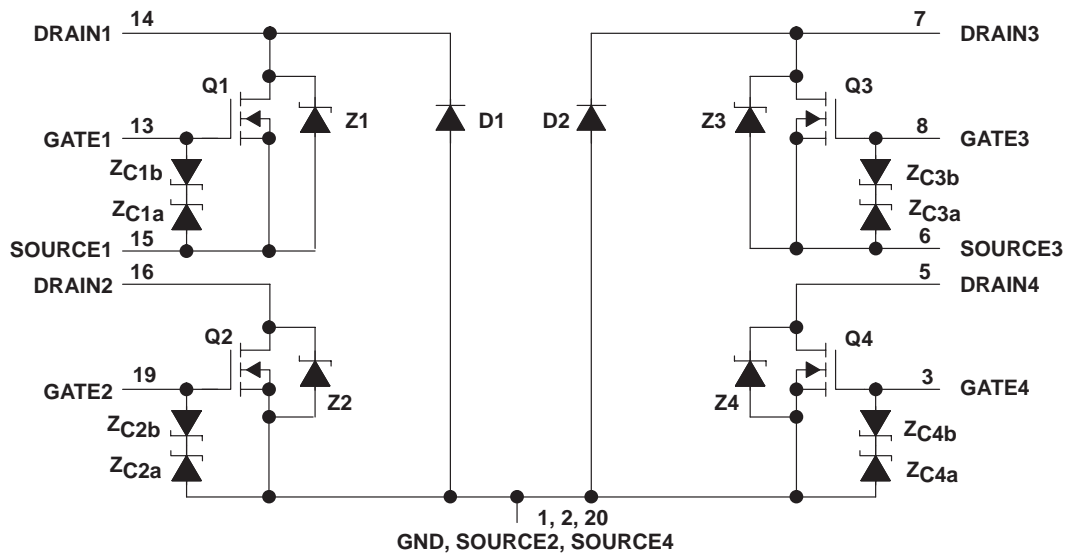
The TPIC5421L is a monolithic gate-protected logic-level power DMOS array that consists of four electrically isolated N-channel enhancement-mode DMOS transistors, two of which are configured with common source. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-k Ω resistor.

The TPIC5421L is offered in a 20-pin wide-body surface-mount (DW) package and a 16-pin thermally-enhanced dual-in-line (NE) package and is characterized for operation over the case temperature of -40°C to 125°C .



NC – No internal connection

schematic



NOTE A: For correct operation, no terminal may be taken below GND.
Pin numbers shown are for the DW package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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electrical characteristics, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	$I_D = 250\ \mu\text{A}$,	$V_{GS} = 0$	60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	$I_D = 1\ \text{mA}$, See Figure 5	$V_{DS} = V_{GS}$,	1.5	1.85	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	$I_{GS} = 250\ \mu\text{A}$		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	$I_{SG} = 250\ \mu\text{A}$		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND current = $250\ \mu\text{A}$		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	$I_D = 1\ \text{A}$, See Notes 2 and 3	$V_{GS} = 5\ \text{V}$,		0.4	0.475	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	$I_S = 1\ \text{A}$, $V_{GS} = 0$ (Z1, Z2, Z3, Z4), See Notes 2 and 3 and Figure 12			0.9	1.1	V
V_F	Forward on-state voltage, GND-to-drain	$I_D = 1\ \text{A}$ (D1, D2), See Notes 2 and 3			4.6		V
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = 48\ \text{V}$, $V_{GS} = 0$	$T_C = 25^\circ\text{C}$	0.05	1		μA
			$T_C = 125^\circ\text{C}$	0.5	10		
I_{GSSF}	Forward-gate current, drain short circuited to source	$V_{GS} = 15\ \text{V}$,	$V_{DS} = 0$		20	200	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	$V_{SG} = 5\ \text{V}$,	$V_{DS} = 0$		10	100	nA
I_{lkg}	Leakage current, drain-to-GND	$V_{DGND} = 48\ \text{V}$	$T_C = 25^\circ\text{C}$	0.05	1		μA
			$T_C = 125^\circ\text{C}$	0.5	10		
$r_{DS(on)}$	Static drain-to-source on-state resistance	$V_{GS} = 5\ \text{V}$, $I_D = 1\ \text{A}$, See Notes 2 and 3 and Figures 6 and 7	$T_C = 25^\circ\text{C}$	0.4	0.475		Ω
			$T_C = 125^\circ\text{C}$	0.65	0.68		
g_{fs}	Forward transconductance	$V_{DS} = 15\ \text{V}$, See Notes 2 and 3 and Figure 9	$I_D = 0.5\ \text{A}$,	1.25	1.4		S
C_{iss}	Short-circuit input capacitance, common source	$V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$,	$V_{GS} = 0$, See Figure 11		220	275	pF
C_{oss}	Short-circuit output capacitance, common source				120	150	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				100	125	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.

3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	$I_S = 0.5\ \text{A}$, $V_{GS} = 0$, See Figures 1 and 14	$V_{DS} = 48\ \text{V}$, $di/dt = 100\ \text{A}/\mu\text{s}$,	Z1 and Z3	55		ns
				Z2 and Z4	150		
				D1 and D2	200		
Q_{RR}	Total diode charge			Z1 and Z3	0.06		μC
				Z2 and Z4	0.3		
				D1 and D2	0.7		



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resistive-load switching characteristics, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 25\text{ V},$ $R_L = 25\ \Omega,$ $t_{r1} = 10\text{ ns},$ See Figure 2		25	50	ns
$t_{d(off)}$	Turn-off delay time			20	40	
t_{r2}	Rise time			21	42	
t_{f2}	Fall time			9	18	
Q_g	Total gate charge	$V_{DS} = 48\text{ V},$ See Figure 3 $I_D = 0.5\text{ A},$ $V_{GS} = 5\text{ V},$		3.9	5	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.55	0.8	
Q_{gd}	Gate-to-drain charge			2.5	3.6	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

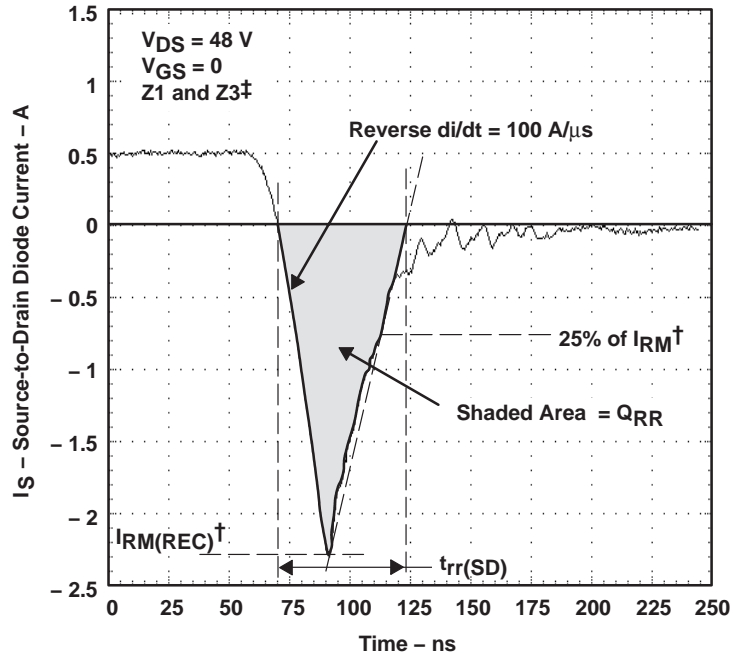
thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	DW package		90		$^\circ\text{C/W}$
		NE package	See Notes 4 and 6	60		
$R_{\theta JB}$	Junction-to-board thermal resistance	DW package	See Notes 4 and 6	53		
$R_{\theta JP}$	Junction-to-pin thermal resistance	DW package	See Notes 5 and 6	30		
		NE package		25		

- NOTES:
- Package mounted on an FR4 printed-circuit board with no heatsink.
 - Package mounted in intimate contact with infinite heatsink.
 - All outputs with equal power

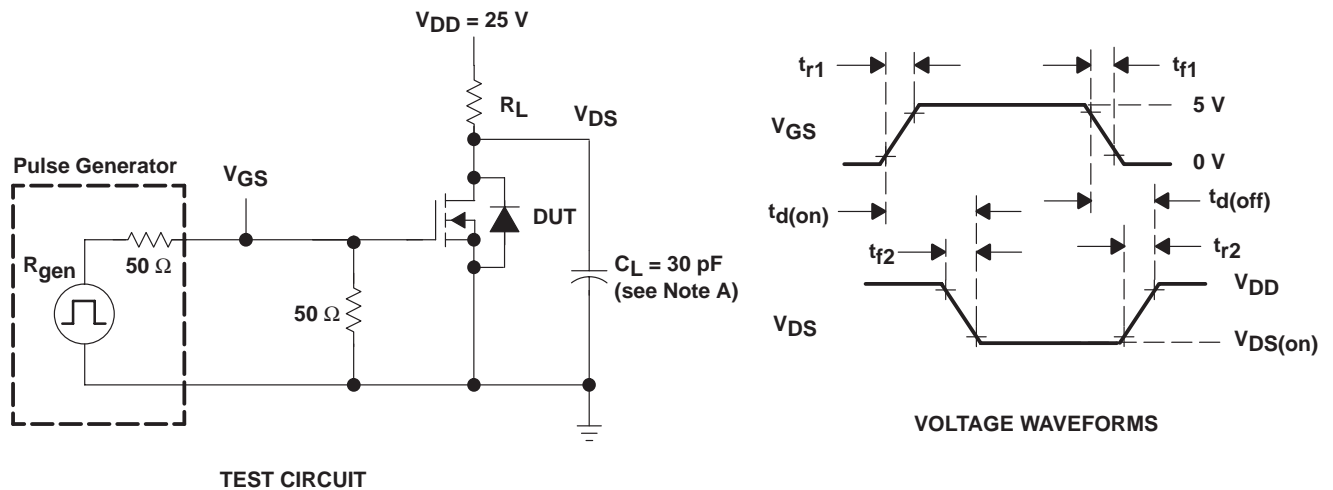


PARAMETER MEASUREMENT INFORMATION



† $I_{RM(REC)}$ = maximum recovery current
 ‡ The above waveform is representative of Z2, Z4, D1, and D2 in shape only.

Figure 1. Reverse-Recovery-Current Waveforms of Source-to-Drain Diode



TEST CIRCUIT

NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION

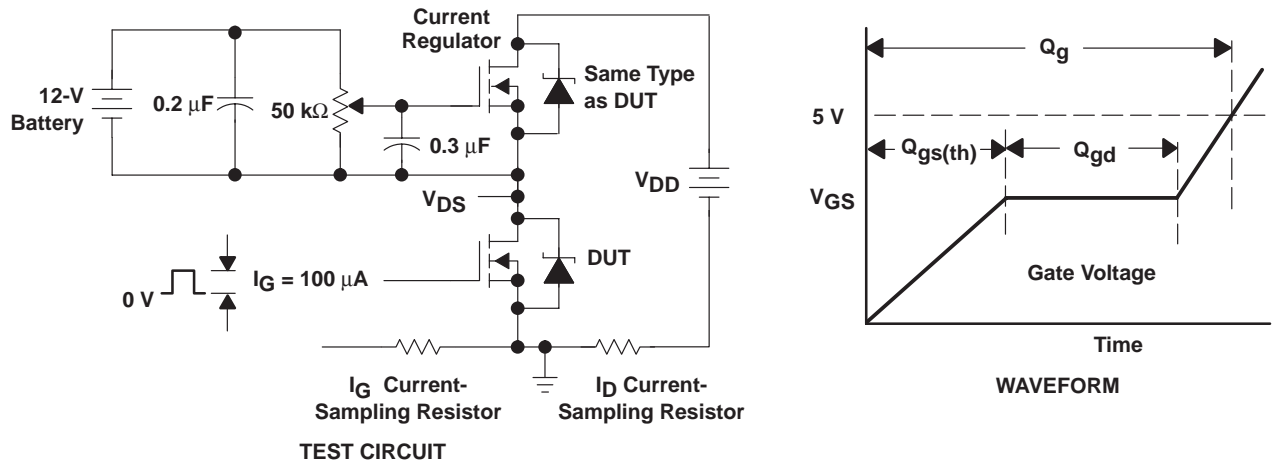
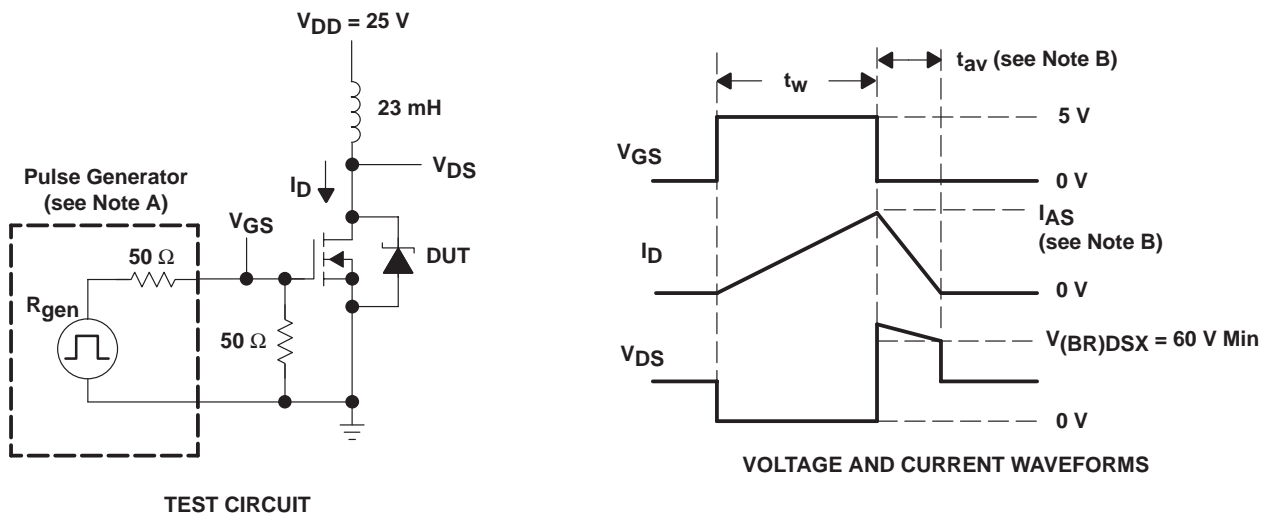


Figure 3. Gate-Charge Test Circuit and Waveform



- NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50 \Omega$.
 B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 3$ A.

Energy test level is defined as $E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 180$ mJ,
 where t_{av} = avalanche time

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

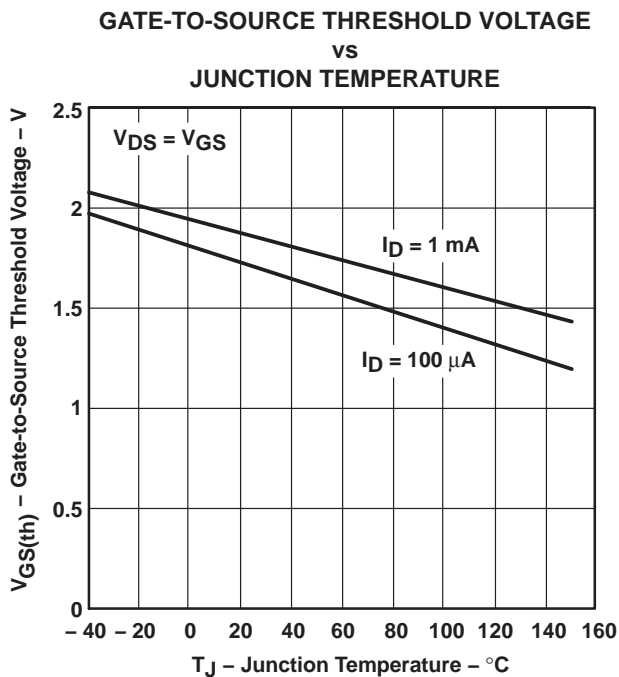


Figure 5

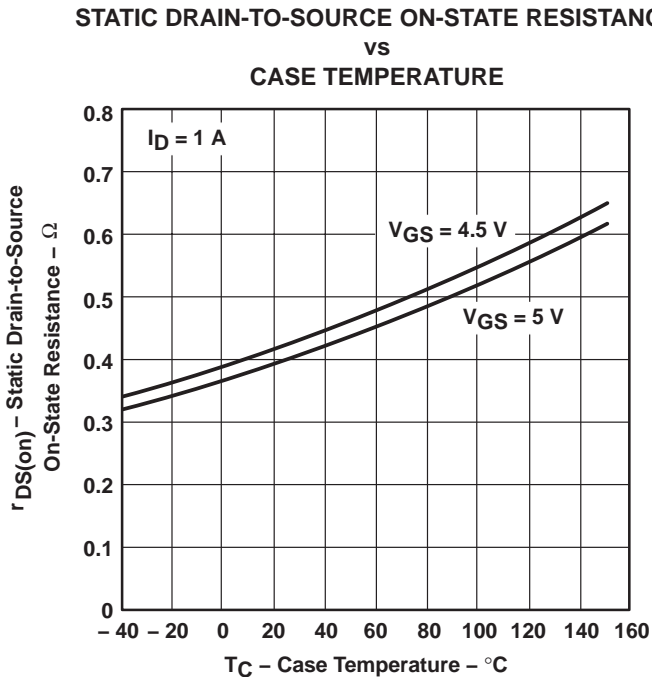


Figure 6

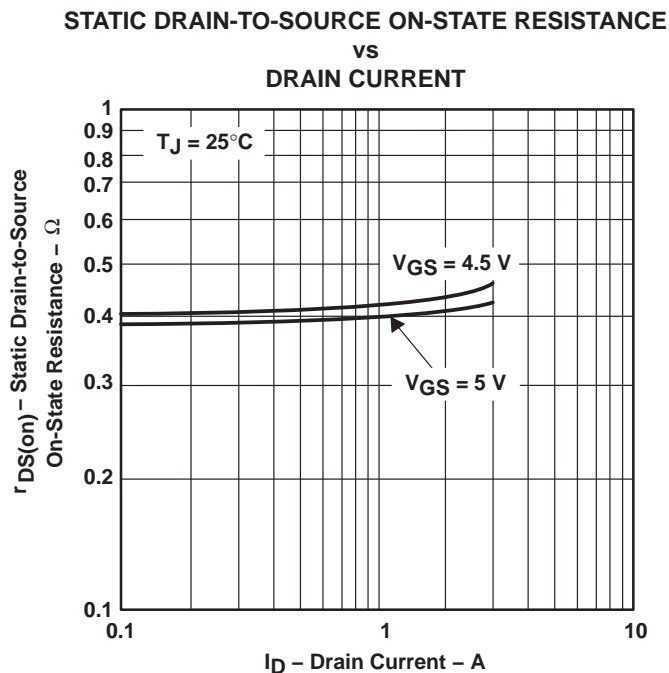


Figure 7

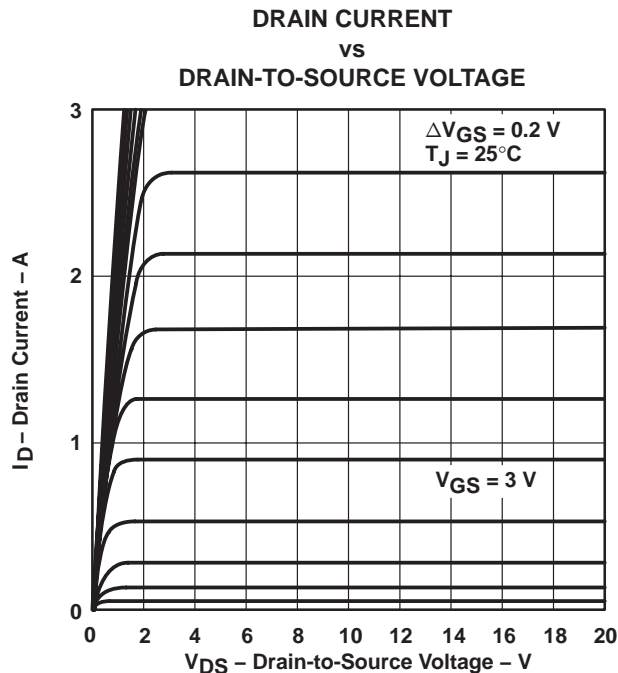


Figure 8

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TYPICAL CHARACTERISTICS

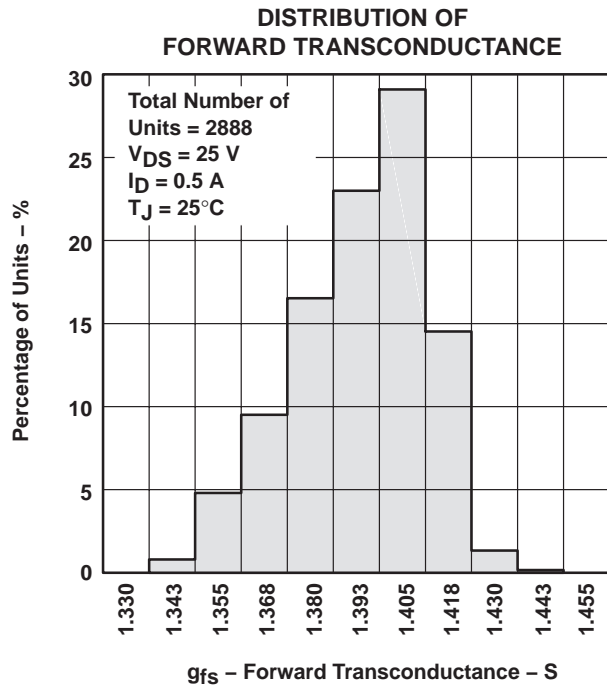


Figure 9

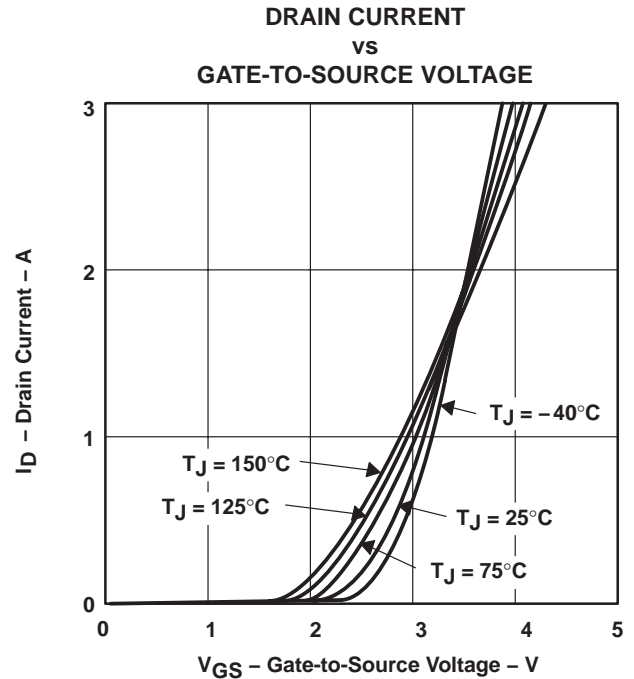


Figure 10

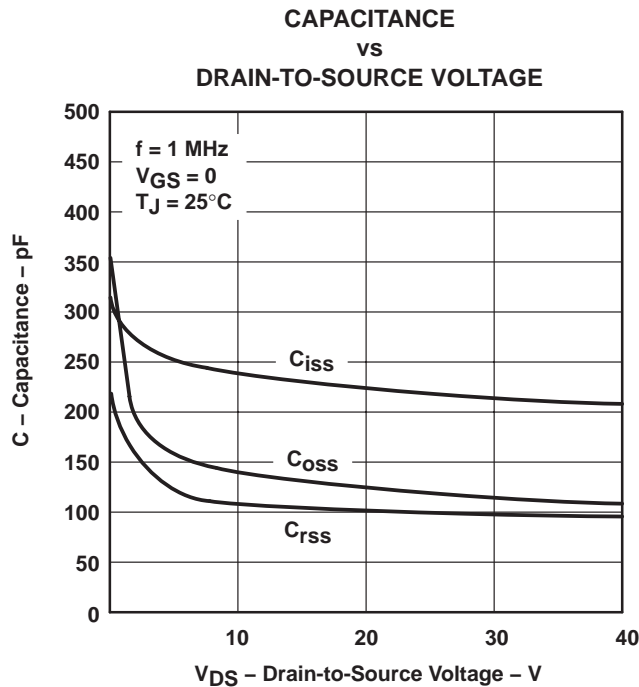


Figure 11

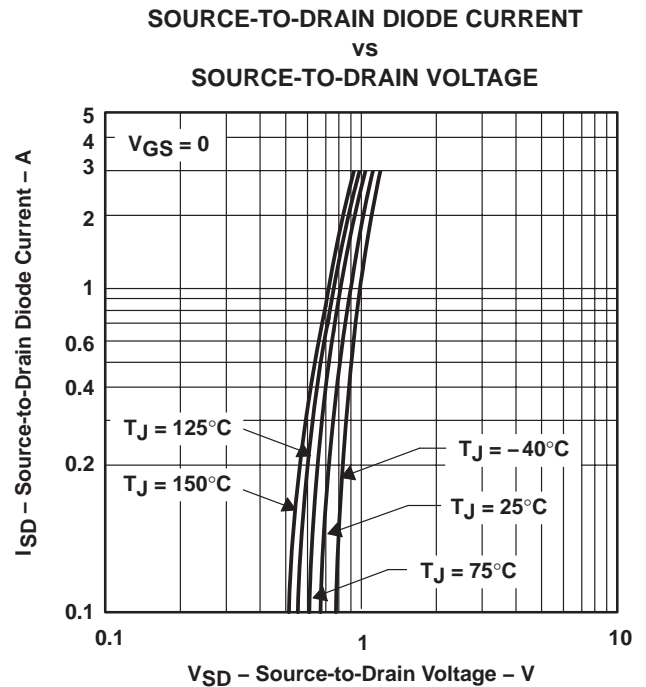


Figure 12

TYPICAL CHARACTERISTICS

**DRAIN-TO-SOURCE VOLTAGE AND
 GATE-TO-SOURCE VOLTAGE
 vs
 GATE CHARGE**

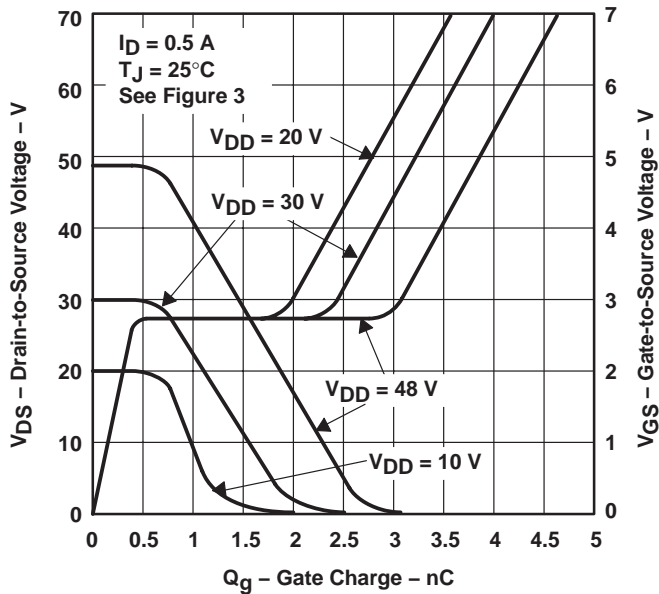


Figure 13

**REVERSE-RECOVERY TIME
 vs
 REVERSE di/dt**

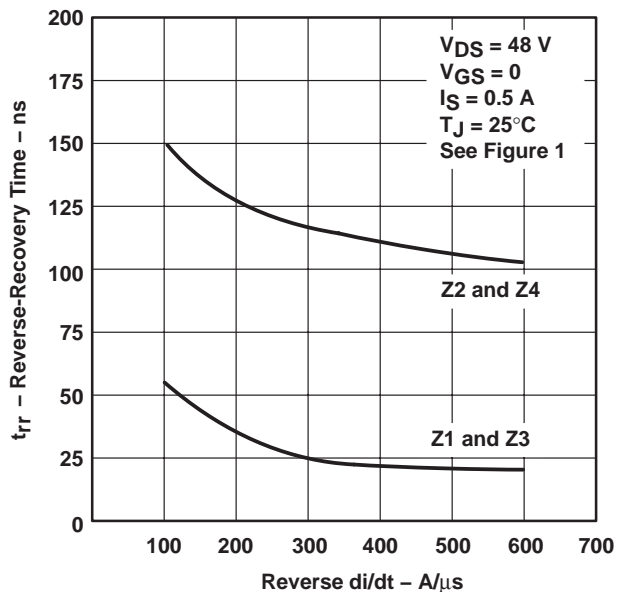


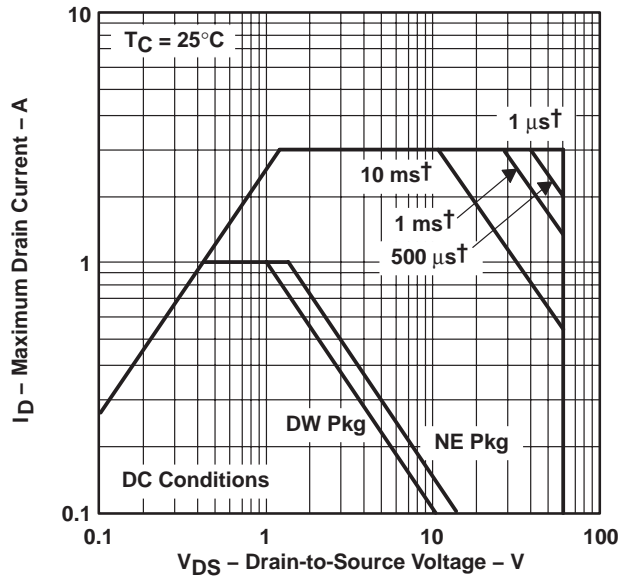
Figure 14

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THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle

Figure 15

MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

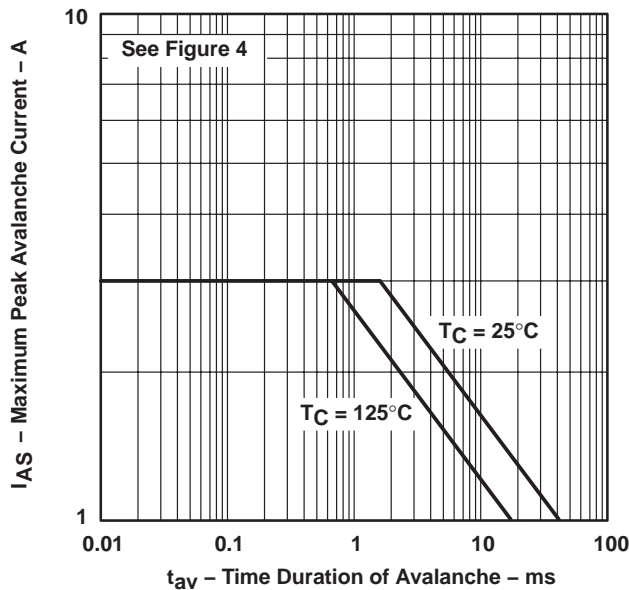
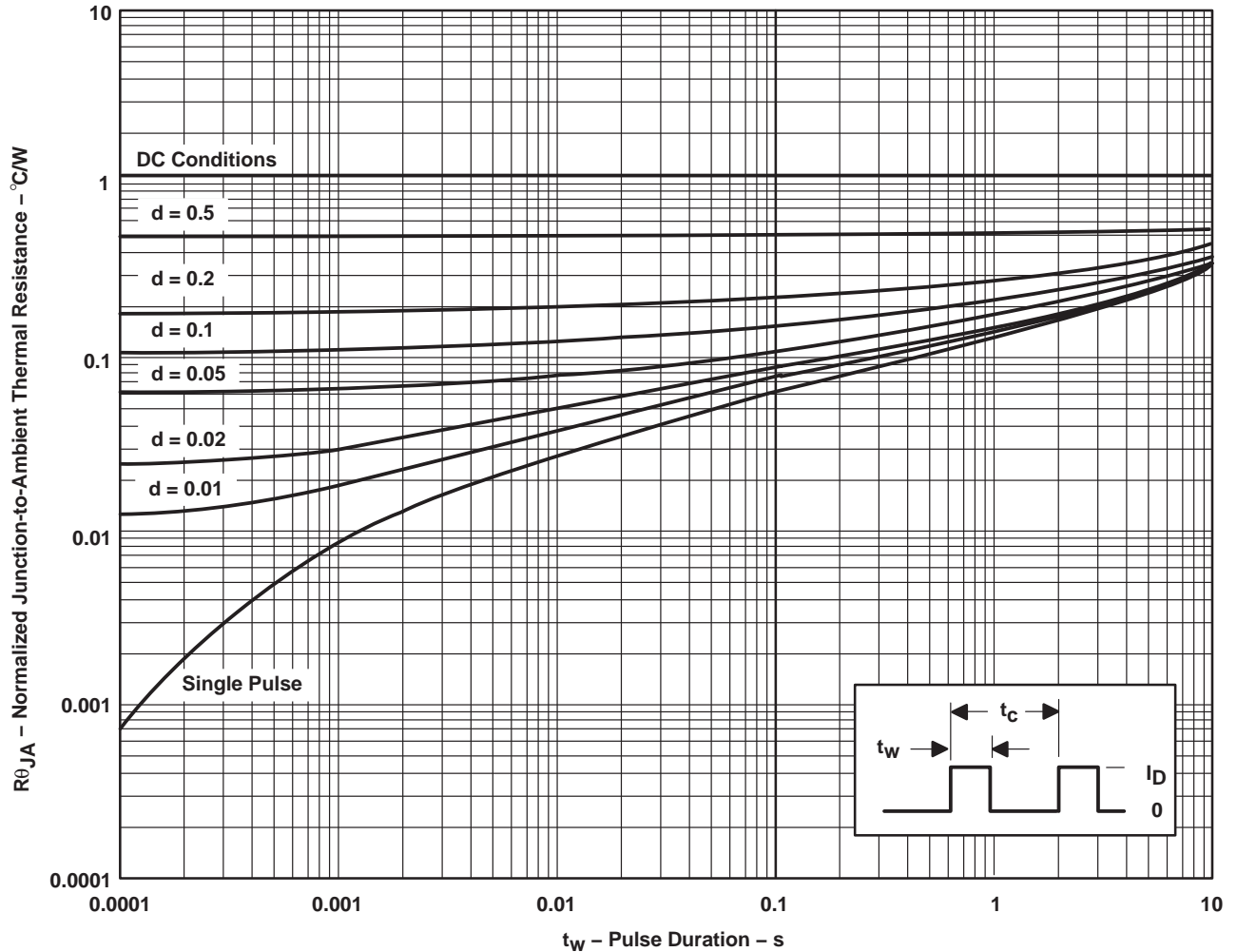


Figure 16

THERMAL INFORMATION

**NE PACKAGE†
 NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
 VS
 PULSE DURATION**



† Device mounted on FR4 printed-circuit board with no heatsink.

NOTES A: $Z_{\theta JA}(t) = r(t) R_{\theta JA}$
 t_w = pulse duration
 t_c = cycle time
 d = duty cycle = t_w/t_c

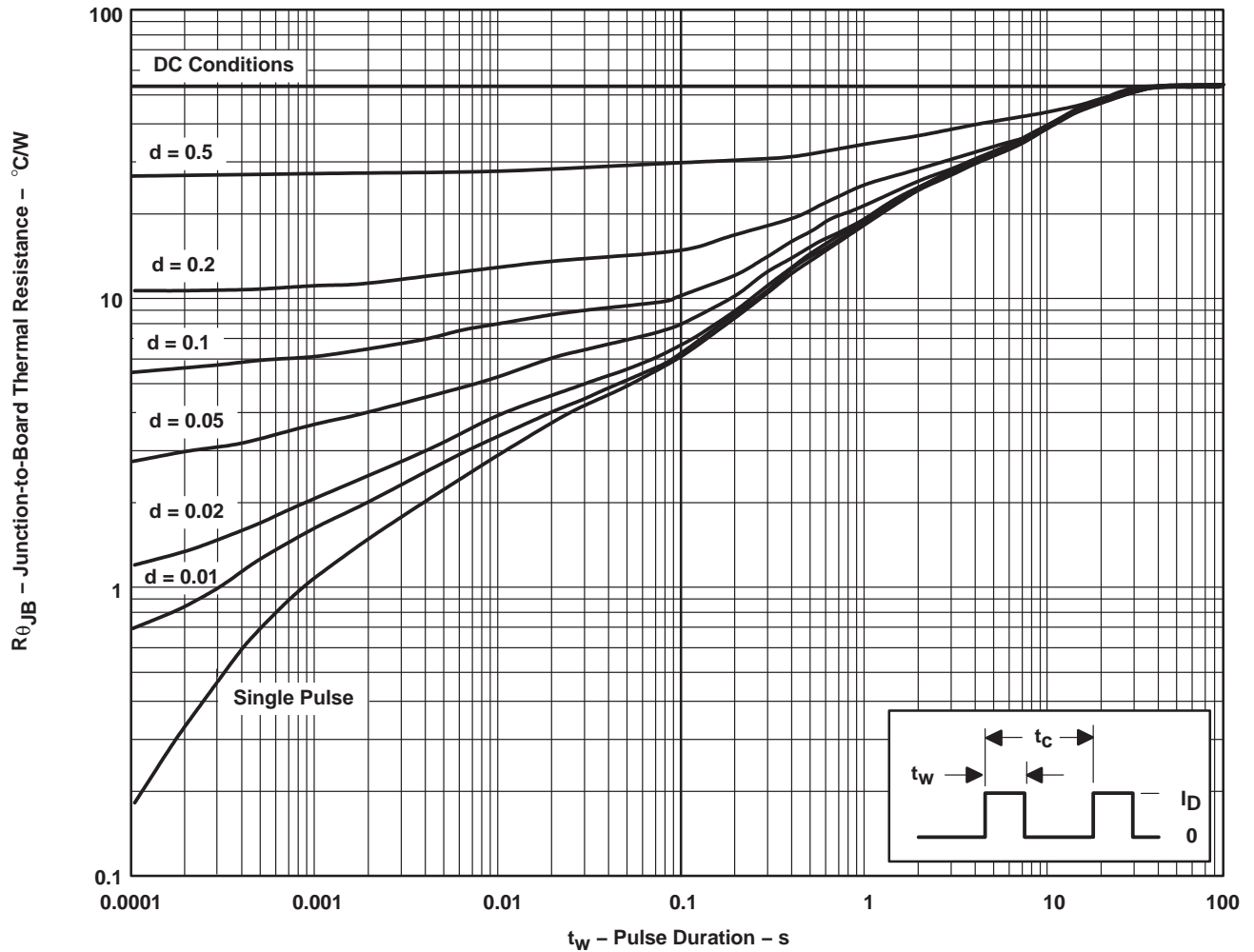
Figure 17

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THERMAL INFORMATION

DW PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
VS
PULSE DURATION



† Device mounted on a 24 in², 4-layer FR4 printed-circuit board with no heatsink.

NOTES A: $Z_{\theta JB}(t) = r(t) R_{\theta JB}$
 t_w = pulse duration
 t_c = cycle time
 d = duty cycle = t_w/t_c

Figure 18

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPIC5421LDW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
TPIC5421LNE	OBSOLETE	PDIP	NE	16		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

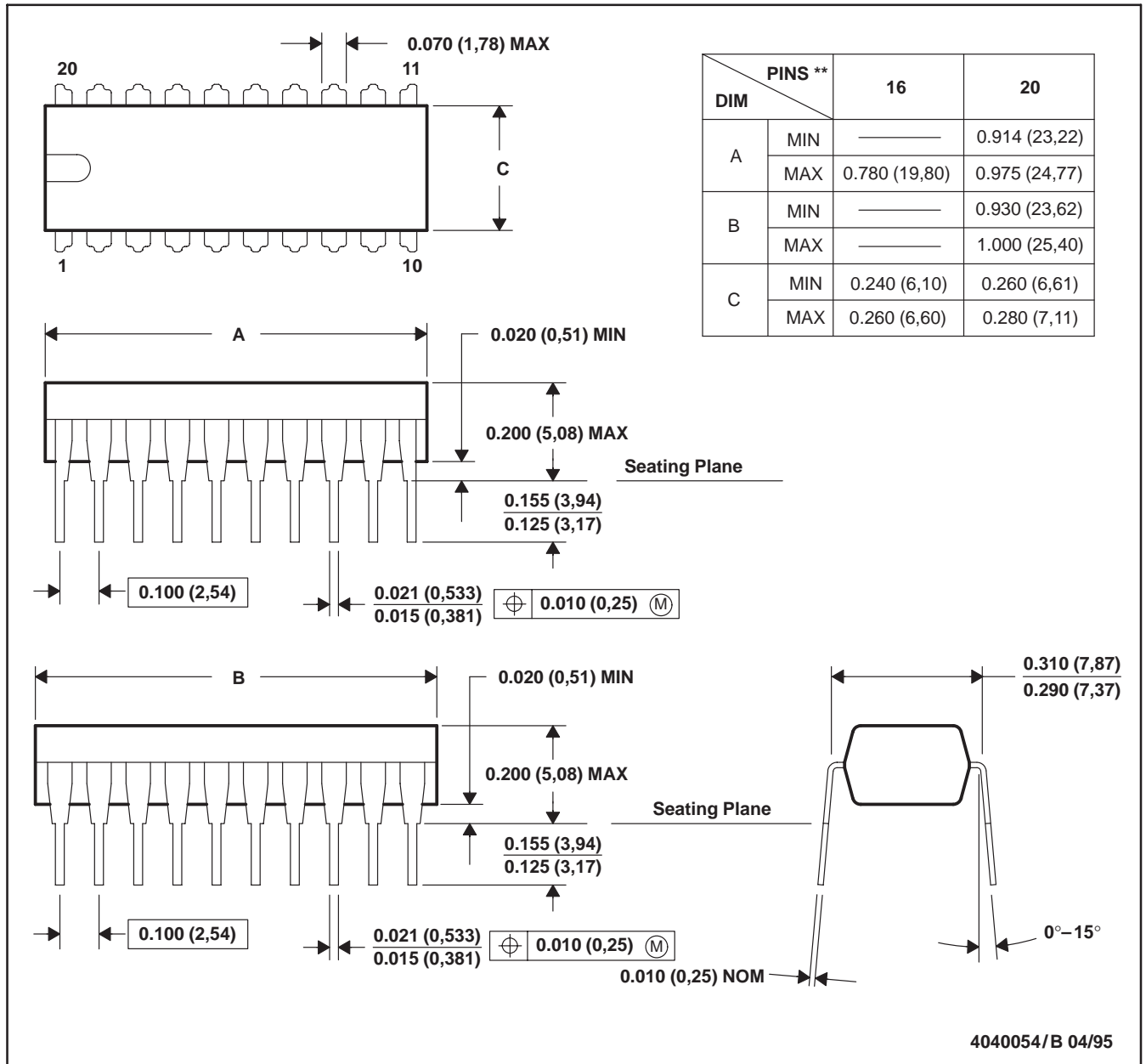
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NE (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 (16 pin only)

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