Buffer With Open-drain Output

Features

- Supply voltage range: 1.65V to 5.5V
- -32mA output drive at 4.5V
- IOFF supports partial-power-down mode operation
- CMOS low power consumption
- Direct interface with TTL levels
- Latch-up performance exceeds ±200mA
- ESD protection：

  Exceeds 2000V Human Body Model

  Exceeds 1500V Charged Device Model
- SOT353 2.07mm X1.26mm X1.1mm-5L package

Applications

- Desktop PCs and Notebooks
- CD/DVD ROM
- HDTV
- DVR

General Description

AWS74LVC1G07STR is a single buffer with open-drain output. The device accepts any supply voltage from 1.65V to 5.5V and the maximum sink current is 32mA.

The AWS74LVC1G07STR can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

The AWS74LVC1G07STR is fully specified for partial power-down applications using off output current (I_{OFF}).The outputs for this device enter a high-impedance state when the device is powered down, preventing any damaging backflow current through the device.

Typical Application Circuit

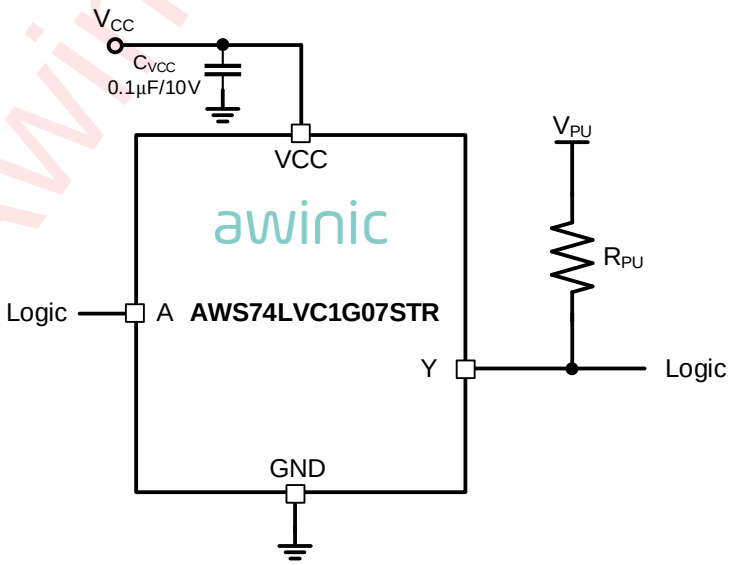

Figure 1 Typical Application

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Pin Configuration And Top Mark

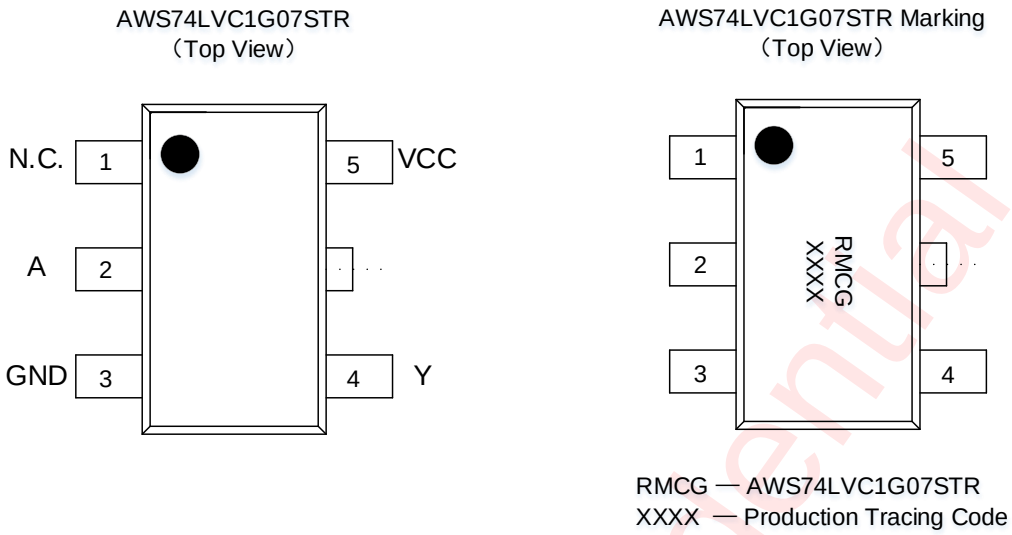

Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	N.C.	Not connected
2	A	Data input
3	GND	Ground
4	Y	Data output
5	VCC	Supply voltage

Pin Functions

Input A	Output Y
H	Hi-Z
L	L

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Functional Block Diagram

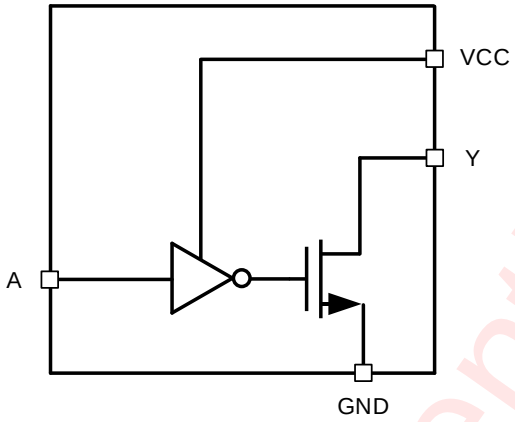

Figure 3 Functional Block Diagram

Typical Application Circuits

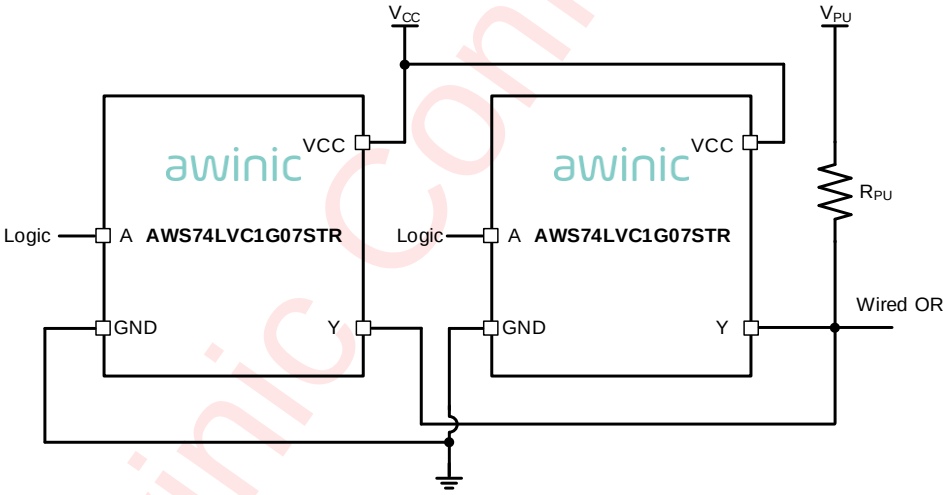

Figure 4 OR Gate Function Application

- ***Notice for typical application circuits:***

1. Figure 4 shows the AWS74LVC1G07STR being used in an active-low wired-OR functions, outputs should not be pulled above 6.5V.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWS74LVC1G07STR	-40°C~125°C	SOT353 2.07mmX1.26mm X1.1mm-5L	RMCG	MSL1	ROHS+HF	3000 units/ Tape and Reel

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Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage range, V_{CC}		-0.3V to 6.5V
Input voltage range		-0.3V to 6.5V
Output voltage range		-0.3V to 6.5V
Input clamp current, I_{Ik}	V_I <0	±50mA
Output clamp current, I_{OK}	V_O <0	±50mA
Output current, I_O	V_O =0V to 4.6V	50mA
Maximum operating junction temperature T_{JMAX}		150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD		
HBM (All pins, per JEDEC JS-001) (NOTE 2)		±2kV
CDM (All pins, per JEDEC JS-002-2018)		±1.5kV
Latch-Up		
Test condition: JESD78E		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

Recommended Operating Conditions

PARAMETERS		CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
V_I	Input voltage(NOTE1)		0	5.5	V
V_O	Output voltage		0	5.5	V
Δt/ΔV	Input transition rise or fall rate	V_{CCI} =1.65V to 2.7V		20	ns/V
		V_{CCI} =3.3V		10	ns/V
T_A	Operating junction temperature T_A		-40	125	°C

NOTE1: All unused data inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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Electrical Characteristics

T_A=25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS							
I_{CC}	VCC supply current	V_I=0V or 5.5V, I_O=0A; V_{CC}=1.65V to 5.5V			0.1		μA
ΔI_{CC}	Additional supply current	V_I= V_{CC} – 0.3V, I_O=0A; V_{CC}=2.3V to 5.5V			0.5		μA
I_I	Input leakage current	V_I=0V or 5.5V; V_{CC}=1.65V to 5.5V			0.1		μA
I_{OZ}	OFF-state output current	V_I=V_{IH}; V_O=V_{CC} or GND; V_{CC}=5.5V			±0.05		μA
I_{OFF}	Power off leakage current	V_I or V_O=5.5V; V_{CC}=0V			±0.05		μA
V_{IH}	High-level input voltage	V_{CC}=1.65V to 1.95V		0.65V_{CCI}			V
		V_{CC}=2.3V to 2.7V		1.6			
		V_{CC}=3.0V to 3.6V		2.0			
		V_{CC}=4.5V to 5.5V		0.7V_{CCI}			
V_{IL}	Low-level input voltage	V_{CC}=1.65V to 1.95V				0.35V_{CCI}	V
		V_{CC}=2.3V to 2.7V				0.7	
		V_{CC}=3.0V to 3.6V				0.9	
		V_{CC}=4.5V to 5.5V				0.3V_{CCI}	
V_{OL}	Low-level output voltage	V_I=V_{IL}	I_O= 100μA; V_{CC}=1.65V to 5.5V			0.1	V
			I_O= 4mA; V_{CC} =1.65V			0.45	
			I_O= 8mA; V_{CC} =2.3V			0.3	
			I_O= 16mA; V_{CC} =3.0V			0.4	
			I_O= 24mA; V_{CC} =3.0V			0.55	
			I_O= 32mA; V_{CC} =4.5V			0.55	
C_I(1)	Input capacitance	V_I=0V or 3.3V, V_{CC}=3.3V			2.0		pF
SWITICHING CHARACTERISTICS							
t_{pd}(2)	Propagation delay	V_{CC}=1.65V to 1.95V			5.7		ns
		V_{CC}=2.3V to 2.7V			4.5		
		V_{CC}=3V to 3.6V			4.1		
		V_{CC}=4.5V to 5.5V			3.6		

(1) Typical value set by simulation only.

(2) Typical values are measured at V_{CC}=1.8V, 2.5V, 3.3V and 5.0V respectively.

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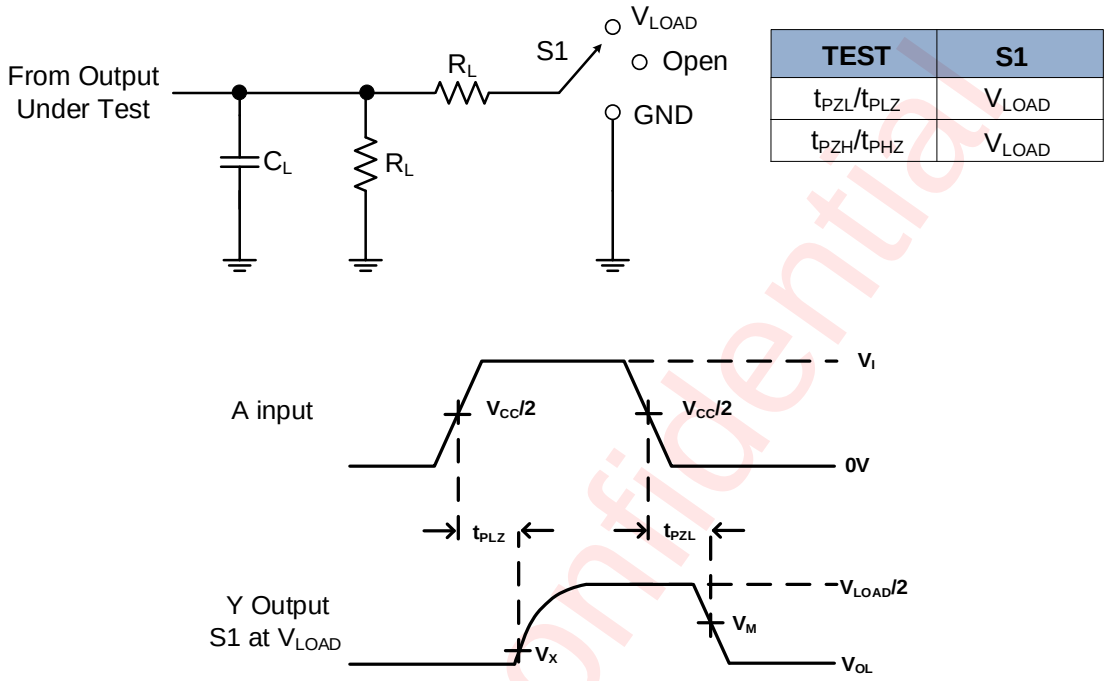
Typical Characteristic

TEST INFORMATION



TEST	S1
t_{PZL}/t_{PLZ}	V_{LOAD}
t_{PZH}/t_{PHZ}	V_{LOAD}

Figure 5 Load Circuit and Propagation Delay Measurement

1. The following table gives the test condition under different supply voltage：

V_{CC}	Input		V_M	R_L	C_L	V_{LOAD}	V_X
	V_I	t_r/t_f					
1.65V to 1.95V	V_{CC}	≤2.0ns	$V_{CC}/2$	1kΩ	30pF	$2\times V_{CC}$	$V_{OL}+0.15V$
2.3V to 2.7V	V_{CC}	≤2.0ns	$V_{CC}/2$	500Ω	30pF	$2\times V_{CC}$	$V_{OL}+0.15V$
3.0V to 3.6V	3V	≤2.5ns	$V_{CC}/2$	500Ω	50pF	6V	$V_{OL}+0.3V$
4.5V to 5.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	500Ω	50pF	$2\times V_{CC}$	$V_{OL}+0.3V$

2. Load capacitance including probe and jig capacitance.

2. t_{PZL} is measured at V_M.

3. t_{PLZ} is measured at V_X.

4. For the open drain device t_{PZL} and t_{PLZ} are same as t_{pd}.

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Detailed Functional Description

AWS74LVC1G07STR is a single buffer with open-drain output. The device accepts any supply voltage from 1.65V to 5.5V and the maximum sink current is 32mA.

The AWS74LVC1G07STR can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The device is fully specified for partial power-down applications using off output current (I_{OFF}).The outputs for this device enter a high-impedance state when the device is powered down, preventing any damaging backflow current through the device.

Functional Modes

Input A	Output Y
H	Hi-Z
L	L

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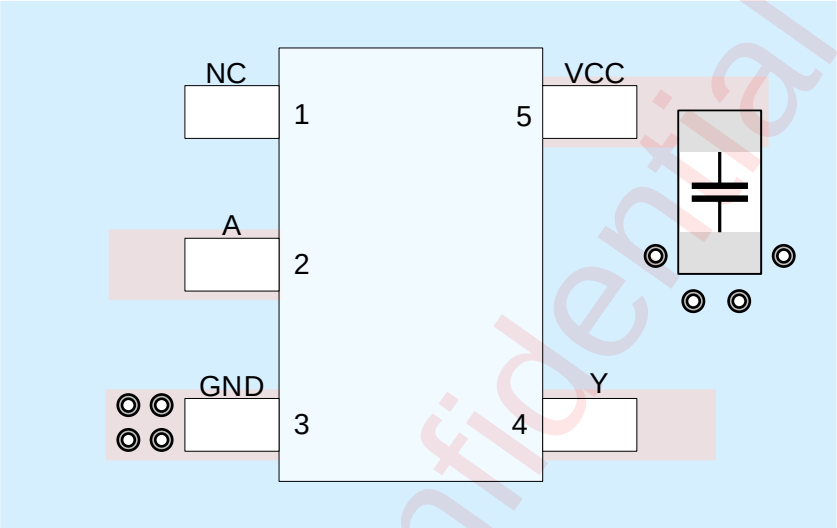
PCB Layout Consideration

To obtain the optimal performance of AWS74LVC1G07STR, PCB layout should be considered carefully. Here are some guidelines:

1. We recommend adding a 0.1μF bypass capacitor to prevent power disturbance. The C_{VCC} should be placed as close to the VCC pin as possible.



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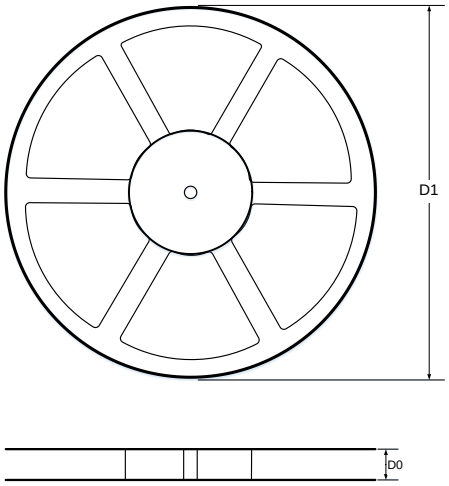
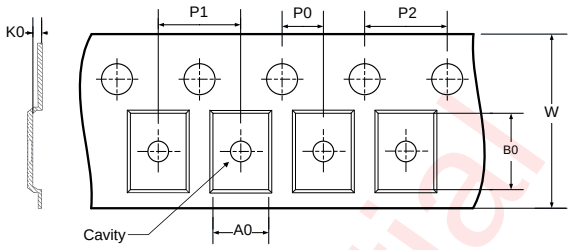
Tape And Reel Information

REEL DIMENSIONS

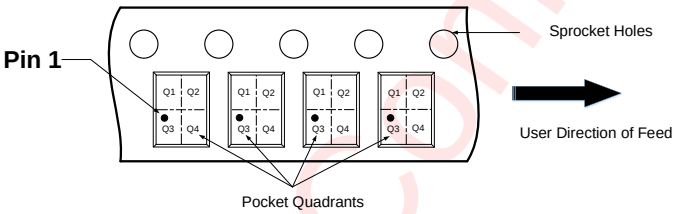


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178.0	8.40	2.40	2.55	1.20	2.00	4.00	4.00	8.00	Q3

All dimensions are nominal

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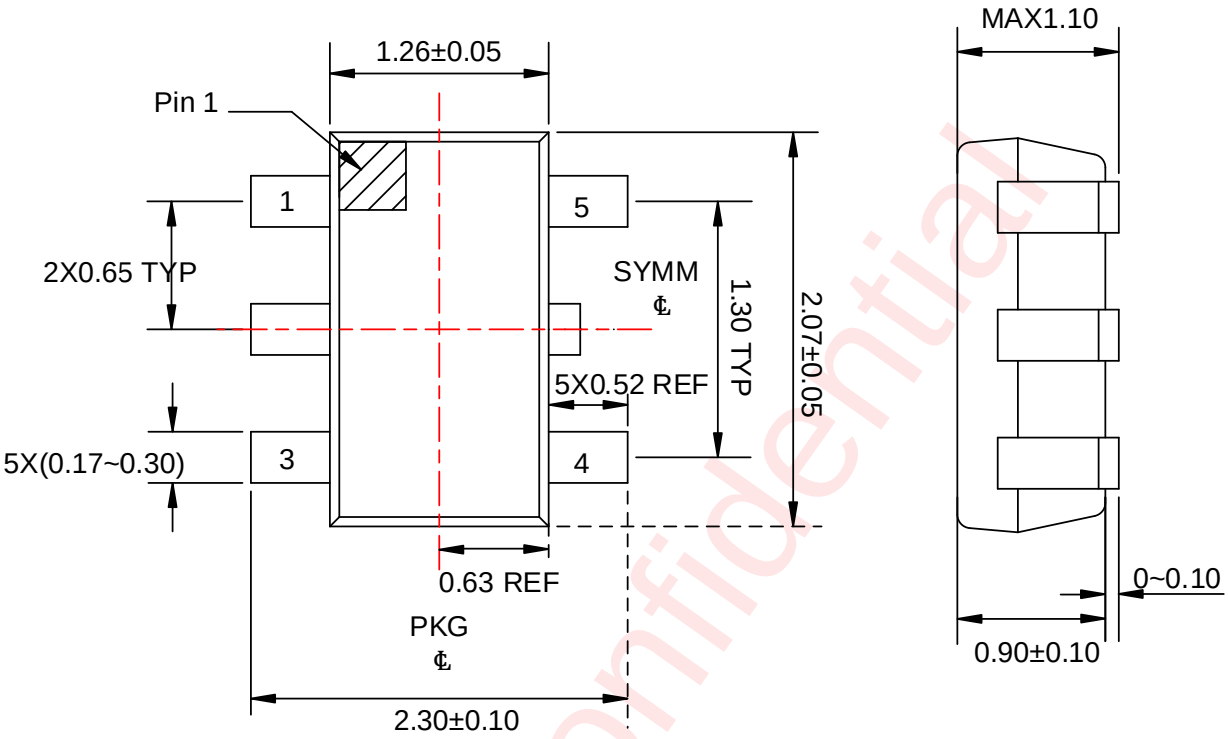
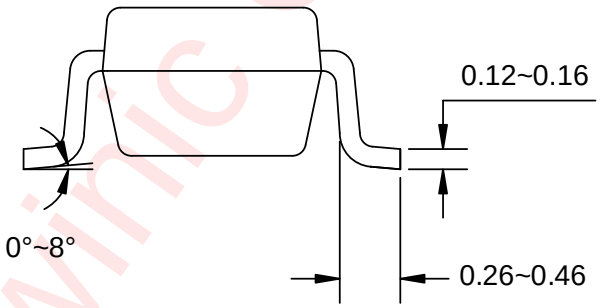
Package Description





Unit: mm

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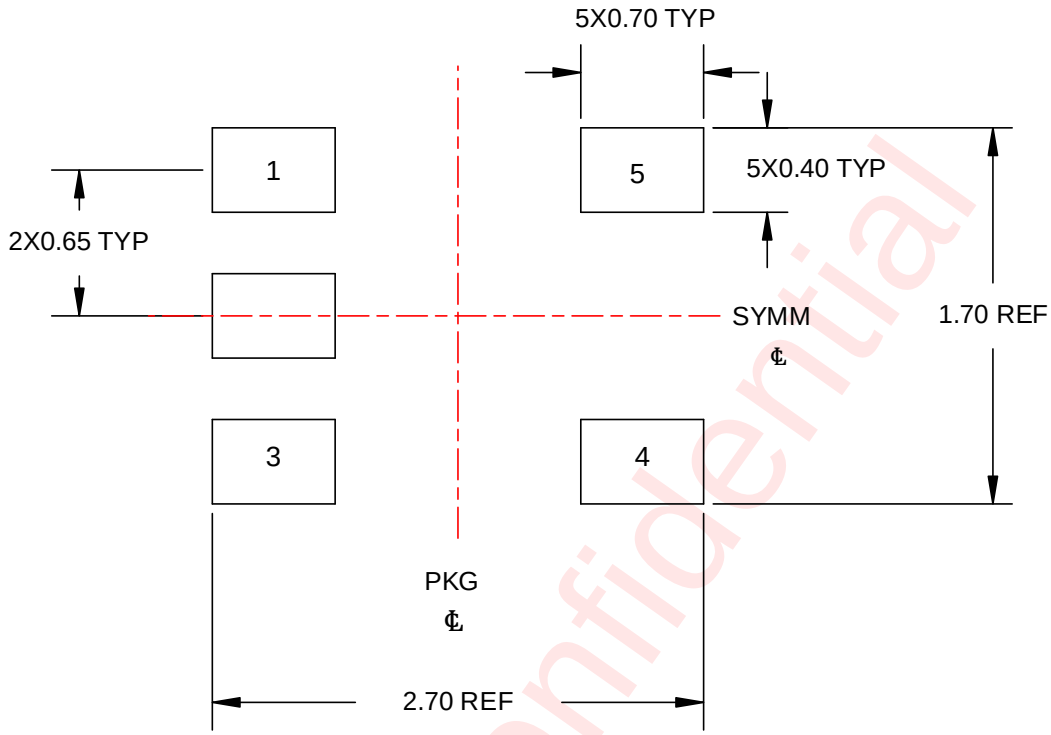
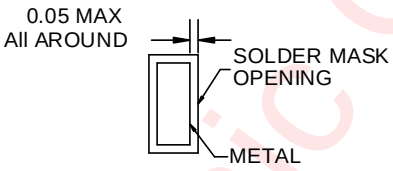
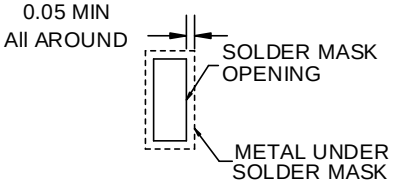
Land Pattern Data





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit：mm

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Revision History

Version	Date	Change Record
V1.0	Feb. 2022	Officially released
V1.1	Jan. 2023	Updated V_{OL} test condition(P5)
V1.2	Feb. 2025	1. Update Supply Voltage Range(P1 P4) 2. Update Absolute Maximum Ratings(P4) 3. Update Typical Application(P1) 4. Update Electrical Characteristics(P5)

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