



钜地半导体
Tudi Semiconductor

Product Specification

TUDI-AT24C512-10PU-1.8/2.7

Two-wire Serial EEPROM

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**semiconductor device
manufacturer**

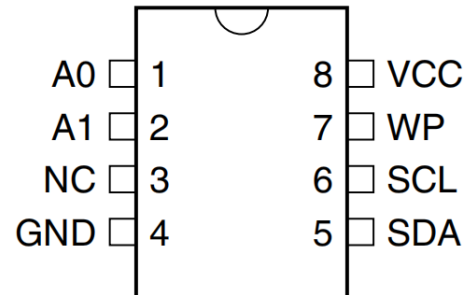
- Design
- research and development
- production
- and sales



Features

- Low-voltage and Standard-voltage Operation
 - 2.7 ($V_{CC} = 2.7V$ to $5.5V$)
 - 1.8 ($V_{CC} = 1.8V$ to $3.6V$)
- Internally Organized 65,536 x 8
- Two-wire Serial Interface
- Schmitt Triggers, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1 MHz (5V), 400 kHz (2.7V) and 100 kHz (1.8V)
- Compatibility
 - Write Protect Pin for Hardware and Software Data Protection
 - 128-byte Page Write Mode (Partial Page Writes Allowed)
 - Self-timed Write Cycle (5 ms Max)
 - High Reliability
 - Endurance: 100,000 Write Cycles
 - Data Retention: 40 Years
 - Automotive Grade, Extended Temperature and Lead-free/Halogen-free Devices Available
 - 8-lead PDIP, 8-lead EIAJ SOIC, 8-lead JEDEC SOIC, 8-lead TSSOP, 8-lead LAP, 8-lead SAP and 8-ball dBG2 Packages
 - Die Sales: Wafer Form, Waffle Pack and Bumped Die

8-lead PDIP



Description

The AT24C512 provides 524,288 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 65,536 words of 8 bits each. The device's cascadable feature allows up to four devices to share a common two-wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The devices are available in space-saving 8-pin PDIP, 8-lead EIAJ SOIC, 8-lead JEDEC SOIC, 8-lead TSSOP, 8-lead Leadless Array (LAP), and 8-lead SAP packages. In addition, the entire family is available in 2.7V (2.7V to 5.5V) and 1.8V (1.8V to 3.6V) versions.

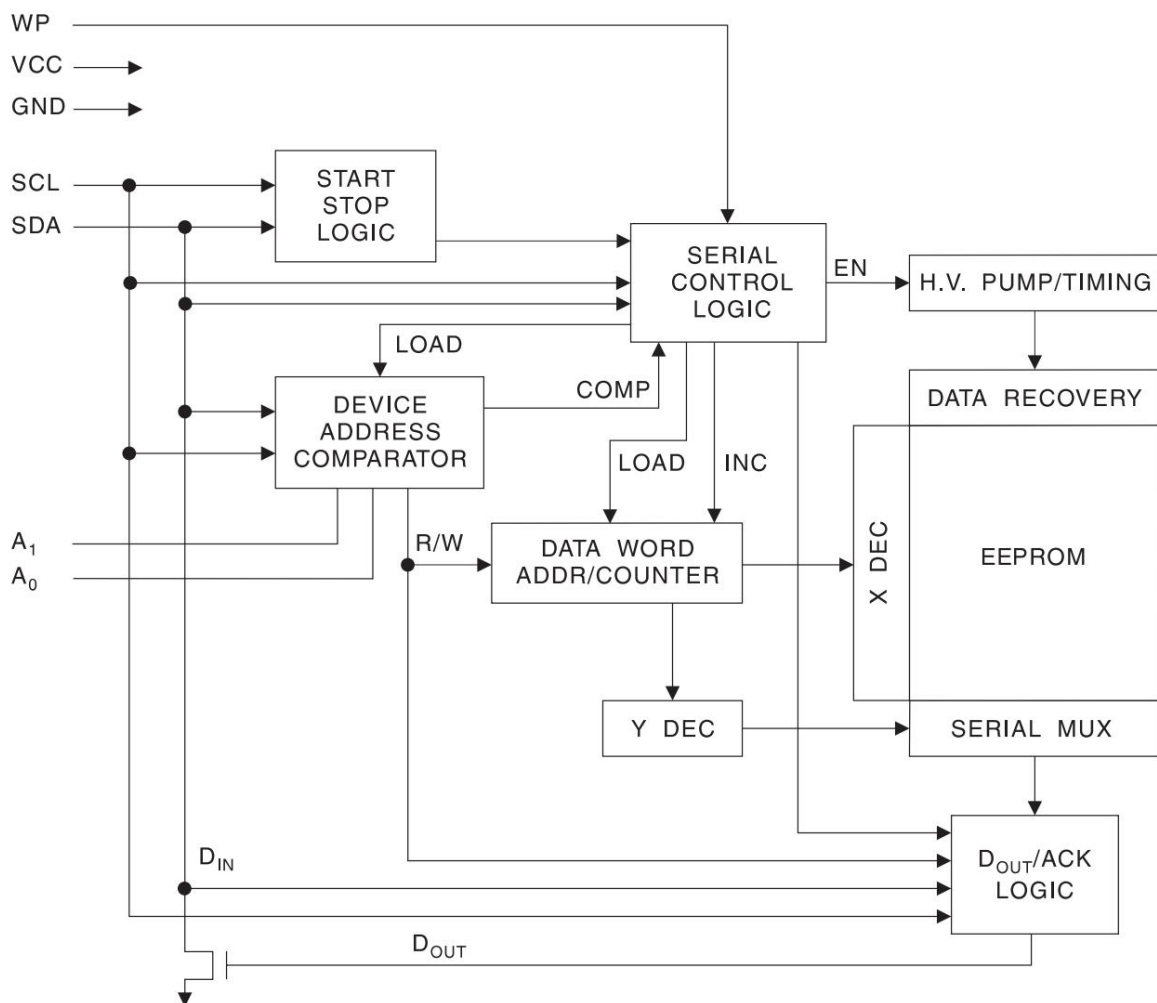


Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current.....	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1. Block Diagram





Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/ADDRESSES (A1, A0): The A1 and A0 pins are device address inputs that are hardwired or left not connected for hardware compatibility with other AT24Cxx devices. When the pins are hardwired, as many as four 512K devices may be addressed on a single bus system (device addressing is discussed in detail under the *Device Addressing section*. If the pins are left floating, the A1 and A0 pins will be internally pulled down to GND if the capacitive coupling to the circuit board V_{CC} plane is <3 pF. If coupling is >3 pF, Atmel recommends connecting the address pins to GND.

WRITE PROTECT (WP): The write protect input, when connected to GND, allows normal write operations. When WP is connected high to V_{CC} , all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND if the capacitive coupling to the circuit board V_{CC} plane is <3 pF. If coupling is >3 pF, Atmel recommends connecting the pin to GND. Switching WP to V_{CC} prior to a write operation creates a software write protect function.

Memory Organization

AT24C512, 512K SERIAL EEPROM: The 512K is internally organized as 512 pages of 128-bytes each. Random word addressing requires a 16-bit data word address.



Table 2. Pin Capacitance⁽¹⁾

Applicable over recommended operating range from $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$, $V_{CC} = +1.8\text{V}$

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O} = 0\text{V}$
C_{IN}	Input Capacitance (A_0 , A_1 , SCL)	6	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested.

Table 3. DC Characteristics

Applicable over recommended operating range from: $T_{AI} = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$, $T_{AC} = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$ (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		3.6	V
V_{CC2}	Supply Voltage			2.7		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC1}	Supply Current	$V_{CC} = 5.0\text{V}$	READ at 400 kHz		1.0	2.0	mA
I_{CC2}	Supply Current	$V_{CC} = 5.0\text{V}$	WRITE at 400 kHz		2.0	3.0	mA
I_{SB1}	Standby Current (1.8V option)	$V_{CC} = 1.8\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}			1.0	μA
		$V_{CC} = 3.6\text{V}$				3.0	
I_{SB2}	Standby Current (2.7V option)	$V_{CC} = 2.7\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}			2.0	μA
		$V_{CC} = 5.5\text{V}$				6.0	
I_{SB3}	Standby Current (5.0V option)	$V_{CC} = 4.5 - 5.5\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}			6.0	μA
I_{LI}	Input Leakage Current	$V_{IN} = V_{CC}$ or V_{SS}			0.10	3.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or V_{SS}			0.05	3.0	μA
V_{IL}	Input Low Level ⁽¹⁾			-0.6		$V_{CC} \times 0.3$	V
V_{IH}	Input High Level ⁽¹⁾			$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL2}	Output Low Level	$V_{CC} = 3.0\text{V}$	$I_{OL} = 2.1\text{ mA}$			0.4	V
V_{OL1}	Output Low Level	$V_{CC} = 1.8\text{V}$	$I_{OL} = 0.15\text{ mA}$			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.



Table 4. AC Characteristics

Applicable over recommended operating range from $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$, $C_L = 100\text{ pF}$ (unless otherwise noted) Test conditions are listed in Note 2.

Symbol	Parameter	1.8 Volt		2.7 Volt		5.0 Volt		Units
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	4.7		1.3		0.4		μs
t_{HIGH}	Clock Pulse Width High	4.0		1.0		0.4		μs
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.05	0.9	0.05	0.55	μs
t_{BUF}	Time the bus must be free before a new transmission can start ⁽¹⁾	4.7		1.3		0.5		μs
$t_{HD.STA}$	Start Hold Time	4.0		0.6		0.25		μs
$t_{SU.STA}$	Start Set-up Time	4.7		0.6		0.25		μs
$t_{HD.DAT}$	Data In Hold Time	0		0		0		μs
$t_{SU.DAT}$	Data In Set-up Time	200		100		100		ns
t_R	Inputs Rise Time ⁽¹⁾		1.0		0.3		0.3	μs
t_F	Inputs Fall Time ⁽¹⁾		300		300		100	ns
$t_{SU.STO}$	Stop Set-up Time	4.7		0.6		0.25		μs
t_{DH}	Data Out Hold Time	100		50		50		ns
t_{WR}	Write Cycle Time		20 or 5 ⁽³⁾		10 or 5 ⁽³⁾		10 or 5 ⁽³⁾	ms
Endurance ⁽¹⁾	5.0V, 25°C, Page Mode	100K		100K		100K		Write Cycles

- Notes:
1. This parameter is characterized and is not 100% tested.
 2. AC measurement conditions:
 R_L (connects to V_{CC}): 1.3 k Ω (2.7V, 5V), 10 k Ω (1.8V)
 Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}
 Input rise and fall times: $\leq 50\text{ ns}$
 Input and output timing reference voltages: 0.5 V_{CC}
 3. The Write Cycle Time of 5 ms only applies to the AT24C512 devices bearing the process letter "A" on the package (the mark is located in the lower right corner on the top side of the package).



Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 4 on page 7). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 5 on page 8).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 5 on page 8).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

STANDBY MODE: The AT24C512 features a low power standby mode which is enabled: a) upon power-up and b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

(a) Clock up to 9 cycles, (b) look for SDA high in each cycle while SCL is high and then (c) create a start condition as SDA is high.



Figure 2. Bus Timing (SCL: Serial Clock, SDA: Serial Data I/O)

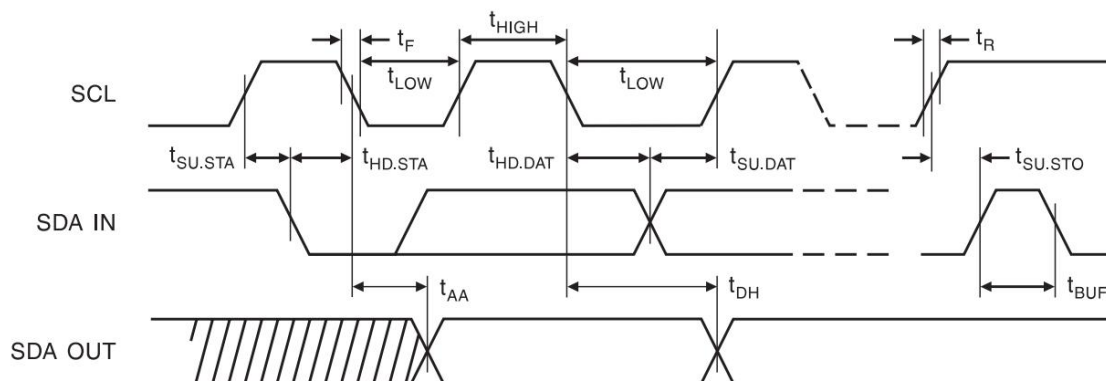
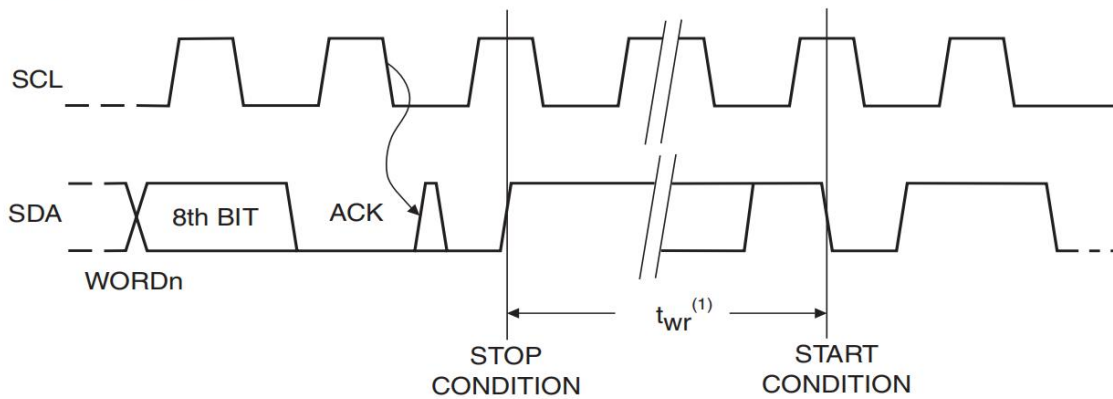


Figure 3. Write Cycle Timing (SCL: Serial Clock, SDA: Serial Data I/O)



Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Figure 4. Data Validity

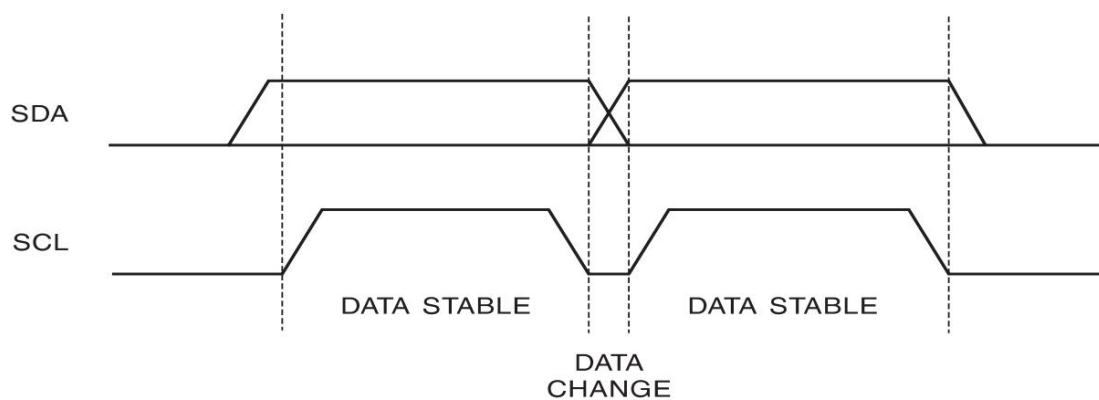




Figure 5. Start and Stop Definition

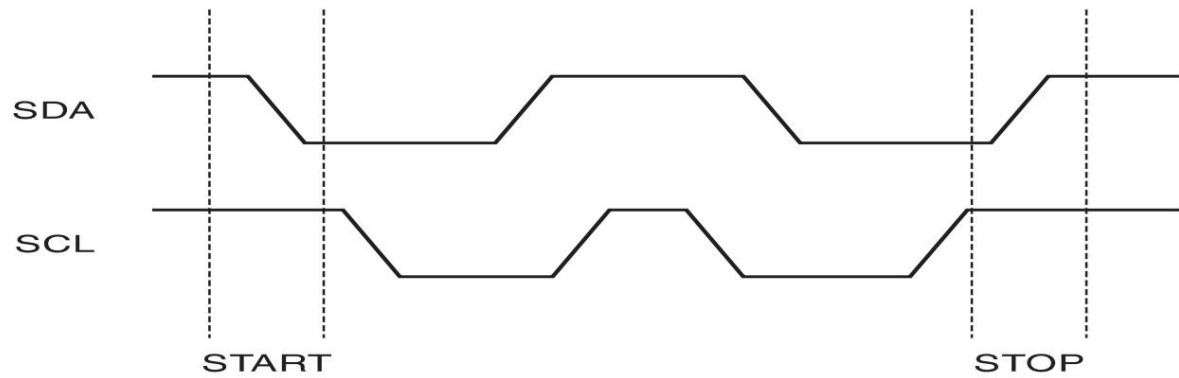
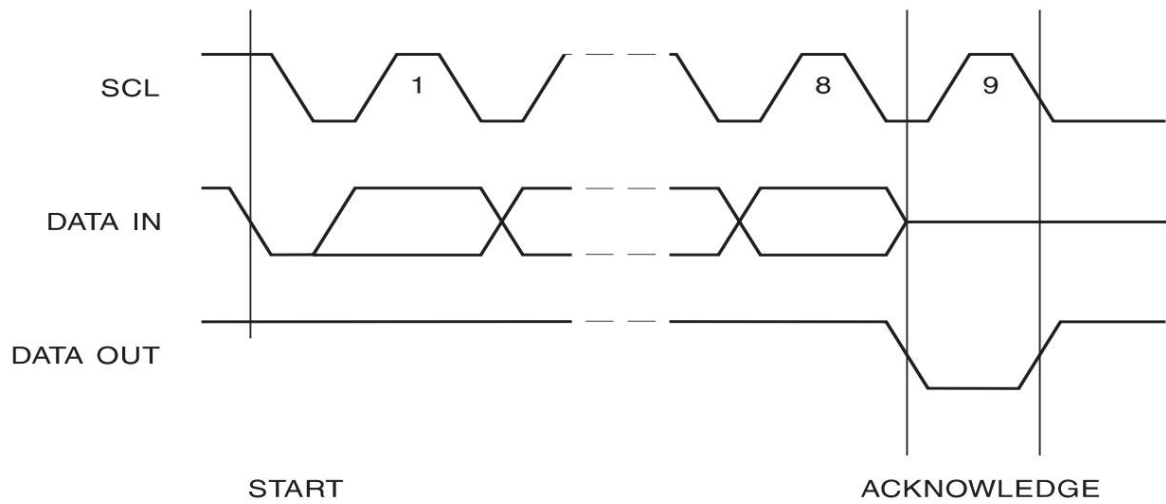


Figure 6. Output Acknowledge





Device Addressing

The 512K EEPROM requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 7 on page 10). The device address word consists of a mandatory “1”, “0” sequence for the first five most significant bits as shown. This is common to all two-wire EEPROM devices.

The 512K uses the two device address bits A1, A0 to allow as many as four devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a “0”. If a compare is not made, the device will return to a standby state.

DATA SECURITY: The AT24C512 has a hardware data protection scheme that allows the user to Write Protect the whole memory when the WP pin is at V_{CC} .

Write Operations

BYTE WRITE: A write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a “0”. The addressing device, such as a microcontroller, then must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR} , to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 8 on page 11).

PAGE WRITE: The 512K EEPROM is capable of 128-byte page writes.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 127 more data words. The EEPROM will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 9 on page 11).

The data word address lower 7 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 128 data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten. The address roll over during write is from the last byte of the current page to the first byte of the same page.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The Read/Write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a “0”, allowing the read or write sequence to continue.



Read Operations

Read operations are initiated the same way as write operations with the exception that the Read/Write select bit in the device address word is set to “1”. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by “1”. This address stays valid between operations as long as the chip power is maintained. The address roll over during read is from the last byte of the last memory page, to the first byte of the first page.

Once the device address with the Read/Write select bit set to “1” is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input “0” but does generate a following stop condition (see Figure 10 on page 11).

RANDOM READ: A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the Read/Write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 11 on page 11).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll over and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 12 on page 12).

Figure 7. Device Address

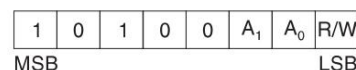




Figure 8. Byte Write

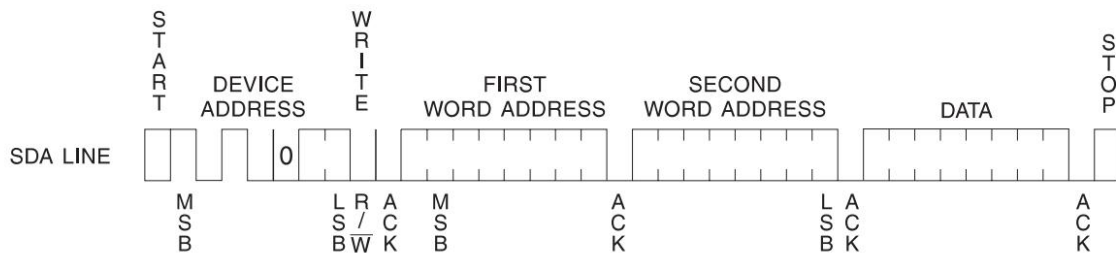


Figure 9. Page Write

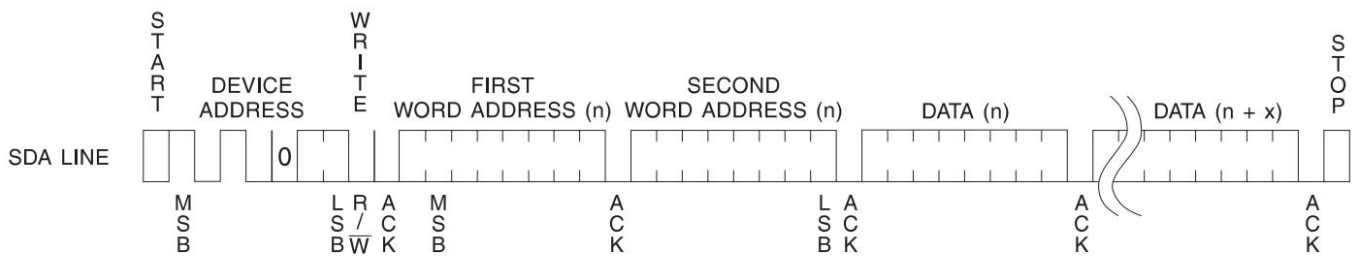


Figure 10. Current Address Read

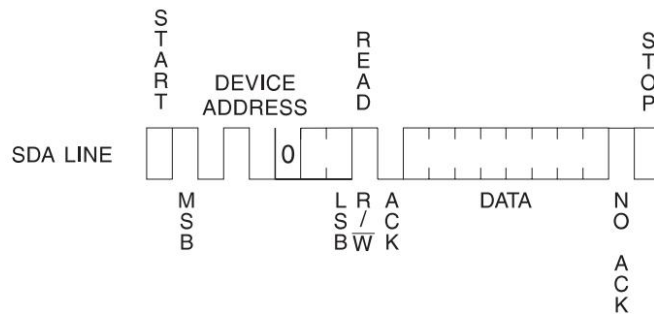


Figure 11. Random Read

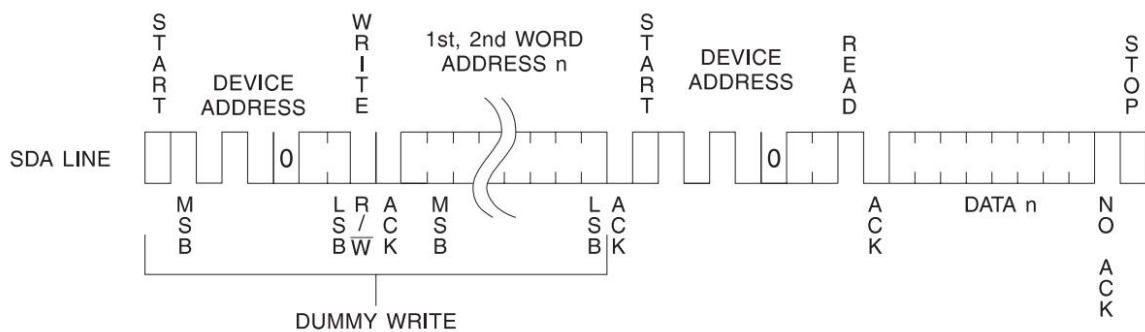
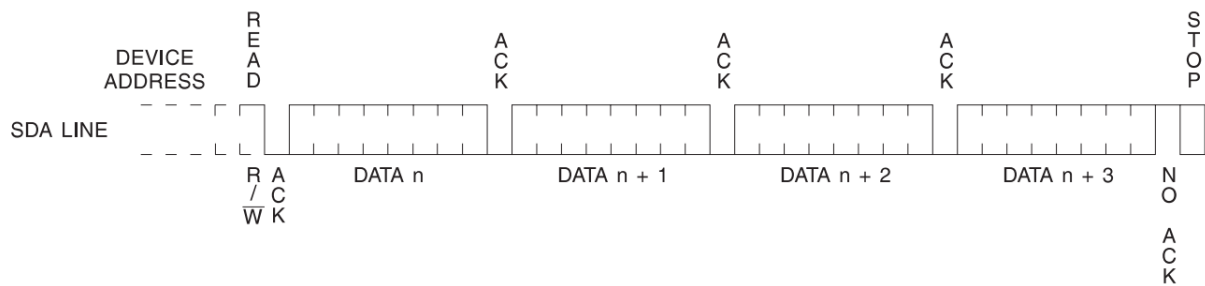




Figure 12. Sequential Read

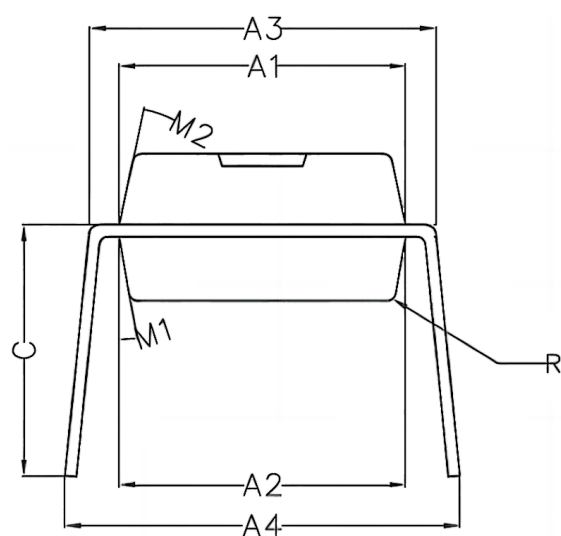
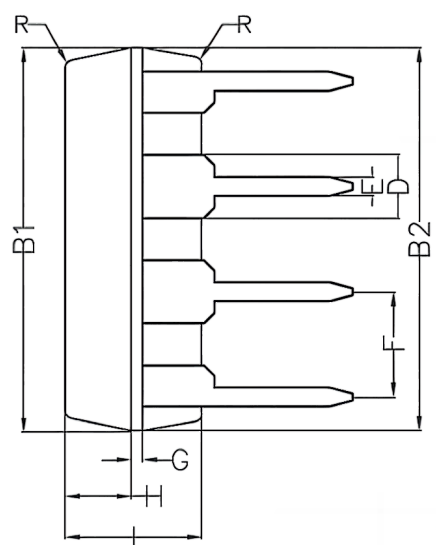
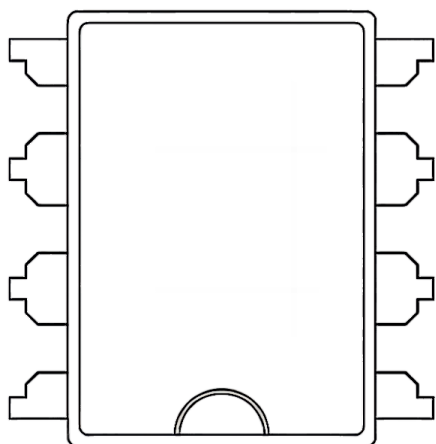




Order information

Order Number	Package	Package Quantity	Marking On The park	Temperature
AT24C512-10PU-1.8-TUDI	DIP8	Tube,50,A box of 2000	AT24C512-10PU-1.8	-40°C to 85°C
AT24C512-10PU-2.7-TUDI	DIP8	Tube,50,A box of 2000	AT24C512-10PU-2.7	

Package DIP8



Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
I	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°



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