钍地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65HVD1040DR

Low-Power CAN Bus Transceiver With Bus Wakeup

网址 www.sztdbdt.com

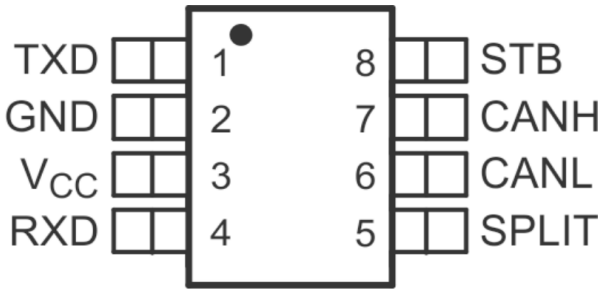
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- Improved Drop-in Replacement for the TJA1040
- ±12 kV ESD Protection
- Low-Current Standby Mode With Bus Wakeup: 5μA Typical
- Bus-Fault Protection of-27 V to 40V
- Rugged Split-Pin Bus Stability
- Dominant Time-Out Function
- Power-Up/Down Glitch-Free Bus Inputs and Outputs
  -High Input Impedance With Low V_{CC}
  -Monotonic Outputs During Power Cycling
- DeviceNetTM Vendor ID Number 806



D Package 8-Pin SOIC
(Top View)

Applications

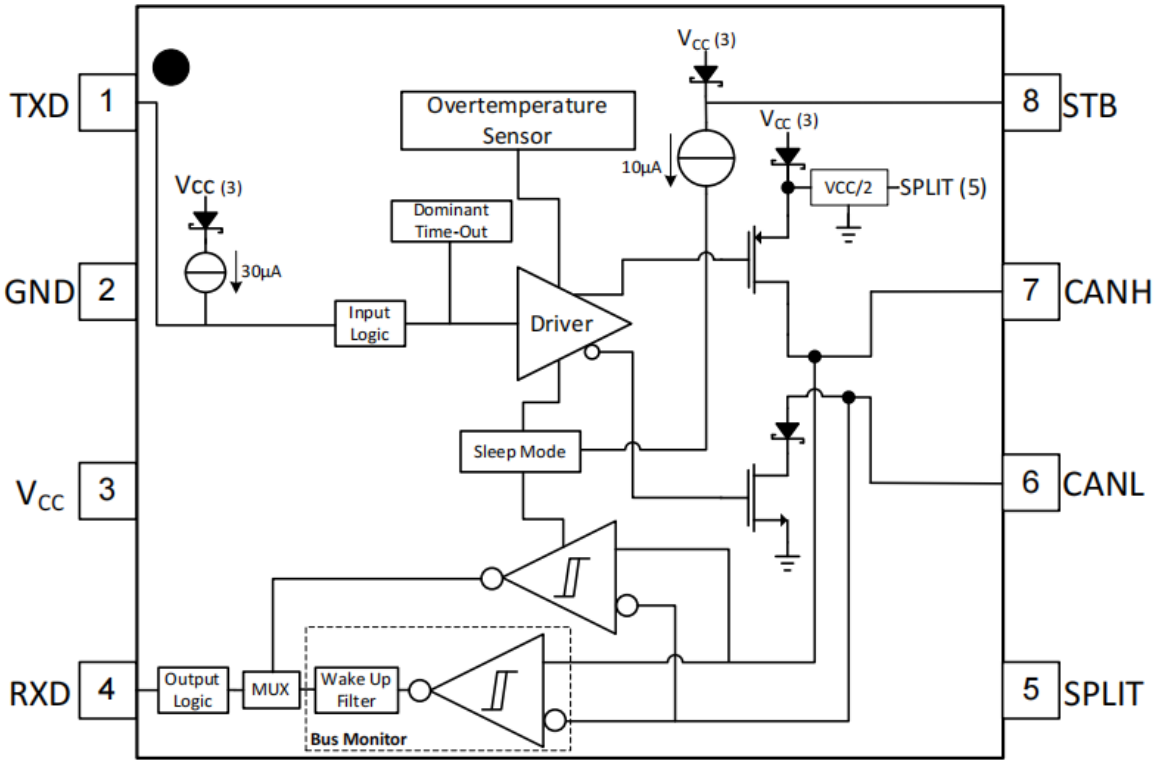
- CAN Bus Applications
- Battery-Operated Applications
- Hand-Held Diagnostics
- Medical Scanning and Imaging
- HVAC
- Security Systems
- Telecom Base Station Status and Control
- SAE J1939 Standard Data Bus Interface
- NMEA 2000 Standard Data Bus Interface
- ISO 11783 Standard Data Bus Interface
- Industrial Automation
  -DeviceNet Data Buses

Description

The SN65HVD1040meets or exceeds thespecifications of the ISO 11898 standard for use inapplications employing a Controller Area Network(CAN).As a CAN bus transceiver,the SN65HVD1040device provides differential transmit and receivecapability for a CAN controller at signaling rates of upto 1 Mbps(1)
Designed for operation in especially harshenvironments,the device features ±12 kV ESDprotection on the bus and split pins,cross-wire,overvoltage and loss of ground protection from-27Vto 40 V, overtemperature shutdown,a-12 V to 12Vcommon-mode range,and will withstanding voltagetransients from-200 V to 200 V according to ISO7637.

The STB input (pin 8) selects between two different modes of operation; high-speed or low-power mode. The high-speed mode of operation is selected by connecting STB to ground.
If a high logic level is applied to the STB pin of the SN65HVD1040, the device enters a low-power bus-monitor standby mode. While the SN65HVD1040 is in the low-power bus-monitor standby mode, a dominant bit greater than 5 μs on the bus is passed by the bus-monitor circuit to the receiver output. The local protocol controller may then reactivate the device when it needs to transmit to the bus.
A dominant time-out circuit in the SN65HVD1040 prevents the driver from blocking network communication during a hardware or software failure. The time-out circuit is triggered by a falling edge on TXD (pin 1). If no rising edge is seen before the time-out constant of the circuit expires, the driver is disabled. The circuit is then reset by the next rising edge on TXD.
The SPLIT output (pin 5) is available on the SN65HVD1040 as a Vcc/2 common-mode bus voltage bias for a split-termination network.
The SN65HVD1040 is characterized for operation from –40 ° C to 125 ° C.

SN65HVD1040 Block Diagram



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
TXD	1	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
GND	2	GND	Device ground
V_{CC}	3	Supply	Transceiver 5-V supply
RXD	4	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
SPLIT	5	O	Reference output voltage (V_{CC}/2)
CANL	6	I/O	Low level CAN bus line
CANH	7	I/O	High level CAN bus line
STB	8	I	Mode select: Strong pulldown to GND for high speed mode, strong pullup to V_{CC} for low power mode.

7 Specifications

7.1 Absolute Maximum Ratings

See Note (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	–0.3	7	V
$V_{I(bus)}$	Voltage at any bus terminal (CANH, CANL, SPLIT)	–27	40	V
$I_{O(OUT)}$	Receiver output current	–20	20	mA
	Voltage input, transient pulse(3), (CANH, CANL, SPLIT)	–200	200	V
V_I	Voltage input (TXD, STB)	–0.5	6	V
T_J	Junction temperature	–55	170	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with ISO 7637, test pulses 1, 2, 3a, 3b, 5, 6 & 7.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	Bus terminals vs GND	±12000	V
		All pins	±4000	
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)		±1000	
	Machine model (MM) ANSI/ESDS5.2-1996		±200	
	IEC Contact Discharge (IEC 61000-4-2)	Bus terminals vs GND	±6000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–12 (1)		12	V
V_{IH}	High-level input voltage	TXD, STB	2		5.25	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{ID}	Differential input voltage		–6		6	V
I_{OH}	High-level output current	Driver	–70			mA
		Receiver	–2			
I_{OL}	Low-level output current	Driver			70	mA
		Receiver			2	
t_{SS}	Maximum pulse width to remain in standby				0.7	µs
T_J	Junction temperature		–40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

7.4 Thermal Information

THERMAL METRIC(1)			SN65HVD1040 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K Thermal Resistance(2)	211	°C/W
		High-K Thermal Resistance	131	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		79	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		53.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter		15.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter		53.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface-mount packages.

7.5 Driver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$V_{O(D)}$	Bus output voltage (Dominant)	CANH	V_I = 0 V, STB at 0 V, R_L = 60 Ω, See Figure 11 and Figure 12	2.9	3.4	4.5	V
		CANL		0.8		1.75	
$V_{O®)}$	Bus output voltage (Recessive)		V_I = 3 V, STB at 0 V, See Figure 11 and Figure 12	2	2.5	3	V
V_O	Bus output voltage (Standby)		R_L = 60 Ω, STB at V_{CC}, See Figure 11 and Figure 12	–0.1		0.1	V
$V_{OD(D)}$	Differential output voltage (Dominant)		V_I = 0 V, R_L = 60 Ω, STB at 0 V, See Figure 11 and Figure 12, and Figure 13	1.5		3	V
			V_I = 0 V, R_L = 45 Ω, STB at 0 V, See Figure 11 and Figure 12	1.4		3	
V_{SYM}	Output symmetry (Dominant or Recessive) [$V_{O(CANH)} + V_{O(CANL)}$]		STB at 0 V, See Figure 12 and Figure 23	0.9 × V_{CC}	V_{CC}	1.1×V_{CC}	V
$V_{OD®)}$	Differential output voltage (Recessive)		V_I = 3 V, R_L = 60 Ω, STB at 0 V, See Figure 11 and Figure 12	–0.012		0.012	V
			V_I = 3 V, STB at 0 V, No Load	–0.5		0.05	
$V_{OC(D)}$	Common-mode output voltage (Dominant)		STB at 0 V, See Figure 18	2	2.3	3	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage				0.3		
I_{IH}	High-level input current, TXD input		V_I at V_{CC}	–2		2	µA
I_{IL}	Low-level input current, TXD input		V_I at 0 V	–50		–10	µA
$I_{O(off)}$	Power-off TXD Leakage current		V_{CC} at 0 V, TXD at 5 V			1	µA
$I_{OS(ss)}$	Short-circuit steady-state output current		V_{CANH} = –12 V, CANL Open, See Figure 22	–120	–72		mA
			V_{CANH} = 12 V, CANL Open, See Figure 22		0.36	1	
			V_{CANL} = –12 V, CANH Open, See Figure 22	–1	–0.5		
			V_{CANL} = 12 V, CANH Open, See Figure 22		71	120	
C_O	Output capacitance		See Input capacitance to ground in *Receiver Electrical Characteristics*.				

(1) All typical values are at 25°C with a 5-V supply.

7.6 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	High-speed mode	STB at 0 V, see Table 1		800	900	mV
V_{IT-}	Negative-going input threshold voltage			500	650		
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)		STB at V_{CC}	100	125		
V_{IT}	Input threshold voltage	Standby mode	STB at V_{CC}	500		1150	
V_{OH}	High-level output voltage		I_O = –2 mA, see Figure 16	4	4.6		V
V_{OL}	Low-level output voltage		I_O = 2 mA, see Figure 16		0.2	0.4	V
$I_{I(off)}$	Power-off bus input current		CANH or CANL = 5 V, V_{CC} at 0 V, TXD at 0 V			5	µA
$I_{O(off)}$	Power-off RXD leakage current		V_{CC} at 0 V, RXD at 5 V			20	µA
C_I	Input capacitance to ground, (CANH or CANL)		TXD at 3 V, V_I = 0.4 sin (4E6πt) + 2.5 V		20		pF
C_{ID}	Differential input capacitance		TXD at 3 V, V_I = 0.4 sin (4E6πt)		10		pF
R_{ID}	Differential input resistance		TXD at 3 V, STD at 0 V	30		80	kΩ
R_{IN}	Input resistance, (CANH or CANL)		TXD at 3 V, STD at 0 V	15	30	40	
$R_{I(m)}$	Input resistance matching [1 – $R_{IN\ (CANH)}$ / $R_{IN\ (CANL)}$)] x 100%		V_{CANH} = V_{CANL}	–3%	0%	3%	

(1) All typical values are at 25°C with a 5-V supply.

7.7 Device Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{loop1}	Total loop delay, driver input to receiver output, Recessive to Dominant	STB at 0 V, see Figure 19	90		230	ns
t_{loop2}	Total loop delay, driver input to receiver output, Dominant to Recessive		90		230	

7.8 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	STB at 0 V, see Figure 14	25	65	120	ns
t_{PHL}	Propagation delay time, high-to-low-level output		25	45	120	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)				25	
t_r	Differential output signal rise time			25		
t_f	Differential output signal fall time			50		
t_{en}	Enable time from silent mode to dominant	See Figure 17			10	µs
t_{dom}	Dominant time-out	See Figure 20	300	450	700	µs

7.9 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}	Propagation delay time, low-to-high-level output	STB at 0 V, TXD at 3 V, See Figure 16	60	100	130	ns
t_{pHL}	Propagation delay time, high-to-low-level output		45	70	130	
t_r	Output signal rise time			8		
t_f	Output signal fall time			8		
t_{BUS}	Dominant time required on bus for wakeup from standby (1)	STB at V_{CC} Figure 21	0.7		5	µs

(1) The device under test shall not signal a wake-up condition with dominant pulses shorter than t_{BUS} (min) and shall signal a wake-up condition with dominant pulses longer than t_{BUS} (max). Dominant pulses with a length between t_{BUS} (min) and t_{BUS} (max) may lead to a wakeup.

7.10 Dissipation Ratings

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Device Power Dissipation	R_L = 60 Ω, S at 0 V, Input to TXD a 500kHz 50% duty-cycle square wave		112	170	mW
T_{JS}	Junction Temperature, Thermal Shutdown (1)			190		°C

(1) Extended operation in thermal shutdown may affect device reliability, see the *Thermal Shutdown*.

7.11 Supply Current

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current, V_{CC}	Dominant	V_I = 0 V, 60 Ω Load, STB at 0 V		50	70	mA
		Recessive	V_I = V_{CC}, STB at 0 V		6	10	
		Standby	STB at V_{CC}, VI = V_{CC}		5	12	µA

7.12 Split-Pin Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	–500 µA < I_O < 500 µA	0.3 × V_{CC}	0.5 × V_{CC}	0.7 × V_{CC}	V
$I_{O(stb)}$	Standby mode leakage current	STB at 2 V, –12 V ≤ V_O ≤ 12 V	–5		5	µA

7.13 STB-Pin Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High level input current	STB at 2 V	–10		0	µA
I_{IL}	Low level input current	STB at 0 V	–10		0	µA

8 Parameter Measurement Information

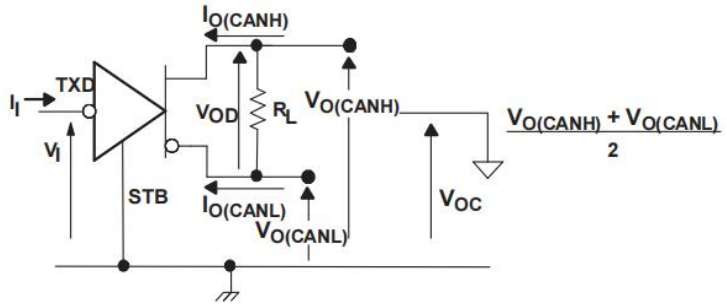


Figure 11. Driver Voltage, Current, and Test Definition

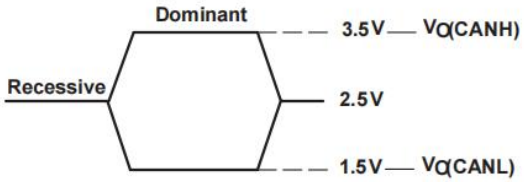


Figure 12. Bus Logic State Voltage Definitions

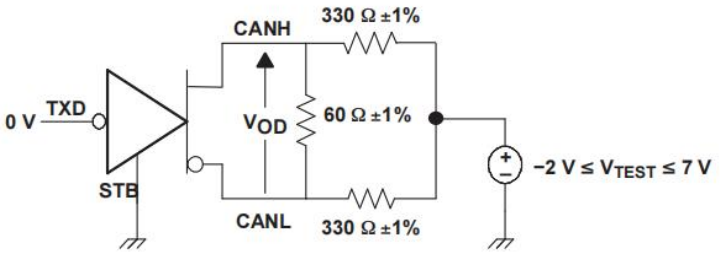


Figure 13. Driver V_{OD} Test Circuit

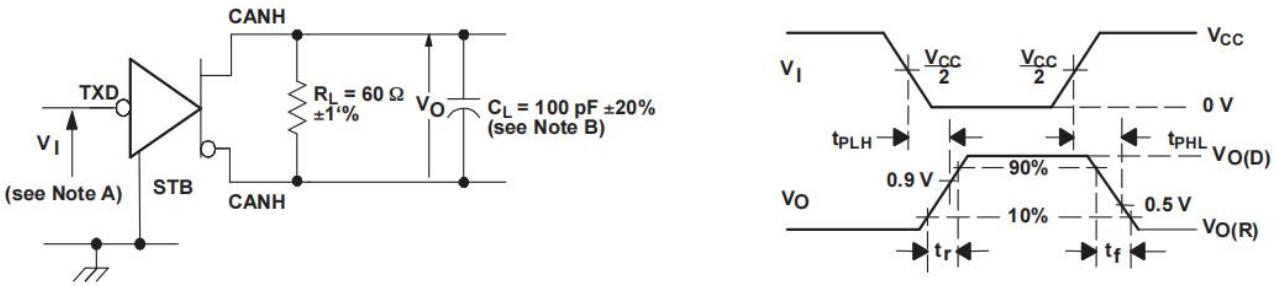


Figure 14. Driver Test Circuit and Voltage Waveforms

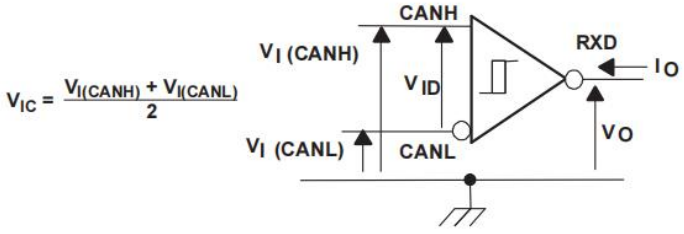
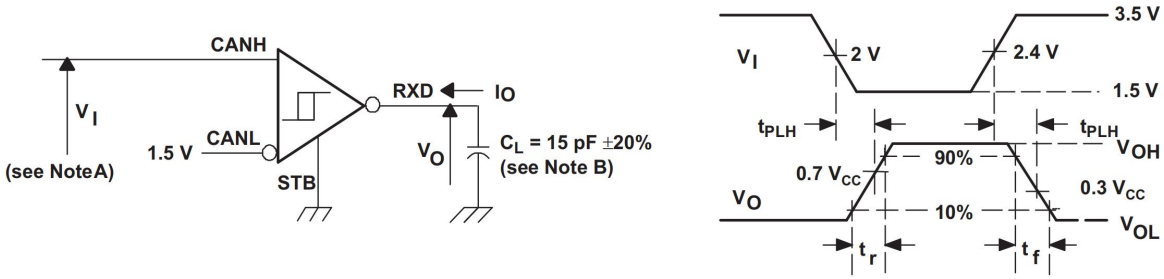


Figure 15. Receiver Voltage and Current Definitions

Parameter Measurement Information (continued)



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 16. Receiver Test Circuit and Voltage Waveforms

Table 1. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R	
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	

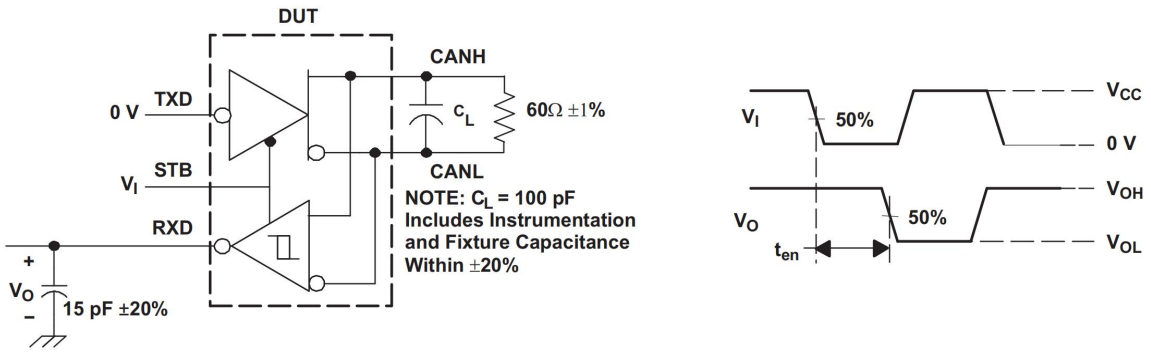
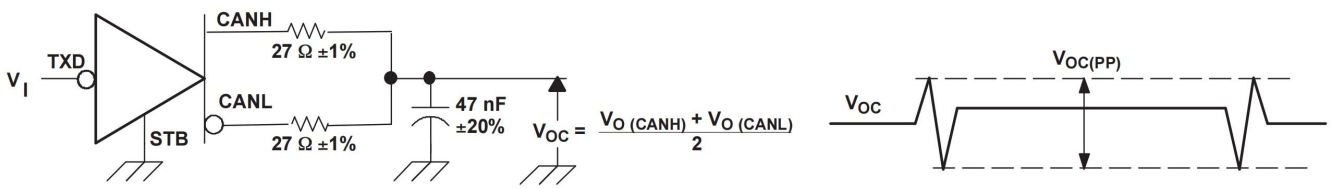
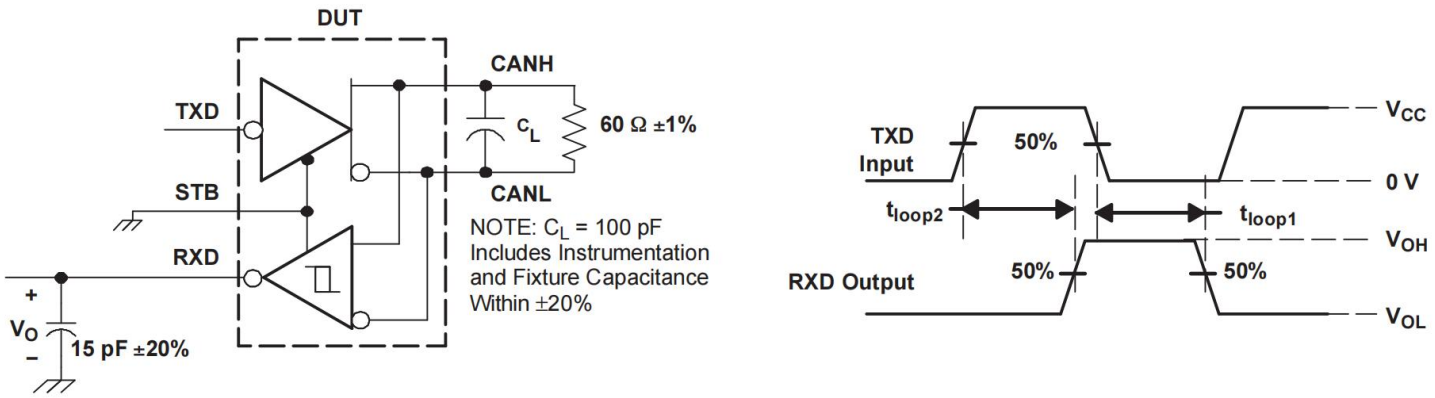


Figure 17. T_{en} Test Circuit and Voltage Waveforms



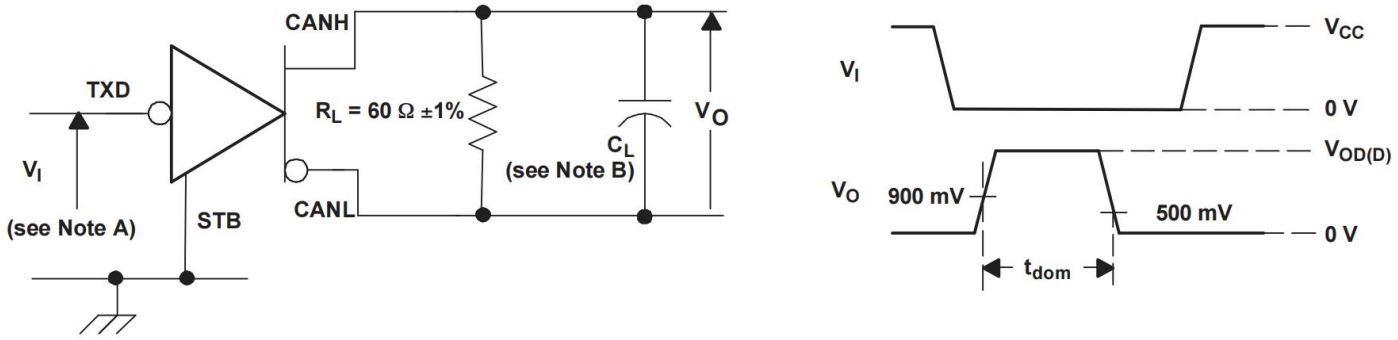
All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 18. Peak-To-Peak Common Mode Output Voltage Test and Waveform



All V_I input pulses are from 0 V to V_{CC} and supplied by a generator with the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

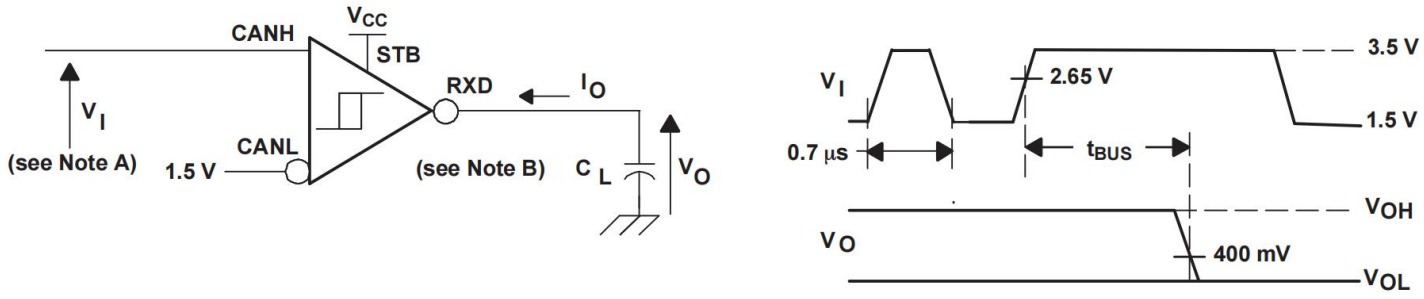
Figure 19. T_{loop} Test Circuit and Voltage Waveforms



All V_I input pulses are from 0 V to V_{CC} and supplied by a generator with the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 500 Hz, 50% duty cycle.

A. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

Figure 20. Dominant Time-Out Test Circuit and Waveform



A. For V_I bit width ≤ 0.7 µs, V_O = V_{OH}. For V_Il bit width ≥ 5 µs, V_O = V_{OL}. V_I input pulses are supplied from a generator with the following characteristics; t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 50 Hz, 30% duty cycle.

B. C_L = 15 pF includes instrumentation and fixture capacitance within ±20%.

Figure 21. T_{BUS} Test Circuit and Waveform

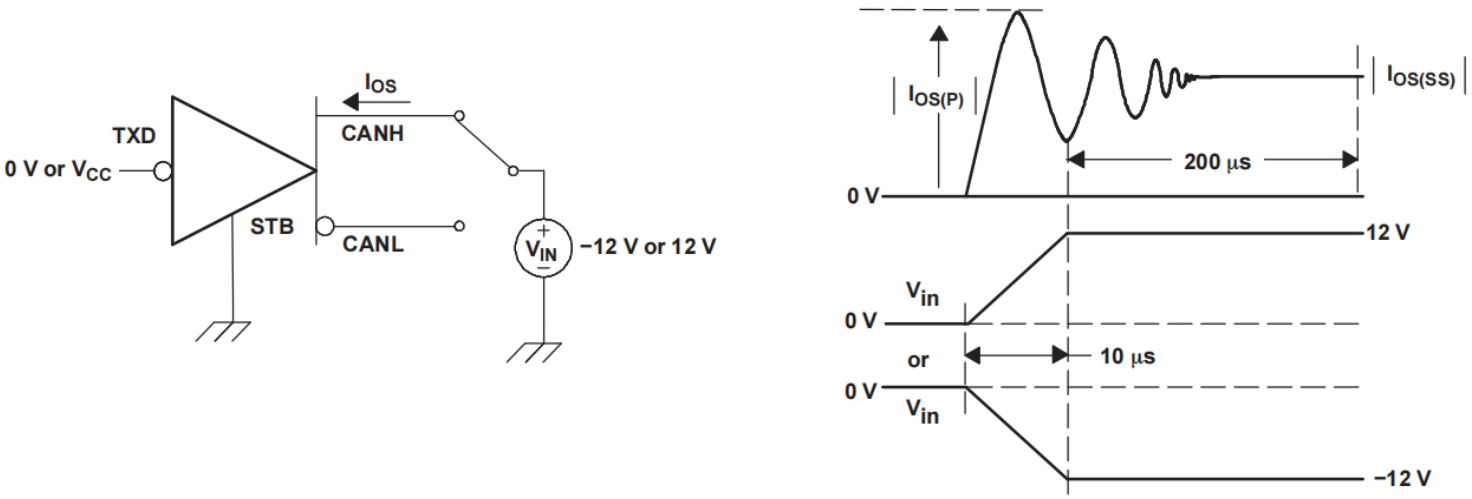


Figure 22. Driver Short-Circuit Current Test and Waveform

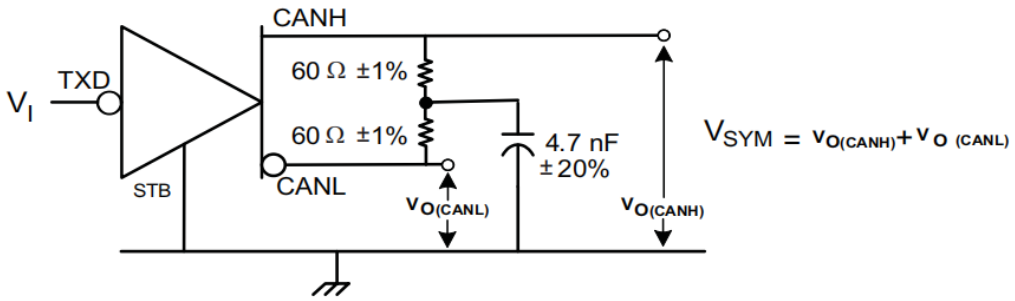


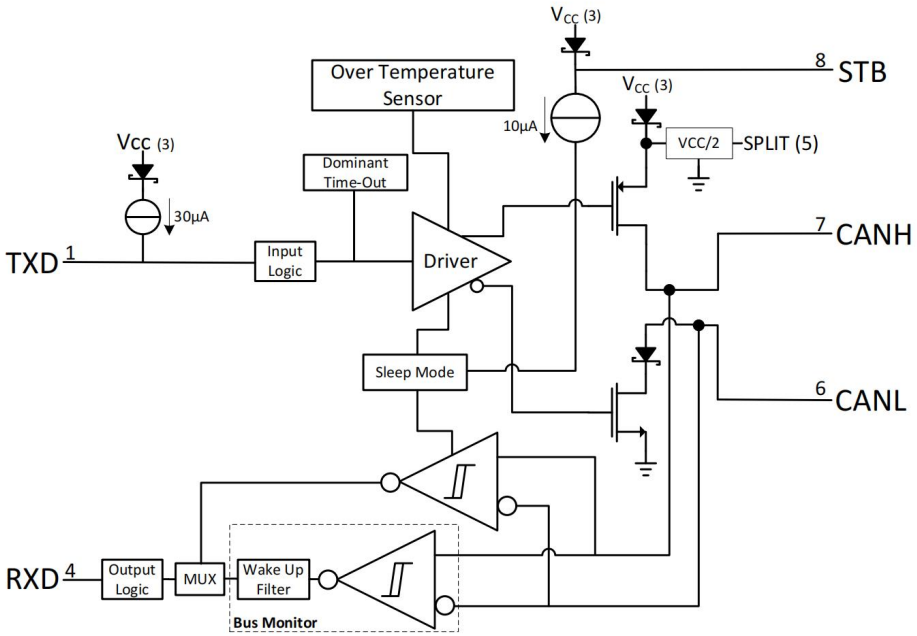
Figure 23. Driver Output Symmetry Test Circuit

9 Detailed Description

9.1 Overview

The SN65HVD1040 CAN bus transceiver meets or exceeds the ISO 11898 standard as a high-speed controller area network (CAN) bus physical layer device. The device is designed to interface between the differential bus lines in controller area network and the CAN protocol controller at data rates up to 1 Mbps.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Mode Control

9.3.1.1 High-Speed Mode

Select the high-speed mode of the device operation by setting the STB pin low. The CAN bus driver and receiver are fully operational and the CAN communication is bidirectional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD.

9.3.1.2 Low-Power Mode

If a high logic level is applied to the STB pin, the device enters a low-power bus-monitor standby mode. While the SN65HVD1040 is in the low-power bus-monitor standby mode, a dominant bit greater than 5 µs on the bus is passed by the bus-monitor circuit to the receiver output. The local protocol controller may then reactivate the device when it needs to transmit to the bus.

9.3.2 Dominant State Time-Out

During normal mode, the mode where the CAN driver is active, the TXD DTO circuit prevents the transceiver from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the time-out period t_{TXD_DTO}. The DTO circuit is triggered on a falling edge on the driver input, TXD. The DTO circuit disables the CAN bus driver if no rising edge is seen on TXD before the time-out period expires. This frees the CAN bus for communication between other nodes on the network. The CAN driver is re-enabled when a rising edge is seen on the drvier input, TXD, thus clearing the TXD DTO condition. The receiver and RXD pin still reflect the CAN bus, and the bus pins are biased to recessive level during a TXD DTO.

9.3.3 Thermal Shutdown

The SN65HVD1040 has a thermal shutdown that turns off the driver outputs when the junction temperature nears 190°C. This shutdown prevents catastrophic failure from bus shorts, but does not protect the circuit from possible damage. The user should strive to maintain recommended operating conditions, and not exceed absolute maximum ratings at all times. If the SN65HVD1040 is subjected to many or long durations faults that can put the device into thermal shutdown, it should be replaced.

9.3.4 SPLIT

A reference voltage (V_{CC}/2) is available through the SPLIT outpit pin. The SPLIT voltage should be tied to the common mode point in a split termination network, hence the pin name, to help stabilize the output common mode voltage. See Figure 29 for more application specific information on properly terminating the CAN bus.

9.3.5 Operating Temperature Range

The SN65HVD1040 is characterized for operation from –40°C to 125°C.

9.4 Device Functional Modes

Table 2. Driver Function Table(1)

INPUTS		OUTPUTS		BUS STATE
TXD	STB	CANH	CANL	
L	L	H	L	DOMINANT
H	L	Z	Z	RECESSIVE
Open	X	Z	Z	RECESSIVE
X	H or Open	Z	Z	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; Z = high impedance

Table 3. Receiver Function Table(1)

DIFFERENTIAL INPUTS V_{ID} = CANH - CANL	STB	OUTPUT RXD	BUS STATE
V_{ID} ≥ 0.9 V	L	L	DOMINANT
V_{ID} ≥ 1.15 V	H or Open	L	DOMINANT
0.5 V < V_{ID} < 0.9 V	X	?	?
V_{ID} ≤ 0.5 V	X	H	RECESSIVE
Open	X	H	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

Table 4. Parametric Cross Reference With the TJA1040

TJA1040 (1)	PARAMETER	HVD10xx
TJA1040 DRIVER SECTION		
V_{IH}	High-level input voltage	Recommended V_{IH}
V_{IL}	Low-level input voltage	Recommended V_{IL}
I_{IH}	High-level input current	Driver I_{IH}
I_{IL}	Low-level input current	Driver I_{IL}
TJA1040 BUS SECTION		
$V_{th(dif)}$	Differential input voltage	Receiver V_{IT} and recommended V_{ID}
$V_{hys(dif)}$	Differential input hysteresis	Receiver V_{hys}
$V_{O(dom)}$	Dominant output voltage	Driver $V_{O(D)}$
$V_{O(reces)}$	Recessive output voltage	Driver $V_{O(R)}$
$V_{I(dif)(th)}$	Differential input voltage	Receiver V_{IT} and recommended V_{ID}
$V_{O(dif0(bus)}$	Differential bus voltage	Driver $V_{OD(D)}$ and $V_{OD(R)}$
I_{LI}	Power-off bus input current	Receiver $I_{I(off)}$
$I_{O(SC)}$	Short-circuit output current	Driver $I_{OS(SS)}$
$R_{I(cm)}$	CANH, CANL input resistance	Receiver R_{IN}
$R_{I(def)}$	Differential input resistance	Receiver R_{ID}
$R_{I(cm)\ (m)}$	Input resistance matching	Receiver $R_{I\ (m)}$
$C_{I(cm)}$	Input capacitance to ground	Receiver C_I
$C_{I(dif)}$	Differential input capacitance	Receiver C_{ID}
TJA1040 RECEIVER SECTION		
I_{OH}	High-level output current	Recommended I_{OH}
I_{OL}	Low-level output current	Recommended I_{OL}
TJA1040 SPLIT PIN SECTION		
V_O	Reference output voltage	V_O
TJA1040 TIMING SECTION		
$t_{d(TXD-BUSon)}$	Delay TXD to bus active	Driver t_{PLH}
$t_{d(TXD-BUSoff)}$	Delay TXD to bus inactive	Driver t_{PHL}
$t_{d(BUSon-RXD)}$	Delay bus active to RXD	Receiver t_{PHL}
$t_{d(BUSoff-RXD)}$	Delay bus inactive to RXD	Receiver t_{PLH}
$t_{PD(TXD–RXD)}$	Prop delay TXD to RXD	Device t_{LOOP1} and t_{LOOP2}
$t_{d(stb-norm)}$	Enable time from standby to dominant	Driver t_{en}
TJA1040 STB PIN SECTION		
V_{IH}	High-level input voltage	Recommended V_{IH}
V_{IL}	Low-level input voltage	Recommended V_{IL}
I_{IH}	High-level input current	I_{IH}
I_{IL}	Low-level input current	I_{IL}

(1) From TJA1040 Product Specification, NXP, February 19, 2003.

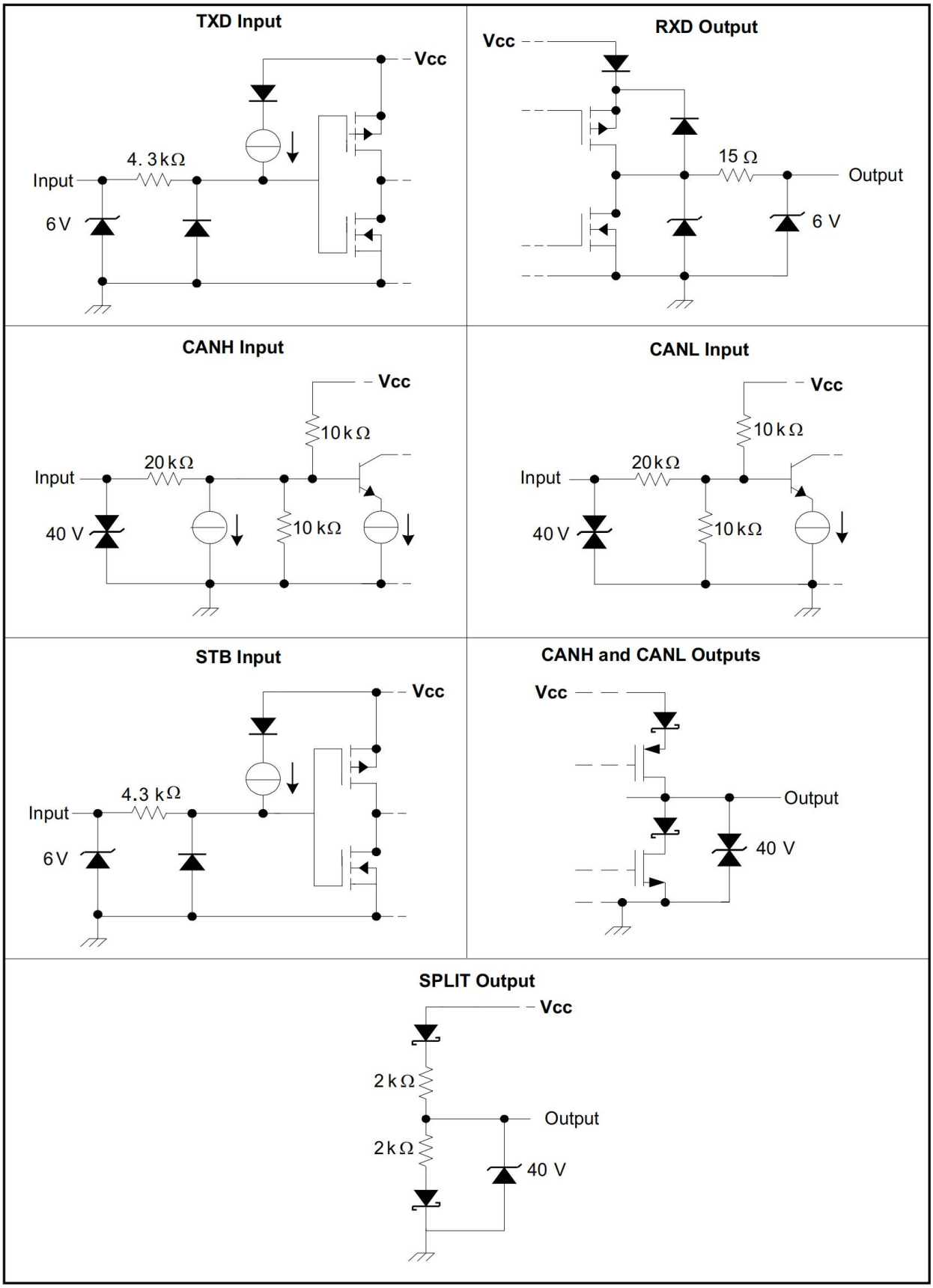
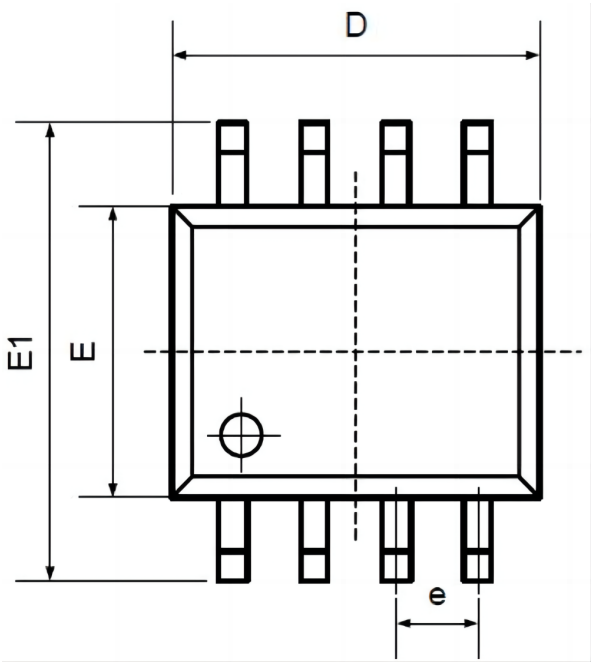


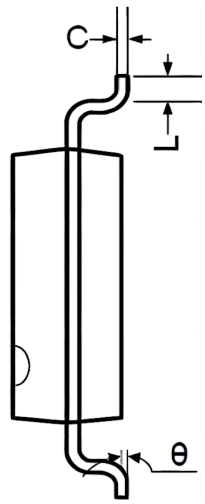
Figure 24. Equivalent Input and Output Schematic Diagrams

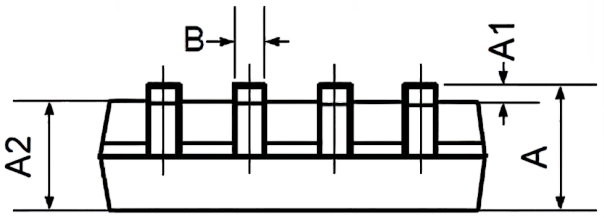
Order information

Order Number	Package	Package Quantity	Marking On The park
SN65HVD1040DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD1040DR

Package SOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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